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Vishay Siliconix

Automotive N-Channel 60 V (D-S) 175 °C MOSFET



Marking Code: Q037

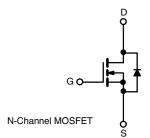
PRODUCT SUMMARY					
V _{DS} (V)	60				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.023				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.028				
I _D (A)	18				
Configuration	Single				
Package	PowerPAK 1212-8W				

FEATURES

- TrenchFET® power MOSFET
- Low thermal resistance PowerPAK® 1212-8 package with 1.07 mm profile
- PWM optimized
- 100 % R_a and UIS tested
- AEC-Q101 qualified
- · Wettable flank terminals
- Material categorization: for definitions of compliance please see <u>www.vishav.com/doc?99912</u>



ROHS COMPLIANT HALOGEN FREE



PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	60	V
Gate-source voltage		V_{GS}	± 20	V
Continuous drain current ^a	T _C = 25 °C	- I _D	18	
	T _C = 125 °C		18	
Continuous source current (diode conduction) ^a		Is	18	Α
Pulsed drain current ^b		I _{DM}	72	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	20	
Single pulse avalanche energy	L=0.11111	E _{AS}	16	mJ
Mayimum navay discination h	T _C = 25 °C	P _D	62	W
Maximum power dissipation ^b	T _C = 125 °C		20	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) d			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount c	R_{thJA}	81	°C/W
Junction-to-case (drain)		R_{thJC}	2.4	C/VV

Notes

- a. Package limited
- b. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- c. When mounted on 1" square PCB (FR4 material)
- d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		1			<u> </u>		
Drain-source breakdown voltage	V _{DS}	V _{GS} :	= 0 V, I _D = 250 μA	60	-	-	l
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	1.5	2	2.5	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
-		V _{GS} = 0 V	V _{DS} = 60 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 60 V, T _J = 125 °C	-	-	50	μΑ
-		V _{GS} = 0 V	V _{DS} = 60 V, T _J = 175 °C	-	-	150	1
On-state drain current a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 \text{ V}$	20	-	-	Α
	, ,	V _{GS} = 10 V	I _D = 8.7 A	-	0.016	0.023	
Duning and an atota projetoway 2	Б	V _{GS} = 10 V	I _D = 8.7 A, T _J = 125 °C	-	-	0.039	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 8.7 A, T _J = 175 °C	-	-	0.050	Ω
		V _{GS} = 4.5 V	I _D = 8.7 A	-	0.019	0.028	
Forward transconductance b	9 _{fs}	V _{DS}	= 15 V, I _D = 8.7 A	-	50	-	S
Dynamic ^b							
Input capacitance	C _{iss}			-	1275	1590	
Output capacitance	C _{oss}	$V_{GS} = 0 V$	$V_{DS} = 30 \text{ V}, f = 1 \text{ MHz}$	-	112	140	рF
Reverse transfer capacitance	C _{rss}			-	42	52	
Total gate charge ^c	Qg			-	19	25	
Gate-source charge ^c	Q_{gs}	$V_{GS} = 10 \text{ V}$	$V_{DS} = 30 \text{ V}, I_{D} = 8.7 \text{ A}$	-	2.6	-	nC
Gate-drain charge ^c	Q_{gd}	1		=	3.6	-	
Gate resistance	Rg		f = 1 MHz	0.6	1.12	1.6	Ω
Turn-on delay time ^c	t _{d(on)}			-	8	10	
Rise time ^c	t _r		= 30 V, $R_L = 30 \Omega$	-	13	16	
Turn-off delay time ^c	t _{d(off)}	$I_D \cong 1 A$,	$V_{GEN} = 10 V, R_g = 1 \Omega$	-	22	26	ns
Fall time ^c	t _f			=	15	18	
Source-Drain Diode Ratings and Char	acteristics b						
Pulsed current ^a	I _{SM}			=	-	72	Α
Forward voltage	V_{SD}	$I_F = 8.7 \text{ A}, V_{GS} = 0 \text{ V}$		_	0.8	1.2	V

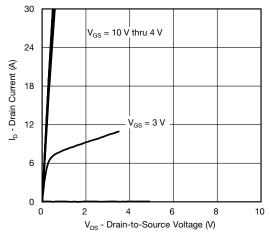
Notes

- a. Pulse test; pulse width $\leq 300~\mu\text{s},$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

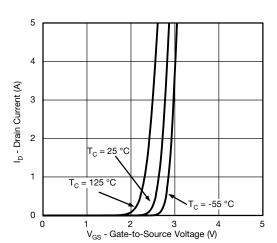
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



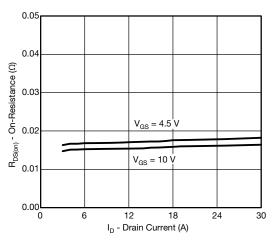
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



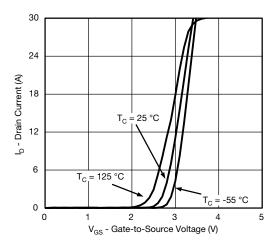
Output Characteristics



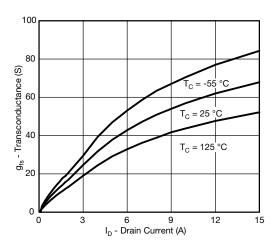
Transfer Characteristics



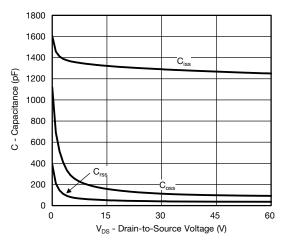
On-Resistance vs. Drain Current



Transfer Characteristics



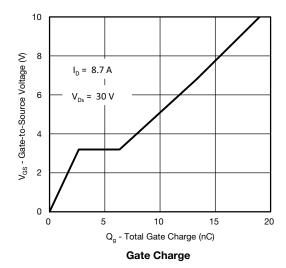
Transconductance

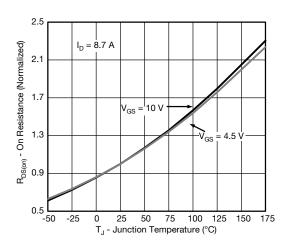


Capacitance

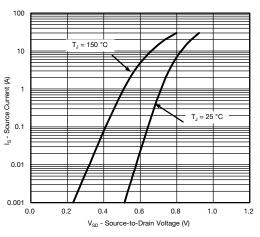


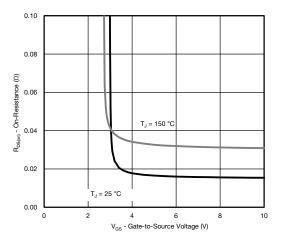
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)





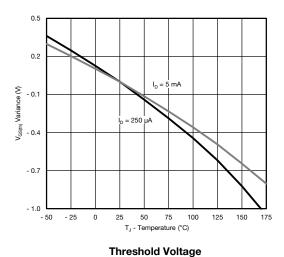
On-Resistance vs. Junction Temperature

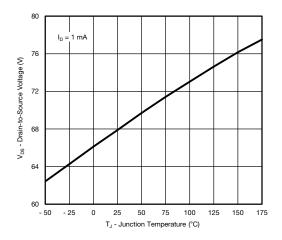




Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

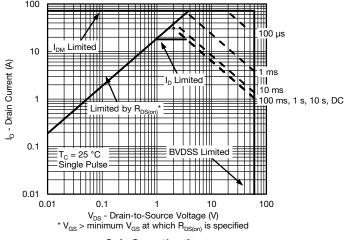




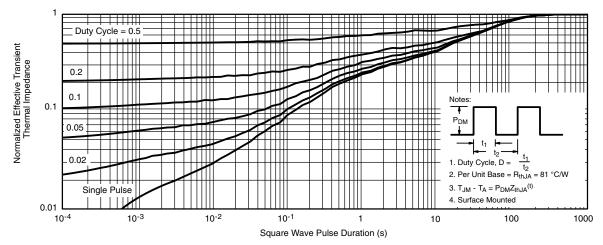
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



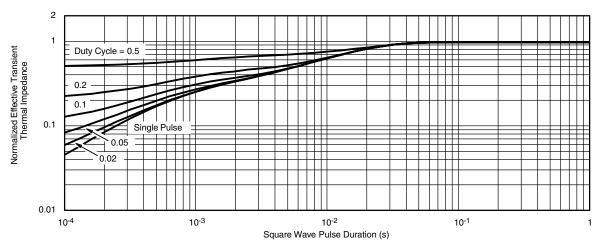
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

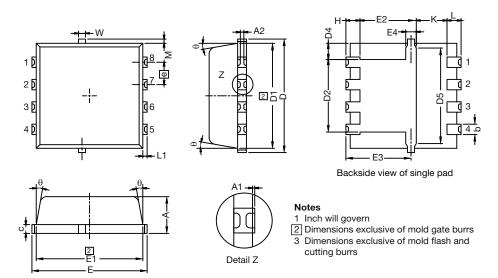
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75674.



PowerPAK® 1212-8W Case Outline

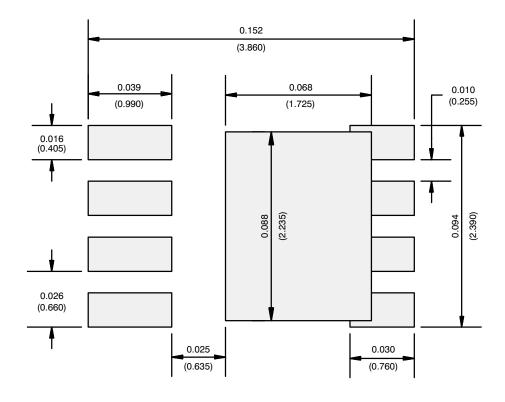


DIM	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.97	1.04	1.12	0.038	0.041	0.044	
A1	0	-	0.05	0	-	0.002	
A2	0	-	0.13	0	-	0.005	
b	0.23	0.30	0.41	0.009	0.012	0.016	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	3.20	3.30	3.40	0.126	0.130	0.134	
D1	2.95	3.05	3.15	0.116	0.120	0.124	
D2	1.98	2.11	2.24	0.078	0.083	0.088	
D4	0.47 typ.			0.0185 typ.			
D5	2.3 typ.			0.090 typ.			
Е	3.20	3.30	3.40	0.126	0.130	0.134	
E1	2.95	3.05	3.15	0.116	0.120	0.124	
E2	1.47	1.60	1.73	0.058	0.063	0.068	
E3	1.75	1.85	1.98	0.069	0.073	0.078	
E4		0.34 typ.			0.013 typ.		
е	0.65 BSC.						
K	0.86 typ.				0.034 typ.		
Н	0.30	0.41	0.51	0.012	0.016	0.020	
L	0.30	0.43	0.56	0.012	0.017	0.022	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
М	0.125 typ.			0.005 typ.			

DWG: 6032



RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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