HARRIS SEMICONDUCTOR

CDP1852, CDP1852C

March 1997

Byte-Wide Input/Output Port

Features

- Static Silicon-Gate CMOS Circuitry
- Parallel 8-Bit Data Register and Buffer
- Handshaking Via Service Request Flip-Flop
- Low Quiescent and Operating Power
- Interfaces Directly with CDP1800-Series Microprocessors
- Single Voltage Supply
- Full Military Temperature Range (-55°C to +125°C)

Ordering Information

PACKAGE	TEMP. RANGE	5V	10V	PKG. NO.
PDIP	-40°C to +85°C	CDP1852CE	CDP1852E	E24.6
SBDIP	-40°C to +85°C	CDP1852CD	CDP1852D	D24.6

Description

The CDP1852 and CDP1852C are parallel, 8-bit, mode-programmable input/output ports. They are compatible and will interface directly with CDP1800-series microprocessors. They are also useful as 8-bit address latches when used with the CDP1800 multiplexed address bus and as I/O ports in general-purpose applications.

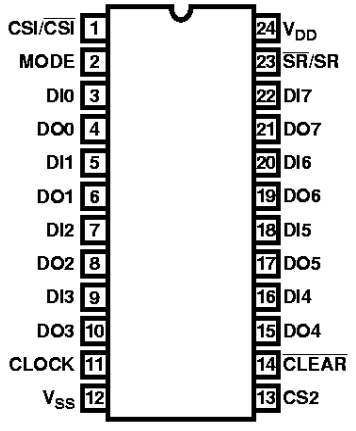
The mode control is used to program the device as an input port (mode = 0) or as an output port (mode = 1). The $\overline{SR}$/SR output can be used as a signal to indicate when data is ready to be transferred. In the input mode, a peripheral device can strobe data into the CDP1852, and microprocessor can read that data by device selection. In the output mode, a microprocessor strobes data into the CDP1852, and handshaking is established with a peripheral device when the CDP1852 is deselected.

In the input mode, data at the data-in terminals (DI0-DI7) is strobed into the port's 8-bit register by a high (1) level on the clock line. The negative high-to-low transition of the clock latches the data in the register and sets the service request output low ($\overline{SR}$/SR = 0). When CS1/$\overline{CS1}$ and CS2 are high (CS1/$\overline{CS1}$ and CS2 = 1), the three-state output drivers are enabled and data in the 8-bit register appear at the data-out terminals (D00-D07). When either CS1/$\overline{CS1}$ or CS2 goes low (CS1/$\overline{CS1}$ or CS2 = 0), the data-out terminals are three-stated and the service request output returns high ($\overline{SR}$/SR =1).

In the output mode, the output drivers are enabled at all times. Data at the data-in terminals (DI0-DI7) is strobed into the 8-bit register when CS1/$\overline{CS1}$ is low (CS1/$\overline{CS1}$ = 0) and CS2 and the clock are high (1), and are present at the data-out terminals (D00-D07). The negative high-to-low transition of the clock latches the data in the register. The $\overline{SR}$/SR output goes high ($\overline{SR}$/SR = 1) when the device is deselected (CS1/$\overline{CS1}$ = 1 or CS2 = 0) and returns low ($\overline{SR}$/SR = 0) on the following trailing edge of the clock.

Pinout

24 LEAD DIP
TOP VIEW



Typical CDP1802 Microprocessor System

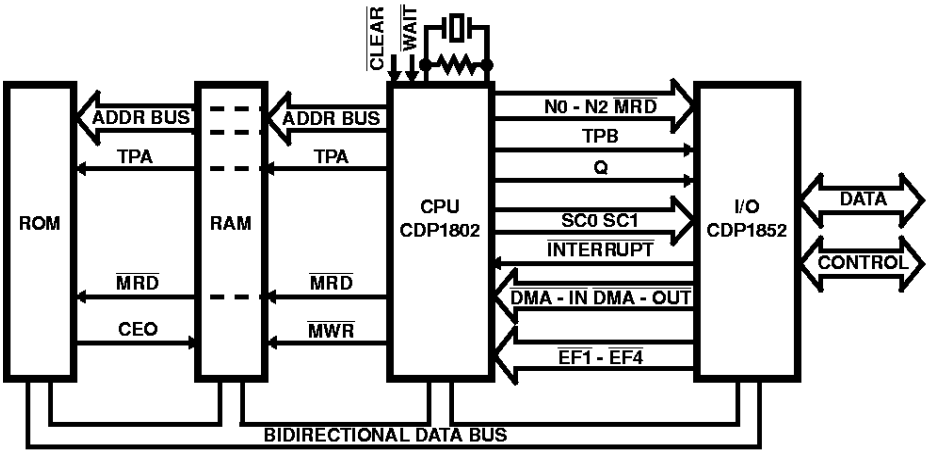


FIGURE 1.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1166.2**

Absolute Maximum Ratings

DC Supply-voltage Range, (V_{DD})
(Voltage Referenced to V_{SS} Terminal)
CDP1852 . . . . . -0.5 to +11V
CDP1852C . . . . . -0.5 to +7V
Input Voltage Range, All Inputs . . . . . -0.5 to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA
Device Dissipation Per Output Transistor 100mW
For T_A = Full Package-Temperature Range
(All Package Type)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	65	N/A
SBDIP Package	65	20

Operating-Temperature Range (T_A)
Package Type D, H . . . . . -55°C to +125°C
Package Type E. . . . . -40°C to +85°C
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (During Soldering): . . . . . +265°C
At Distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from Case for 10s max

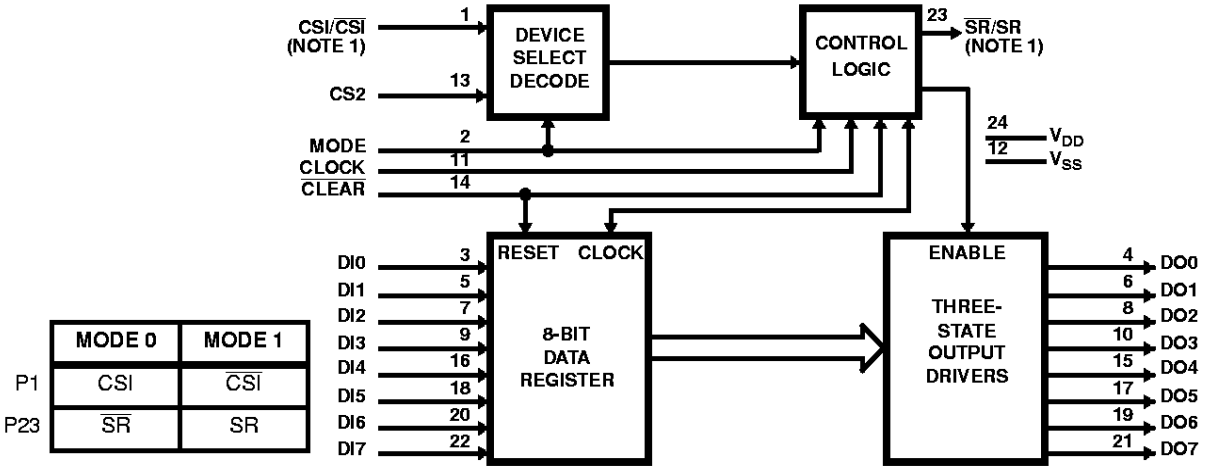
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

At T_A = Full Package Temperature Range. For Maximum Reliability, Operating Conditions Should be Selected so that Operation is Always within the Following Ranges:

PARAMETER	LIMITS				UNITS
	CDP1852		CDP1852C		
	MIN	MAX	MIN	MAX	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V

Functional Diagram



	MODE 0	MODE 1
P1	CSI	$\overline{CSI}$
P23	$\overline{SR}$	SR

NOTE:

1. Polarity depends on mode.

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM FOR CDP1852

A $\overline{CLEAR}$ control is provided for resetting the port's register (DO0-DO7 = 0) and service request flip-flop (input mode: $\overline{SR}$/ SR = 1 and output mode: $\overline{SR}$/SR = 0).

The CDP1852 is functionally identical to the CDP1852C. The CDP1852 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1852C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1852 and CDP1852C are supplied in 24-lead, hermetic, dual-in-line ceramic packages (D suffix), in 24-lead dual-in-line plastic packages (E suffix). The CDP1852C is also available in chip form (H suffix).

Logic Diagram

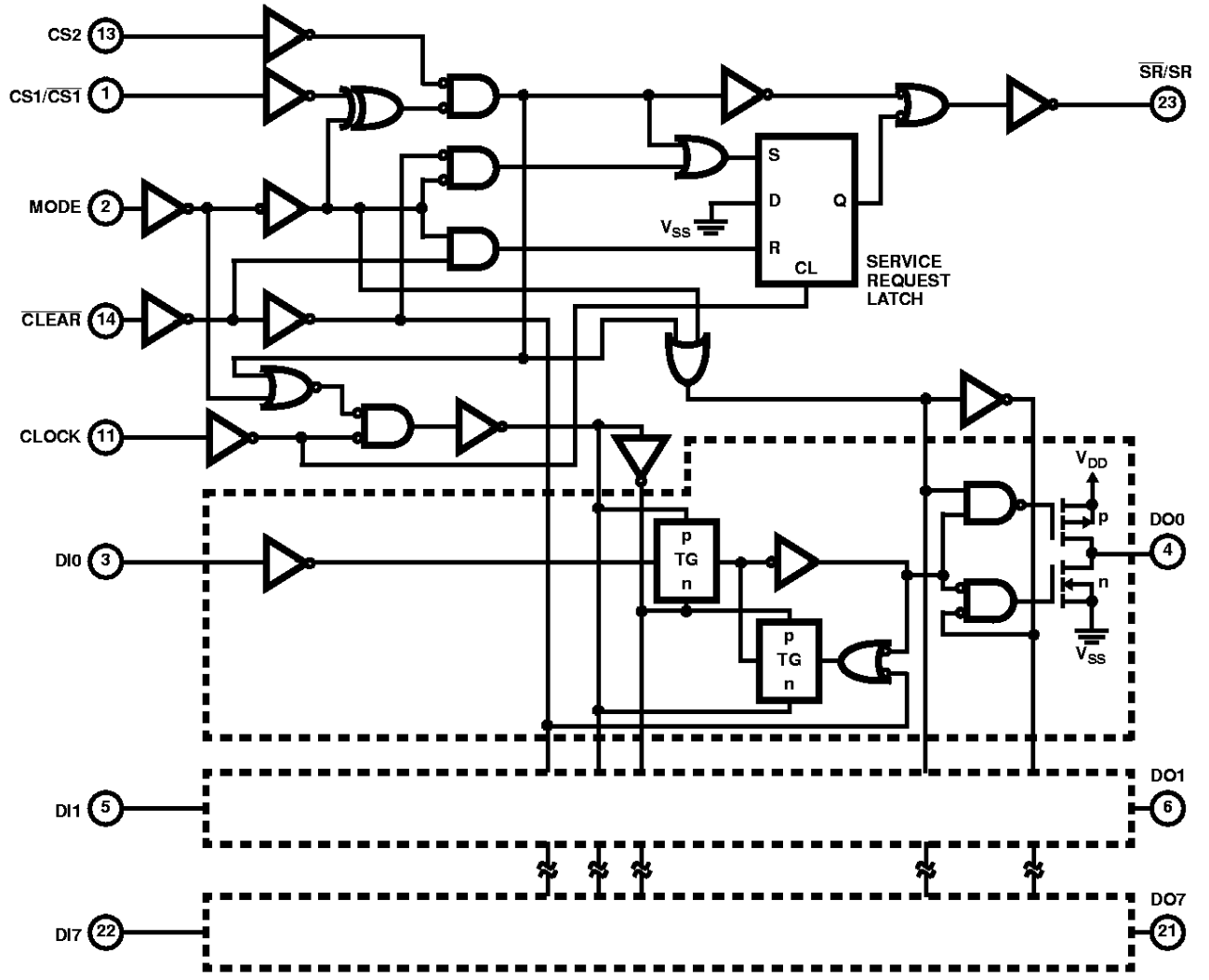


FIGURE 3. CDP1852 LOGIC DIAGRAM

Static Electrical Specifications At T_A = -40°C to +85°C, Unless Otherwise Specified

PARAMETER		CONDITIONS			LIMITS						UNITS
					CDP1852			CDP1852C			
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE1) TYP	MAX	MIN	(NOTE1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	-	10	-	-	50	µA
		-	0, 10	10	-	-	100	-	-	-	µA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	1.6	3.2	-	mA
		0.5	0, 10	10	3	6	-	-	-	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	-1.15	-2.3	-	mA
		9.5	0, 10	10	-3	-6	-	-	-	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V

Static Electrical Specifications At T_A = -40°C to +85°C, Unless Otherwise Specified (Continued)

PARAMETER		CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS CDP1852 MIN	LIMITS CDP1852 (NOTE1) TYP	LIMITS CDP1852 MAX	LIMITS CDP1852C MIN	LIMITS CDP1852C (NOTE1) TYP	LIMITS CDP1852C MAX	UNITS
Output Voltage High Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	I_{IN}	-	0, 5	5	-	-	±1	-	-	±1	µA
		-	0, 10	10	-	-	±2	-	-	-	µA
Three-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	-	-	±1	-	-	±1	µA
		0, 10	0, 10	10	-	-	±2	-	-	-	µA
Operating Current (Note 3)	I_{DD1}	-	0, 5	5	-	130	300	-	150	300	µA
		-	0, 10	10	-	550	800	-	-	-	µA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	5	7.5	-	-	-	pF

NOTES:

1. Typical values are for T_A = 25°C and nominal V_{DD}.
2. $I_{OL} = I_{OH}$ = 1µA
3. Operating current is measured at 2MHz in an CDP1802 system with open outputs and a program of 6N55, 6NAA, 6N55, 6NAA,....

Dynamic Electrical Specifications At T_A = -40°C to +85°C, V_{DD} = ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, and 1 TTL Load

PARAMETER		V_{DD} (V)	LIMITS MIN	LIMITS (NOTE 1) TYP	LIMITS MAX	UNITS
MODE 0 - INPUT PORT (See Figure 4)						
Minimum Select Pulse Width	t_{SW}	5	-	180	360	ns
		10	-	90	180	ns
Minimum Write Pulse Width	t_{WW}	5	-	90	180	ns
		10	-	45	90	ns
Minimum Clear Pulse Width	t_{CLR}	5	-	80	160	ns
		10	-	40	80	ns

Dynamic Electrical Specifications At T_A = -40°C to +85°C, V_{DD} = ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, and 1 TTL Load **(Continued)**

PARAMETER		V_{DD} (V)	LIMITS MIN	LIMITS (NOTE 1) TYP	LIMITS MAX	UNITS
Minimum Data Setup Time	t_{DS}	5	-	-10	0	ns
		10	-	-5	0	ns
Minimum Data Hold Time	t_{DH}	5	-	75	150	ns
		10	-	35	75	ns
Data Out Hold Time (Note 2)	t_{DOH}	5	30	185	370	ns
		10	15	100	200	ns
Propagation Delay Times, t_{PLH}, t_{PHL} Select to Data Out (Note 2)	t_{SDO}	5	30	185	370	ns
		10	15	100	200	ns
Clear to SR	t_{RSR}	5	-	170	340	ns
		10	-	85	170	ns
Clock to SR	t_{CSR}	5	-	110	220	ns
		10	-	55	110	ns
Select to SR	t_{SSR}	5	-	120	240	ns
		10	-	60	120	ns

NOTES:

1. Typical values are for T_A = 25°C and nominal V_{DD}.
2. Minimum value is measured from CS2, maximum value is measured from CS1/$\overline{CS1}$.

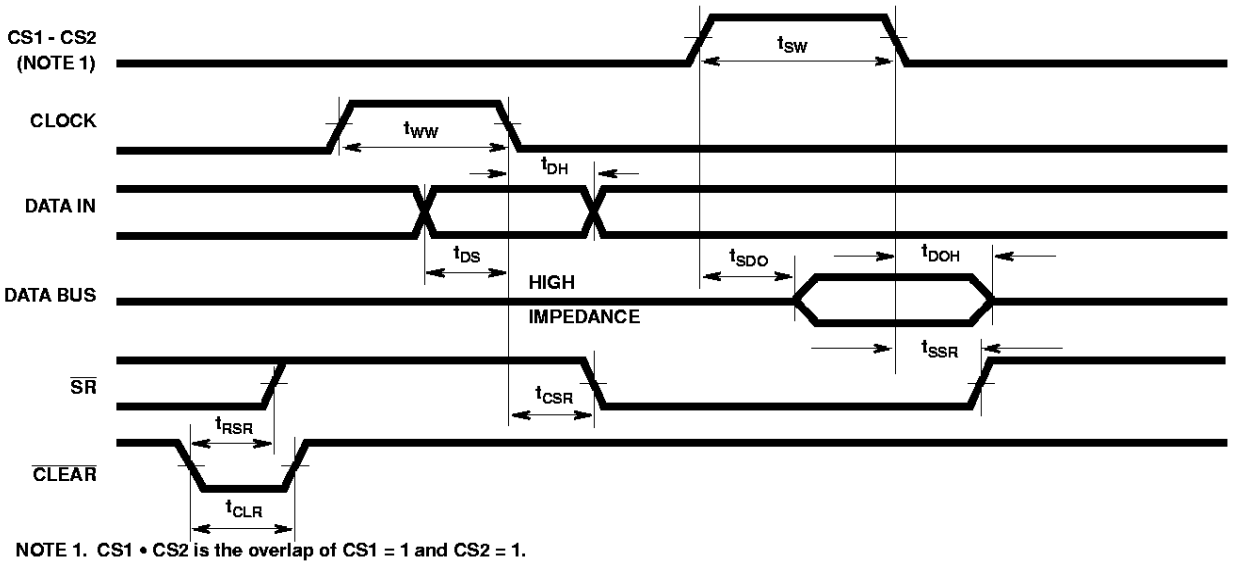
Input Port Mode 0 - Typical Operation

General Operation

When the mode control is tied to V_{SS}, the CDP1852 becomes an input port. In this mode, the peripheral device places data into the CDP1852 with a strobe pulse and the CDP1852 signals the microprocessor that data is ready to be transferred on the strobe's trailing edge via the $\overline{SR}$ output line. The CDP1802 then issues an input instruction that enables the CDP1852 to place the information from the peripheral device on the data bus to be entered into a memory location and the accumulator of the microprocessor.

Detailed Operation (See Figure 5)

The STROBE from the peripheral device places DATA into the 8-bit register of the CDP1852 when it goes high and latches the DATA on its trailing edge. The $\overline{SR}$ output is set low on the strobe's trailing edge. This output is connected to a flag line of the CDP1802 microprocessor and software polling will determine that the flag line has gone low and peripheral data is ready to be transferred. The CDP1802 then issues an input instruction that places an N_X line high. With the $\overline{MRD}$ line also high, the CDP1852 is selected and its output drivers place the DATA from the peripheral device on the DATA BUS. When the CDP1802 selected the CDP1852, it also selected and addressed the memory via one of the 16 internal address registers selected by an internal "X" register. The data from the CDP1852 is therefore entered into the memory [Bus → M(R(X))]. The data is also transferred to the D register (accumulator) in the microprocessor (Bus → D). When the CDP1802's execute cycle is completed, the CDP1852 is deselected by the N_X line returning low and its data output pins are three-stated. The $\overline{SR}$ output returns high.



NOTE 1. CS1 • CS2 is the overlap of CS1 = 1 and CS2 = 1.

MODE 0 TRUTH TABLE

CLOCK	† CS1-CS2	$\overline{CLEAR}$	DATA OUT EQUALS
X	0	X	High Impedance
0	1	0	0
0	1	1	Data Latch
1	1	X	Data In

† CS1 • CS2: CS1 = 1, CS2 = 1

SERVICE REQUEST TRUTH TABLE

CLOCK ↓	CS1 or CS2 or $\overline{CLEAR}$ ↓
$\overline{SR}$/SR 0	$\overline{SR}$/SR 1

FIGURE 4. MODE 0 INPUT PORT TIMING WAVEFORMS AND TRUTH TABLES

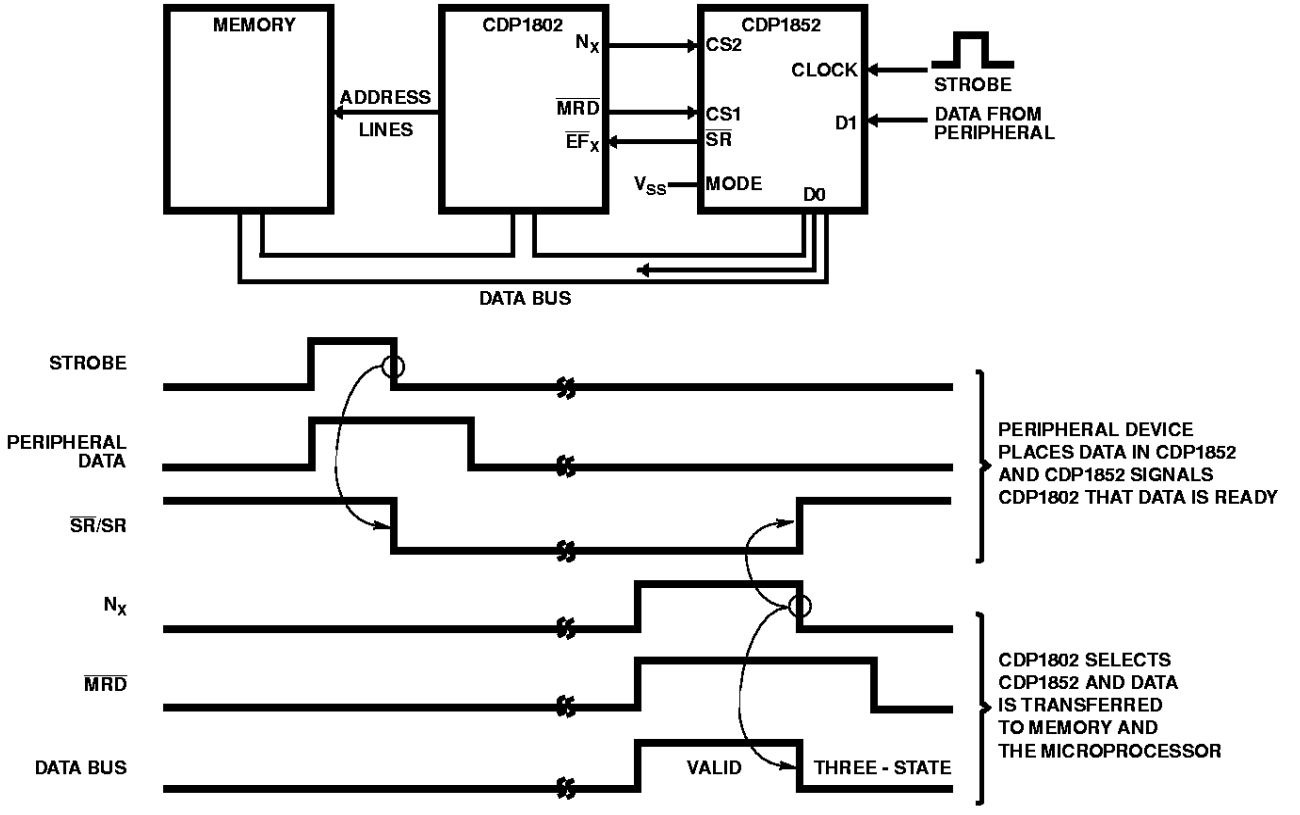


FIGURE 5. INPUT PORT MODE 0 FUNCTIONAL DIAGRAM AND WAVEFORMS - TYPICAL OPERATION

Dynamic Electrical Specifications At T_A = -40°C to +85°C, V_{DD} = ±5%, t_R, t_F = 20ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100pF, and 1 TTL Load

PARAMETER		V_{DD} (V)	LIMITS MIN	LIMITS (NOTE 1) TYP	LIMITS MAX	UNITS
MODE 1- OUTPUT PORT (See Figure 6)						
Minimum Clock Pulse Width	t_{CLK}	5	-	130	260	ns
		10	-	65	130	ns
Minimum Write Pulse Width	t_{WW}	5	-	130	260	ns
		10	-	65	130	ns
Minimum Clear Pulse Width	t_{CLR}	5	-	60	120	ns
		10	-	30	60	ns
Minimum Data Setup Time	t_{DS}	5	-	-10	0	ns
		10	-	-5	0	ns
Minimum Data Hold Time	t_{DH}	5	-	75	150	ns
		10	-	35	75	ns
Minimum Select-After-Clock Hold Time	t_{SH}	5	-	-10	0	ns
		10	-	-5	0	ns
Propagation Delay Times, t_{PLH}, t_{PHL} Clear to Data Out	t_{RDO}	5	-	140	280	ns
		10	-	70	140	ns
Write to Data Out	t_{WDO}	5	-	220	440	ns
		10	-	110	220	ns
Data In to Data Out	t_{DDO}	5	-	100	200	ns
		10	-	50	100	ns
Clear to SR	t_{RSR}	5	-	120	240	ns
		10	-	60	120	ns
Clock to SR	t_{CSR}	5	-	120	240	ns
		10	-	60	120	ns
Select to SR	t_{SSR}	5	-	120	240	ns
		10	-	60	120	ns

NOTE:

1. Typical values are for T_A = 25°C and nominal V_{DD}.

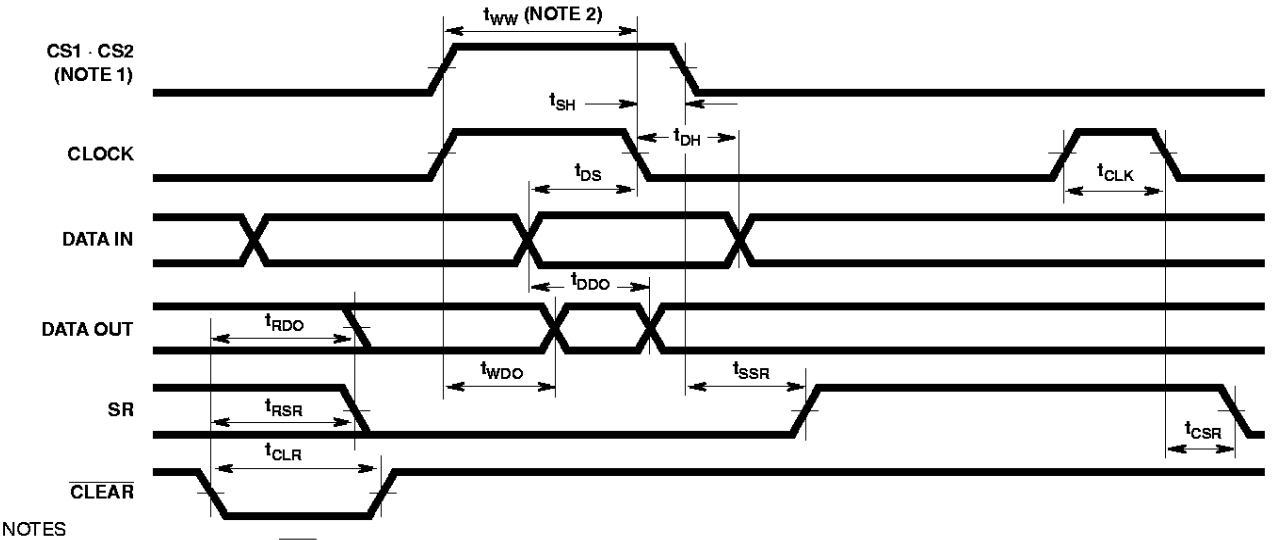
Output Port Mode 1 - Typical Operation

General Operation

Connecting the mode control to V_{DD} configures the CDP1852 as an output port. The output drivers are always on in this mode, so any data in the 8-bit register will be present at the data-out lines when the CDP1852 is selected. The N line and $\overline{MRD}$ connections between the CDP1852 and CDP1802 remain the same as in the input mode configuration, but now the clock input of the CDP1852 is tied to the TPB output of the CDP1802 and the SR output of the CDP1852 will be used to signal the peripheral device that valid data is present on its input lines. The microprocessor issues an output instruction, and data from the memory is strobed into the CDP1852 with the TPB pulse. When the CDP1852 is deselected, the SR output goes high to signal the peripheral device.

Detailed Operation (See Figure 7)

The CDP1802 issues an output instruction. The N_X line goes high and the $\overline{MRD}$ line goes low. The memory is accessed M(R(X)) → BUS and places data on the DATA BUS. This data are strobed into the 8-bit register of the CDP1852 when TPB goes high and latched on the TPB's trailing edge. The valid data thus appears on the CDP1852 output lines. When the CDP1802 output instruction cycle is complete, the N_X line goes low and the SR output goes high. SR will remain high until the trailing edge of the next TPB pulse, when it will return low.



NOTES
1. CS1 • CS2 is the overlap of $\overline{CS1}$ = 0 and CS2 = 1.
2. Write is the overlap of CS1 • CS2 and CLOCK.

MODE 1 TRUTH TABLE

CLOCK	† $\overline{CS1}$-CS2	$\overline{CLEAR}$	DATA OUT EQUALS
0	X	0	0
0	X	1	Data Latch
X	0	1	Data Latch
1	1	X	Data In

† $\overline{CS1}$ • CS2 : $\overline{CS1}$ = 0, CS2 = 1

SERVICE REQUEST TRUTH TABLE

$\overline{CS1}$ or CS2 ↕	CLOCK or $\overline{CLEAR}$ ↓
$\overline{SR}$/SR 1	$\overline{SR}$/SR 0

FIGURE 6. MODE 1 OUTPUT PORT TIMING WAVEFORMS AND TRUTH TABLES

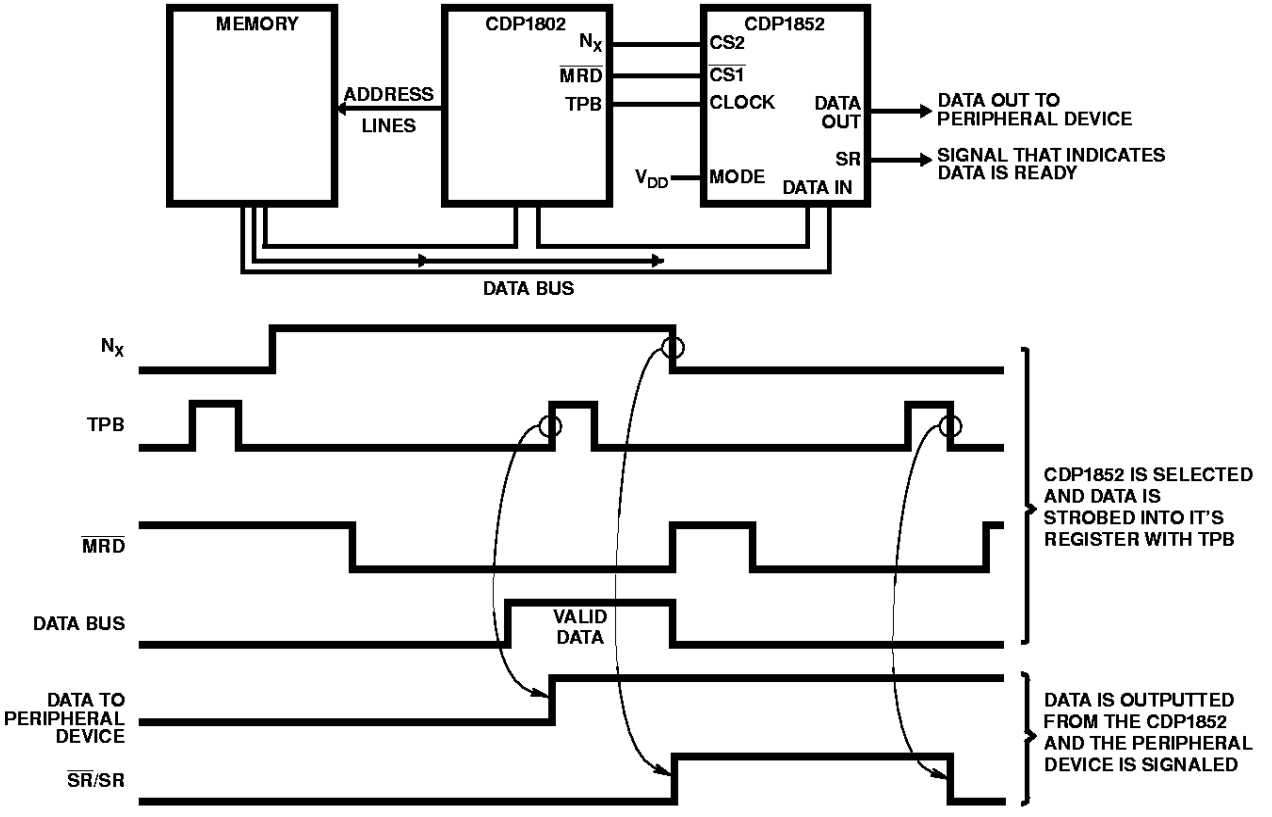


FIGURE 7. OUTPUT PORT MODE 1 FUNCTIONAL DIAGRAM AND WAVEFORMS - TYPICAL OPERATION

Application Information

In a CDP1800 series microprocessor-based system where $\overline{MRD}$ is used to distinguish between INP and OUT instructions, an INP instruction is assumed to occur at the beginning of every I/O cycle because $\overline{MRD}$ starts high. Therefore, at the start of an OUT instruction, which uses the same 3-bit N code as that used for selection of an input port, the input device is selected for a short time (see Figure 8). This condition forces SR low and sets the internal SR latch (see Figure 3). In a small system with unique N codes for inputs and outputs, this situation does not arise. Using the CDP1853 N-bit decoder or equivalent logic to decode the N lines after TPA prevents dual selection in larger systems (see Figure 9 and Figure 10).

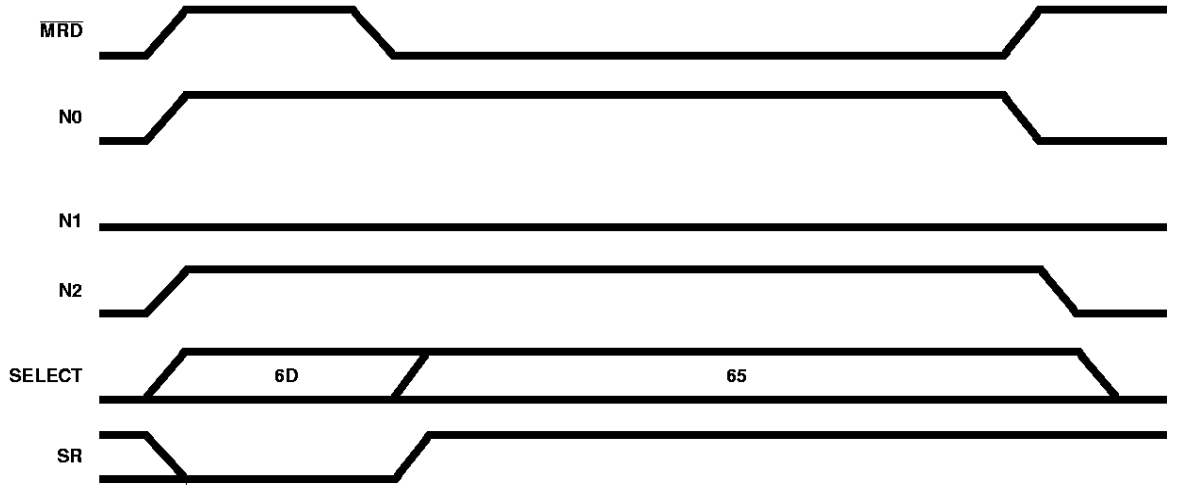


FIGURE 8. EXECUTION OF A "65" OUTPUT INSTRUCTION SHOWING MOMENTARY SELECTION OF INPUT PORT "D"

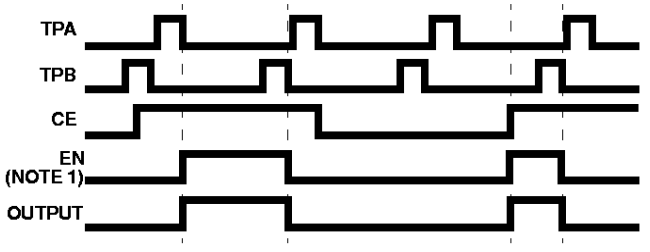


FIGURE 9. CDP1853 TIMING WAVEFORMS

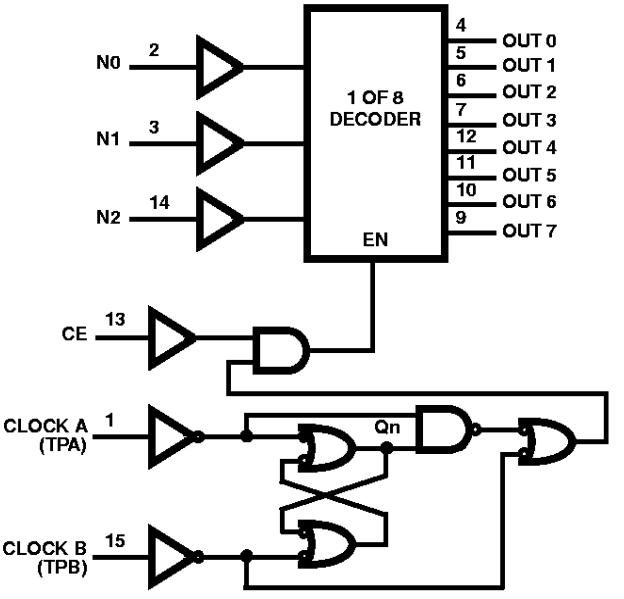


FIGURE10. CDP1853 FUNCTIONAL DIAGRAM

NOTE:

1. Output enabled when EN = HIGH. Internal signal shown for reference only (See Figure 1).