# 74LVC138A

## 3-to-8 line decoder/demultiplexer; inverting

Rev. 5 — 19 October 2011 Product data sheet

## 1. General description

The 74LVC138A is a 3-to-8 line decoder/demultiplexer. It accepts three binary weighted address inputs (A0, A1 and A2) and, when enabled, provides eight mutually exclusive outputs ($\overline{Y}0$ to $\overline{Y}7$) that are LOW when selected.

There are three enable inputs: two active LOW ($\overline{E}1$ and $\overline{E}2$) and one active HIGH (E3). Every output will be HIGH unless $\overline{E}1$ and $\overline{E}2$ are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LVC138A devices and one inverter. The 74LVC138A can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

## 2. Features and benefits

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Mutually exclusive outputs
- Output drive capability 50 Ω transmission lines at 125 °C
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC138AD | −40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74LVC138ADB | −40 °C to +125 °C | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74LVC138APW | −40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74LVC138ABQ | −40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal-enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

## 4. Functional diagram

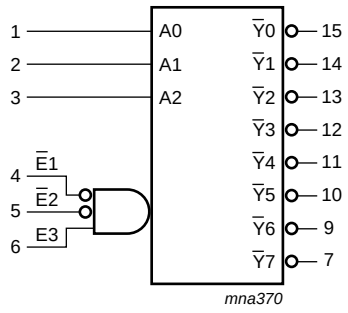



**Fig 1. Logic symbol**

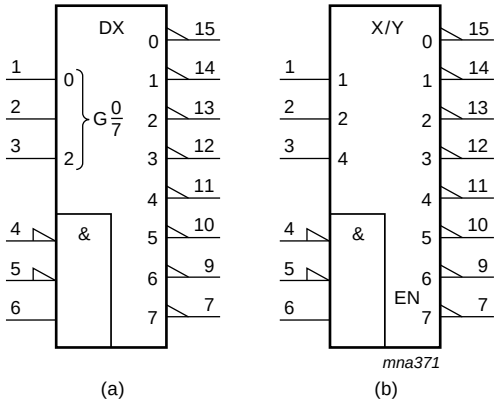



**Fig 2. IEC logic symbol**

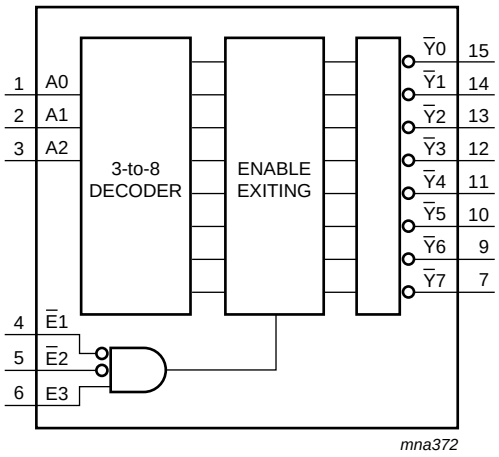



**Fig 3. Functional diagram**

# 5. Pinning information

## 5.1 Pinning

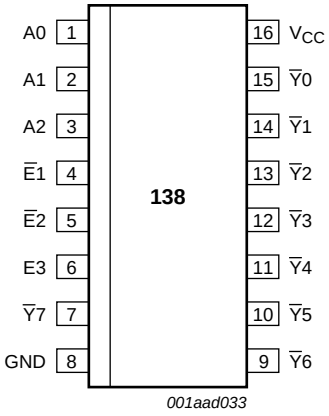
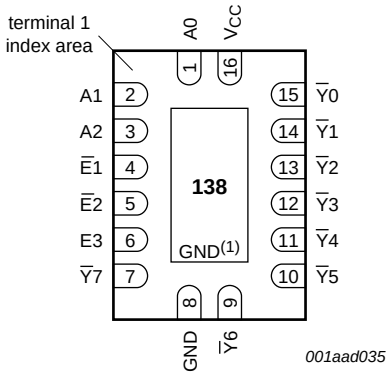



Fig 4. Pin configuration for SO16 and (T)SSOP16




Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration for DHVQFN16

## 5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|---|---|
| A0 | 1 | address input |
| A1 | 2 | address input |
| A2 | 3 | address input |
| $\overline{E}1$ | 4 | enable input (active LOW) |
| $\overline{E}2$ | 5 | enable input (active LOW) |
| E3 | 6 | enable input (active HIGH) |
| GND | 8 | ground (0 V) |
| $\overline{Y}[0:7]$ | 15, 14, 13, 12, 11, 10, 9, 7 | output |
| $V_{CC}$ | 16 | supply voltage |

## 6. Functional description

**Table 3. Function table [1]**

| Input | | | | | | Output | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{E1}$ | $\overline{E2}$ | E3 | A0 | A1 | A2 | $\overline{Y0}$ | $\overline{Y1}$ | $\overline{Y2}$ | $\overline{Y3}$ | $\overline{Y4}$ | $\overline{Y5}$ | $\overline{Y6}$ | $\overline{Y7}$ |
| H | X | X | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | L | X | X | X | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | L | H | H | H | H | H | H | H |
| | | | H | L | L | H | L | H | H | H | H | H | H |
| | | | L | H | L | H | H | L | H | H | H | H | H |
| | | | H | H | L | H | H | H | L | H | H | H | H |
| | | | L | L | H | H | H | H | H | L | H | H | H |
| | | | H | L | H | H | H | H | H | H | L | H | H |
| | | | L | H | H | H | H | H | H | H | H | L | H |
| | | | H | H | H | H | H | H | H | H | H | H | L |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | −0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | −50 | - | mA |
| $V_I$ | input voltage | | [1] | −0.5 | +6.5 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | | - | ±50 | mA |
| $V_O$ | output voltage | output HIGH or LOW state | [2] | −0.5 | $V_{CC}$ + 0.5 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | | - | ±50 | mA |
| $I_{CC}$ | supply current | | | - | 100 | mA |
| $I_{GND}$ | ground current | | | −100 | - | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = −40 °C to +125 °C | [3] | - | 500 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO16 packages: above 70 °C the value of $P_D$ derates linearly with 8 mW/K.
For (T)SSOP16 packages: above 60 °C the value of $P_D$ derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C the value of $P_D$ derates linearly with 4.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.65 | - | 3.6 | V |
| | | functional | 1.2 | - | - | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | V |
| $V_O$ | output voltage | output HIGH or LOW state | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | −40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 1.65 V to 2.7 V | 0 | - | 20 | ns/V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 0 | - | 10 | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | −40 °C to +85 °C | | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.2 V | 1.08 | - | - | 1.08 | - | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | - | - | 0.65 × $V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.2 V | - | - | 0.12 | - | 0.12 | V |
| | | $V_{CC}$ = 1.65 V to 1.95 V | - | - | 0.35 × $V_{CC}$ | - | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = −100 μA; $V_{CC}$ = 1.65 V to 3.6 V | $V_{CC}$ − 0.2 | - | - | $V_{CC}$ − 0.3 | - | V |
| | | $I_O$ = −4 mA; $V_{CC}$ = 1.65 V | 1.2 | - | - | 1.05 | - | V |
| | | $I_O$ = −8 mA; $V_{CC}$ = 2.3 V | 1.8 | - | - | 1.65 | - | V |
| | | $I_O$ = −12 mA; $V_{CC}$ = 2.7 V | 2.2 | - | - | 2.05 | - | V |
| | | $I_O$ = −18 mA; $V_{CC}$ = 3.0 V | 2.4 | - | - | 2.25 | - | V |
| | | $I_O$ = −24 mA; $V_{CC}$ = 3.0 V | 2.2 | - | - | 2.0 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = 100 μA; $V_{CC}$ = 1.65 V to 3.6 V | - | - | 0.2 | - | 0.3 | V |
| | | $I_O$ = 4 mA; $V_{CC}$ = 1.65 V | - | - | 0.45 | - | 0.65 | V |
| | | $I_O$ = 8 mA; $V_{CC}$ = 2.3 V | - | - | 0.6 | - | 0.8 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | - | 0.4 | - | 0.6 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | - | 0.55 | - | 0.8 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 3.6 V; $V_I$ = 5.5 V or GND | - | ±0.1 | ±5 | - | ±20 | μA |

**Table 6. Static characteristics** *...continued*

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | −40 °C to +85 °C | | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $I_{CC}$ | supply current | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A | - | 0.1 | 10 | - | 40 | μA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 2.7 V to 3.6 V; $V_I$ = $V_{CC}$ − 0.6 V; $I_O$ = 0 A | - | 5 | 500 | - | 5000 | μA |
| $C_I$ | input capacitance | $V_{CC}$ = 0 V to 3.6 V; $V_I$ = GND to $V_{CC}$ | - | 4.0 | - | - | - | pF |

[1] All typical values are measured at $V_{CC}$ = 3.3 V (unless stated otherwise) and $T_{amb}$ = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.*

| Symbol | Parameter | Conditions | | −40 °C to +85 °C | | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | An to $\overline{Y}$n; see Figure 6 | [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 14 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | 0.5 | 5.2 | 11.5 | 0.5 | 12.7 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 1.5 | 3.0 | 6.5 | 1.5 | 7.3 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.5 | 3.2 | 6.8 | 1.5 | 8.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 1.0 | 2.7 | 5.8 | 1.0 | 7.5 | ns |
| | | E3 to $\overline{Y}$n; see Figure 6 | [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 14 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | 1.0 | 5.5 | 11.4 | 1.0 | 12.5 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 1.5 | 3.2 | 6.5 | 1.5 | 7.1 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.5 | 3.3 | 6.8 | 1.5 | 8.5 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 1.0 | 2.9 | 5.8 | 1.0 | 7.5 | ns |
| | | $\overline{E}$n to $\overline{Y}$n; see Figure 7 | [2] | | | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 15 | - | - | - | ns |
| | | $V_{CC}$ = 1.65 V to 1.95 V | | 1.0 | 5.6 | 11.5 | 1.0 | 12.8 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 1.8 | 3.3 | 6.5 | 1.8 | 7.3 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.5 | 3.4 | 6.4 | 1.5 | 8.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | 1.0 | 2.9 | 5.8 | 1.0 | 7.5 | ns |
| $t_{sk(o)}$ | output skew time | | [3] | - | - | 1.0 | - | 1.5 | ns |

**Table 7. Dynamic characteristics** *…continued*

*Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.*

| Symbol | Parameter | Conditions | −40 °C to +85 °C | | | −40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $C_{PD}$ | power dissipation capacitance | $V_I$ = GND to $V_{CC}$ [4] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | - | 9.9 | - | | | pF |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | 15.8 | - | | | pF |
| | | $V_{CC}$ = 3.0 V to 3.6 V | - | 21.1 | - | | | pF |

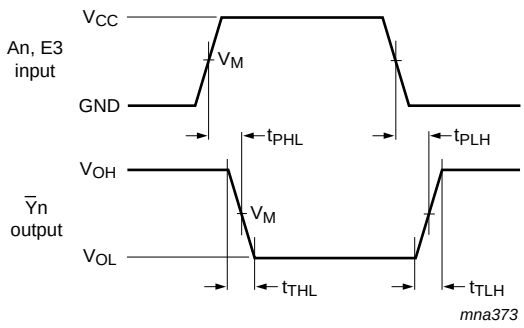
[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz
$C_L$ = output load capacitance in pF
$V_{CC}$ = supply voltage in V
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

## 11. Waveforms

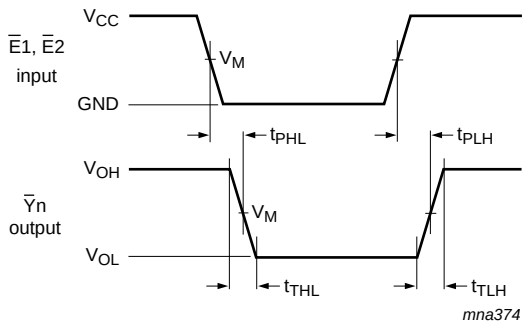



$V_M$ = 1.5 V at $V_{CC} \geq$ 2.7 V;

$V_M$ = 0.5 × $V_{CC}$ at $V_{CC}$ < 2.7 V;

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 6. The inputs An, E3 to outputs $\overline{Y}$n propagation delays**

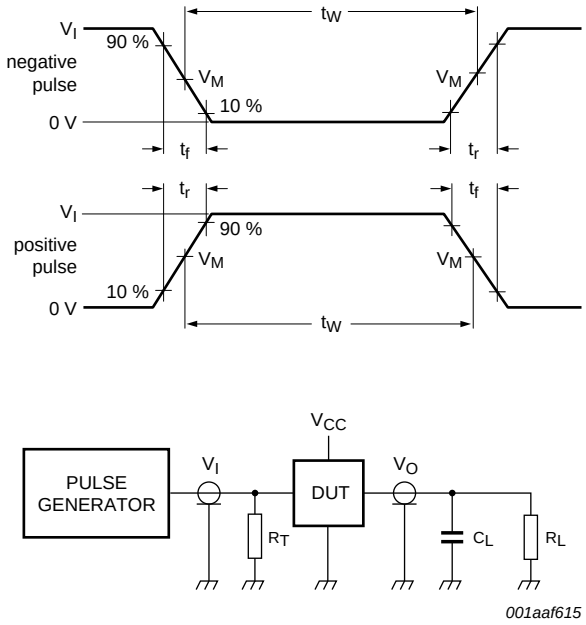



$V_M$ = 1.5 V at $V_{CC} \geq$ 2.7 V;

$V_M$ = 0.5 × $V_{CC}$ at $V_{CC}$ < 2.7 V;

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 7. The inputs $\overline{E}$n to outputs $\overline{Y}$n propagation delays**




Test data is given in Table 8. Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

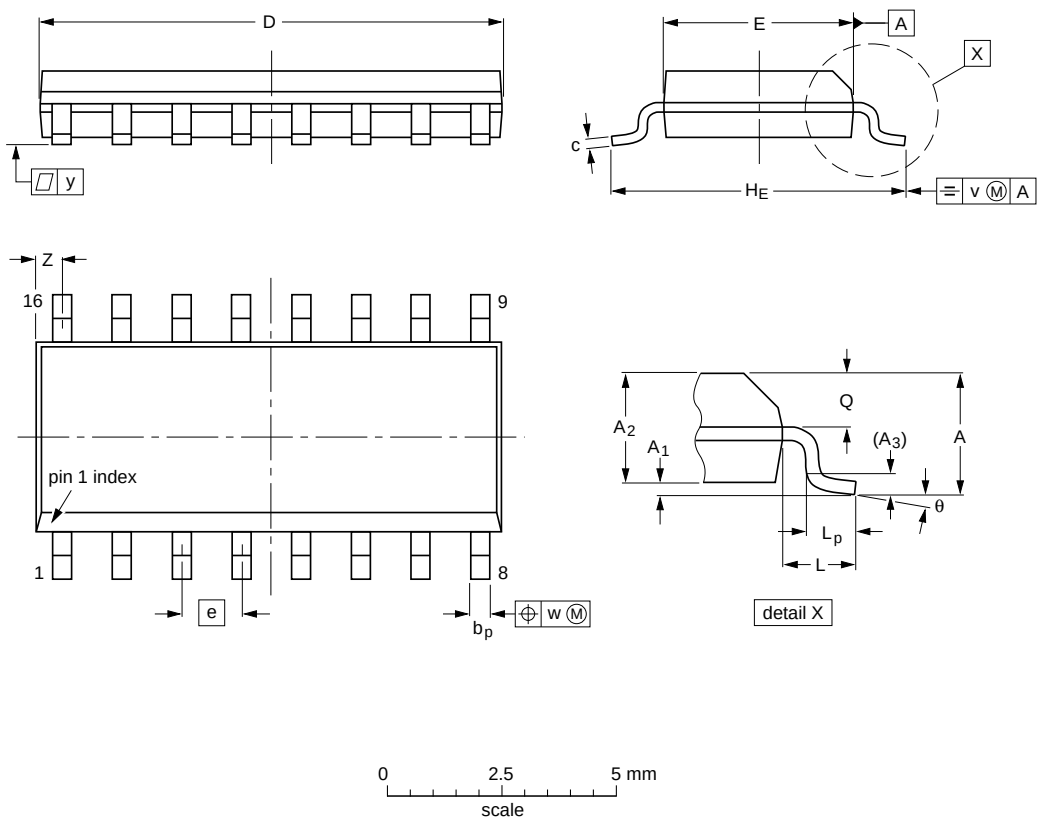
**Fig 8. Test circuit for measuring switching times**

**Table 8. Test data**

| Supply voltage | Input | | Load | |
|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ |
| 1.2 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 1 kΩ |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 1 kΩ |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2 ns | 30 pF | 500 Ω |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω |

## 12. Package outline

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

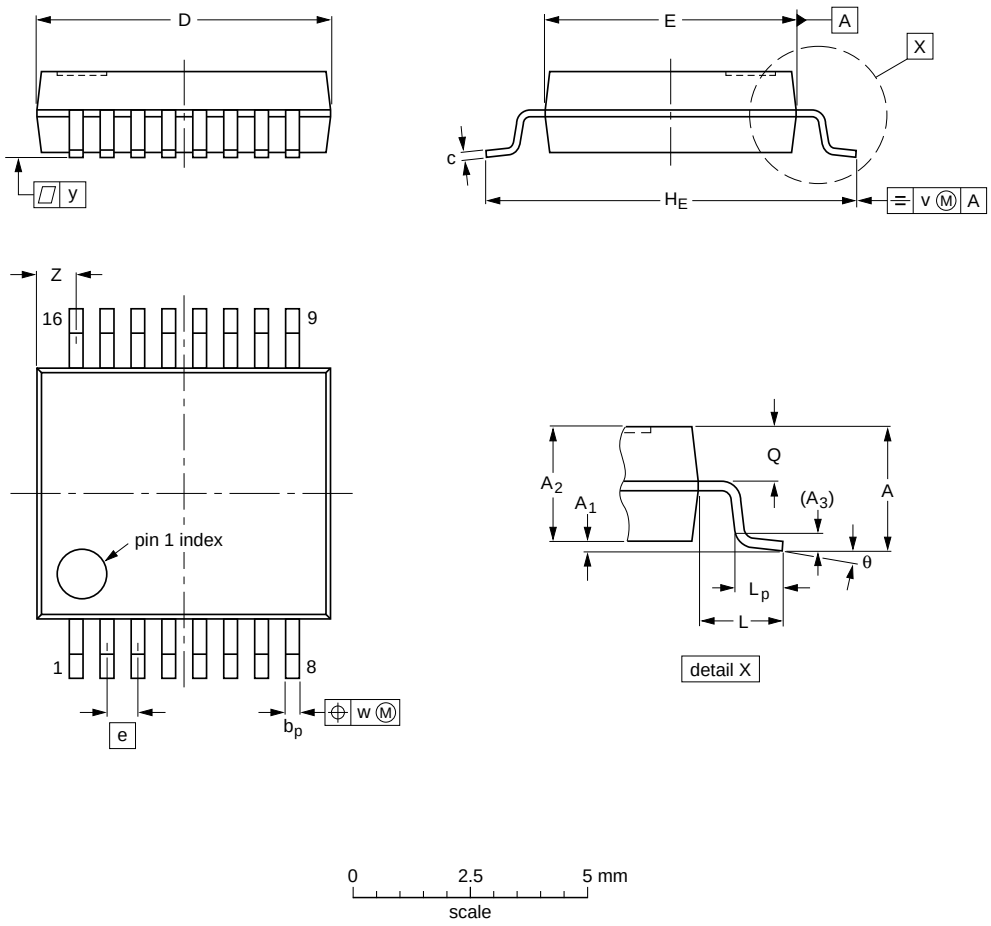
**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 9. Package outline SOT109-1 (SO16)**

**SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm** **SOT338-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 6.4<br>6.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.00<br>0.55 | $8^o$<br>$0^o$ |

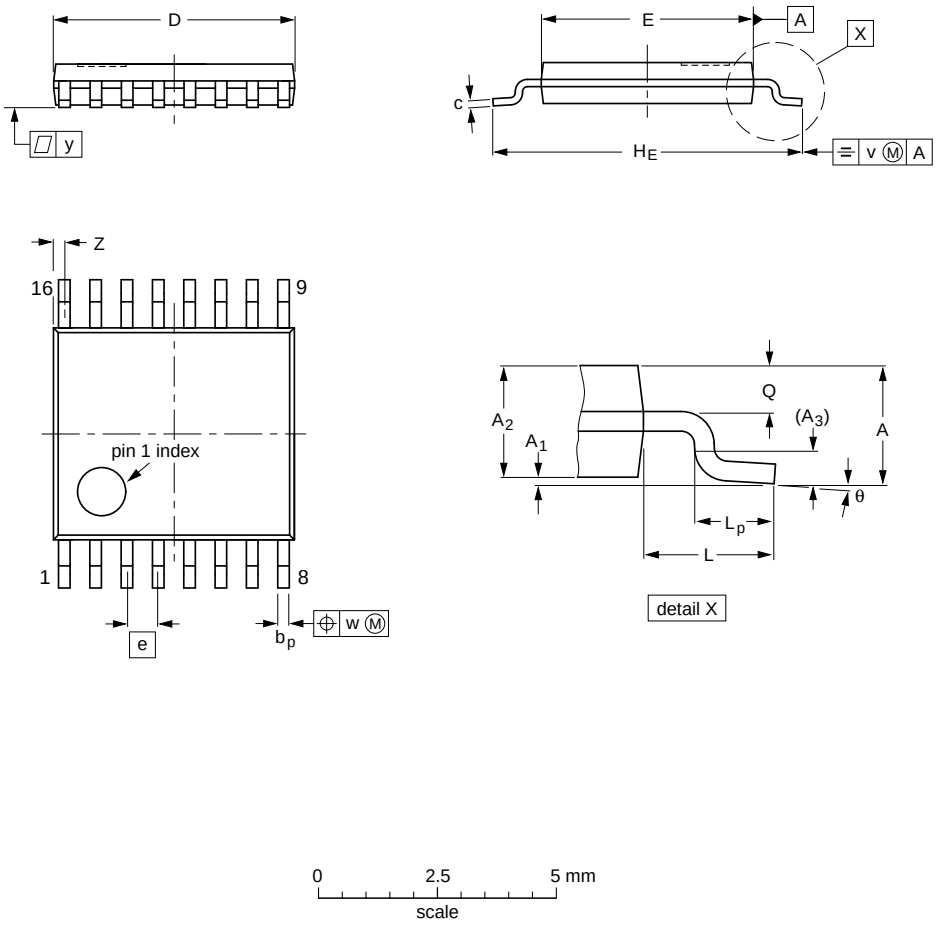
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT338-1 | | MO-150 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 10. Package outline SOT338-1 (SSOP16)**

**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | $8^o$<br>$0^o$ |

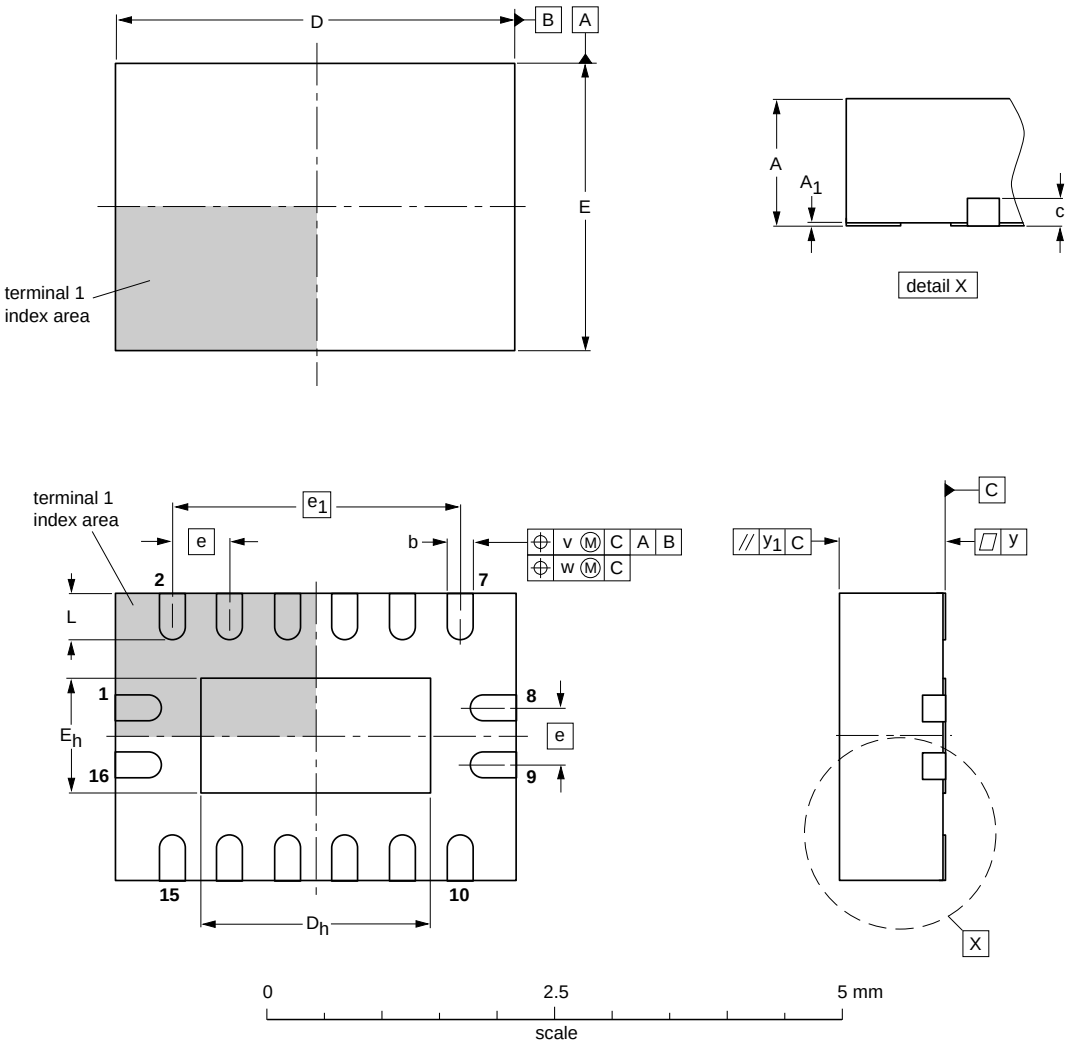
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 11. Package outline SOT403-1 (TSSOP16)**

**DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm** **SOT763-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 3.6<br>3.4 | 2.15<br>1.85 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 2.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT763-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

**Fig 12. Package outline SOT763-1 (DHVQFN16)**

## 13. Abbreviations

**Table 9. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 10. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC138A v.5 | 20111019 | Product data sheet | - | 74LVC138A v.4 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Table 4, Table 5, Table 6, Table 7 and Table 8: values added for lower voltage ranges. | | | |
| 74LVC138A v.4 | 20030506 | Product specification | - | 74LVC138A v.3 |
| 74LVC138A v.3 | 20020312 | Product specification | - | 74LVC138A v.2 |
| 74LVC138A v.2 | 19980428 | Product specification | - | 74LVC138A v.1 |
| 74LVC138A v.1 | - | - | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 17. Contents





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