SL38000

Programmable 4-PLL CG with VCXO and SSCG

Key Features

- 4 Programmable PLLs with up to 9 Clock Outputs and 2 REFCLKs
- Wide 2.5V to 3.3V +/-10% power supply range
- CLKOUTs support 3.3V to 2.5V or 1.8V +/-10%
- Low power dissipation and low jitter
- Programmable VCXO and SSCG options
- EEPROM or I2C Programmability
- Programmable Center or Down Spread Modulation from 0.25 to 5.0%
- 8 to 48 MHz external crystal range
- 8 to 166 MHz external clock input range
- Programmable 1 to 200 MHz clock output range
- Integrated internal voltage regulator
- Programmable PD#/OE/SSON#/FS functions
- Programmable CL at XIN and XOUT pins
- Programmable output rise and fall times
- 28-pin TSSOP package with commercial and industrial temperature ranges

Applications

- Printers, MFPs, Digital Copiers
- DTV, HDTV, DVD-R/W and STB
- General Purpose Frequency Synthesising

Description

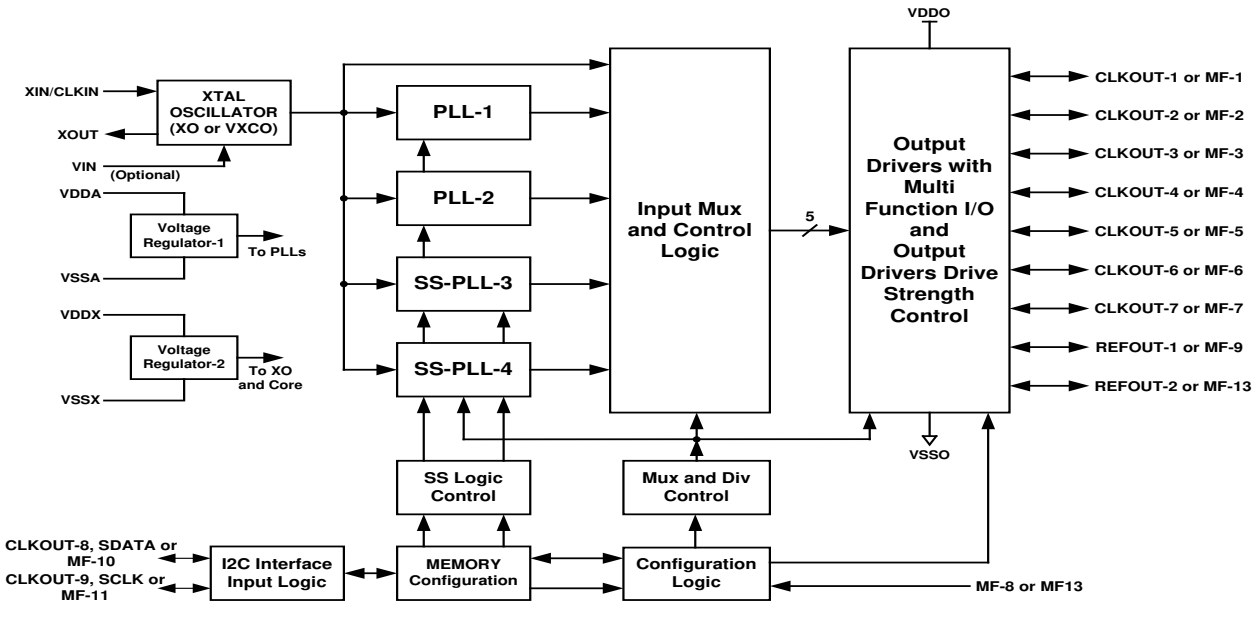
The SL38000 a fully integrated 4 PLL programmable low power Clock Generator with SSCG and VCXO functions used for reducing Electromagnetic Interference (EMI) and general purpose frequency synthesizing. The product is designed using SpectraLinear proprietary programmable **EProClock™** phase-locked loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the input clock. The modulated clock can significantly reduce the measured EMI levels, and leading to the compliance with regulatory agency requirements.

Up to 9 output clock frequencies and 2 REFOUT clocks, Spread %, output rise and fall times for each clock outputs, crystal load, modulation frequency and PD#/OE/SSON#/FS functions can be programmed to meet the needs of wide range of applications. The SL38000 operates from 2.5V to 3.3V power supply voltage range. The output clocks (CLKOUTs) can support 3.3 to 2.5V or 1.8V +/-10%. The product is offered in 28-pin TSSOP package with commercial and industrial grades.

Benefits

- Peak EMI reduction of 8 to 16 dB
- Fast time-to-market
- Cost Reduction
- Reduction of PCB layers
- Eleminates the need for XOs and VCXOs

Block Diagram



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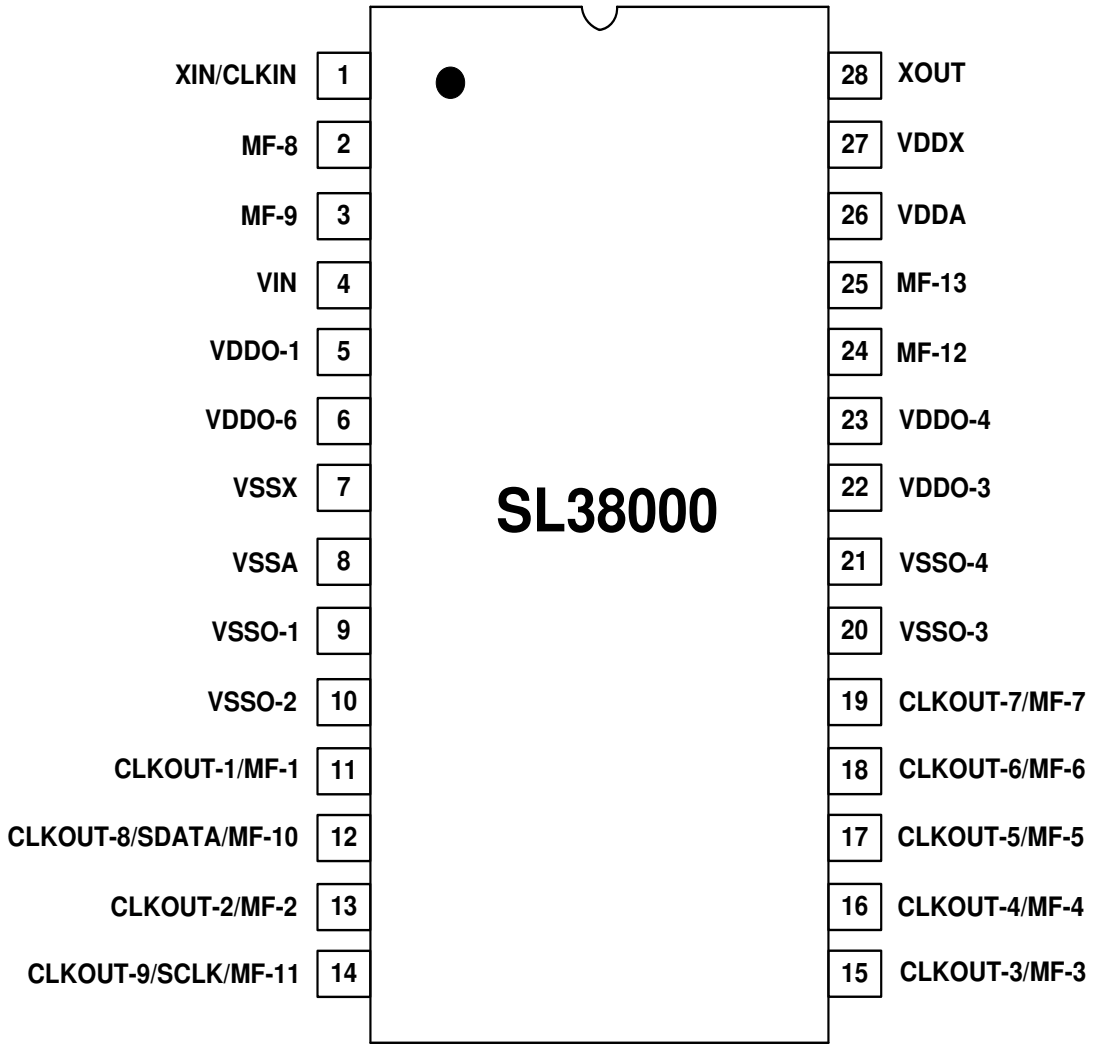
Pin Configuration



28-Pin TSSOP Package

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	XIN/CLKIN	Input	Crystal oscillator or external clock input.
2	MF-8	Input	Multi function input/output. Programmed as OE, FS. There is no programmable pull-up/down resistor.
3	MF-9	I/O	Multi function input/output. Programmed as REFOUT-1, OE, PD#, SSON# or FS. Only programmable pull-up resistor available.
4	VIN	Input	VCXO control pin VIN.
11	CLKOUT-1 or MF-1	I/O	Programmable Clock Output-1. This pin can be programmed as OE, PD#, SSON# or FS. Programmable pull-up/down resistor is available.
12	CLKOUT-8, SDATA or MF-10	I/O	Programmed as Clock Output-8 or Serial Data Input or multi function input. This pin can be programmed as OE, PD#, SSON# or FS. Programmable pull-up/down resistor is available.
13	CLKOUT-2 or MF-2	I/O	Programmable Clock Output-2. This pin can be programmed as OE, PD#, SSON# or FS. This pin can be programmed as OE, PD#, SSON# or FS. Programmable pull-up/down resistor is available.
14	CLKOUT-9, SCLK or MF-11	I/O	Programmable Clock Output-9, Serial Data Input Clock or multi function input. This pin can be programmed as OE, PD#, SSON# or FS. Programmable pull-up/down resistor is available.
15	CLKOUT-3 or MF-3	I/O	Programmable Clock Output-3. This pin can be programmed as OE, PD#, SSON# or FS. Programmable pull-up/down resistor is available.
16	CLKOUT-4 or MF-4	I/O	Programmable Clock Output-4. This pin can be programmed as OE, PD#, SSON# or FS. Programmable pull-up/down resistor is available.
17	CLKOUT-5 or MF-5	I/O	Programmable Clock Output-5. This pin can be programmed as OE, PD#, SSON# or FS. Programmable pull-up/down resistor is available.
18	CLKOUT-6 or MF-6	I/O	Programmable Clock Output-6. This pin can be programmed as OE, PD#, SSON# or FS. Programmable pull-up/down resistor is available.
19	CLKOUT-7 or MF-7	I/O	Programmable Clock Output-7. This pin can be programmed as OE, PD#, SSON# or FS. Programmable pull-up/down resistor is available.
24	MF-12	Input	Multi function input. Programmed as OE, PD#, SSON# or FS. Programmable pull-up/down resistor is available.
25	MF-13	I/O	Multi function input/output. Programmed as REFOUT-2, OE, PD#, SSON# or FS. Programmable pull-up/down resistor is available.
26	VDDA	Power	Power supply, 3.3V to 2.5V, for PLLs.
27	VDDX	Power	Power supply, 3.3V to 2.5V, for oscillator and core logic.
7	VSSX	Power	Power supply ground for oscillator and core logic.
8	VSSA	Power	Power supply ground for PLLs.
5	VDDO-1	Power	Power supply for CLKOUT-3, 3.3V to 2.5V or 1.8V, VDDO ≤ VDD.
6	VDDO-2	Power	Power supply for CLKOUT-1/2/8/9, 3.3V to 2.5V or 1.8V, VDDO ≤ VDD.

22	VDDO-3	Power	Power supply for CLKOUT-5/6/7, 3.3V to 2.5V or 1.8V, VDDO ≤ VDD.
23	VDDO-4	Power	Power supply for CLKOUT-4, 3.3V to 2.5V or 1.8V, VDDO ≤ VDD.
9	VSSO-1	Power	Power ground for CLKOUT-3.
10	VSSO-2	Power	Power ground for CLKOUT-1/2/8/9.
20	VSSO-3	Power	Power ground for CLKOUT-5/6/7.
21	VSSO-4	Power	Power ground for CLKOUT-4.
28	XOUT	Output	Leave unconnected when external clock is used.

Absolute Maximum Ratings

Description	Condition	Min	Max	Unit
Supply voltage, VDD	**VDDA and VDDX**	**-0.5**	**4.2**	**V**
Supply voltage, VDDO	**VDDO≤VDDA=VDDX**	**-**	**VDD**	**V**
All Inputs and Outputs		**-0.5**	**VDD+0.5**	**V**
Ambient Operating Temperature	**In operation, C-Grade**	**0**	**70**	**°C**
Ambient Operating Temperature	**In operation, I-Grade**	**-40**	**85**	**°C**
Storage Temperature	**No power is applied**	**-65**	**150**	**°C**
Junction Temperature	**In operation, power is applied**	**-**	**125**	**°C**
Soldering Temperature		**-**	**260**	**°C**
ESD Rating (Human Body Model)	**JEDEC22-A114D**	**-4,000**	**4,000**	**V**
ESD Rating (Charge Device Model)	**JEDEC22-C101C**	**-1,500**	**1,500**	**V**
ESD Rating (Machine Model)	**JEDEC22-A115D**	**-250**	**250**	**V**

DC Electrical Characteristics (C-Grade)

Unless otherwise stated VDDA=VDDX=2.5V to 3.3V+/-10%, CL=15pF and Ambient Temperature range 0 to +70 Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	V
Input Low Voltage	VIL	CMOS Level, Pins programmed as PD#, OE, SSON# or FS	0	-	0.3VDD	V
Input High Voltage	VIH	CMOS Level, Pins programmed as PD#, OE, SSON# or FS	0.7VDD	-	VDD	V
Output High Voltage	VOH1	IOH=-6mA , Pins programmed as CLKOUT/REFOUT	VDDO-0.5	-	-	V
Output Low Voltage	VOL1	IOL=6mA , Pins programmed as CLKOUT/REFOUT	-	-	0.5	V
Output High Voltage	VOH2	IOH=-4mA , Pins programmed as CLKOUT/REFOUT	VDDO-0.4	-	-	V
Output Low Voltage	VOL2	IOL=4mA , Pins programmed as CLKOUT/REFOUT	-	-	0.4	V

Input High Current	IIH	VIN=VDD, Input Pins are programmed as PD#, OE, SSON# or FS, and no pull-up/down resister used	-10	-	10	µA
Input Low Current	IIL	VIN=GND, Input Pins are programmed as PD#, OE, SSON# or FS, and no pull-up/down resister used	-10	-	10	µA
Pull-up or Down Resistors	RPU/D	If Programmed at pins PD#, OE, SSON#, FS and CLKOUT	100	175	250	kΩ
Operating Supply Current	IDD1	FIN=27MHz and all 7 clocks are at 33MHz and CL=0	-	16	TBD	mA
Operating Supply Current	IDD2	FIN=27MHz and all 9 clocks are at 66MHz and CL=0	-	22	TBD	mA
Standby Current	ISBC	PD#=GND	-	90	120	µA
Output Leakage Current	IOL	OE=GND at CLKOUT pins	-10	-	10	µA
Programmable Input Capacitance at Pins 1 and 28	Cin Cout	Minimum setting value	-	8	-	pF
		Maximum setting value	-	40	-	pF
		Resolution (programming steps)	-	0.5	-	pF
Input Capacitance	CIN2	Pins 4 and 8 if programmed as PD#, OE, SSON or FS	-	4	6	pF
Load Capacitance	CL	All CLKOUT outputs	-	-	15	pF

AC Electrical Characteristics (C-Grade)

Unless otherwise stated VDDA=VDDX= 2.5V to 3.3V+/-10%, CL=15pF and Ambient Temperature range 0 to +70 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal or Ceramic Resonator	8	-	48	MHz
Input Frequency Range	FIN2	External Clock	3	-	166	MHz
Output Frequency Range	FOUT1	CLKOUT, VDDO=3.3V to 2.5V	3	-	200	MHz
Output Frequency Range	FOUT2	CLKOUT, VDDO=1.8V	3	-	166	MHz
Output Frequency Range	FOUT3	REFCLK, crystal or resonator input	0.25	-	48	MHz
Output Duty Cycle	DC1	SSCLK	45	50	55	%
Output Duty Cycle	DC2	REFCLK , Xtal input	45	50	55	%
Output Duty Cycle	DC3	REFCLK, clock input	40	50	60	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	40	50	60	%
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ1	FIN=27MHz, all 7 clocks are programmed at 66MHz, CL=15pF	-	180	TBD	ps
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ2	FIN=27MHz, all 9 clocks are programmed at 66MHz, CL=15pF	-	220	TBD	ps
Power Supply Ramp Time	tPSR	Time for VDD reaching minimum specified value and monolithic power supply ramp	0	-	12	ms

PLL Lock Time	tPLL	Time from VDD reaching minimum specified value to valid output frequencies at all outputs	-	7.8	9.0	ms
PD# Power-up Time (Crystal or Clock)	tPU2	Time from PD# rising edge to valid frequency at outputs	-	5.0	7.0	ms
Output Enable Time	tOE	Time from OE falling edge to Hi-Z at outputs	-	200	350	ns
Output Disable Time	tOD	Time from OE falling edge to Hi-Z at outputs	-	200	350	ns
Spread Percent Range	SPR-1	Center Spread	+/-0.125	-	+/-2.5	%
Spread Percent Range	SPR-2	Down Spread	-5.0	-	-0.25	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	26	31.5	120	kHz

DC Electrical Characteristics (C-Grade)

Unless otherwise stated VDDA=VDDX=2.5V to 3.3V+/-10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	V
Input Low Voltage	VIL	CMOS Level, Pins programmed as PD#, OE, SSON# or FS	0	-	0.3VDD	V
Input High Voltage	VIH	CMOS Level, Pins programmed as PD#, OE, SSON# or FS	0.7VDD	-	VDD	V
Output High Voltage	VOH1	IOH=-6mA , Pins programmed as CLKOUT/REFOUT	VDDO-0.5	-	-	V
Output Low Voltage	VOL1	IOL=6mA , Pins programmed as CLKOUT/REFOUT	-	-	0.5	V
Output High Voltage	VOH2	IOH=-4mA , Pins programmed as CLKOUT/REFOUT	VDDO-0.4	-	-	V
Output Low Voltage	VOL2	IOL=4mA , Pins programmed as CLKOUT/REFOUT	-	-	0.4	V
Input High Current	IIH	VIN=VDD, Input Pins are programmed as PD#, OE, SSON# or FS, and no pull-up/down resister used	-15	-	15	µA
Input Low Current	IIL	VIN=GND, Input Pins are programmed as PD#, OE, SSON# or FS, and no pull-up/down resister used	-15	-	15	µA
Pull-up or Down Resistors	RPU/D	If Programmed at pins PD#, OE, SSON#, FS and CLKOUT	100	175	250	kΩ
Operating Supply Current	IDD1	FIN=27MHz and all 7 clocks are at 33MHz and CL=0	-	20	TBD	mA
Operating Supply Current	IDD2	FIN=27MHz and all 9 clocks are at 66MHz and CL=0	-	28	TBD	mA
Standby Current	ISBC	PD#=GND	-	140	200	µA

Output Leakage Current	IOL	OE=GND at CLKOUT pins	-15	-	15	µA
Programmable Input Capacitance at Pins 1 and 28	Cin Cout	Minimum setting value	-	8	-	pF
		Maximum setting value	-	40	-	pF
		Resolution (programming steps)	-	0.5	-	pF
Input Capacitance	CIN2	Pins 4 and 8 if programmed as PD#, OE, SSON or FS	-	4	6	pF
Load Capacitance	CL	All CLKOUT outputs	-	-	15	pF

AC Electrical Characteristics (C-Grade)

Unless otherwise stated VDDA=VDDX= 2.5V to 3.3V+/-10%, CL=15pF and Ambient Temperature range -40 to +85 Deg C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	Crystal or Ceramic Resonator	8	-	48	MHz
Input Frequency Range	FIN2	External Clock	3	-	166	MHz
Output Frequency Range	FOUT1	CLKOUT, VDDO=3.3V to 2.5V	3	-	200	MHz
Output Frequency Range	FOUT2	CLKOUT, VDDO=1.8V	3	-	166	MHz
Output Frequency Range	FOUT3	REFCLK, crystal or resonator input	0.25	-	48	MHz
Output Duty Cycle	DC1	SSCLK	45	50	55	%
Output Duty Cycle	DC2	REFCLK , Xtal input	45	50	55	%
Output Duty Cycle	DC3	REFCLK, clock input	40	50	60	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	40	50	60	%
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ1	FIN=27MHz, all 7 clocks are programmed at 66MHz, CL=15pF	-	200	TBD	ps
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ2	FIN=27MHz, all 9 clocks are programmed at 66MHz, CL=15pF	-	250	TBD	ps
Power supply Ramp Time	tPSR	Time for VDD reaching minimum specified value and monolithic power supply ramp	-	-	12	ms
PLL Lock Time	tPLL	Time from VDD reaching minimum specified value to valid output frequencies at all outputs	-	7.8	9.0	ms
PD# Power-up Time (Crystal or Clock)	tPU2	Time from PD# rising edge to valid frequency at outputs	-	5.5	8.0	ms
Output Enable Time	tOE	Time from OE falling edge to Hi-Z at outputs	-	250	400	ns
Output Disable Time	tOD	Time from OE falling edge to Hi-Z at outputs	-	250	400	ns
Spread Percent Range	SPR-1	Center Spread	+/-0.125	-	+/-2.5	%
Spread Percent Range	SPR-2	Down Spread	-5.0	-	-0.25	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	25	31.5	120	kHz

Programmable Output Clock (CLKOUT) Rise and Fall Times

The output clock rise and fall times (tr/tf) of each clock output can be programmed independently to match drive level to load impedance.

Programming Code	VDDO=3.3V CL=15pF	VDDO=2.5V CL=15pF	VDDO=1.8V CL=15pF	Unit
000	4.00	4.80	5.60	ns
001	2.00	2.60	3.20	ns
010	1.40	1.80	2.20	ns
011	1.10	1.40	1.70	ns
100	0.85	1.10	1.40	ns
101	0.70	0.90	1.10	ns
110	0.55	0.70	0.90	ns

Table 1. Programmable CLKOUT Rise and Fall Times

Notes:

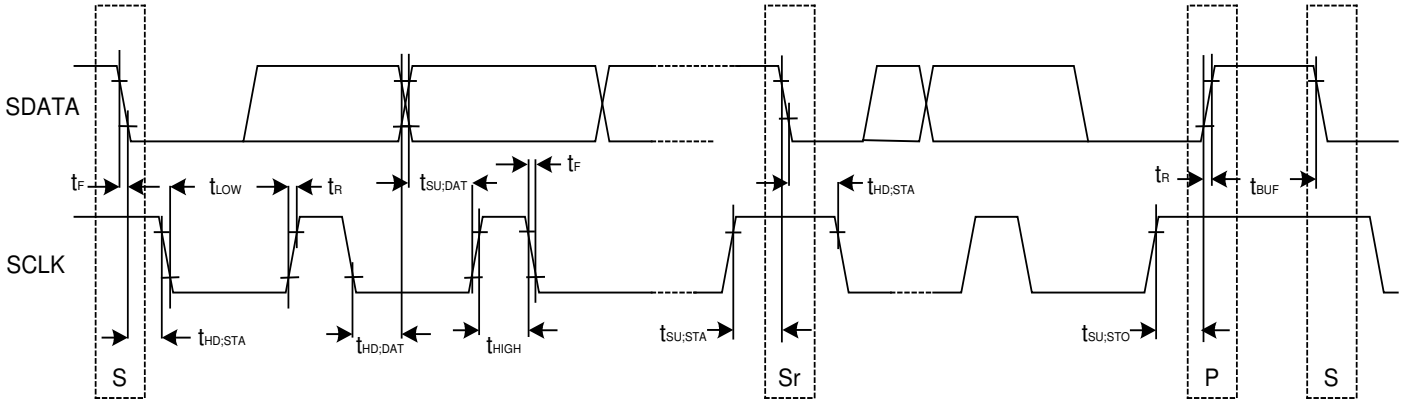
1. All typical values are at respective nominal VDD values.
2. The worst case rise and fall times variations are +/- 20% for C-Grade and +/-30% for I-grade.

I2C-Bus Timing Specifications

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
START hold time	$t_{HD;STA}$	4.0	-	0.6	-	µs
SCLK LOW period	t_{LOW}	4.7	-	1.3	-	µs
SCLK HIGH period	t_{HIGH}	4.0	-	0.6	-	µs
START Set-up time	$t_{SU;DAT}$	4.7	-	0.6	-	µs
SDA set-up time	$t_{SU;DAT}$	250	-	100	-	ns
SDA/SCLK rise time	t_R	-	1000	-	300	ns

SDA/SCLK fall time	t_F	-	300	-	300	ns
STOP set-up time	$t_{SU;STO}$	4.0	-	0.6	-	ns
Bus free time	t_{BUF}	4.7	-	1.3	-	µs

Table 2. I2C-Bus Timing Specification



I2C-Bus Timing Diagram

External Components & Design Considerations

Typical Application Schematic

TBD

Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between all VDD and VSS pins on PCB. Place the capacitor on the component side of the PCB as close to the VDD pins as possible. The PCB trace to the VDD pins and to the GND via should be kept as short as possible Do not use vias between the decoupling capacitor and the VDD pins.

Series Termination Resistor: A series termination resistor is recommended if the distance between the outputs (CLKOUT or REFCLK pins) and the load is over 1 ½ inch. The nominal impedance of the all clock outputs are about 25 Ω. Use 20 Ω resistor in series with the output to terminate 50Ω trace impedance and place 20 Ω resistor as close to the SSCLK output as possible.

Crystal and Crystal Load: Use only parallel resonant fundamental crystals. DO NOT USE higher overtone crystals. To meet the crystal initial accuracy specification (in ppm); the internal on-chip programmable capacitors PCin and PCout must be programmed to match the crystal load requirement. These values are given by the formula below:

$$PCin(pF) = PCout(pF) = [(CL(pF) - Cp(pF)/2)] \times 2$$

Where CL is crystal load capacitor as given by the crystal datasheet and Cp(pF) is the compensation factor for the total parasitic capacitance at XIN or XOUT pin including PCB related parasitic capacitance.

As an example; if a crystal with CL=18pF is used and Cp=4pF, by using the above formula, PCin=PCout=[(18-(4/2)] x 2 = 32pF. Programming PCin and PCout to 32pF assures that this crystal sees an equivalent load of 18pF and no other external crystal load capacitor is needed. Deviating from the crystal load specification could cause an increase in frequency accuracy in ppm. Refer to the Table 5 for the recommended crystal specifications.

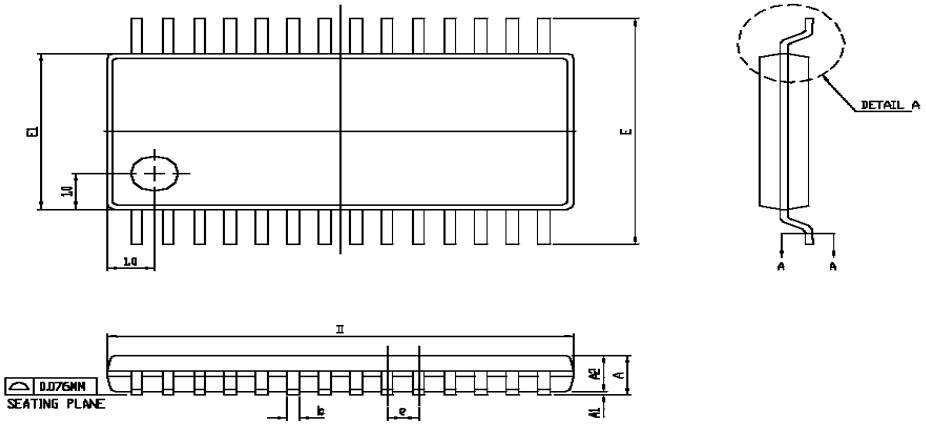
Recommended External Crystal Specifications (XO Version)

Parameter	Description	Min	Typ	Max	Unit	Comments
FNOM	Nominal Crystal Frequency Range	8	-	48	MHz	Fundamental Mode – AT Cut
CL	Nominal Crystal Load	6	12	18	pF	Load for +/-0 ppm Fo resonance value
R1,1	Equivalent Series Resistance	20	40	100	Ohm	F-Range: 8.0 to 12.999 MHz
R1,2	Equivalent Series Resistance	12.5	25	60	Ohm	F-Range: 13.0 to 19.999 MHz
R1,3	Equivalent Series Resistance	10	20	50	Ohm	F-Range: 20.0 to 48.000 MHz
DL1,1	Crystal Drive Level	-	-	200	µW	F-Range: 8.0 to 19.999 MHz
DL1,2	Crystal Drive Level	-	-	150	µW	F-Range: 20.0 to 48.000 MHz
Co1	Shunt Capacitance	-	4	5.4	pF	SMD Xtals
Co2	Shunt Capacitance	-	5	7.2	pF	Through Hole (Leaded) Xtals

Table 3. Recommended Crystal Specifications

Package Outline and Package Dimensions

28-Pin TSSOP Package



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			.047
A1	0.05		0.15	.002		.006
A2	0.80	0.90	1.05	.031	.035	.041
L	0.45	0.60	0.75	.018	.024	.030
D	9.60	9.70	9.80	.378	.382	.386
E	6.30	6.40	6.50	.248	.252	.256
E1	4.30	4.40	4.50	.169	.173	.177
R	0.09			.004		
R1	0.09			.004		
b	0.19		0.30	.007		.012
b1	0.19	0.22	0.25	.007	.009	.010
c	0.09		0.20	.004		.008
c1	0.09		0.16	.004		.006
L1	1.0 REF.			.039 REF.		
e	0.65 BSC.			.026 BSC.		
θ1	0		8	0		8
θ2	12 REF.			12 REF.		
θ3	12 REF.			12 REF.		
N	28					
REF	JEDEC MO-153 VAR. AE					

Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ JA	Still air	-	TBD	-	°C/W
	θ JA	1m/s air flow	-	TBD	-	°C/W
	θ JA	3m/s air flow	-	TBD	-	°C/W
Thermal Resistance Junction to Case	θ JC	Independent of air flow	-	TBD	-	°C/W

Ordering Information [1]

Ordering Number [2]	Marking	Shipping Package	Package	Temperature
SL38000ZC-XXX	SL38000ZC-XXX	Tube	28-pin TSSOP	0 to 70°C
SL38000ZC-XXXT	SL38000ZC-XXX	Tape and Reel	28-pin TSSOP	0 to 70°C
SL38000ZI-XXX	SL380004ZI-XXX	Tube	28-pin TSSOP	-40 to 85°C
SL38000ZI-XXXT	SL38000ZI-XXX	Tape and Reel	28-pin TSSOP	-40 to 85°C

Notes:

1. All SLI products are RoHS compliant.
2. “XXX” is “Dash” number and will be assigned by SLI for final programmed samples and production units based on customer programming requirements.

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