



FC4B22180L1

Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

■ Features

- Low source-source ON resistance: $R_{ss(on)}$ typ. = 10 m Ω (VGS = 3.8 V)
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL: Level 1 compliant)

■ Marking Symbol: 17

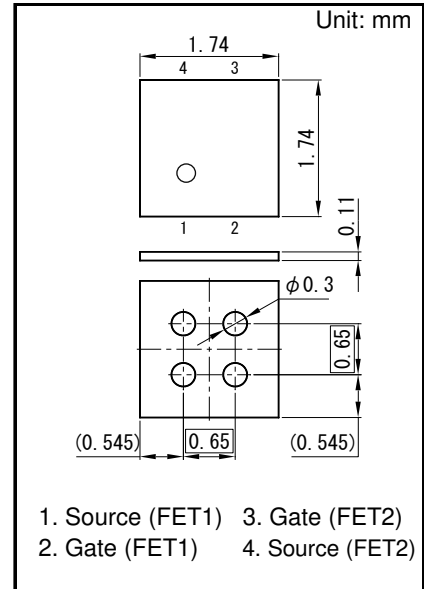
■ Packaging

Embossed type (Thermo-compression sealing) : 1 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

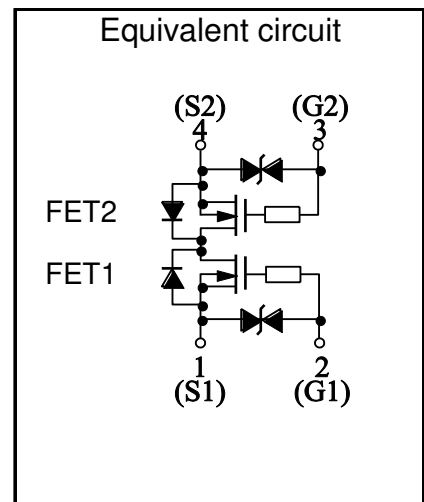
Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	20	V
Gate-source Voltage	VGS	±8	V
Source Current	DC ^{*1}	IS1	5
	DC ^{*2}	IS2	10
	Pulse ^{*3}	ISp	50
Total Power Dissipation	DC ^{*1}	PD1	0.4
	DC ^{*2}	PD2	1.5
Channel Temperature	Tch	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Thermal Resistance (ch-a)	DC ^{*1}	Rth1	312
	DC ^{*2}	Rth2	83

- Note *1 Mounted on FR4 board
 (25.4mm × 25.4mm × t1.0mm, 36 μ m Copper)
 *2 Mounted on Ceramic substrate
 (70 mm × 70 mm × t1.0 mm).
 *3 t = 10 μ s, Duty Cycle ≤ 1 %



1. Source (FET1) 3. Gate (FET2)
 2. Gate (FET1) 4. Source (FET2)

Panasonic	MLGA004-W-1717-RB
JEITA	—
Code	—



■ Electrical Characteristics Ta = 25 °C ± 3 °C

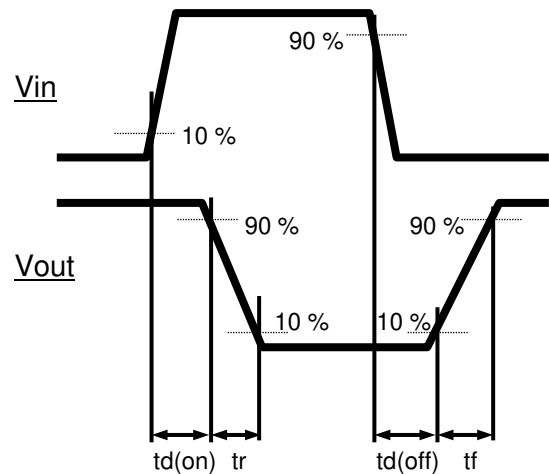
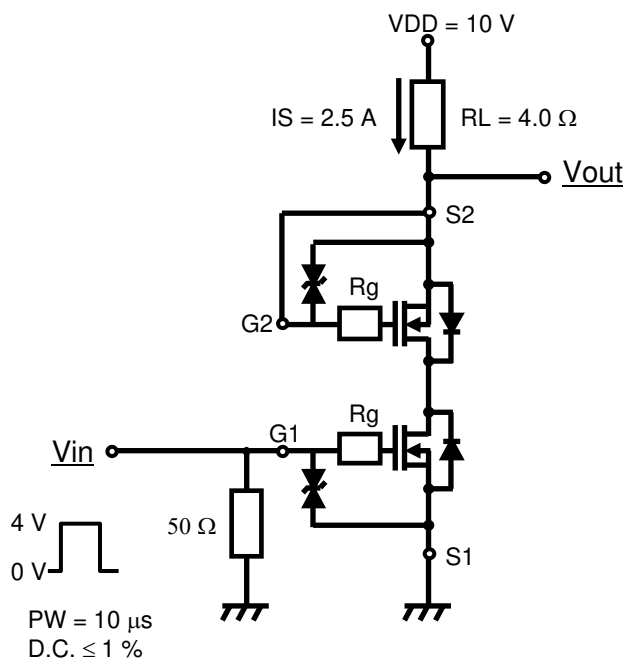
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	20			V
Zero Gate Voltage Source Current	ISSS	VSS = 20 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±10	μA
		VGS = ±5 V, VSS = 0 V			±1.0	
Gate-source Threshold Voltage	Vth	IS = 0.64 mA, VSS = 10 V	0.35	0.90	1.4	V
Source-source On-state Resistance	RSS(on)1	IS = 2.5 A, VGS = 4.5 V	7	9.4	11.9	mΩ
	RSS(on)2	IS = 2.5 A, VGS = 3.8 V	7.3	10	12.9	
	RSS(on)3	IS = 2.5 A, VGS = 3.1 V	8.1	11.1	15.8	
	RSS(on)4	IS = 2.5 A, VGS = 2.5 V	8.6	13.4	22.6	
Body Diode Forward Voltage	VF(s-s)	IF = 2.5 A, VGS = 0 V		0.8	1.2	V
Input Capacitance ^{*1}	Ciss	VSS = 10 V, VGS = 0 V, f = 1 MHz		2440		pF
Output Capacitance ^{*1}	Coss			200		
Reverse Transfer Capacitance ^{*1}	Crss			160		
Turn-on delay Time ^{*1,*2}	td(on)	VDD = 10 V, VGS = 0 to 4.0 V		0.9		μs
Rise Time ^{*1,*2}	tr	IS = 2.5 A		1.6		
Turn-off delay Time ^{*1,*2}	td(off)	VDD = 10 V, VGS = 4.0 to 0 V		5		μs
Fall Time ^{*1,*2}	tf	IS = 2.5 A		2.4		
Total Gate Charge ^{*1}	Qg	VDD = 10 V		23		nC
Gate-source Charge ^{*1}	Qgs	VGS = 0 to 4.0 V,		6		
Gate-drain Charge ^{*1}	Qgd	IS = 2.5 A		5		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

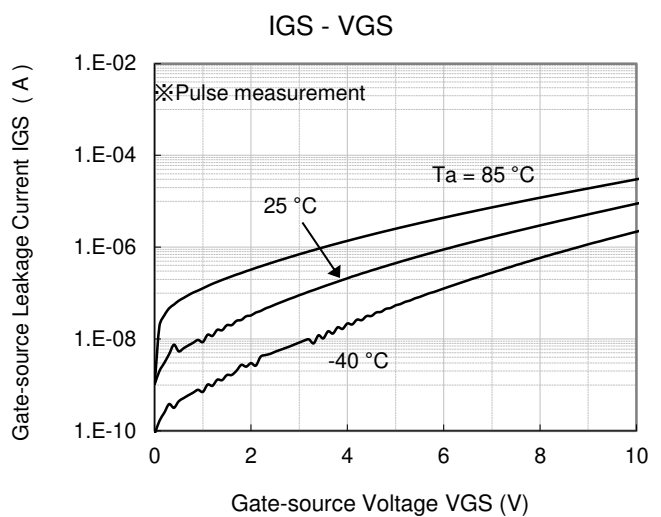
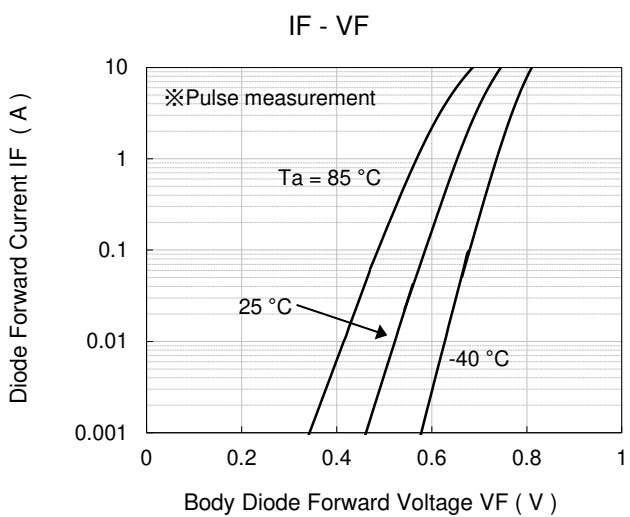
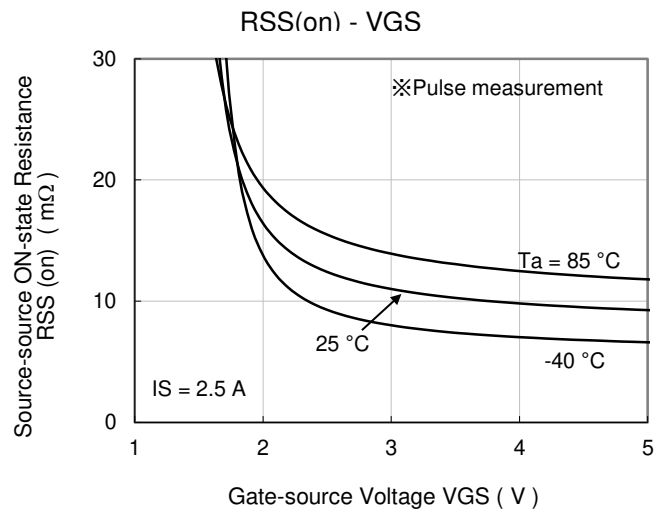
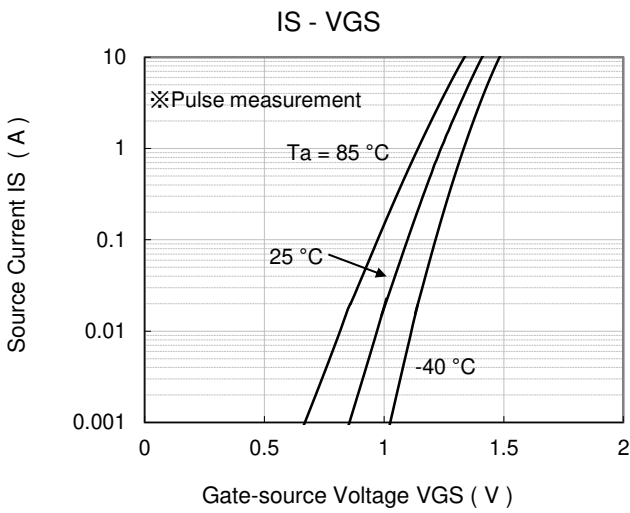
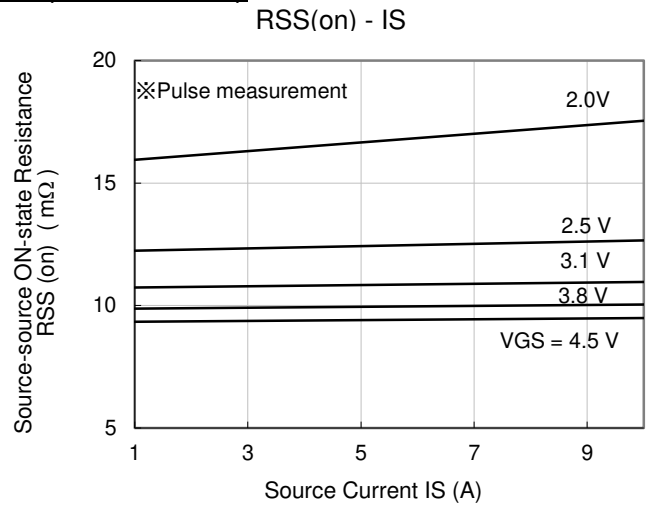
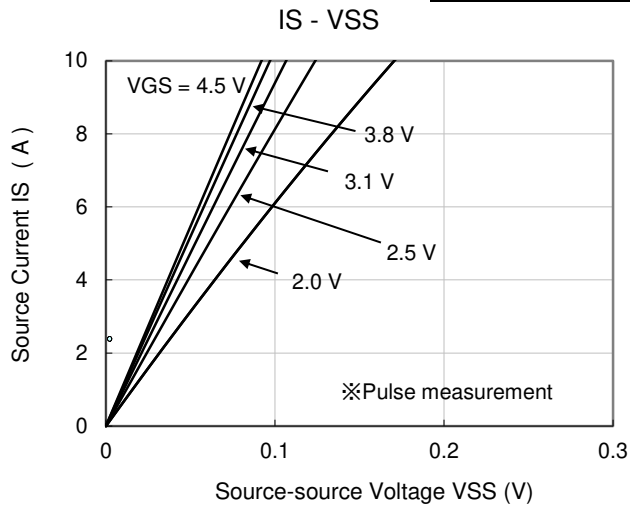
*1 Guaranteed by design, not subject to production testing

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

Note2 : Measurement circuit

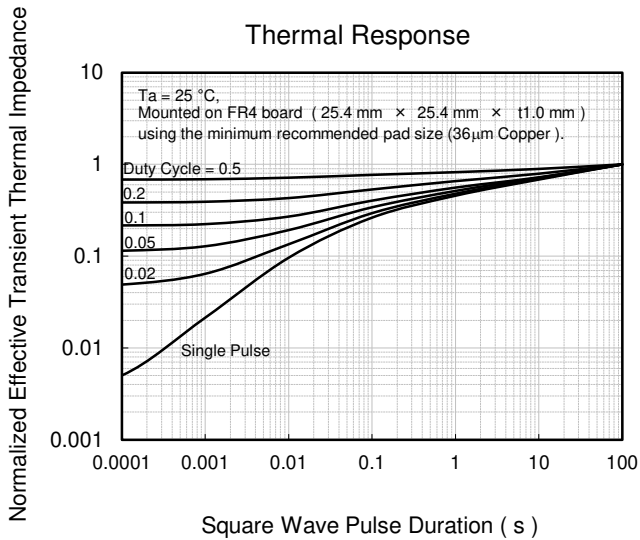
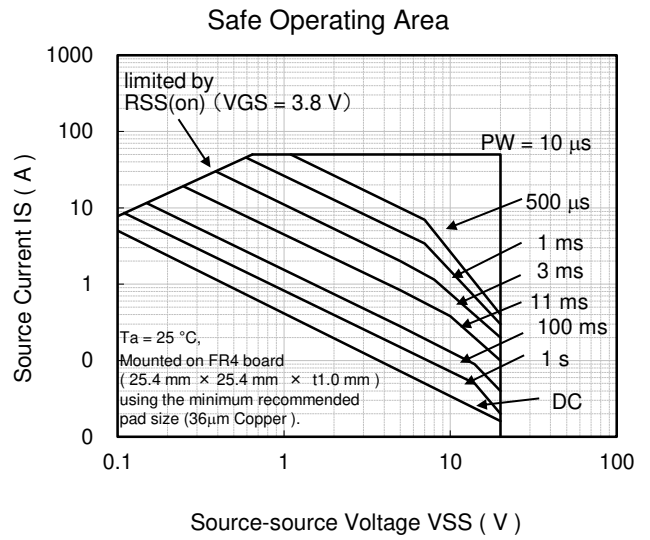
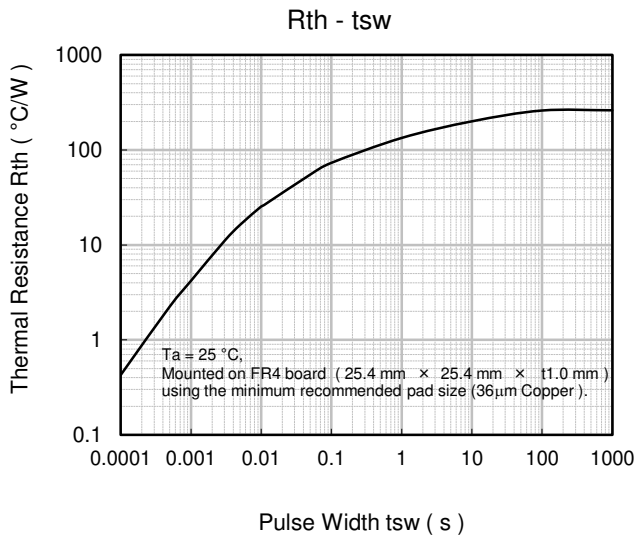
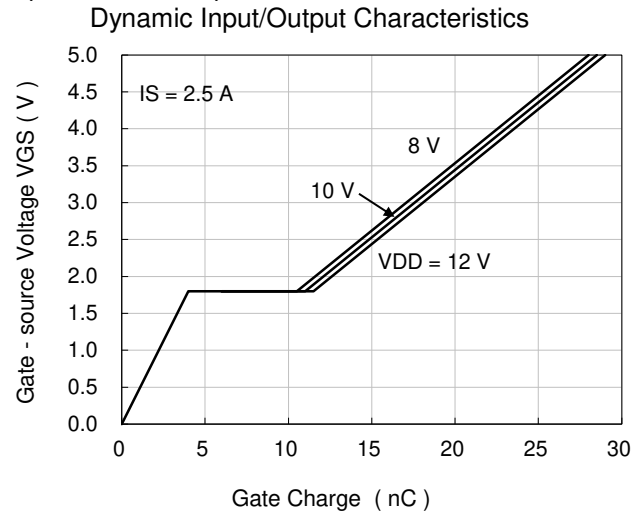
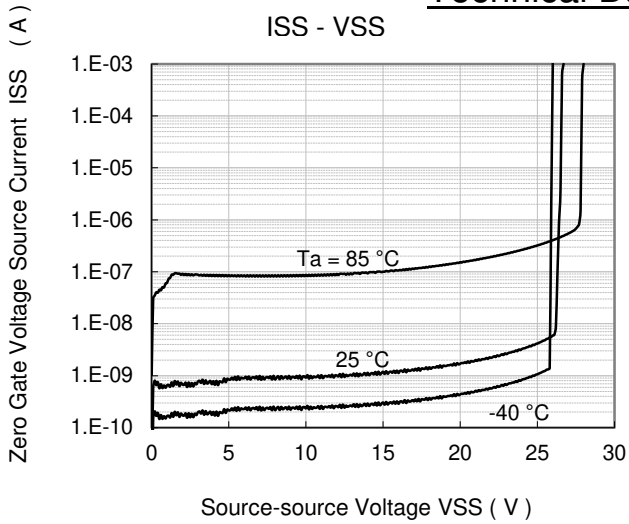


Technical Data (reference)



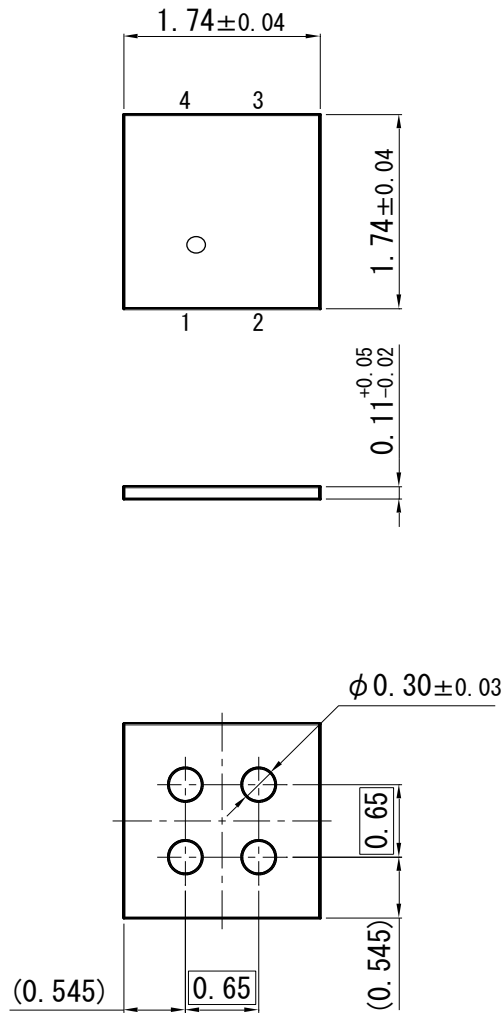


Technical Data (reference)



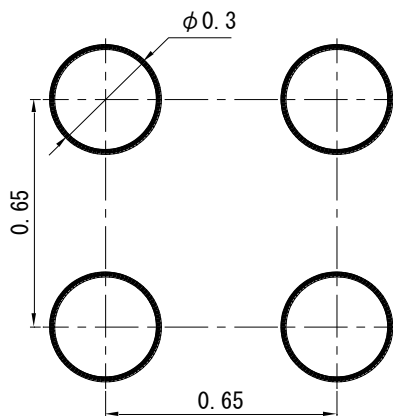
■ Outline (MLGA004-W-1717-RB)

Unit: mm



■ Land Pattern (Reference)

Unit: mm



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