Product data sheet

1. General description

Dual small-signal P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- 2 kV ElectroStatic Discharge (ESD) protection

3. Applications

- · Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
Per transistor	Per transistor							
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	-20	V	
V _{GS}	gate-source voltage			-8	-	8	V	
I _D	drain current	$V_{GS} = -4.5 \text{ V}; T_{amb} = 25 \text{ °C}; t \le 5 \text{ s}$	[1]	-	-	-4.5	Α	
Static characteristics (per transistor)								
R _{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -2 A; T_j = 25 °C		-	58	67	mΩ	

^[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	6 5 4	D1 D2
2	G1	gate TR1		
3	D2	drain TR2	7 8	G1 $G2$ $G2$
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1	Transparent top view DFN2020-6 (SOT1118)	S1 S2 017aaa260
7	D1	drain TR1	5. 112020 3 (0011110)	
8	D2	drain TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
PMDPB58UPE	DFN2020-6	DFN2020-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118		

7. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB58UPE	2A

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit	
Per transistor							
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V	
V_{GS}	gate-source voltage			-8	8	V	
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-4.5	Α	
		V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-3.6	Α	
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-2.3	Α	

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Symbol	Parameter	Conditions		Min	Max	Unit
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10$ μs		-	-14.4	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	515	mW
			[1]	-	1210	mW
		T _{sp} = 25 °C		-	8330	mW
Per device			- 1			1
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-dra	ain diode					
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.3	Α
ESD maxin	num rating	1			1	
V _{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ	[3]	-	2000	V

- Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.

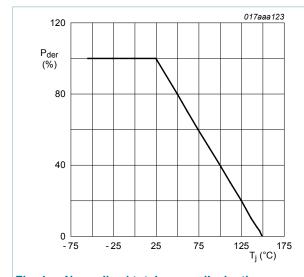


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

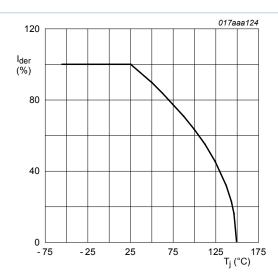


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

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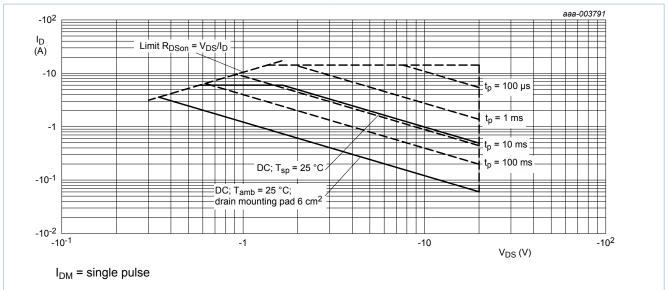


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Table 0. The	illiai Cilai acteristics						
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor							
R _{th(j-a)} thermal resistance		in free air	[1]	-	212	244	K/W
from ju ambie	from junction to		[2]	-	90	104	K/W
	ambient	in free air; t ≤ 5 s	[2]	-	55	64	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	11	15	K/W

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

4/14

^[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

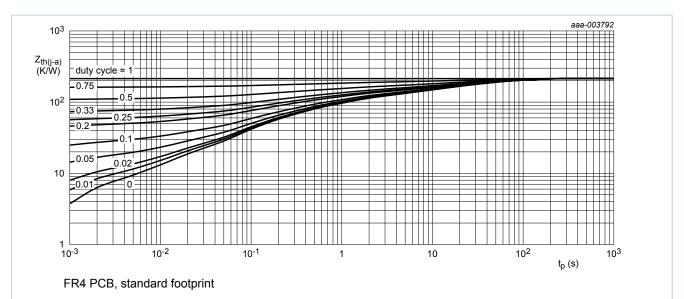


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

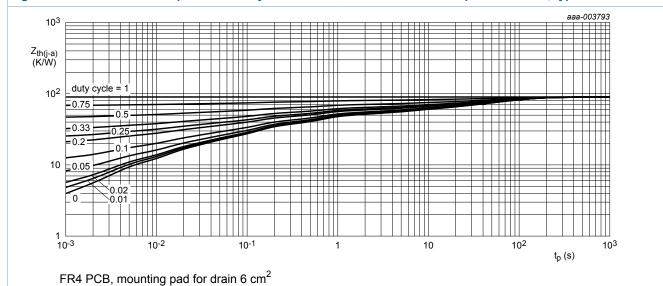


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics (per transistor)					
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \ \mu\text{A}; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^{\circ}\text{C}$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \ \mu A; \ V_{DS} = V_{GS}; \ T_j = 25 \ ^{\circ}C$	-0.45	-0.7	-0.95	V
I _{DSS} drain leakage	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-1	μΑ
		V _{DS} = -20 V; V _{GS} = 0 V; T _j = 150 °C	-	-	-10	μΑ
I _{GSS}	gate leakage current	V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C	-	-	10	μΑ
		V _{GS} = -8 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-10	μA
R _{DSon} drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -2 \text{ A}; T_j = 25 \text{ °C}$	-	58	67	mΩ	
	resistance	V_{GS} = -4.5 V; I_D = -2 A; T_j = 150 °C	-	82	95	mΩ
		V _{GS} = -2.5 V; I _D = -1.5 A; T _j = 25 °C	-	74	95	mΩ
		V _{GS} = -1.8 V; I _D = -1 A; T _j = 25 °C	-	97	137	mΩ
9 _{fs}	forward transconductance	V_{DS} = -10 V; I_{D} = -2 A; T_{j} = 25 °C	-	9	-	S
Dynamic cl	haracteristics (per transist	or)				
Q _{G(tot)}	total gate charge	V_{DS} = -10 V; I_{D} = -2 A; V_{GS} = -4.5 V;	-	6.3	9.5	nC
Q_{GS}	gate-source charge	T _j = 25 °C	-	1.2	-	nC
Q_{GD}	gate-drain charge		-	0.9	-	nC
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V;	-	804	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	95	-	pF
C _{rss}	reverse transfer capacitance		-	66	-	pF
t _{d(on)}	turn-on delay time	V_{DS} = -10 V; I_{D} = -2 A; V_{GS} = -4.5 V;	-	7	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	15	-	ns
t _{d(off)}	turn-off delay time		-	41	-	ns
t _f	fall time		-	14	-	ns
Source-dra	in diode (per transistor)		l l	1		
V_{SD}	source-drain voltage	$I_S = -0.5 \text{ A}; V_{GS} = 0 \text{ V}; T_i = 25 ^{\circ}\text{C}$	-	-0.7	-1.2	V

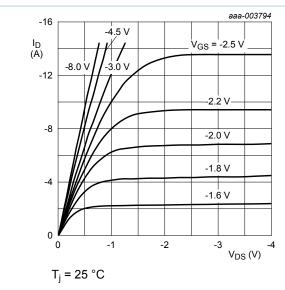
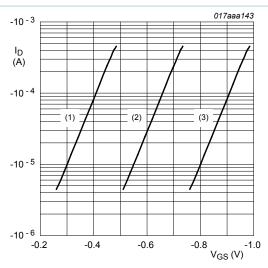


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



$$T_i$$
 = 25 °C; V_{DS} = -3 V

- (1) minimum values
- (2) typical values
- (3) maximum values

Fig. 7. Sub-threshold drain current as a function of gate-source voltage

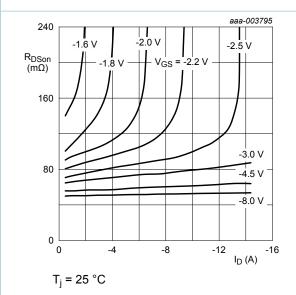


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

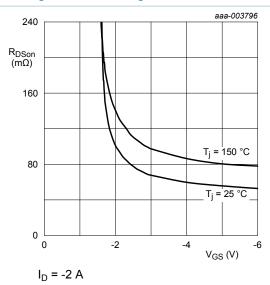


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

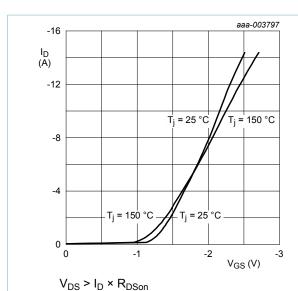


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

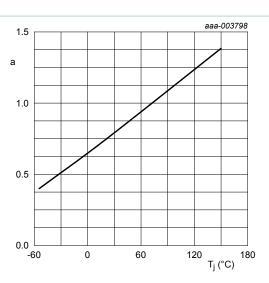


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

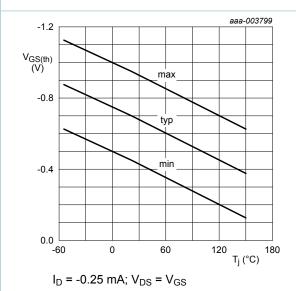
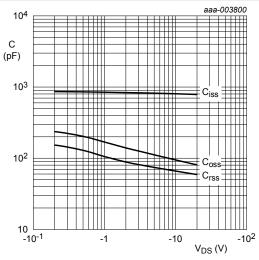


Fig. 12. Gate-source threshold voltage as a function of junction temperature



 $f = 1 MHz; V_{GS} = 0 V$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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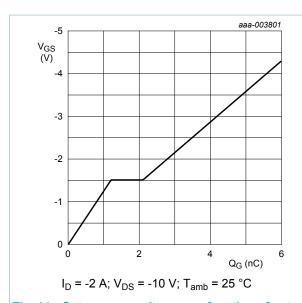


Fig. 14. Gate-source voltage as a function of gate charge; typical values

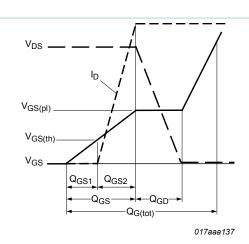


Fig. 15. Gate charge waveform definitions

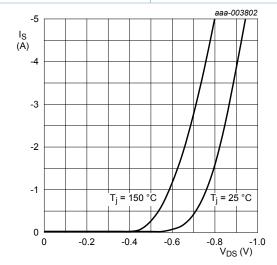
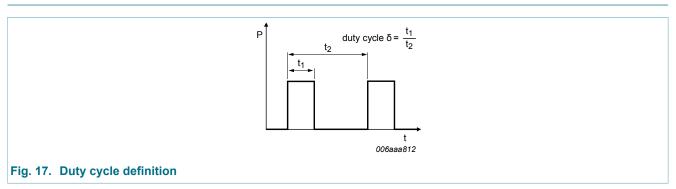


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

 $V_{GS} = 0 V$



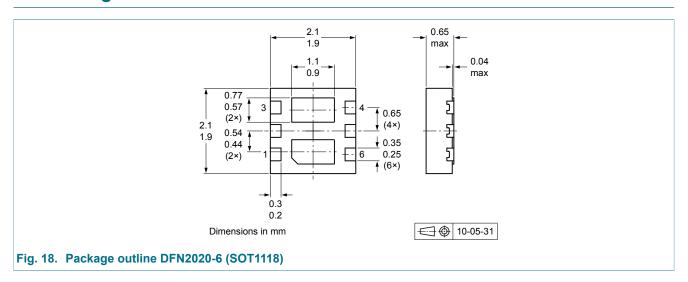
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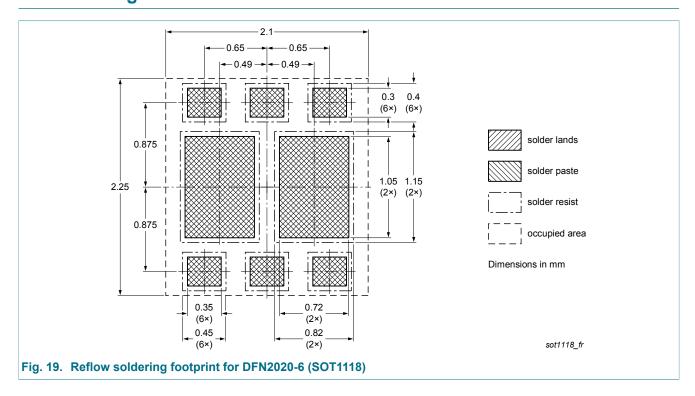
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20 V dual P-channel Trench MOSFET

12. Package outline



13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB58UPE v.2	20160203	Product data sheet	-	PMDPB58UPE v.1
Modifications:	Figure 9: corrected			
PMDPB58UPE v.1	20120619	Product data sheet	-	-

20 V dual P-channel Trench MOSFET

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20 V dual P-channel Trench MOSFET

16. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	2
8	Limiting values	2
9	Thermal characteristics	4
10	Characteristics	6
11	Test information	9
12	Package outline	10
13	Soldering	10
14	Revision history	11
15	Legal information	12
15.1	Data sheet status	12
15.2	Definitions	12
15.3	Disclaimers	12
15.4	Trademarks	13

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