

# TYPES SN5480, SN7480 GATED FULL ADDERS

DECEMBER 1972 - REVISED DECEMBER 1983

## logic

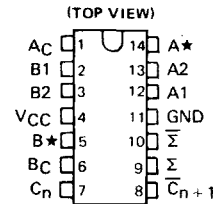
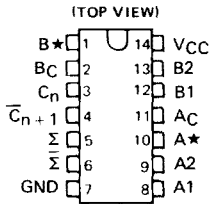
SN5480 . . . J PACKAGE  
SN7480 . . . J OR N PACKAGE

SN5480 . . . W PACKAGE

FUNCTION TABLE  
(See Notes 1, 2, and 3)

INPUTS			OUTPUTS		
C <sub>n</sub>	B	A	C <sub>n+1</sub>	Σ	Σ̄
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

H = high level, L = low level



- NOTES: 1.  $A = \bar{A}C + \bar{A}A + A1 \cdot A2$ ,  $B = \bar{B}C + \bar{B}A + B1 \cdot B2$ .  
 2. When A\* is used as an input, A1 or A2 must be low. When B\* is used as an input, B1 or B2 must be low.  
 3. When A1 and A2 or B1 and B2 are used as inputs, A\* or B\*, respectively, must be open or used to perform dot-AND logic.

## description

These single-bit, high-speed, binary full adders with gated complementary inputs, complementary sum ( $\Sigma$  and  $\bar{\Sigma}$ ) outputs and inverted carry output are designed for medium-and high-speed, multiple-bit, parallel-add/serial-carry application. These circuits (see schematic) utilize diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs and are entirely compatible with the TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V <sub>CC</sub> (see Note 4)	7 V
Input voltage (see Note 5)	5.5 V
Operating free-air temperature range: SN5480 Circuits	-55°C to 125°C
SN7480 Circuits	0° to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 4. Voltage values are with respect to network ground terminal.  
 5. Input signals must be zero or positive with respect to network ground terminal.

## recommended operating conditions

	SN5480		SN7480		UNIT		
	MIN	NOM	MAX	MIN		NOM	MAX
Supply voltage, V <sub>CC</sub>	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I <sub>OH</sub>	Σ or Σ̄		-400			-400	μA
	C <sub>n+1</sub>		-200			-200	
	A* or B*		-120			-120	
Low-level output current, I <sub>OL</sub>	Σ or Σ̄		16			16	mA
	C <sub>n+1</sub>		8			8	
	A* or B*		4.8			4.8	
Operating free-air temperature, T <sub>A</sub>	-55	125		0	70		°C

**PRODUCTION DATA**  
 This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



# TYPES SN5480, SN7480 GATED FULL ADDERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5480			SN7480			UNIT		
			MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V <sub>IH</sub>	High-level input voltage		2			2			V		
V <sub>IL</sub>	Low-level input voltage		0.8			0.8			V		
V <sub>OH</sub>	High-level output voltage	$\Sigma$ or $\Sigma$	V <sub>CC</sub> = MIN, I <sub>OH</sub> = -400 $\mu$ A		2.4	3.5	2.4	3.5	V		
		$\bar{C}_{n+1}$	V <sub>IH</sub> = 2 V, I <sub>OH</sub> = -200 $\mu$ A								
		A* or B*	V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -120 $\mu$ A								
V <sub>OL</sub>	Low-level output voltage	$\Sigma$ or $\Sigma$	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 16 mA		0.22	0.4	0.22	0.4	V		
		$\bar{C}_{n+1}$	V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA								
		A* or B*	V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 4.8 mA								
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V	1			1			mA		
I <sub>IH</sub>	High-level input current	A <sub>1</sub> , A <sub>2</sub> , B <sub>1</sub> , B <sub>2</sub> , A <sub>C</sub> , or B <sub>C</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V		15			15			$\mu$ A
		A* or B*			-1.1			-1.1			
		C <sub>n</sub>			200			200			
I <sub>IL</sub>	Low-level input current	A <sub>1</sub> , A <sub>2</sub> , B <sub>1</sub> , B <sub>2</sub> , A <sub>C</sub> , or B <sub>C</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-1.6			-1.6			mA
		A* or B*			-2.6			-2.6			
		C <sub>n</sub>			-8			-8			
I <sub>OS</sub>	Short-circuit output-current‡	$\Sigma$ or $\Sigma$	V <sub>CC</sub> = MAX		-20			-18			mA
		$\bar{C}_{n+1}$			-20			-70			
		A* or B*			-0.9			-2.9			
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 6	21 31			21 35			mA		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 6: I<sub>CC</sub> is measured with all inputs and outputs open.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>PLH</sub>	C <sub>n</sub>	$\bar{C}_{n+1}$	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 780 $\Omega$ , See Note 7	13	17	ns		
t <sub>PHL</sub>				8	12			
t <sub>PLH</sub>	B <sub>C</sub>	$\bar{C}_{n+1}$		18	25			
t <sub>PHL</sub>				38	65			
t <sub>PLH</sub>	A <sub>C</sub>	$\Sigma$	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 $\Omega$ , See Note 7	52	70	ns		
t <sub>PHL</sub>				62	80			
t <sub>PLH</sub>	B <sub>C</sub>	$\bar{\Sigma}$		38	55			
t <sub>PHL</sub>				56	75			
t <sub>PLH</sub>	A <sub>1</sub>	A*		C <sub>L</sub> = 15 pF, See Note 7	48		65	ns
t <sub>PHL</sub>					17		25	
t <sub>PLH</sub>	B <sub>1</sub>	B*	48		65			
t <sub>PHL</sub>			17		25			

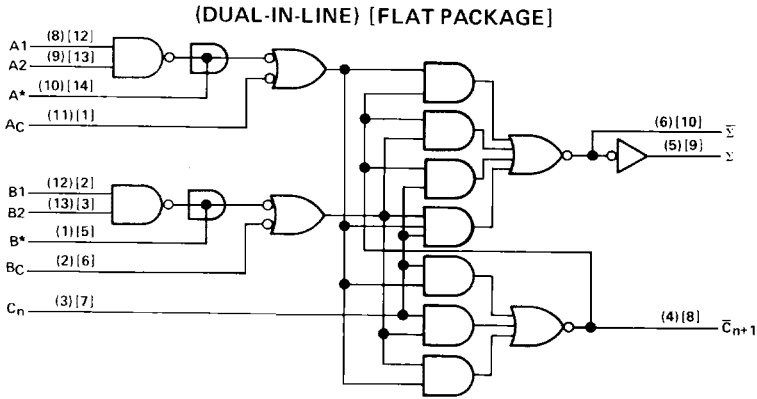
¶ t<sub>PLH</sub>  $\equiv$  propagation delay time, low-to-high-level output

t<sub>PHL</sub>  $\equiv$  propagation delay time, high-to-low-level output

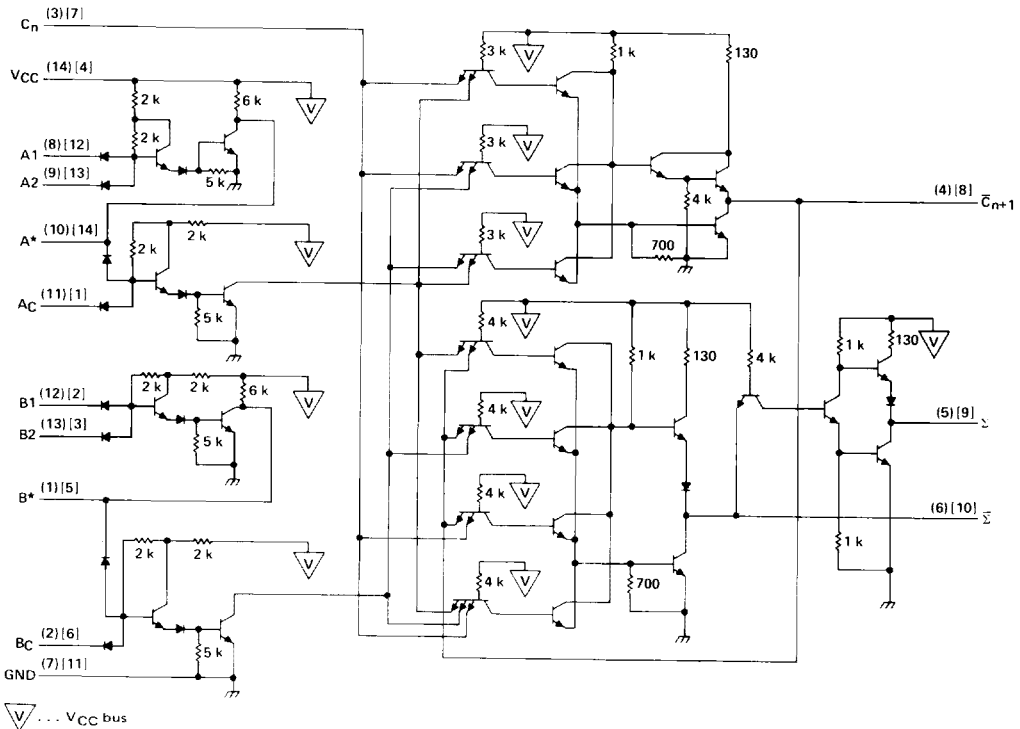
NOTE 7: The load for testing outputs A\* and B\* consists only of capacitance C<sub>L</sub> to ground. See General Information Section for load circuits and voltage waveforms.

# TYPES SN5480, SN7480 GATED FULL ADDERS

## logic diagram



## schematic



Resistor values shown are nominal and in ohms.

Pin numbers shown in ( ) are for the N or J package and pin numbers shown in | | are for the W package.

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