TEXAS INSTRUMENTS

CSD75207W15

SLPS418A – JUNE 2013 – REVISED JUNE 2014

CSD75207W15 Dual P-Channel NexFET™ Power MOSFET

1 Features

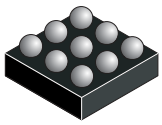
- Dual P-Channel MOSFETs
- Common Source Configuration
- Small Footprint 1.5-mm × 1.5-mm
- Gate-Source Voltage Clamp
- Gate ESD Protection >4 kV
  - HBM JEDEC standard JESD22-A114
- Pb and Halogen Free
- RoHS Compliant

2 Applications

- Battery Management
- Battery Protection
- Load and Input Switching

3 Description

The CSD75207W15 device is designed to deliver the lowest on-resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. Low on-resistance coupled with the small footprint and low profile make the device ideal for battery-operated space-constrained applications. The device has also been awarded with U.S. patents 7952145, 7420247, 7235845, and 6600182.



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{D1D2}	Drain-to-Drain Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	2.9		nC
Q_{gd}	Gate Charge Gate to Drain	0.4		nC
$R_{D1D2(on)}$	Drain-to-Drain On Resistance	V_{GS} = –1.8 V	119	mΩ
		V_{GS} = –2.5 V	64	mΩ
		V_{GS} = –4.5 V	45	mΩ
$V_{GS(th)}$	Threshold Voltage	–0.8		V

Ordering Information(1)

Device	Package	Media	Qty	Ship
CSD75207W15	1.5-mm × 1.5-mm Wafer Level Package	7-Inch Reel	3000	Tape and Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

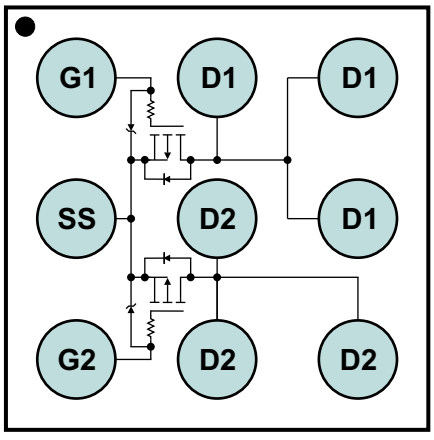
T_A = 25°C		VALUE	UNIT
V_{D1D2}	Drain-to-Drain Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–6.0	V
I_{D1D2}	Continuous Drain to Drain Current(1) (2)	–3.9	A
	Pulsed Drain to Drain Current, T_C = 25°C(3)	–24	A
I_S	Continuous Source Pin Current	–1.2	A
	Pulsed Source Pin Current(3)	–15	A
I_G	Continuous Gate Clamp Current	–0.5	A
	Pulsed Gate Clamp Current(3)	–7	A
P_D	Power Dissipation(1)	0.7	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C

(1) Per device, both sides in conduction

(2) Device operating at a temperature of 105ºC

(3) Pulse duration 10 µs, duty cycle ≤2%

Top View



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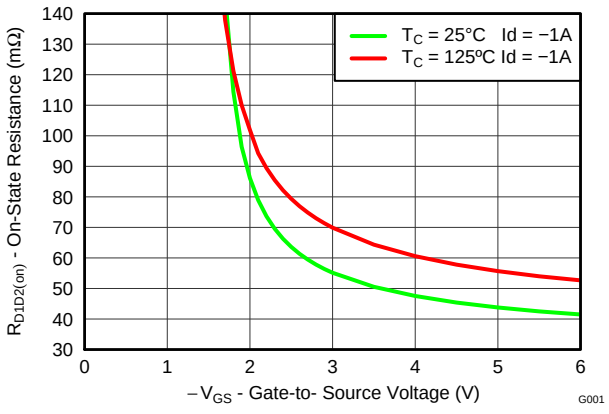
$R_{D1D2(on)}$ vs V_{GS}



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4 Revision History

Changes from Original (June 2013) to Revision A **Page**

- Increased continuous drain to drain current to 3.9 A ... 1
- Updated the continuous drain to drain current conditions to specify a temperature of 105ºC ... 1

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated). Specifications and graphs are Per MOSFET unless otherwise stated. Drain to Drain measurements are done with both MOSFETs in series (common source configuration.

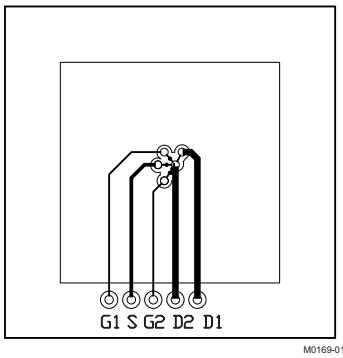
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{D1D2}	Drain-to-Drain Voltage	V_{GS} = 0 V, I_{D1D2} = –250 µA	–20			V
BV_{GSS}	Gate-to-Source Voltage	V_{D1D2} = 0 V, I_G = -250 µA	–6			V
I_{DDS}	Drain-to-Drain Leakage Current	V_{GS} = 0 V, V_{D1D2} = –16 V			–1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{D1D2} = 0 V, V_{GS} = –6 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{D1D2} = V_{GS}, I_{DS} = –250 µA	–0.6	–0.8	–1.1	V
$R_{D1D2(on)}$	Drain-to-Drain On-Resistance	V_{GS} = –1.8 V, I_{D1D2} = –1 A		119	162	mΩ
		V_{GS} = –2.5 V, I_{D1D2} = –1 A		64	77	mΩ
		V_{GS} = –4.5 V, I_{D1D2} = –1 A		45	54	mΩ
g_{fs}	Transconductance	V_{D1D2} = –10 V, I_{D1D2} = –1 A		6.2		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{D1D2} = –10 V, f = 1 MHz		458	595	pF
C_{OSS}	Output Capacitance			225	293	pF
C_{RSS}	Reverse Transfer Capacitance			10.4	13.5	pF
R_g	Series Gate Resistance			27		Ω
Q_g	Gate Charge Total (–4.5 V)	V_{D1D2} = –10 V, I_{D1D2} = –1 A		2.9	3.7	nC
Q_{gd}	Gate Charge – Gate to Drain			0.4		nC
Q_{gs}	Gate Charge – Gate to Source			0.7		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.4		nC
Q_{OSS}	Output Charge	V_{D1D2} = –9.5 V, V_{GS} = 0 V		3.1		nC
$t_{d(on)}$	Turn On Delay Time	V_{D1D2} = –10 V, V_{GS} = –4.5 V, I_{D1D2} = –1 A, R_G = 30 Ω		12.8		ns
t_r	Rise Time			8.6		ns
$t_{d(off)}$	Turn Off Delay Time			32.1		ns
t_f	Fall Time			16.0		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{D1D2} = –1 A, V_{GS} = 0 V		–0.8	–1	V
Q_{rr}	Reverse Recovery Charge	V_{dd} = –10 V, I_F = –1 A, di/dt = 200 A/µs		10.5		nC
t_{rr}	Reverse Recovery Time	V_{dd} = –10 V, I_F = –1 A, di/dt = 200 A/µs		23		ns

5.2 Thermal Information

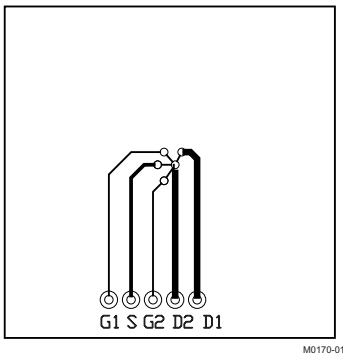
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		TYPICAL VALUE	UNIT
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance (1) (2)	70	°C/W
	Junction-to-Ambient Thermal Resistance (3) (2)	165	

(1) Device mounted on FR4 material with Minimum Cu mounting area.
(2) Measured with both devices biased in a parallel condition.
(3) Device mounted on FR4 material with 1-inch^2 of Cu (2 oz).



Typ $R_{\theta JA}$ = 70°C/W when mounted on 1-inch^2 of 2 oz. Cu.



Typ $R_{\theta JA}$ = 165°C/W when mounted on minimum pad area of 2-oz. Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

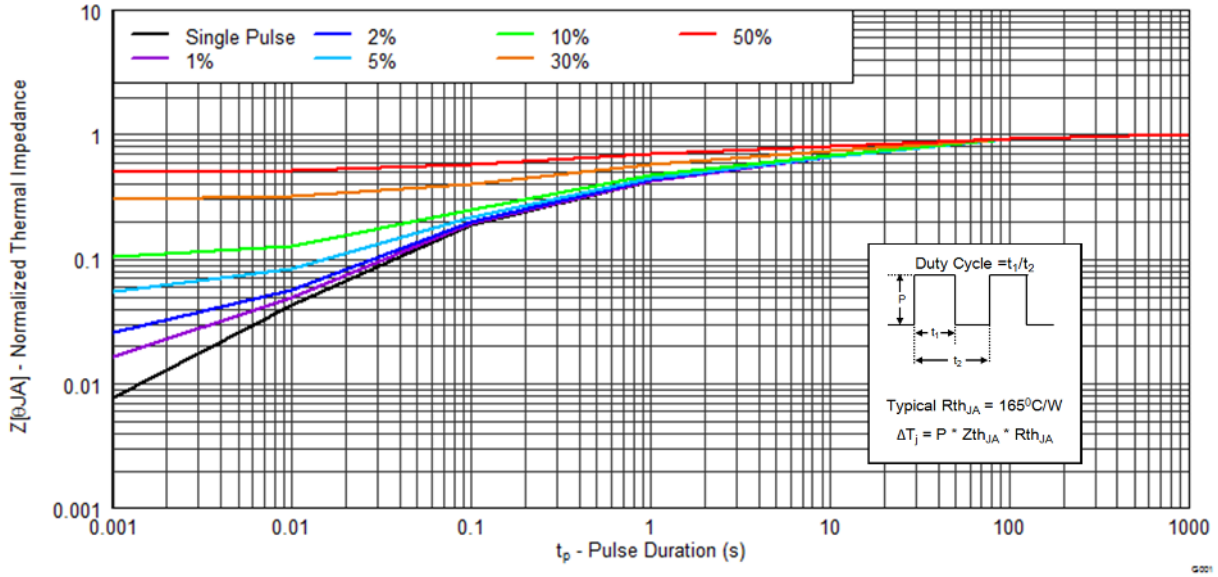


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

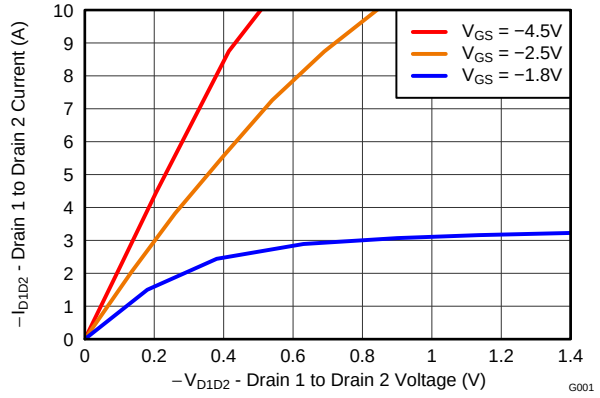


Figure 2. Saturation Characteristics

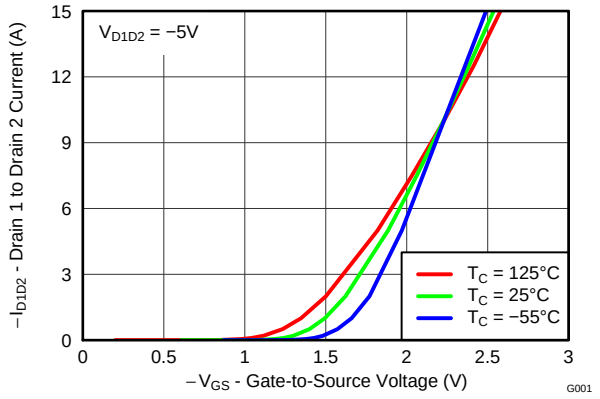


Figure 3. Transfer Characteristics

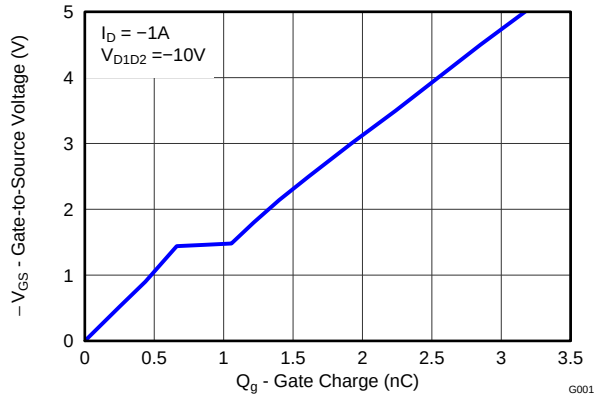


Figure 4. Gate Charge

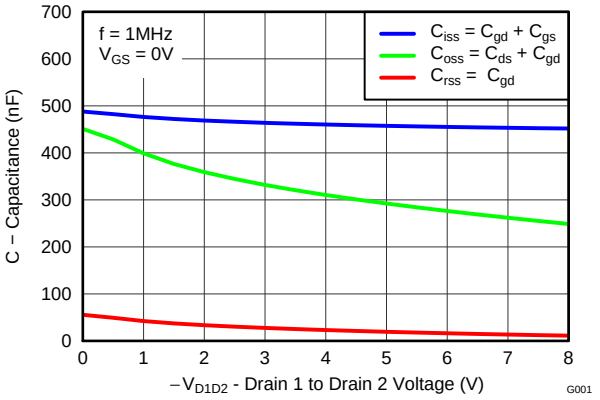


Figure 5. Capacitance

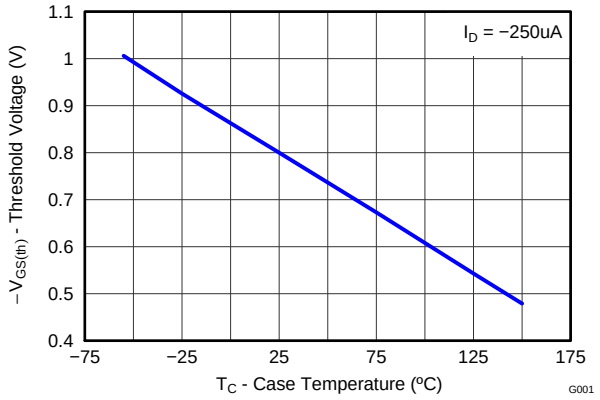


Figure 6. Threshold Voltage vs Temperature

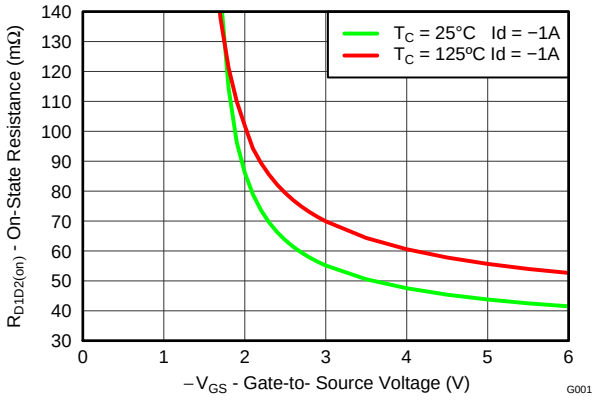


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

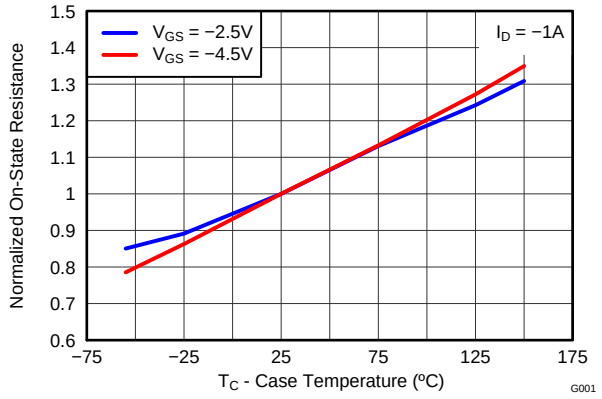


Figure 8. Normalized On-State Resistance vs Temperature

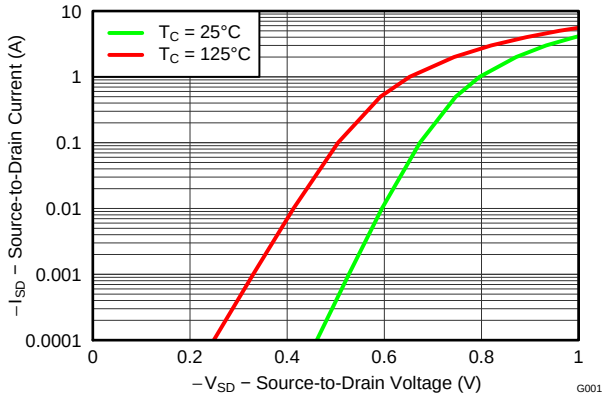


Figure 9. Typical Diode Forward Voltage

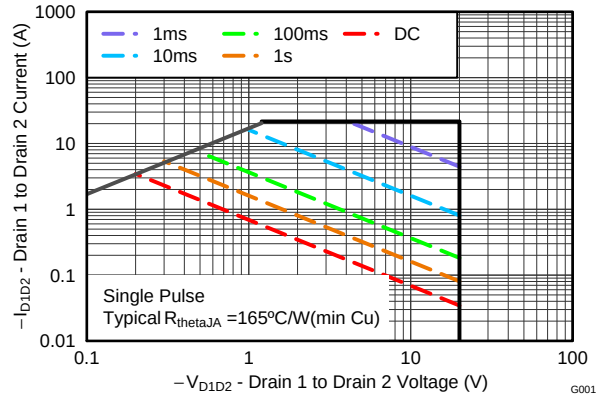


Figure 10. Maximum Safe Operating Area

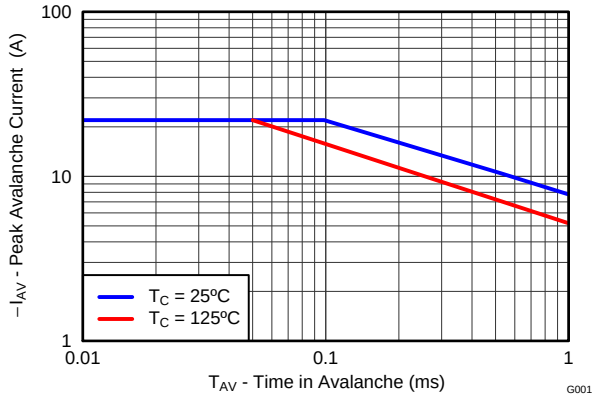


Figure 11. Single Pulse Unclamped Inductive Switching

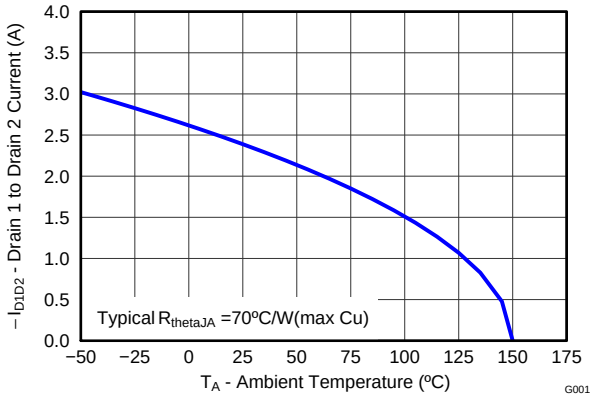


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

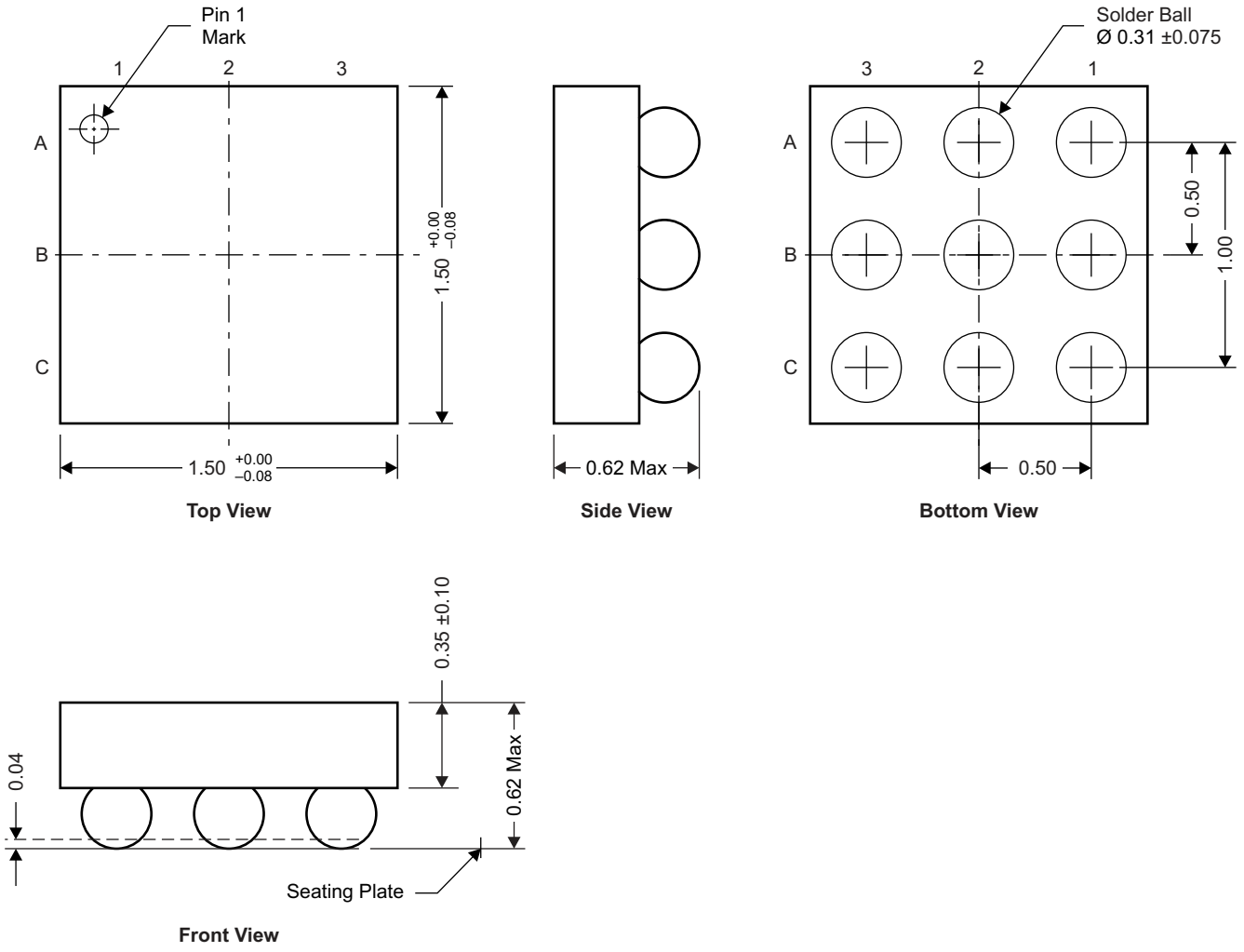
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD75207W15 Package Dimensions

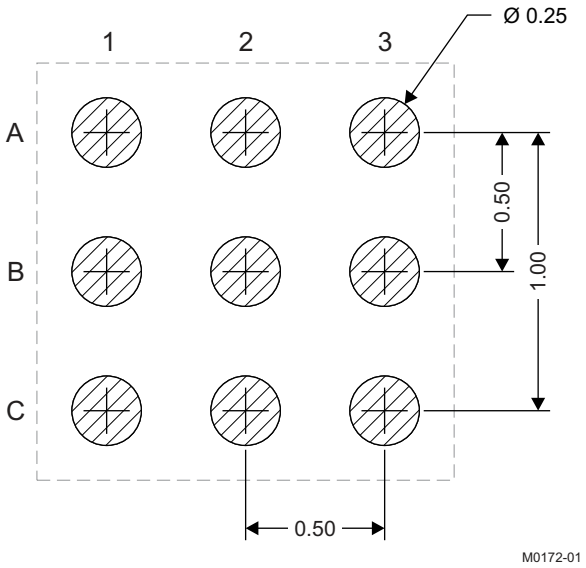


NOTE: All dimensions are in mm (unless otherwise specified)

Pinout

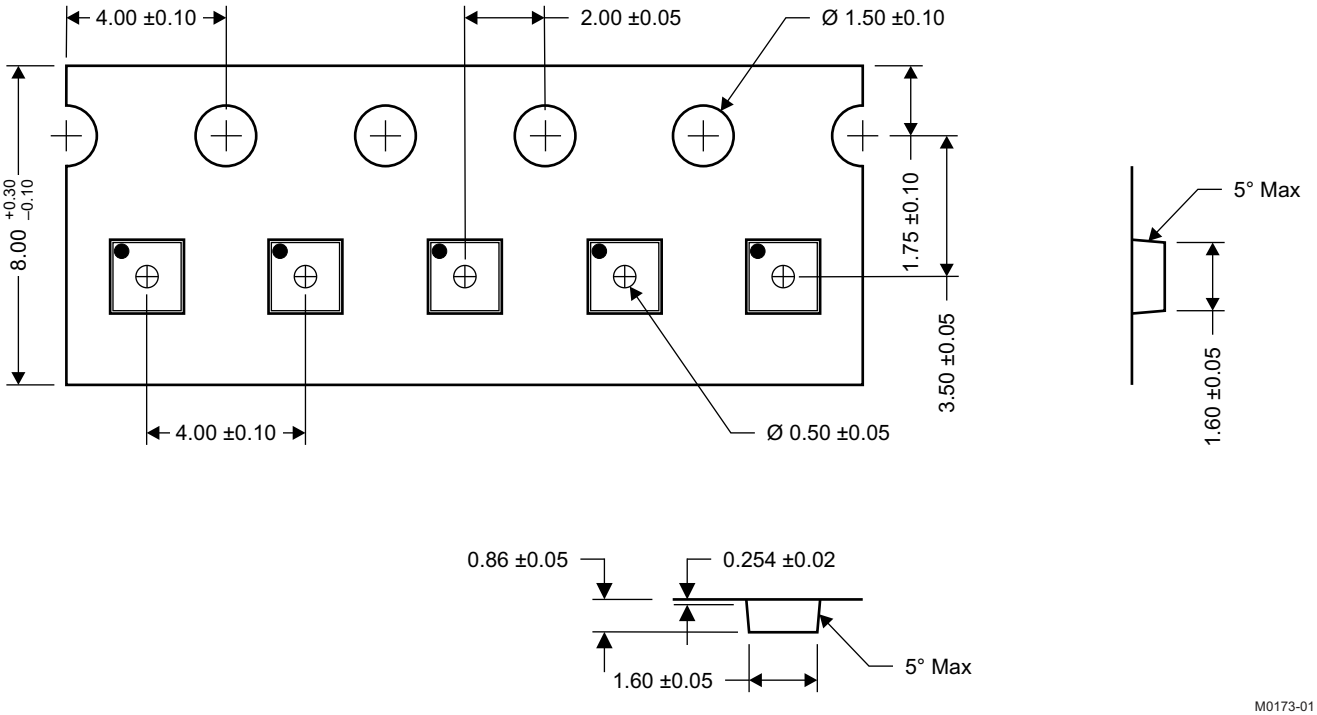
POSITION	DESIGNATION
A1	Gate1
A2, A3, B3	Drain1
C1	Gate2
C2, C3, B2	Drain2
B1	Source Sense

7.2 Recommended PCB Land Pattern



NOTE: All dimensions are in mm (unless otherwise specified).

7.3 Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD75207W15	ACTIVE	DSBGA	YZF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-55 to 150	75207	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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