74LVC3GU04

Triple unbuffered inverter

Rev. 11 — 9 April 2013 Product data sheet

1. General description

The 74LVC3GU04 is a triple unbuffered inverter.

Inputs can be driven from either 3.3 V or 5 V devices. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- ±24 mA output drive at V_{CC} = 3.0 V
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC3GU04DP	−40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC3GU04DC	−40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC3GU04GT	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC3GU04GF	−40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
74LVC3GU04GD	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT996-2

Table 1. Ordering information *...continued*

Type number	Package			
	Temperature range	Name	Description	Version
74LVC3GU04GM	−40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2
74LVC3GU04GN	−40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74LVC3GU04GS	−40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74LVC3GU04DP	VU04
74LVC3GU04DC	VU4
74LVC3GU04GT	VU4
74LVC3GU04GF	YD
74LVC3GU04GD	VU4
74LVC3GU04GM	VU4
74LVC3GU04GN	YD
74LVC3GU04GS	YD

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

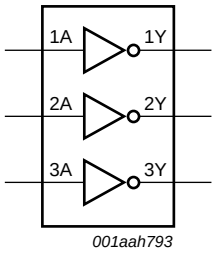


Fig 1. Logic symbol

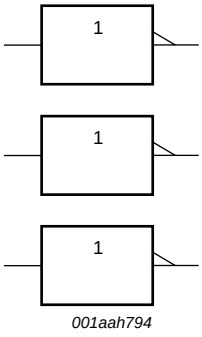


Fig 2. IEC logic symbol

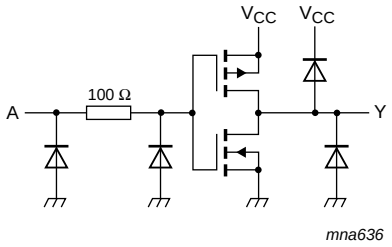


Fig 3. Logic diagram (one gate)

6. Pinning information

6.1 Pinning

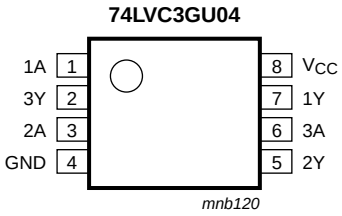
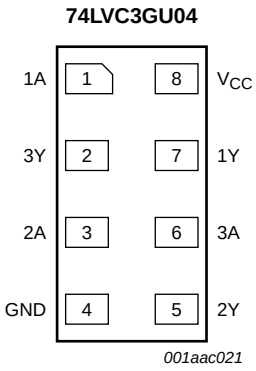
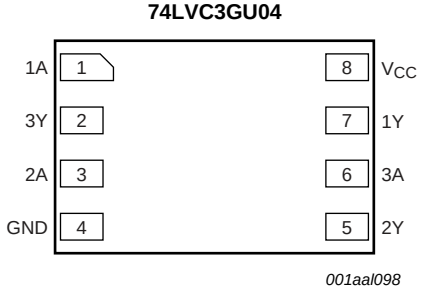


Fig 4. Pin configuration SOT505-2 and SOT765-1



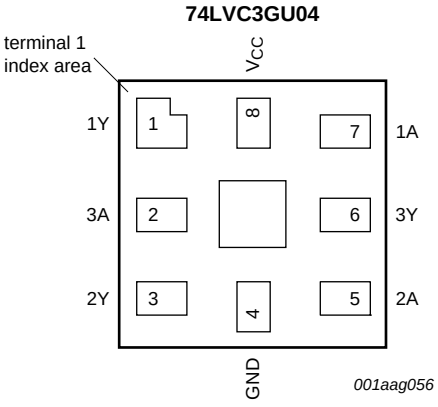
Transparent top view

Fig 5. Pin configuration SOT833-1, SOT1089, SOT1116 and SOT1203



Transparent top view

Fig 6. Pin configuration SOT996-2



Transparent top view

Fig 7. Pin configuration SOT902-2

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT833-1, SOT1089, SOT996-2, SOT1116 and SOT1203	SOT902-2	
1A, 2A, 3A	1, 3, 6	7, 5, 2	data input
GND	4	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	1, 3, 6	data output
V_{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table[1]

Input nA	Output nY
L	H
H	L

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+6.5	V
V_I	input voltage		[1]	−0.5	+6.5	V
V_O	output voltage	Active mode	[1]	−0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V		−50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			−100	-	mA
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C	[2]	-	250	mW
T_{stg}	storage temperature			−65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 packages: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8 and XQFN8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	5.5	V
T_{amb}	ambient temperature		−40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 5.5 V	0.75 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 5.5 V	-	-	0.25 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −100 μA; V_{CC} = 1.65 V to 5.5 V	V_{CC} − 0.1	-	-	V
		I_O = −4 mA; V_{CC} = 1.65 V	1.2	-	-	V
		I_O = −8 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = −12 mA; V_{CC} = 2.7 V	2.2	-	-	V
		I_O = −24 mA; V_{CC} = 3.0 V	2.3	-	-	V
		I_O = −32 mA; V_{CC} = 4.5 V	3.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	±0.1	±5	μA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	0.1	10	μA
C_I	input capacitance		-	5	-	pF

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 5.5 V	0.8 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 5.5 V	-	-	0.2 × V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –100 μA; V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1	-	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	0.95	-	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.7	-	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	1.9	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.0	-	-	V
		I_O = –32 mA; V_{CC} = 4.5 V	3.4	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.80	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	±20	μA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	-	40	μA

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 9.

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Figure 8 [2]						
		V_{CC} = 1.65 V to 1.95 V	0.5	2.3	5.0	0.5	6.3	ns
		V_{CC} = 2.3 V to 2.7 V	0.3	1.8	4.0	0.3	4.0	ns
		V_{CC} = 2.7 V	0.3	2.6	4.5	0.3	5.6	ns
		V_{CC} = 3.0 V to 3.6 V	0.3	2.3	3.7	0.3	4.5	ns
		V_{CC} = 4.5 V to 5.5 V	0.3	1.7	3.0	0.3	3.8	ns

Table 8. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 9.

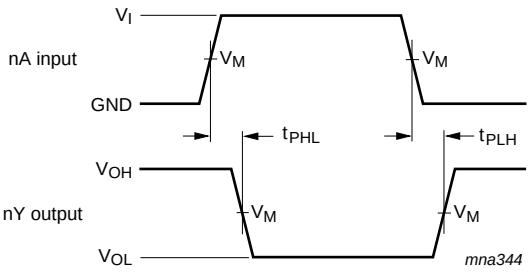
Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V [3]	-	7	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



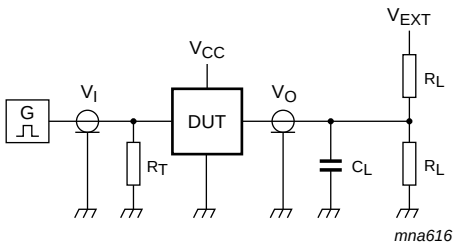
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The input (nA) to output (nY) propagation delays

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	0.5 × V_{CC}	0.5 × V_{CC}
2.3 V to 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V_{CC}	0.5 × V_{CC}



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

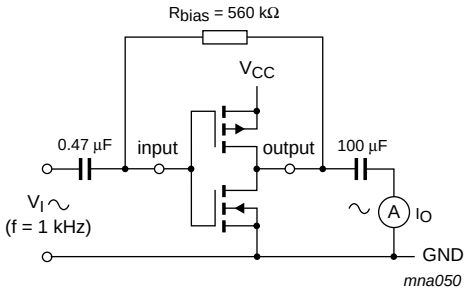
V_{EXT} = External voltage for measuring switching times.

Fig 9. Test circuit for measuring switching times

Table 10. Test data

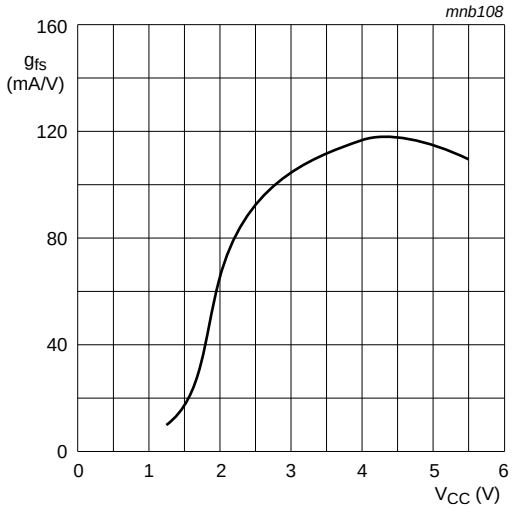
Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Additional characteristics



$$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$$

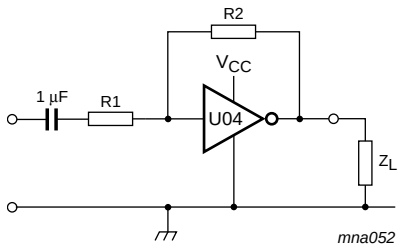
Fig 10. Test set-up for measuring forward transconductance



T_{amb} = 25 °C.

Fig 11. Typical forward transconductance as a function of supply voltage

14. Application information



Z_L > 10 kΩ

R1 ≥ 3 kΩ

R2 ≤ 1 MΩ

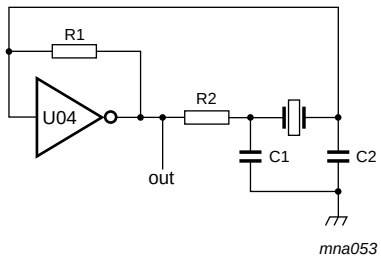
Open loop gain: G_{ol} = 20

Voltage gain: $G_v = -\dfrac{G_{ol}}{1 + \dfrac{R1}{R2}(1 + G_{ol})}$

$V_{o(p\text{-}p)} = V_{CC}$ − 1.5 V centered at 0.5 × V_{CC}

Unity gain bandwidth product is 5 MHz.

Fig 12. Linear amplifier application



C1 = 47 pF

C2 = 22 pF

R1 = 1 MΩ to 10 MΩ

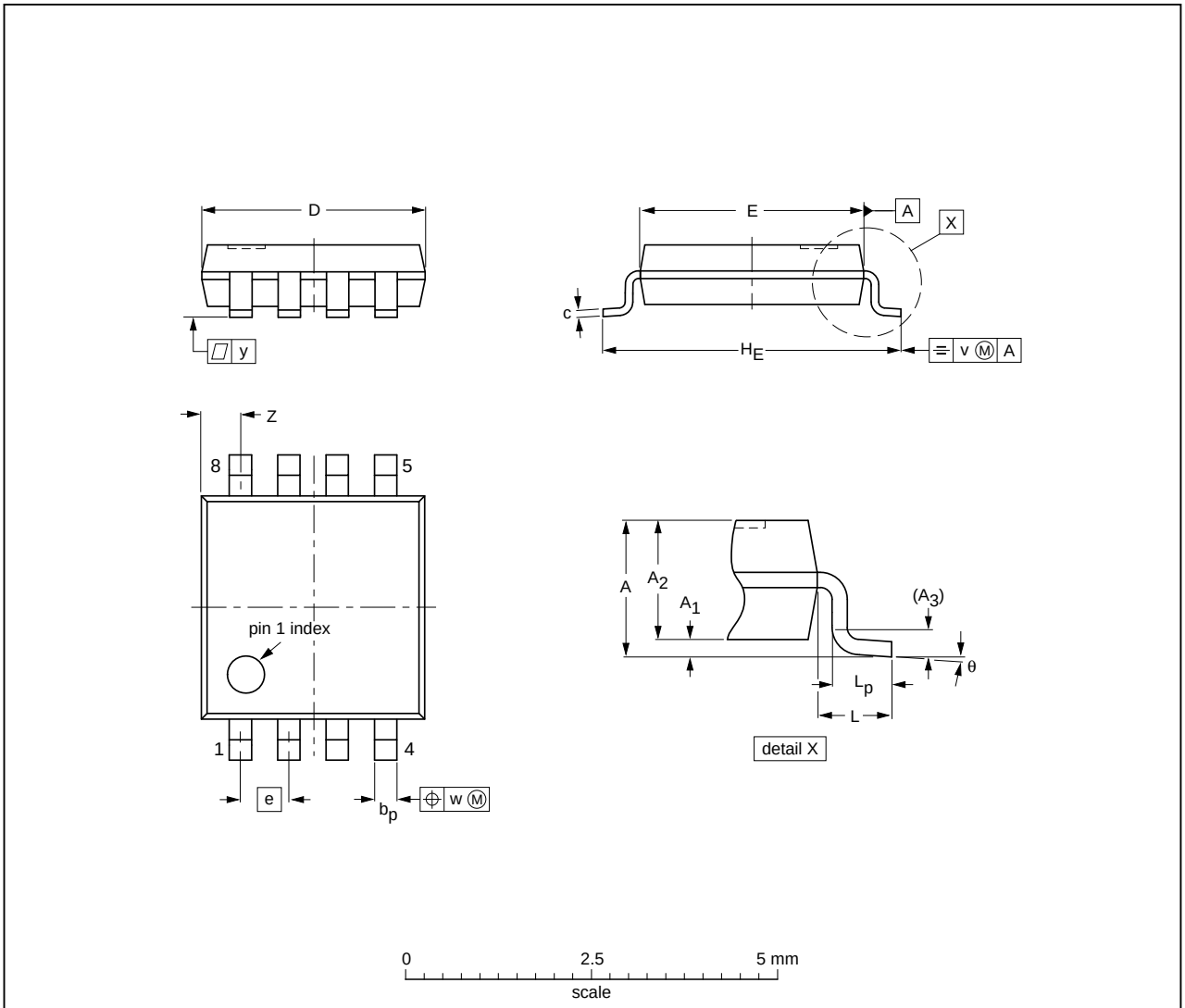
R2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} = 2 mA at V_{CC} = 3.3 V and f = 10 MHz).

Fig 13. Crystal oscillator application

Remark: All values given are typical values unless otherwise specified.

15. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

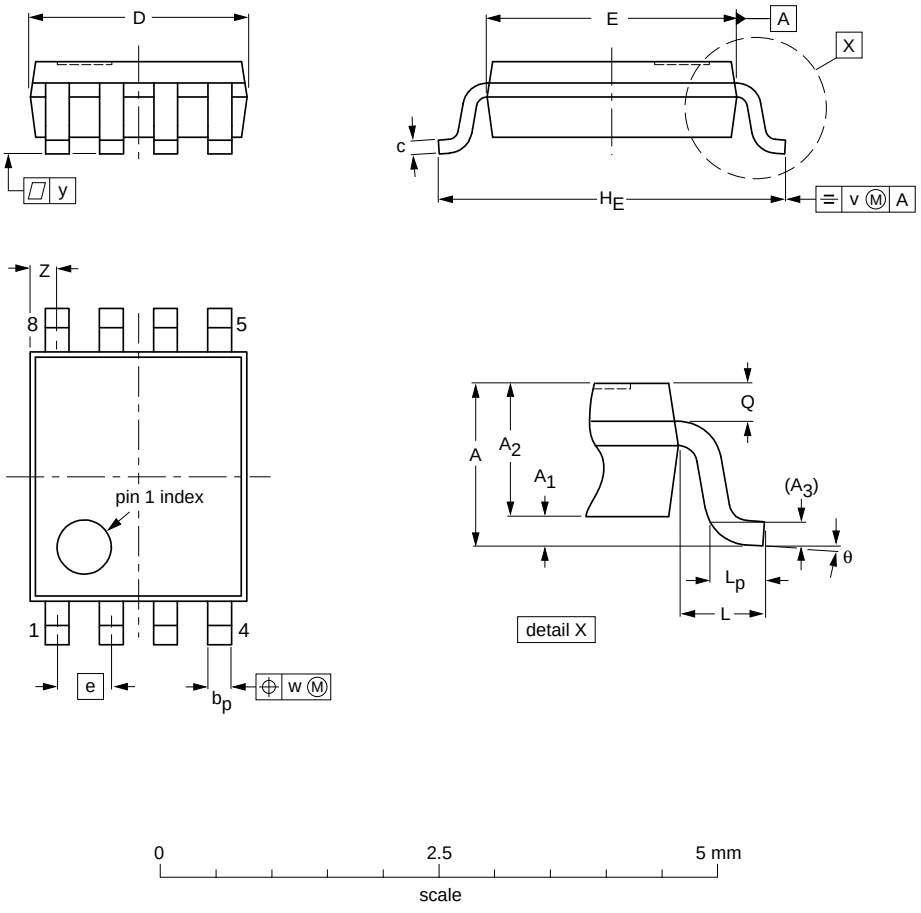
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 14. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

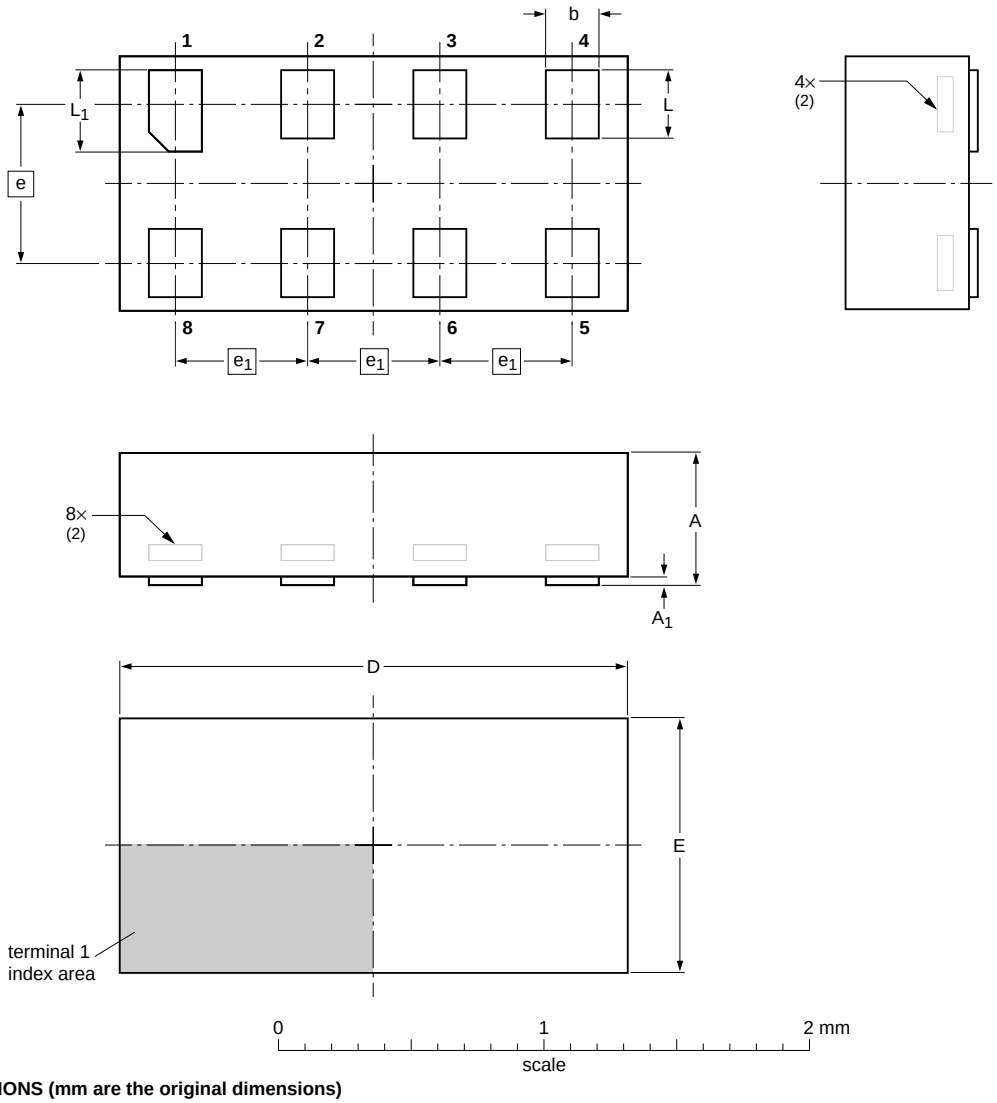
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 15. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

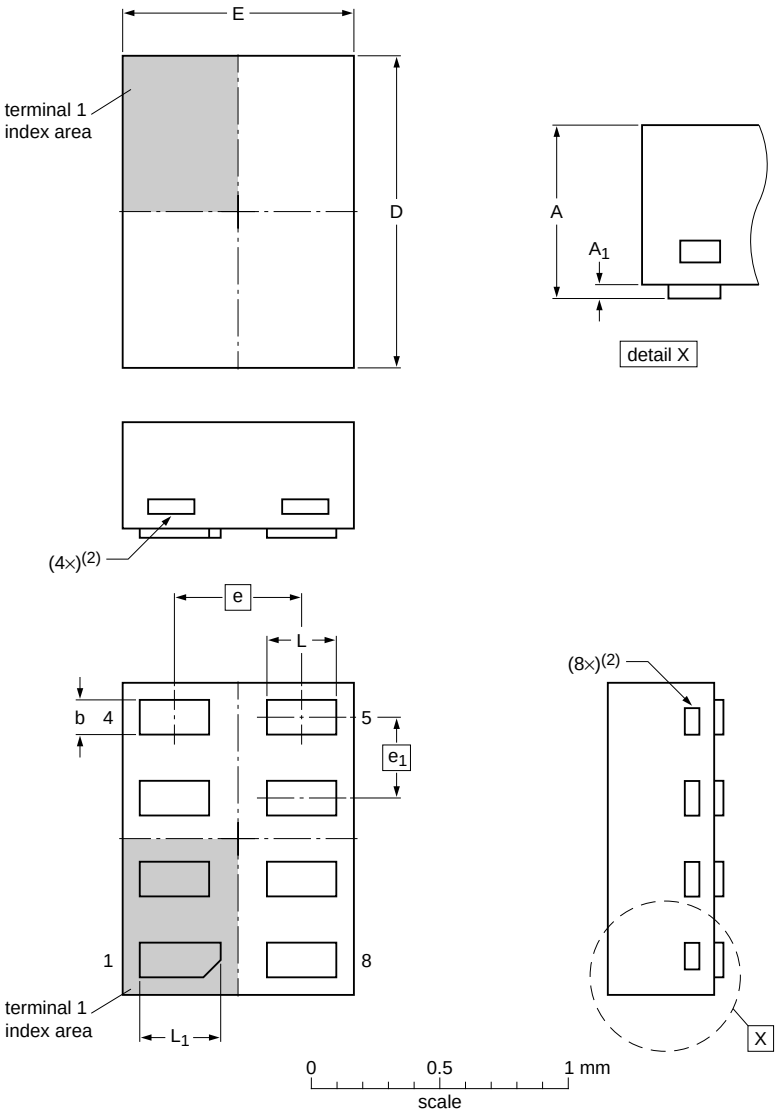
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig 16. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm **SOT1089**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.20	1.40	1.05			0.35	0.40
	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

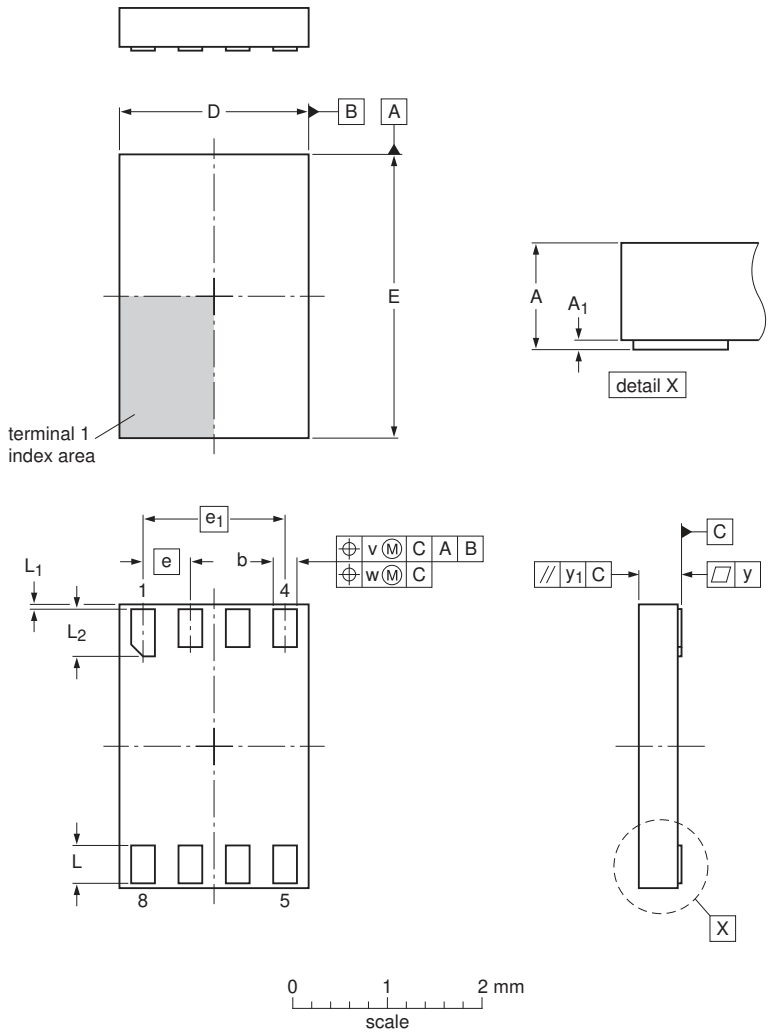
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1089_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1089		MO-252				~~10-04-09~~ 10-04-12

Fig 17. Package outline SOT1089 (XSON8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 3 x 2 x 0.5 mm **SOT996-2**



Dimensions (mm are the original dimensions)

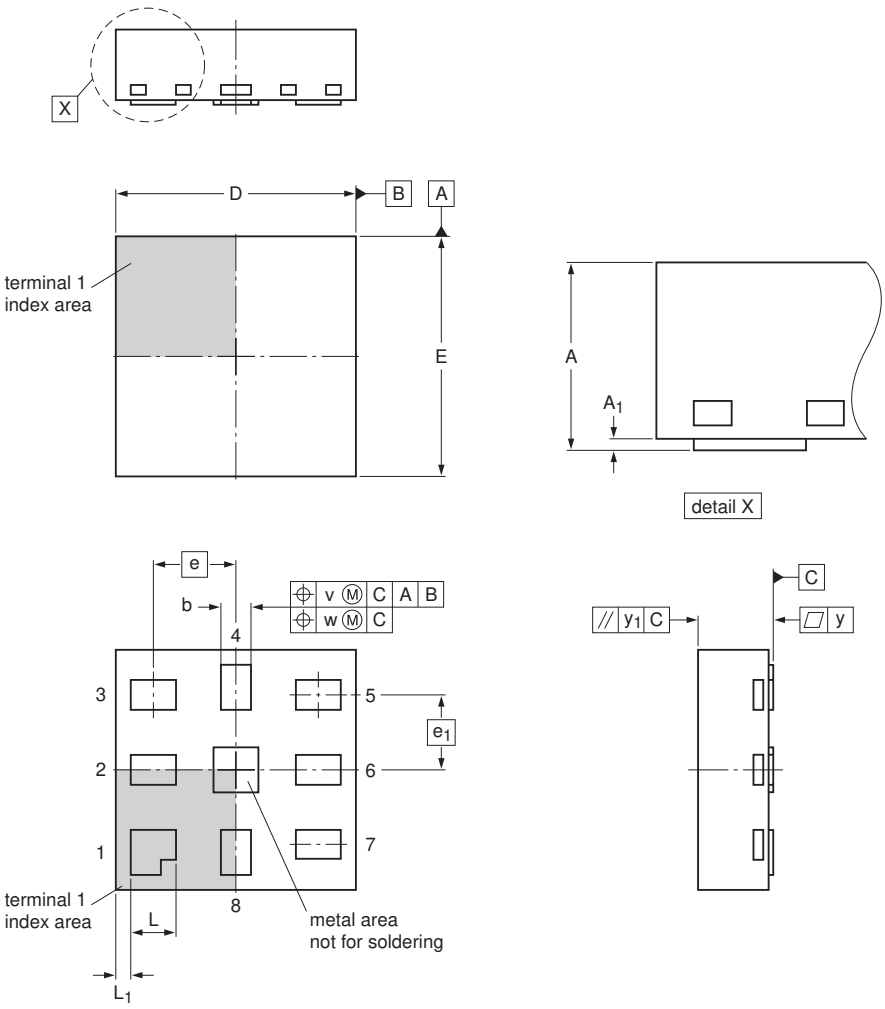
Unit[1]		A	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
mm	max	0.5	0.05	0.35	2.1	3.1	0.5	1.5	0.5	0.15	0.6	0.1	0.05	0.05	0.1
	nom														
	min		0.00	0.15	1.9	2.9			0.3	0.05	0.4				

sot996-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT996-2						~~07-12-21~~ 12-11-20

Fig 18. Package outline SOT996-2 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm **SOT902-2**



Dimensions

Unit(1)		A	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	1.65	1.65			0.35	0.15				
	nom			0.20	1.60	1.60	0.55	0.5	0.30	0.10	0.1	0.05	0.05	0.05
	min		0.00	0.15	1.55	1.55			0.25	0.05				

Note

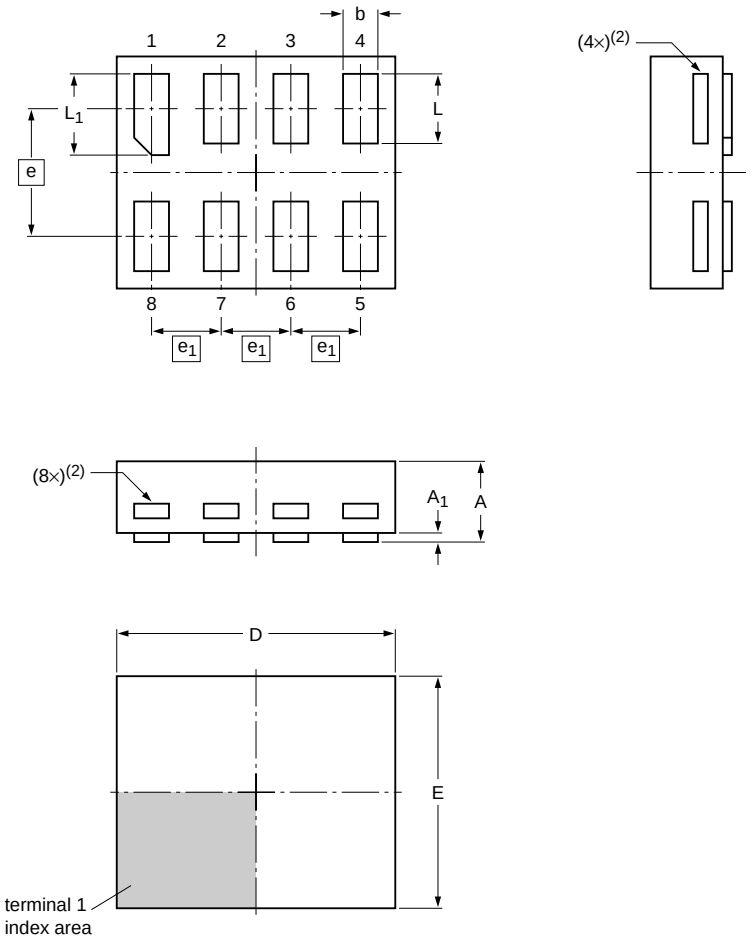
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT902-2	- - -	MO-255	- - -			~~10-11-02~~ 11-03-31

Fig 19. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm **SOT1116**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.25	1.05			0.35	0.40
	nom			0.15	1.20	1.00	0.55	0.3	0.30	0.35
	min			0.12	1.15	0.95			0.27	0.32

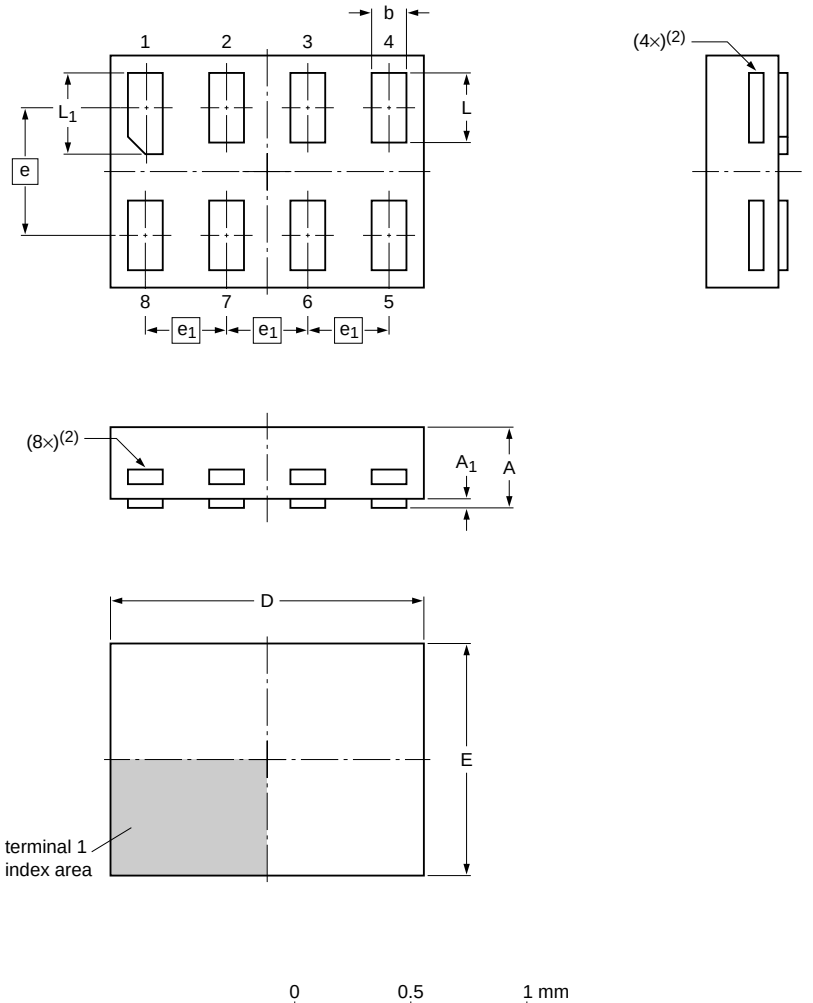
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1116_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1116						~~10-04-02~~ 10-04-07

Fig 20. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm **SOT1203**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.40	1.05			0.35	0.40
	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1203_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						~~10-04-02~~ 10-04-06

Fig 21. Package outline SOT1203 (XSON8)

16. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

17. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC3GU04 v.11	20130409	Product data sheet	-	74LVC3GU04 v.10
Modifications:	• For type number 74LVC3GU04GD XSON8U has changed to XSON8.			
74LVC3GU04 v.10	20120706	Product data sheet	-	74LVC3GU04 v.9
Modifications:	• For type number 74LVC3GU04GM the SOT code has changed to SOT902-2.			
74LVC3GU04 v.9	20111123	Product data sheet	-	74LVC3GU04 v.8
Modifications:	• Legal pages updated.			
74LVC3GU04 v.8	20101110	Product data sheet	-	74LVC3GU04 v.7
74LVC3GU04 v.7	20091111	Product data sheet	-	74LVC3GU04 v.6
74LVC3GU04 v.6	20080304	Product data sheet	-	74LVC3GU04 v.5
74LVC3GU04 v.5	20071005	Product data sheet	-	74LVC3GU04 v.4
74LVC3GU04 v.4	20070315	Product data sheet	-	74LVC3GU04 v.3
74LVC3GU04 v.3	20050201	Product data sheet	-	74LVC3GU04 v.2
74LVC3GU04 v.2	20041027	Product data sheet	-	74LVC3GU04 v.1
74LVC3GU04 v.1	20040512	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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