74LVC1G06

Inverter with open-drain output Rev. 10 — 29 June 2012

Product data sheet

General description 1.

The 74LVC1G06 provides the inverting buffer.

Input can be driven from either 3.3 V or 5 V devices. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The output of the device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- \pm 24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +125 °C



3. Ordering information

Table 1. Ordering information

Type number	Package						
	Temperature range	Name	Description	Version			
74LVC1G06GW	–40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1			
74LVC1G06GV	–40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753			
74LVC1G06GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1.45 \times 0.5$ mm	SOT886			
74LVC1G06GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1 \times 0.5$ mm	SOT891			
74LVC1G06GN	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $0.9 \times 1.0 \times 0.35$ mm	SOT1115			
74LVC1G06GS	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $1.0 \times 1.0 \times 0.35$ mm	SOT1202			
74LVC1G06GX	–40 °C to +125 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body $0.8 \times 0.8 \times 0.35$ mm	SOT1226			

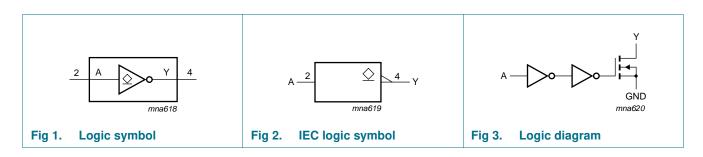
4. Marking

Table 2. Marking codes

Type number	Marking[1]
74LVC1G06GW	VR
74LVC1G06GV	V06
74LVC1G06GM	VR
74LVC1G06GF	VR
74LVC1G06GN	VR
74LVC1G06GS	VR
74LVC1G06GX	VR

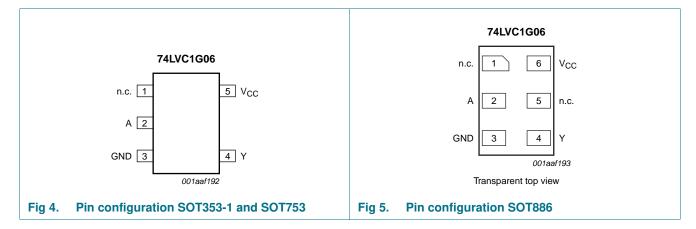
^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

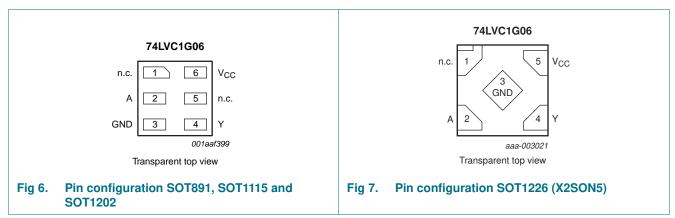
5. Functional diagram



6. Pinning information

6.1 Pinning





6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5 and X2SON5 XS		
n.c.	1	1	not connected
Α	2	2	data input
GND	3	3	ground (0 V)
Υ	4	4	data output
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table[1]

Input	Output
A	Υ
L	Z
Н	L

^[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
VI	input voltage		<u>[1]</u> –0.5	+6.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0 \text{ V}$	-	±50	mA
V _O	output voltage	Active mode and Power-down mode	[1][2] -0.5	+6.5	V
I _{O(sink/source)}	output sink or source current	$V_O = 0 V \text{ to } V_{CC}$	-	±50	mA
I _{CC}	supply current		-	+100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[3] _	250	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_{I}	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	5.5	V
		Power-down mode; V _{CC} = 0 V	0	-	5.5	V
T _{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V _{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

^[2] When $V_{CC} = 0 \ V$ (Power-down mode), the output voltage can be 5.5 V in normal operation.

^[3] For TSSOP5 and SC-74A packages: above 87.5 $^{\circ}$ C the value of P_{tot} derates linearly with 4.0 mW/K. For XSON6 and X2SON5 package: above 118 $^{\circ}$ C the value of P_{tot} derates linearly with 7.8 mW/K.

10. Static characteristics

Static characteristics Table 7.

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	–40 °C to +85 °C			+125 °C	Unit
		Min	Typ[1]	Max	Min	Max		
V_{IH}	HIGH-level	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
	input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level	V _{CC} = 1.65 V to 1.95 V	-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V
	input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	8.0	-	8.0	V
		V _{CC} = 4.5 V to 5.5 V	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
V_{OL}	LOW-level	$V_{I} = V_{IH}$ or V_{IL}						
output vo	output voltage	$I_O = 100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.10	-	0.10	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.70	٧
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.30	-	0.45	٧
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.40	-	0.60	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.80	V
		$I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.55	-	0.80	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±5	-	±100	μА
l _{OFF}	power-off leakage current	$V_{I} \text{ or } V_{O} = 5.5 \text{ V}; V_{CC} = 0 \text{ V}$	-	±0.1	±10	-	±200	μΑ
I _{CC}	supply current	$V_{I} = 5.5 \text{ V or GND}; I_{O} = 0 \text{ A};$ $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	0.1	10	-	200	μА
ΔI_{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A};$ $V_{CC} = 2.3 \text{ V to } 5.5 \text{ V}; \text{ per pin}$	-	5	500	-	5000	μА
C _I	input capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}	-	5	-	-	-	pF

^[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for load circuit see Figure 9.

Symbol	Parameter	Conditions		–40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	A to Y; see Figure 8	[2]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		1.0	3	6.5	1.0	8.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.5	1.9	4	0.5	5.5	ns
		$V_{CC} = 2.7 \text{ V}$		0.5	2.5	4.5	0.5	6	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		0.5	2.3	4	0.5	5.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		0.5	1.7	3	0.5	4	ns
C_{PD}	power dissipation capacitance	$V_I = GND$ to V_{CC} ; $V_{CC} = 3.3 \text{ V}$	[3]	-	14	-	-	-	pF

^[1] Typical values are measured at $T_{amb} = 25$ °C and $V_{CC} = 1.8$ V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

 f_i = input frequency in MHz;

 $f_o = output frequency in MHz;$

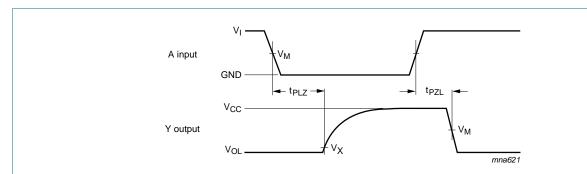
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_o) = sum \text{ of outputs.}$

12. Waveforms



Measurement points are given in Table 9.

V_{OL} is the typical output voltage level that occurs with the output load.

Fig 8. The input A to output Y propagation delay times

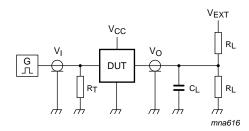
^[2] t_{pd} is the same as t_{PLZ} and t_{PZL} .

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Table 9. Measurement points

Supply voltage	Input	Output	Output		
V _{CC}	V _M	V _M	V _X		
1.65 V to 1.95 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V		
2.3 V to 2.7 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V		
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V		
3.0 V to 3.6 V	1.5 V	1.5 V	V _{OL} + 0.3 V		
4.5 V to 5.5 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.3 V		



Test data is given in Table 10.

Definitions test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Fig 9. Test circuit for measuring switching times

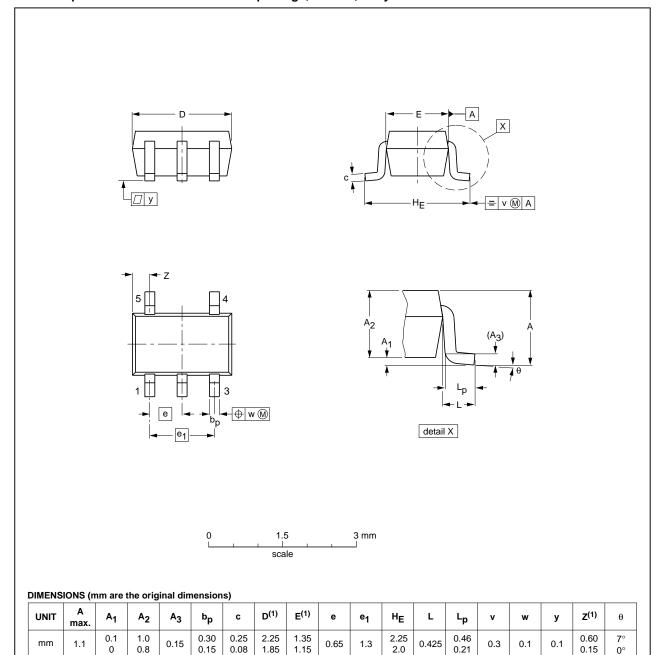
Table 10. Test data

Supply voltage	Input	Input			V _{EXT}
V _{CC}	VI	$t_r = t_f$	CL	RL	t _{PZL} , t _{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	2V _{CC}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	2V _{CC}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	2V _{CC}

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE	OUTLINE REFERENCES			EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT353-1		MO-203	SC-88A			-00-09-01 03-02-19

Fig 10. Package outline SOT353-1 (TSSOP5)

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Plastic surface-mounted package; 5 leads

SOT753

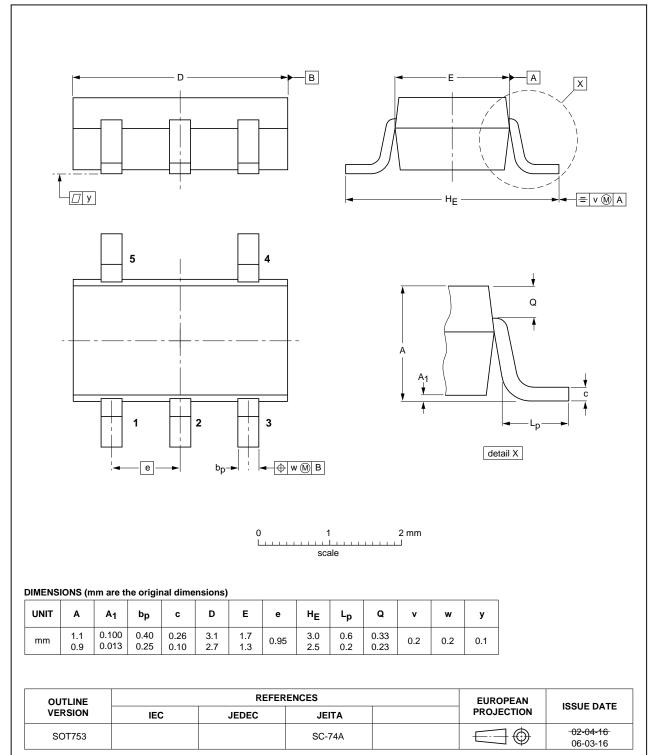


Fig 11. Package outline SOT753 (SC-74A)

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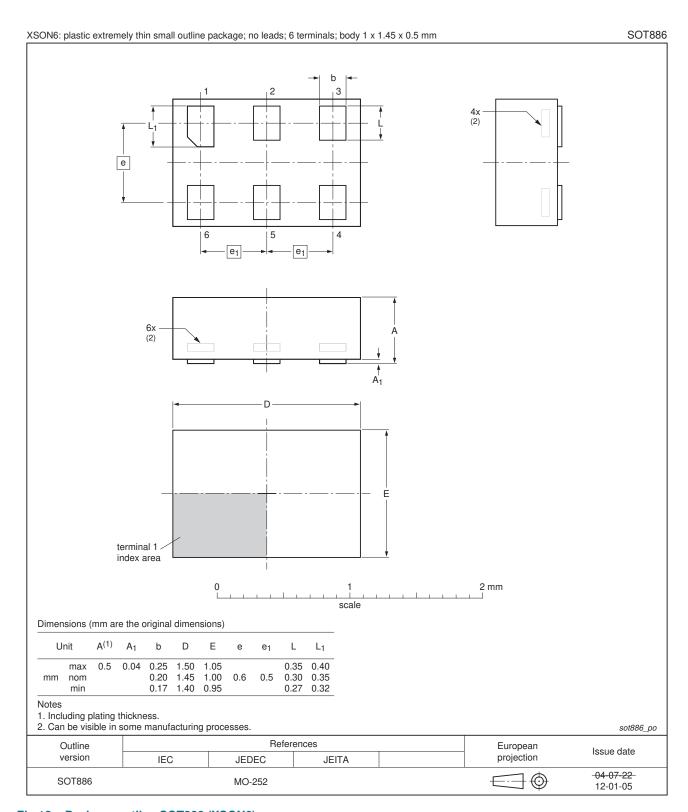


Fig 12. Package outline SOT886 (XSON6)

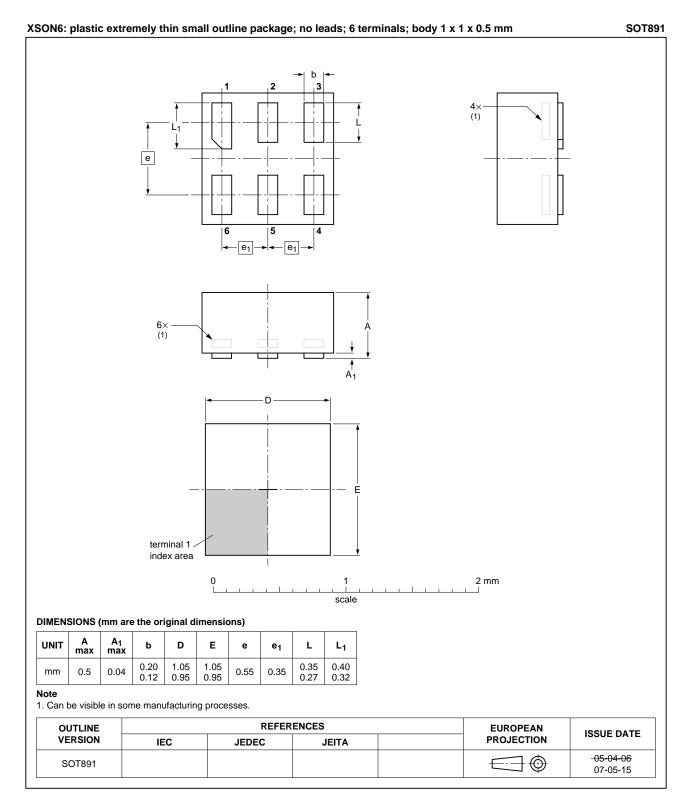


Fig 13. Package outline SOT891 (XSON6)

74LVC1G06

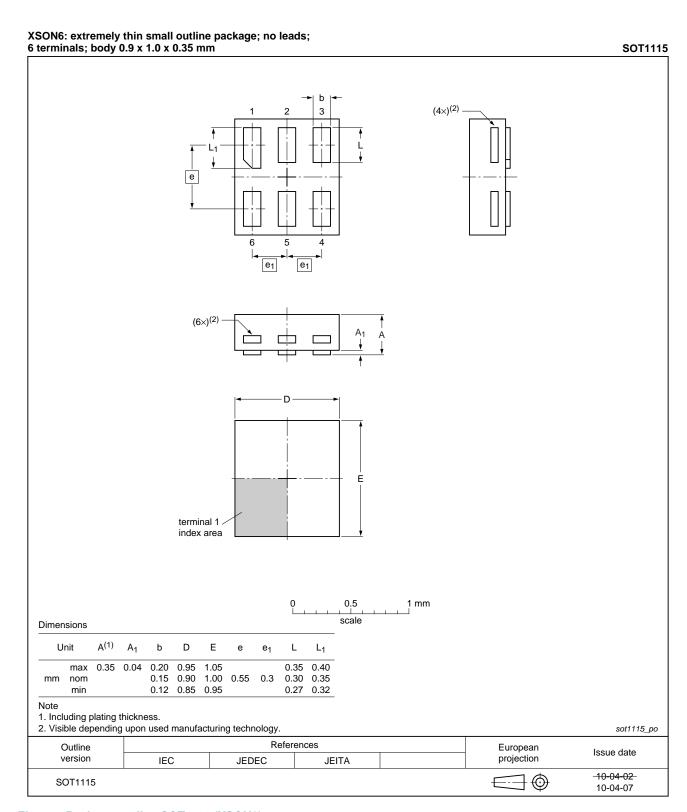


Fig 14. Package outline SOT1115 (XSON6)

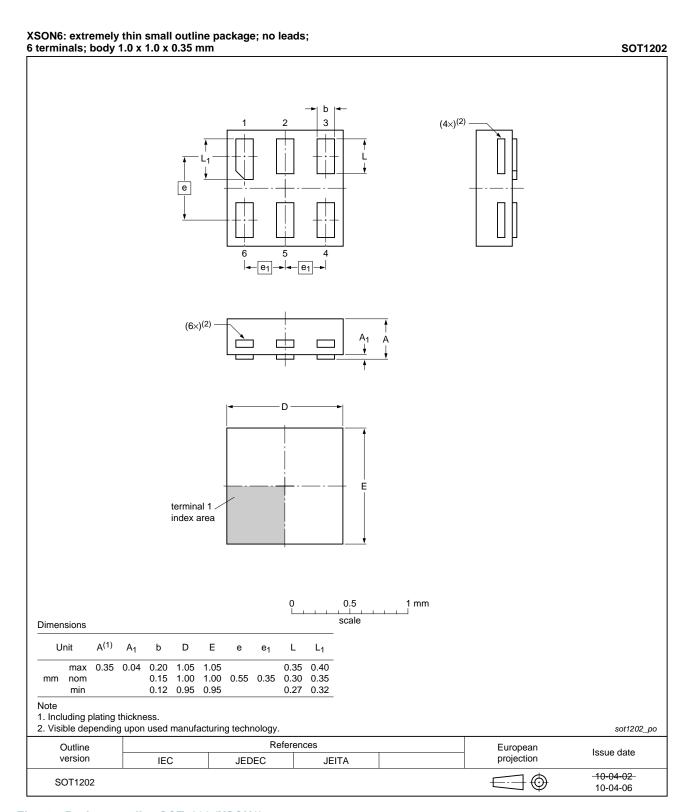


Fig 15. Package outline SOT1202 (XSON6)

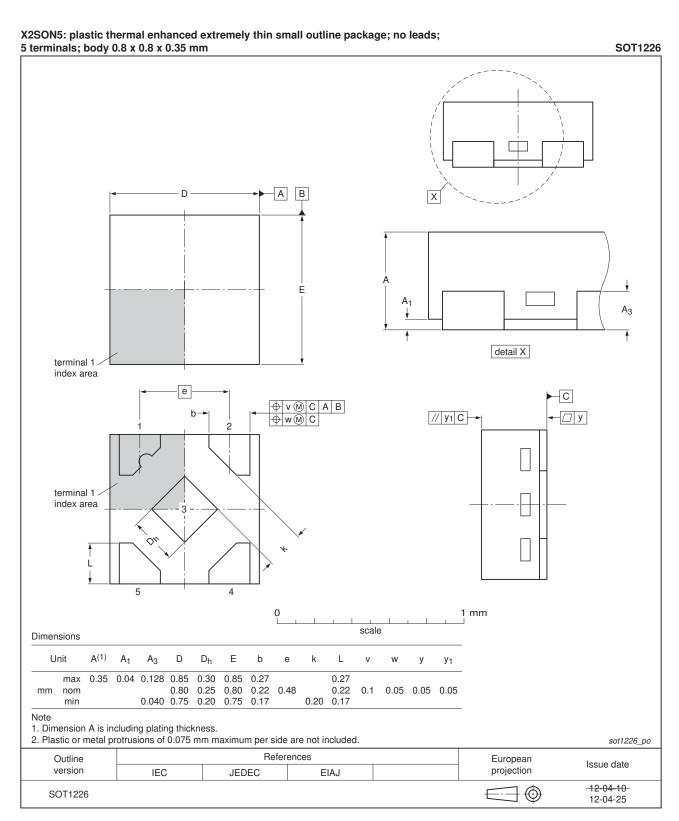


Fig 16. Package outline SOT1226 (X2SON5)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G06 v.10	20120629	Product data sheet	-	74LVC1G06 v.9
Modifications:	 Added type 	number 74LVC1G06GX (S	OT1226)	
	 Package ou 	ıtline drawing of SOT886 (<u>F</u>	Figure 12) modified.	
74LVC1G06 v.9	20111207	Product data sheet	-	74LVC1G06 v.8
Modifications:	 Legal pages 	s updated.		
74LVC1G06 v.8	20101026	Product data sheet	-	74LVC1G06 v.7
74LVC1G06 v.7	20070712	Product data sheet	-	74LVC1G06 v.6
74LVC1G06 v.6	20060912	Product data sheet	-	74LVC1G06 v.5
74LVC1G06 v.5	20040907	Product specification	-	74LVC1G06 v.4
74LVC1G06 v.4	20030303	Product specification	-	74LVC1G06 v.3
74LVC1G06 v.3	20020529	Product specification	-	74LVC1G06 v.2
74LVC1G06 v.2	20010405	Product specification	-	74LVC1G06 v.1
74LVC1G06 v.1	20001121	Product specification	-	-

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16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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