

# JLC1563

## I2C Bus Transceiver

JLC1563 is an I2C-bus signal transceiver and “conditioner”. Currently, systems complexity and I2C-bus device types and functionality are only increasing. As a result of I2C-bus loading the Clock line and Data line signals degrade. The JLC1563 I2C-Bus Transceiver restores clean signals in the system leading to improvements in system performance and reliability.

This device has two pins, SCL1 (Serial Clock Input) and SDA1 (Serial Data I/O), on the Master I2C-bus side; and two pins, SCL2 (Serial Clock Output) and SDA2 (Serial Data I/O), on the Slave I2C-bus side.

Two reset pins, Reset1 and Reset2, drive separate internal comparators and a system Power-On-Reset function is supported.

### Features

- Low Power Dissipation
- Two Pin Reset/Power-On-Reset
- Waveform Cleaning

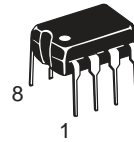


**ON Semiconductor**

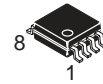
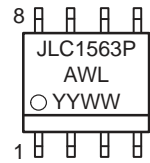
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**HIGH-PERFORMANCE CMOS**  
LOW-POWER COMPLEMENTARY  
MOS SILICON-GATE

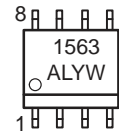
### MARKING DIAGRAMS



PDIP-8  
P SUFFIX  
CASE 626



SOEIAJ-8  
M SUFFIX  
CASE 968



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

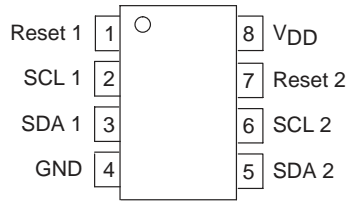
Device	Package	Shipping
JLC1563P	PDIP-8	50 Units/Rail
JLC1563M	SOEIAJ-8	See Note 1.
JLC1563ML1	SOEIAJ-8	See Note 1.

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

# JLC1563

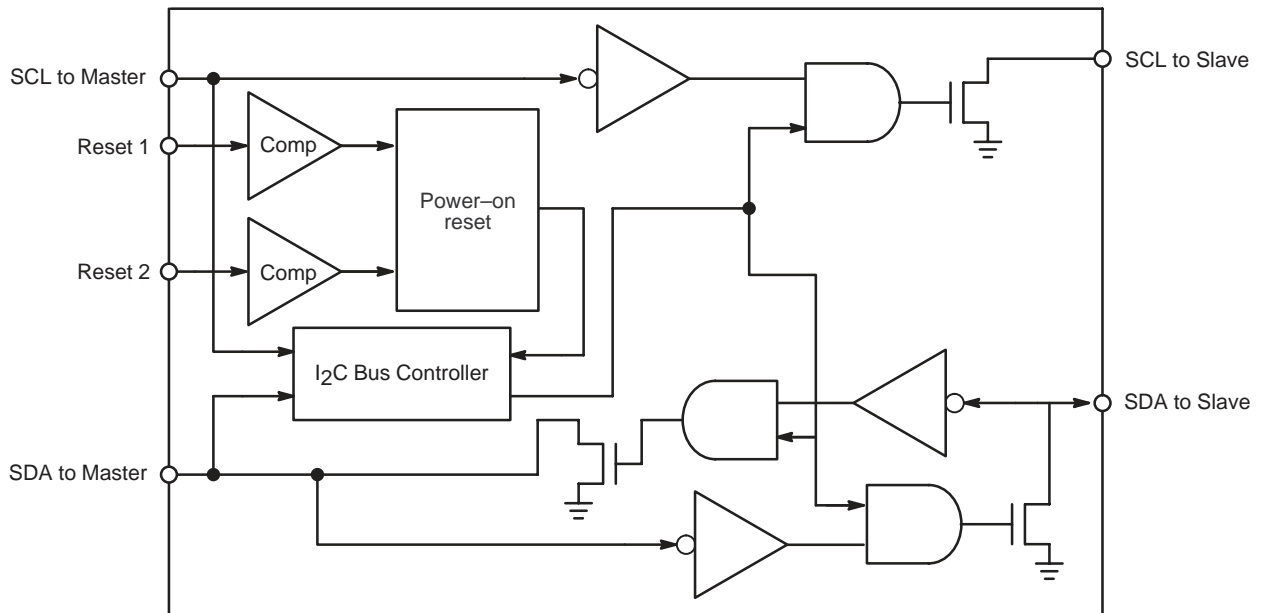
## PIN CONNECTIONS

### CASE 626/968



PIN LIST	
SCL 1	MASTER Serial Clock
SCL 2	SLAVE Serial Clock
SDA 1	MASTER Serial Data
SDA 2	SLAVE Serial Data
Reset 1	Reset Input 1 (Active Low)
Reset 2	Reset Input 2 (Active Low)

## BLOCK DIAGRAM



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## MAXIMUM RATINGS (V<sub>SS</sub> Reference)

Rating	Symbol	Value	Unit
DC Supply Voltage	V <sub>DD</sub>	-0.5 to +7.0	V
DC Input Voltage	V <sub>in</sub>	-0.5 to V <sub>DD</sub> + 0.5	V
DC Output Voltage	V <sub>out</sub>	-0.5 to V <sub>DD</sub> + 0.5	V
DC Input Output Current (per Pin)	I	25	mA
DC Supply Current (V <sub>DD</sub> and GND Pin)	I <sub>dd</sub>	75	mA
Storage Temperature	T <sub>stg</sub>	-65 to +150	°C
Lead Temperature (1 mm from case for 10 sec)	T <sub>L</sub>	300	°C

## RECOMMENDED OPERATING CONDITIONS

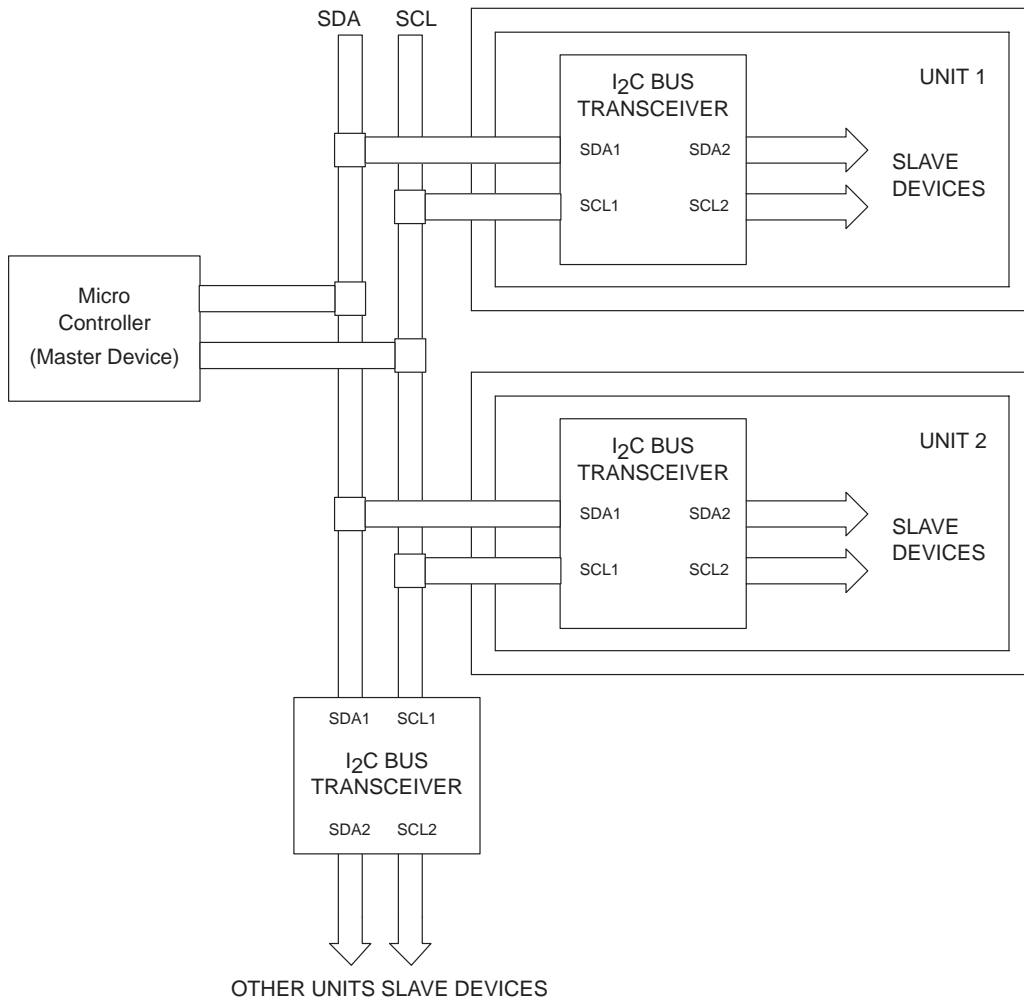
Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V <sub>DD</sub>	4.0	6.0	V
DC Input Voltage	V <sub>in</sub>	0.0	V <sub>DD</sub>	V
Operating Temperature	T <sub>A</sub>	-40	+85	°C

## DC CHARACTERISTICS (V<sub>SS</sub> Reference)

Characteristic	Symbol	Guaranteed Limits		Unit
		Min	Max	
Input Voltage "H" Level	V <sub>IH</sub>	0.7 V <sub>DD</sub>	-	V
Input Voltage "L" Level	V <sub>IL</sub>	-	0.3 V <sub>DD</sub>	V
Output Voltage "L" Level I <sub>out</sub> = 4 mA	V <sub>OL</sub>	-	0.3	V
Input Leakage Current V <sub>in</sub> = V <sub>DD</sub> or V <sub>SS</sub>	I <sub>in</sub>	-	±1.0	μA
Tri-State Leakage Current Output = High Impedance; V <sub>out</sub> = GND	I <sub>oz</sub>	-	±5.0	μA
Offset Voltage (Reset 1, Reset 2)	V <sub>IO</sub>	-	±0.1	V
Input Pin Capacitance	C <sub>in</sub>	-	10	pF
Output Pin Capacitance	C <sub>out</sub>	-	15	pF
In/Out Pin Capacitance	C <sub>i/o</sub>	-	15	pF
Quiescent Supply Current (per package)	I <sub>cc</sub>	-	5.0	mA

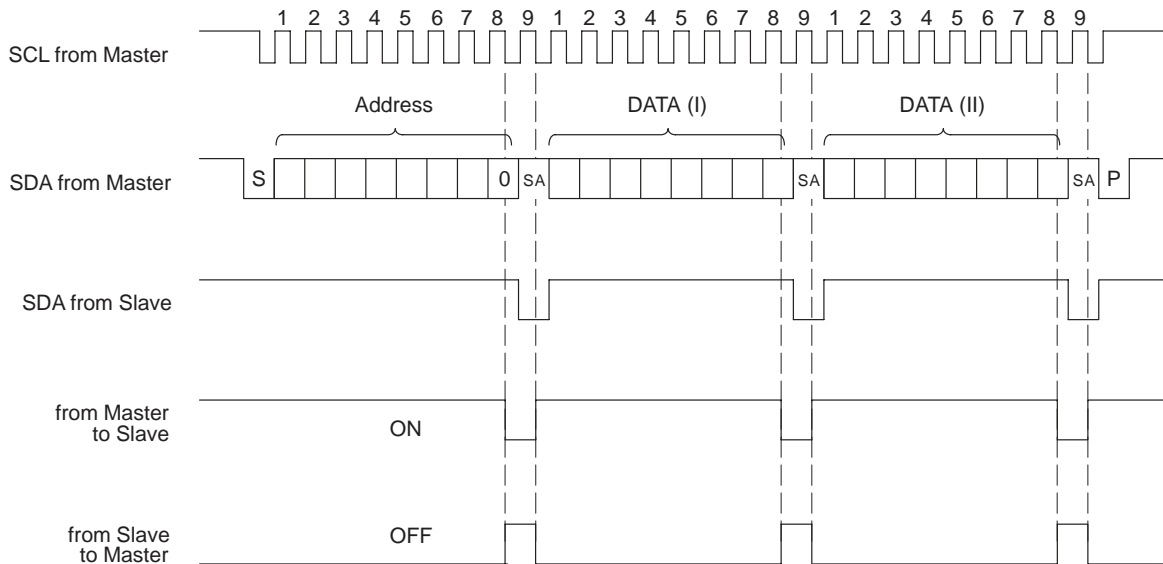
# JLC1563

## APPLICATION BLOCK



## I<sup>2</sup>C BUS TRANSCEIVER SIGNALS

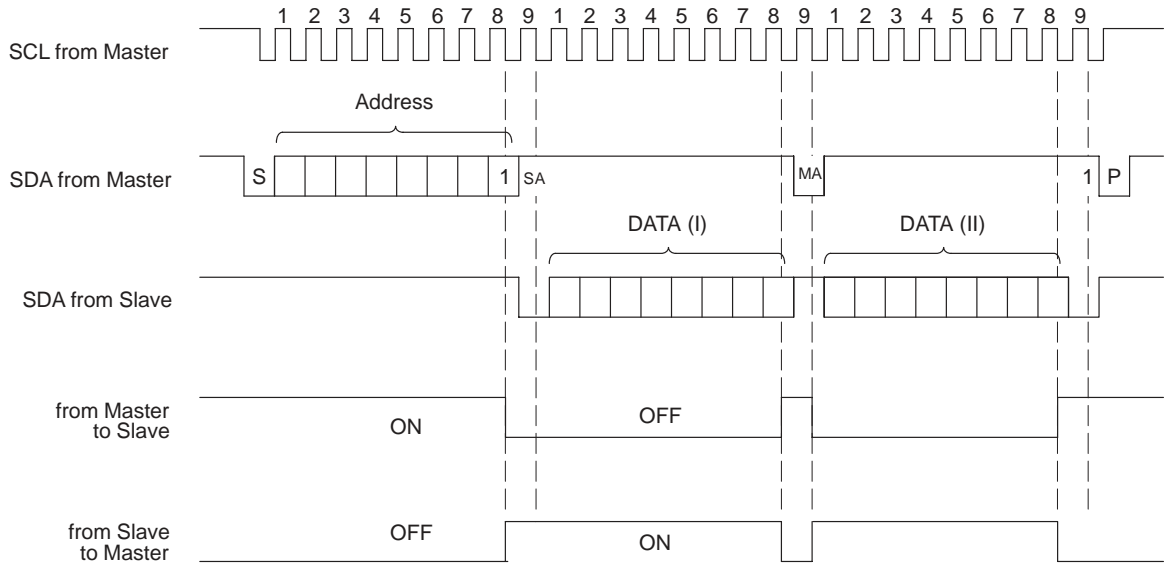
<<WRITE MODE>>



# JLC1563

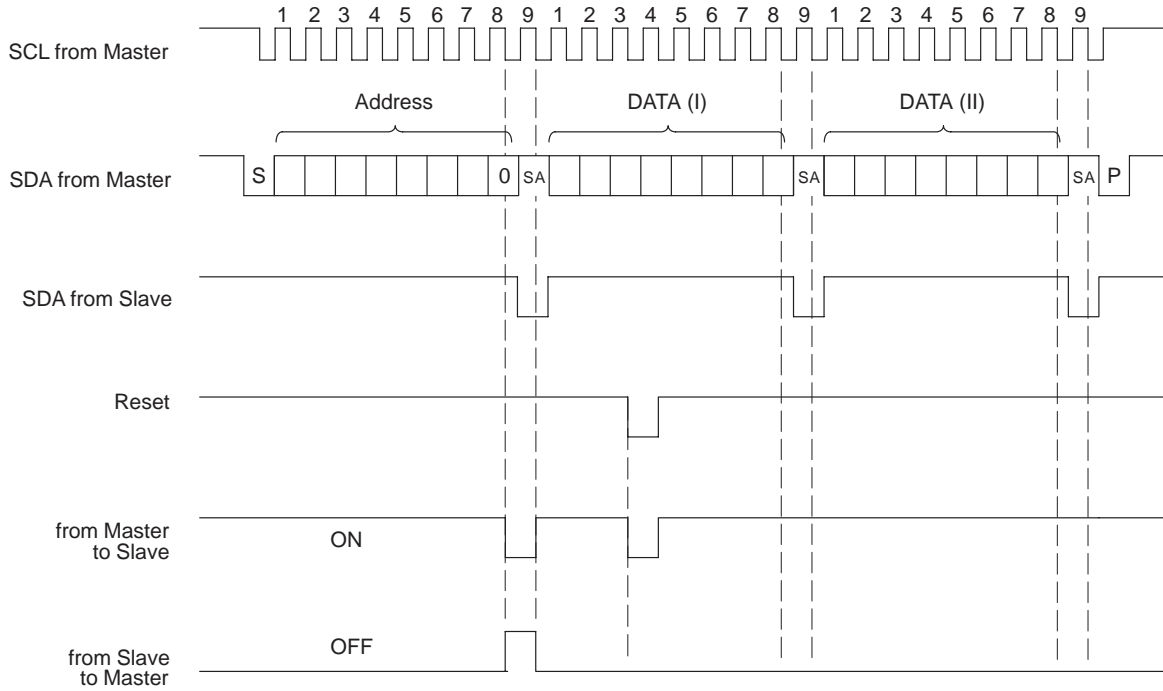
## I<sup>2</sup>C BUS TRANSCEIVER SIGNALS

<<READ MODE>>



## I<sup>2</sup>C BUS TRANSCEIVER SIGNALS (during RESET)

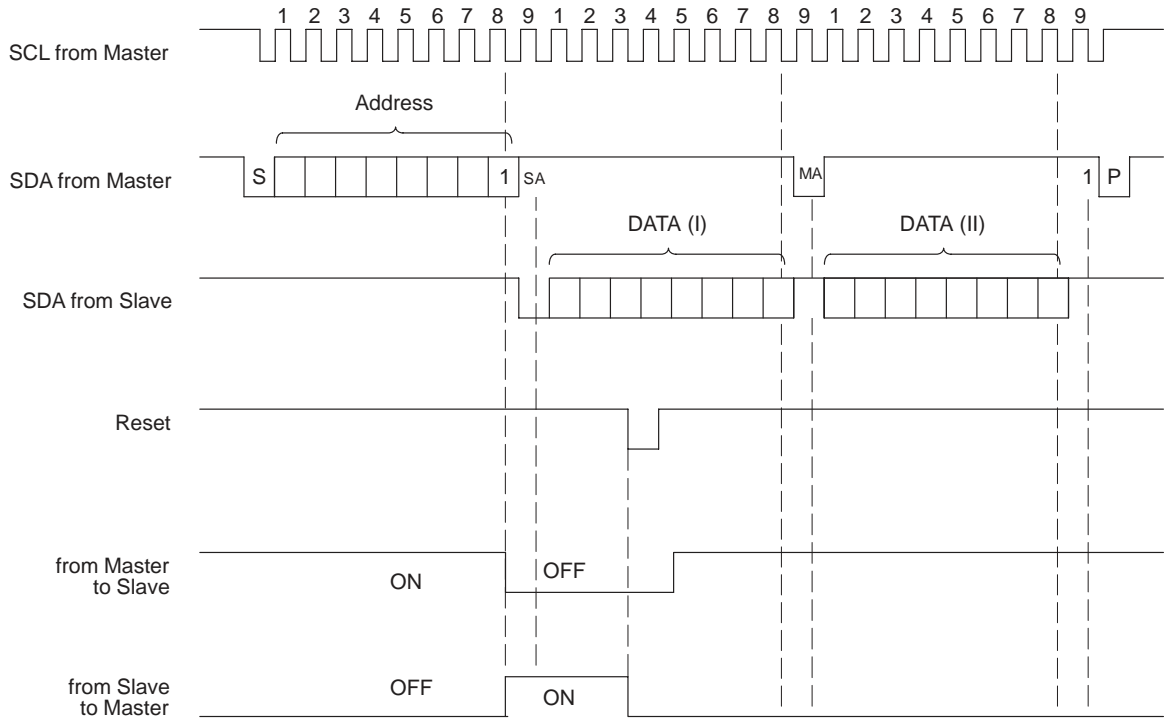
<<WRITE MODE>>



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## I<sup>2</sup>C BUS TRANSCEIVER SIGNALS (during RESET)

<<READ MODE>>



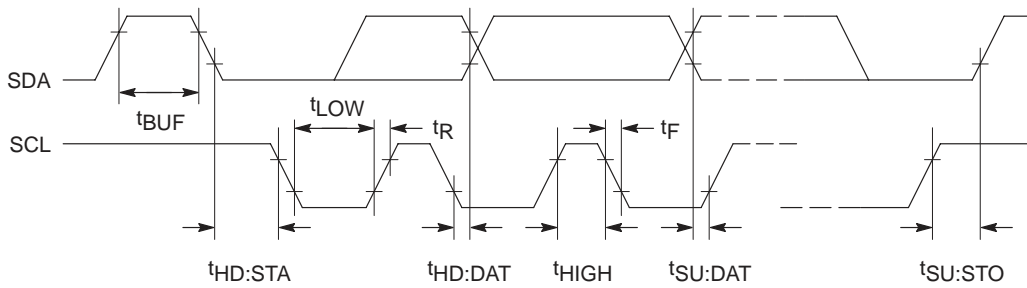
### BUS CONDITION KEY:

- S = START
- SA = SLAVE ACKNOWLEDGE
- MA = MASTER ACKNOWLEDGE
- P = STOP

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## I<sup>2</sup>C BUS STANDARDS (See Switching Chart for actual device parameters)

Parameter	Symbol	Guaranteed Limits		Unit
		Min	Max	
SCL Clock Frequency	$f_{CL}$	0	100	kHz
STOP Condition to START Condition Bus Free Time	$t_{BUF}$	4.7	–	$\mu$ s
START Condition Hold Time	$t_{HD:STA}$	4.0	–	$\mu$ s
SCL Clock LOW Hold Time	$t_{LOW}$	4.7	–	$\mu$ s
SCL Clock HI Hold Time	$t_{HIGH}$	4.0	–	$\mu$ s
SDA Data Hold Time	$t_{HD:DAT}$	0	–	$\mu$ s
SDA Data Setup Time	$t_{SU:DAT}$	250	–	nS
SDA and SCL Signal Rise Time	$t_R$	–	1000	nS
SDA and SCL Signal Fall Time	$t_F$	–	300	nS
STOP Condition Setup Time	$t_{SU:STO}$	4.0	–	$\mu$ s



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## SWITCHING CHART ( $V_{CC} = 5.0\text{ V}$ , $t_R = 1000\text{ nS}$ , $t_F = 300\text{ nS}$ )

Parameter	Symbol	Nominal 25°C	Guaranteed Limits		Unit
			Min	Max	
Maximum Delay SCL1 to SCL2	$t_{PHL}:SCL$	–	–	500	nS
Maximum Delay SCL1 to SCL2	$t_{PLZ}:SCL$	–	–	500	nS
Maximum Delay SDA1 to SDA2	$t_{PHL}:SDA$	–	–	500	nS
Maximum Delay SDA1 to SDA2	$t_{PLZ}:SDA$	–	–	500	nS
Maximum Delay SCL1 to SDA1,2 (Direction Change DATA = L)	$t_{PHL}:SCL-SDA$	–	–	500	nS
Maximum Delay SCL1 to SDA1,2 (Direction Change DATA = H)	$t_{PLZ}:SCL-SDA$	–	–	500	nS
Maximum Delay Reset to SDA1,2	$t_{PLZ}:RES$	–	–	500	nS
Maximum Output Fall Time SCL	$t_{THL}:SCL$	5.0	–	20	nS
Maximum Output Rise Time SDA	$t_{THL}:SDA$	5.0	–	20	nS
Maximum Group Delay $t_{PHL}:SCL-t_{PHL}:SDA$	$t_{PHL}$	1.0	–	10	nS
Maximum Group Delay $t_{PLZ}:SCL-t_{PLZ}:SDA$	$t_{PLZ}$	1.0	–	10	nS
Power On Reset Pulse Width	$t_W:ROR$	1500	–	–	nS

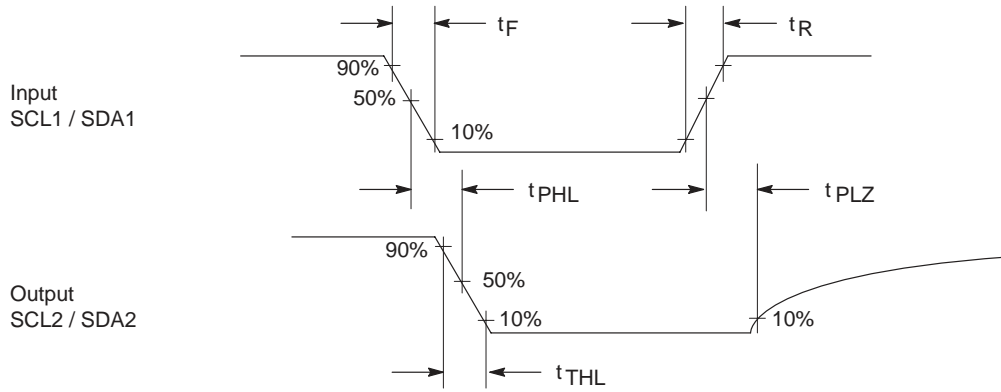
## TIMING CONDITIONS ( $V_{DD} = 5.0\text{ V}$ )

Parameter	Symbol	Nominal 25°C	Guaranteed Limits		Unit
			Min	Max	
Minimum Pulse Width Reset	$t_W:RES$	–	50	–	nS

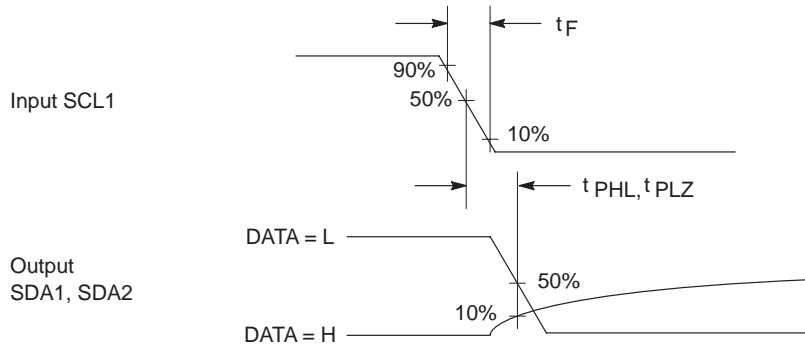


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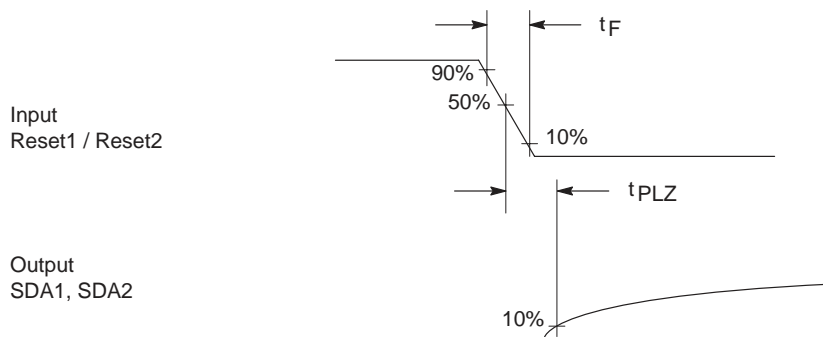
(1)  $t_{PHL:SCL}$ ,  $t_{PLZ:SCL}$ ,  $t_{PHL:SDA}$ ,  $t_{PLZ:SDA}$ ,  $t_{THL:SCL}$ ,  $t_{THL:SDA}$



(2)  $t_{PHL:SCL-SDA}$ ,  $t_{PLZ:SCL-SDA}$

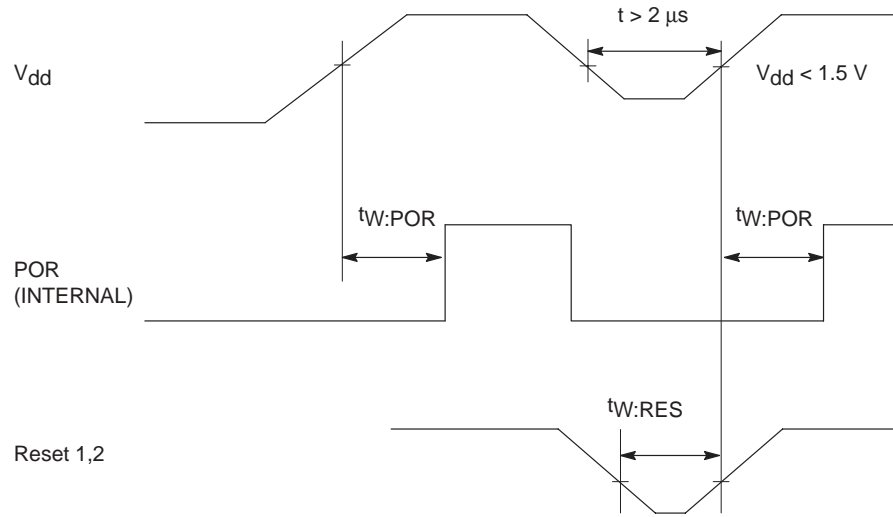


(3)  $t_{PLZ:RES}$

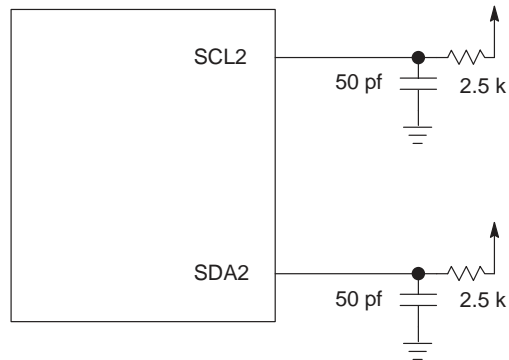


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(4)  $t_{W:POR}$ ,  $t_{W:RES}$



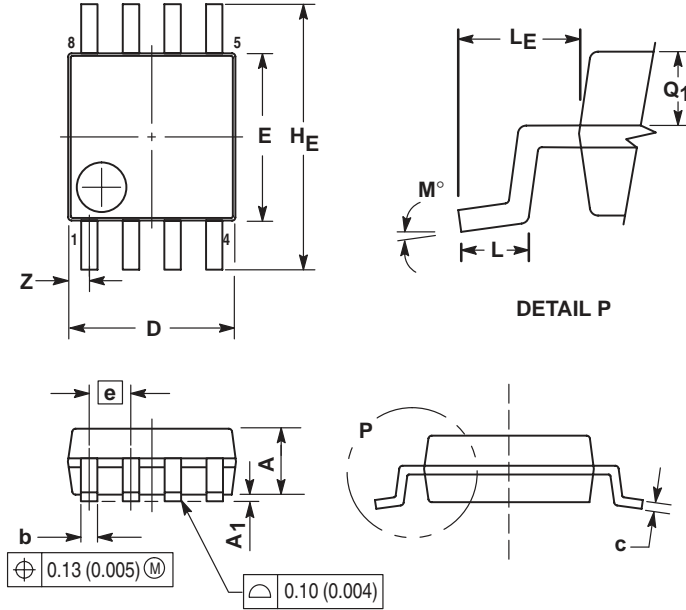
## TEST CIRCUIT



# JLC1563

## PACKAGE DIMENSIONS

### SOEIAJ-8 M SUFFIX CASE 968-01 ISSUE O

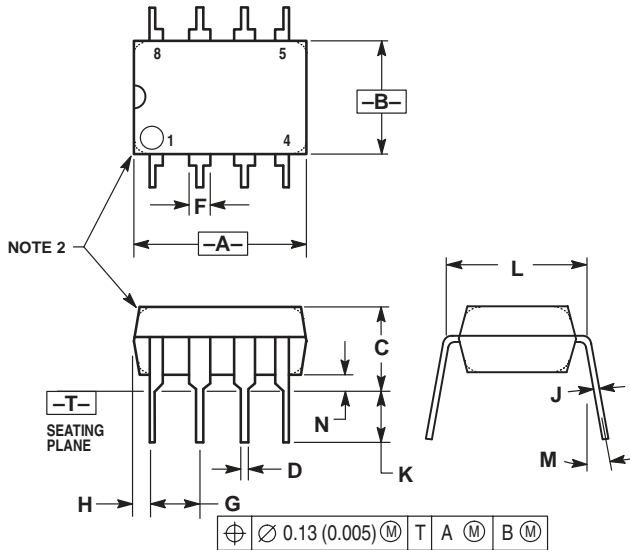


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSION D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	5.10	5.50	0.201	0.217
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q1	0.70	0.90	0.028	0.035
Z	—	0.94	—	0.037


### PDIP-8 P SUFFIX CASE 626-05 ISSUE K



NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

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