General Description

The MAX5980A is a quad, power-sourcing equipment (PSE) power controller designed for use in IEEE® 802.3at/af-compliant PSE. This device provides powered device (PD) discovery, classification, current limit, and load disconnect detection. The device supports both fully automatic operation and software programmability. The device also supports new 2-Event classification and Class 5 for detection and classification of high-power PDs. The device supports single-supply operation, provides up to 70W to each port (Class 5 enabled), and still provides high-capacitance detection for legacy PDs.

The device features an I2C-compatible, 3-wire serial interface, and is fully software configurable and programmable. The device provides instantaneous readout of port current and voltage through the I2C interface. The device's extensive programmability enhances system flexibility, enables field diagnosis, and allows for uses in other, nonstandard applications.

The device is available in a space-saving, 32-pin TQFN (5mm x 5mm) power package and is rated for the automotive (-40ºC to +105ºC) temperature range.

Applications

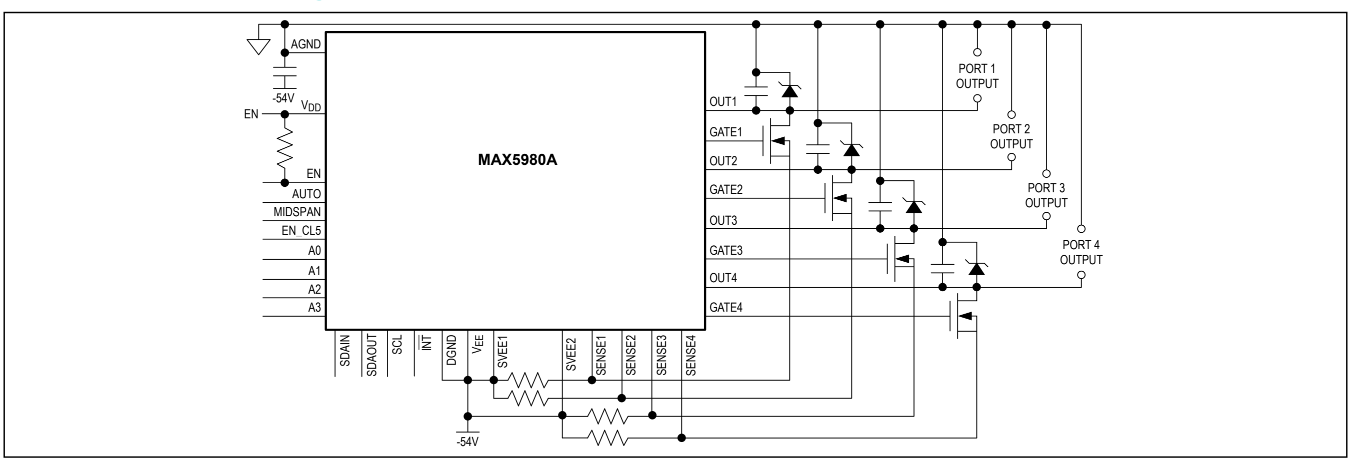
- PSE-ICM
- Power-Sourcing Equipment (PSE)
- Switches/Routers
- Midspan Power Injectors

Benefits and Features

- IEEE 802.3at/af Compliance Enables PD Discovery, Classification, Current Limit, and Load-Disconnect Detection
  - Provides Interoperability with Any Compliant PD
  - Two-Point Slope Measurement Verifies the Device Connected to the Port
  - Appropriate Settling Times Implemented to Reject 50Hz/60Hz Power-Line Noise Coupling
  - High Power Beyond IEEE 802.3at/af Standard Supported with Additional Classification (Class 5) when Needed
- IEEE Power-over-Ethernet (PoE) Transmission Facilitates Signaling Between Power-Sourcing Equipment (PSE) and Powered Devices (PDs)
  - Single-Supply Operation Provides Up to 70W per Port for PSE Applications, Allowing High-Capacitance Detection for Legacy PDs
  - 0.25Ω Current-Sensing Resistor Helps Eliminate Power Losses when Sensing High Currents
- Software-Configurable/Programmable Registers through I2C-Compatible, 3-Wire Serial Interface Produces Instantaneous Readout of Port Current and Voltage through 9-Bit Port Current and Voltage Monitoring
  - Supports DC Load-Removal Detection
- Saves Space with Thermally Efficient Power Package
  - Available in a 32-Pin (5mm x 5mm) TQFN with an Exposed Pad for Heat Dissipation

***Ordering Information* appears at end of data sheet.**

Simplified Operating Circuit



Absolute Maximum Ratings

(Voltages referenced to V_{EE}, unless otherwise noted.)
AGND ....-0.3V to +80V
DGND, SVEE_ ....-0.3V to +0.3V
V_{DD}........................ -0.3V to the lower (V_{AGND} + 0.3V) and +4V
OUT_ ....-0.3V to (V_{AGND} + 0.3V)
GATE_, SENSE_..-0.3V to +22V
A3, A2, A1, A0, MIDSPAN, EN_CL5, AUTO,
$\overline{\text{INT}}$, SCL, SDAIN, SDAOUT, EN to DGND ....-0.3V to +6V
Maximum Current into $\overline{\text{INT}}$ and OUT 20mA
Maximum Current into OUT_ ....Internally Regulated
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C)...2758.6mW
Operating Temperature Range......................... -40°C to +105°C
Storage Temperature Range .... -65°C to +150°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Package Thermal Characteristics

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....+29°C/W
Junction-to-Case Thermal Resistance (θ_{JC})...........+1.7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, and default register settings. Currents are positive when entering the pin, and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Voltage Range	V_{AGND}	V_{AGND} - V_{EE}	32		60	V
Supply Currents	I_{EE}	$V_{OUT\_}$ = $V_{SENSE\_}$ = V_{EE}; $\overline{\text{INT}}$, SDAOUT, and all logic inputs unconnected; V_{SCL} = V_{SDAIN} = V_{DD}; measured at AGND in power mode after GATE_ pullup		5	7	mA
GATE DRIVER AND CLAMPING						
GATE_ Pullup Current	I_{PU}	Power mode, gate drive on, $V_{GATE\_}$ = V_{EE}	-40	-50	-60	µA
GATE_ Pulldown Current	I_{PDW}	Port SHDN mode enabled; $V_{GATE\_}$ = V_{EE} + 10V		40		µA
Strong Pulldown Current	I_{PDS}	$V_{SENSE\_}$ = 500mV, $V_{GATE\_}$ = V_{EE} + 2V		25		mA
External Gate Drive	V_{GS}	$V_{GATE\_}$ - V_{EE}, power mode, gate-drive on	8.5	9.5	10.5	V
CURRENT LIMIT AND OVERCURRENT						
Current-Limit Clamp Voltage	V_{SU_LIM}	Maximum $V_{SENSE\_}$ allowed during current-limit conditions, $V_{OUT\_}$ = 0V (Note 3); $I_{LIM\_}$ register set to 80h, Class 0–3	101	106.25	111.5	mV
		$I_{LIM\_}$ register set to C0h, Class 4	200	212.5	225	
		$I_{LIM\_}$ register set to C0h, Class 5	405	430	455	

Electrical Characteristics (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, and default register settings. Currents are positive when entering the pin, and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Overcurrent Threshold after Startup	V_{CUT}	Overcurrent $V_{SENSE\_}$ threshold allowed for t ≤ t_{FAULT} after startup, $V_{OUT\_}$ = 0V	$I_{CUT\_}$ register set to 14h, Class 0 and 3	89	93.75	98.5	mV
			$I_{CUT\_}$ register set to 22h, Class 4	151	159	167	
			$I_{CUT\_}$ register set to 22h, Class 5	303	319	335	
Foldback Initial Voltage	V_{FLBK_ST}	V_{AGND} - $V_{OUT\_}$ above which the current-limit trip voltage starts folding back	I_{LIM} register set to 80h		32		V
			I_{LIM} register set to C0h		18		
Foldback Final Voltage	V_{FLBK_END}	V_{AGND} - $V_{OUT\_}$ above which the current limit reaches V_{TH_FB}			46		V
Minimum Foldback Current-Limit Threshold	V_{TH_FB}	$V_{OUT\_}$ = V_{AGND} = 60V			35		mV
SENSE_ Input Bias Current		$V_{SENSE\_}$ = V_{EE}				-2	µA
SUPPLY MONITORS							
V_{EE} Undervoltage Lockout	V_{EE_UVLO}	V_{AGND} - V_{EE}, V_{AGND} - V_{EE} increasing			29		V
V_{EE} Undervoltage Lockout Hysteresis	V_{EE_UVLOH}	Ports shut down if: V_{AGND} - V_{EE} < V_{EE_UVLO} - V_{EE_UVLOH}			3		V
V_{EE} Overvoltage Lockout	V_{EE_OV}	Ports shut down if: V_{AGND} - V_{EE} > V_{EE_OV}, V_{AGND} - V_{EE} increasing			62		V
V_{EE} Overvoltage-Lockout Hysteresis	V_{EE_OVH}				1		V
V_{EE} Undervoltage	V_{EE_UV}	V_{EE_UV} event bit sets if: V_{AGND} - V_{EE} < V_{EE_UV}, V_{AGND} - V_{EE} increasing			40		V
V_{DD} Output Voltage	V_{DD}	I_{DD} = 0 to 10mA		3.0	3.3	3.6	V
V_{DD} Undervoltage Lockout	V_{DD_UVLO}				2		V
Thermal-Shutdown Threshold	T_{SHD}	Port is shut down and device resets if the junction temperature exceeds this limit, temperature increasing (Note 4)			+140		°C
Thermal-Shutdown Hysteresis	T_{SHDH}	Temperature decreasing (Note 4)			20		°C
OUTPUT MONITOR							
OUT_ Input Current	I_{BOUT}	$V_{OUT\_}$ = V_{AGND}, during idle				2	µA
		V_{AGND} - V_{EE} = 48V, $V_{OUT\_}$ = V_{EE}, during power-on mode				-70	
Idle Pullup Resistance at OUT_	R_{DIS}	Detection and classification off, port shut down		0.7	1	1.25	MΩ
PGOOD High Threshold	PG_{TH}	$V_{OUT\_}$ - V_{EE}, OUT_ decreasing		1.5	2.0	2.5	V

Electrical Characteristics (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, and default register settings. Currents are positive when entering the pin, and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGOOD Hysteresis	PG_{HYS}			220		mV
PGOOD Low-to-High Glitch Filter	t_{PGOOD}	Time $V_{OUT\_}$ - V_{EE} has to exceed PGTH to set the PGOOD_ bit in register 10h	2		4	ms
LOAD DISCONNECT						
DC Load Disconnect Threshold	V_{DCTH}	Minimum $V_{SENSE\_}$ allowed before disconnect (DC disconnect active), $V_{OUT\_}$ = 0V	1.25	1.875	2.5	mV
Load Disconnect Time	t_{DISC}	Time from $V_{SENSE\_} < V_{DCTH}$ to gate shutdown (Note 5)	300		400	ms
DETECTION						
Detection Probe Voltage (First Phase)	V_{DPH1}	V_{AGND} - V_{DET} during the first detection phase	3.8	4	4.2	V
Detection Probe Voltage (Second Phase)	V_{DPH2}	V_{AGND} - V_{DET} during the second detection phase	8.8	9.1	9.4	V
Current-Limit Protection	I_{DLIM}	$V_{OUT\_}$ = V_{AGND}, current measured through OUT_ during detection	1.50		2	mA
Short-Circuit Threshold	V_{DCP}	If $V_{AGND} - V_{OUT\_} < V_{DCP}$ after the first detection phase, a short circuit to AGND is detected		1.5		V
Open-Circuit Threshold	I_{D_OPEN}	First point measurement current threshold for open condition		12.5		µA
Resistor Detection Window	R_{DOK}	(Note 5)	19		26.5	kΩ
Resistor Rejection Window	R_{DBAD}	Detection rejects lower values			15.2	kΩ
		Detection rejects higher values	32			
CLASSIFICATION						
Classification Probe Voltage	V_{CL}	V_{AGND} - $V_{OUT\_}$ during classification	15.5		20	V
Current-Limit Protection	I_{CL_LIM}	$V_{OUT\_}$ = V_{AGND}, current measured through OUT_	65	75	86	mA
Classification Event Timing	t_{CL_E}		14	18	22	ms
Mark Event Voltage	V_{MARK}	V_{AGND} - V_{DET} during mark event	8		9.6	V
Mark Event Current Limit	I_{MARK_LIM}	V_{DET} = V_{AGND}, during mark event measure current through DET	34	40	46	mA
Mark Event Timing	t_{MARK_E}		7	9	11	ms
Classification Current Thresholds	I_{CL}	Classification current thresholds between classes: Class 0, Class 1	5.5	6.5	7.5	mA
		Class 1, Class 2	13.0	14.5	16.0	
		Class 2, Class 3	21	23	25	
		Class 3, Class 4	31	33	35	
		Class 4 upper limit (Note 6)	45	48	51	

Electrical Characteristics (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, and default register settings. Currents are positive when entering the pin, and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS/OUTPUTS (Voltages Referenced to V_{EE})							
Digital Input Low	V_{IL}					0.8	V
Digital Input High	V_{IH}			2			V
Internal Input Pullup/Pulldown Resistor	R_{DIN}	Pullup (pulldown) resistor to V_{DD} (DGND) to set default level		25	50	75	kΩ
Open-Drain Output Low Voltage	V_{OL}	I_{SINK} = 10mA				0.4	V
Open-Drain Leakage	I_{OL}	Open-drain high impedance, $V_{OUT\_}$ = 3.3V				1	µA
SCL, SDAIN Input Leakage	I_{DL}	Input connected to the pull voltage				1	µA
Hardware Reset Pulse Width		Minimum low pulse duration on EN to lead to a hardware reset event		120			µs
TIMING							
Startup Time	t_{START}	Time during which a current limit set by V_{SU_LIM} is allowed, starts when the GATE_ is turned on		50	60	70	ms
Fault Time	t_{FAULT}	Time allowed for an overcurrent fault set by V_{FLT_LIM} after startup		50	60	70	ms
Current Limit	t_{LIM}	Time during after startup (Note 7)		50	60	70	ms
Port_ Turn-Off Time	t_{OFF}	Minimum delay between any port turn-off, does not apply in a reset case			0.1		ms
Detection Reset Time		Time allowed for the port voltage to reset before detection starts			80		ms
Detection Time	t_{DET}	Maximum time allowed before detection is completed				330	ms
Midspan Mode Detection Delay	t_{DMID}			2			s
Classification Time	t_{CLASS}	Time allowed for classification			19	25	ms
V_{EE_UVLO} Turn-On Delay	t_{DLY}	Time V_{AGND} must be above the V_{EE_UVLO} threshold before the device operates		2		4	ms
Restart Timer	$t_{RESTART}$	Time the device waits before turning on after an overcurrent fault, MIDSPAN disabled		0.8	0.96	1.1	s
Startup Sequence Delay	t_{SEQ}	Time between any port power-up in auto mode			0.5		s
ADC PERFORMANCE (Power-On Mode)							
Resolution					9		Bits
Offset Error		Voltage reading	T_A = -5°C to +85°C			2.5	LSB
			T_A = -40°C to +10°C			3	
		Current reading	T_A = -5°C to +85°C			2.5	
			T_A = -40°C to +105°C			3	

Electrical Characteristics (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, and default register settings. Currents are positive when entering the pin, and negative otherwise.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error		Gain error voltage	T_A = -5°C to +85°C	-0.5		+4	%
			T_A = -40°C to +10°C	-1		+4.5	
		Gain error current	T_A = -5°C to +85°C	-2		+2	
			T_A = -40°C to +105°C	-2.5		+2.5	
V_{EE} Voltage Accuracy		V_{AGND} - V_{EE} = 48V	T_A = -5°C to +85°C	-0.5		+4.5	%
			T_A = -40°C to +105°C	-0.5		+5	
Integral Nonlinearity	INL					1	LSB
Differential Nonlinearity	DNL					1	LSB
Current Reading Range		Classes 0–4			1		A
		Class 5			2		
Current LSB Step Size		Classes 0–4			1.956		mA
		Class 5			3.912		
Voltage Reading Range		All classes			95.6		V
Voltage LSB Step Size		All classes			187		mV
TIMING CHARACTERISTICS (3-Wire Fast Mode)							
Serial Clock Frequency	f_{SCL}			10		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}			1.3			µs
Hold Time for a START Condition	$t_{HD, STA}$			0.6			µs
Low Period of the SCL Clock	t_{LOW}			1.3			µs
High Period of the SCL Clock	t_{HIGH}			0.6			µs
Setup Time	$t_{SU, STA}$	START and STOP conditions		0.6			µs
Data Hold Time	$t_{HD, DAT}$	Receive		0			ns
		Transmit		100		300	
Data in Setup Time	$t_{SU, DAT}$			100			ns
Cumulative Clock Low Extend Time	t_{LOW_EXT}					25	ms
Fall Time of SDAOUT Transmitting	t_F	(Note 8)				250	ns
Setup Time for STOP Condition	$t_{SU, STO}$			0.6			µs
Pulse Width of Spike Suppressed	t_{SP}	(Note 8)			30		ns

Note 2: Production testing done at +25°C. Overtemperature limits are guaranteed by design and not production tested.

Note 3: The current-limit thresholds are programmed through the I^2C interface (see the *Register Map and Description* section and Table 41).

Note 4: Functional test is performed over thermal shutdown entering test mode.

Note 5: R_{DOK} = (V_{OUT2} - V_{OUT1})/(I_{OUT2} - I_{OUT1}). V_{OUT1}, V_{OUT2}, I_{OUT1}, and I_{OUT2} represent the voltage at OUT_ and the current into OUT_ during phase 1 and 2 of the detection, respectively.

Note 6: If Class 5 is enabled, this value is the classification current threshold from Class 4 to Class 5, and classification currents between 51mA and I_{CL_LIM} will be classified as Class 5.

Note 7: Default value. The fault timer can be reprogrammed through the I^2C interface (TLIM_[3:0]).

Note 8: Guaranteed by design. Not subject to production testing.

Typical Operating Characteristics

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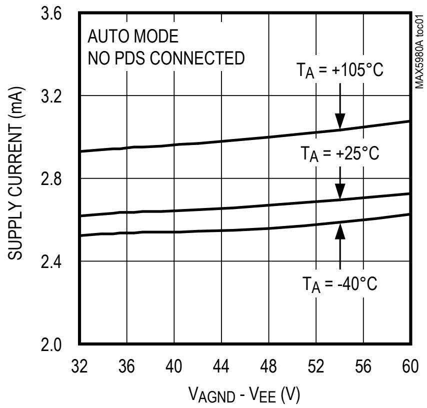
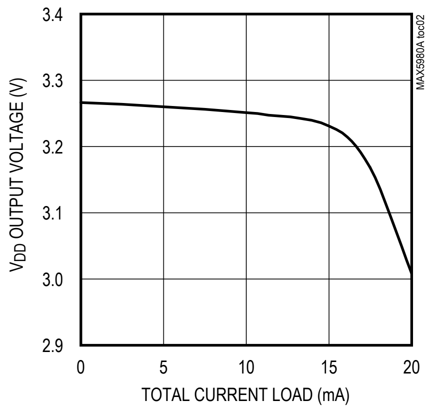
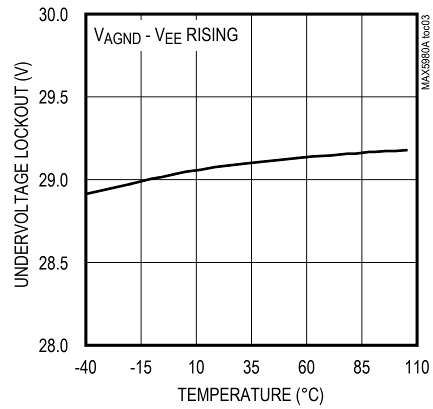
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



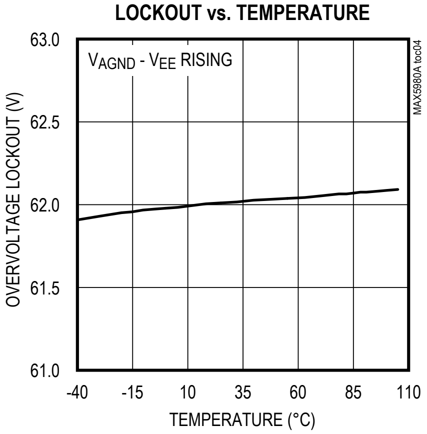
DIGITAL SUPPLY REGULATED VOLTAGE vs. LOAD CURRENT



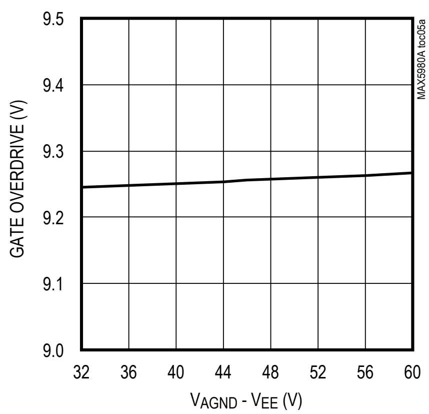
ANALOG SUPPLY UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



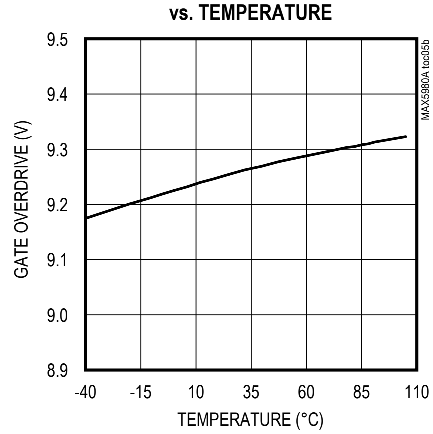
ANALOG SUPPLY OVERVOLTAGE LOCKOUT vs. TEMPERATURE



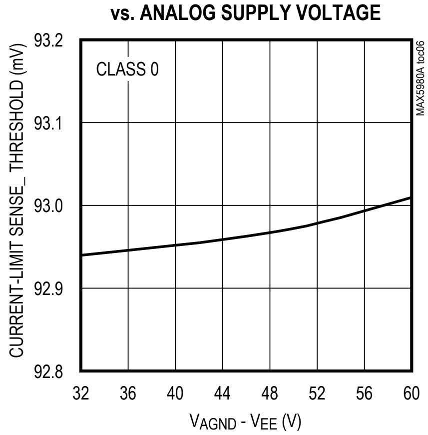
GATE OVERDRIVE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



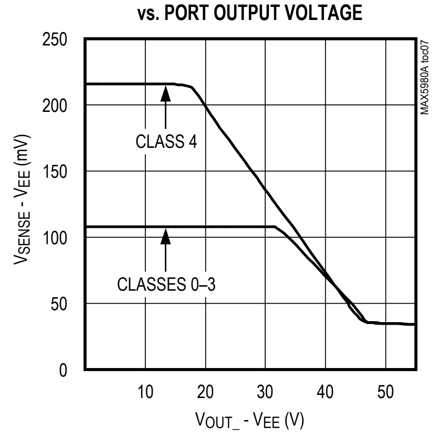
GATE OVERDRIVE VOLTAGE vs. TEMPERATURE



CURRENT-LIMIT SENSE_ THRESHOLD vs. ANALOG SUPPLY VOLTAGE



FOLDBACK CURRENT-LIMIT SENSE_ THRESHOLD vs. PORT OUTPUT VOLTAGE



Typical Operating Characteristics (continued)

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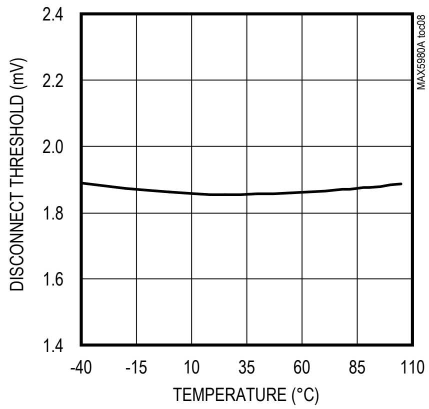
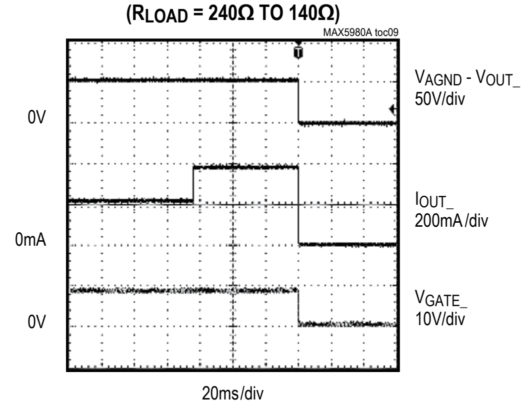
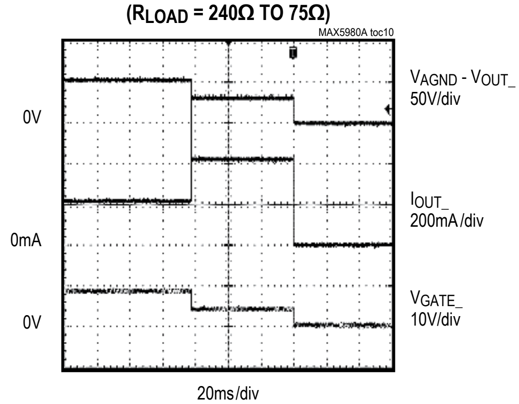
DC LOAD DISCONNECT SENSE_ THRESHOLD vs. TEMPERATURE



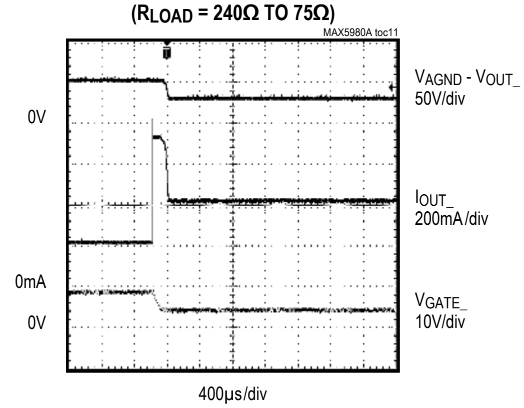
OVERCURRENT TIMEOUT (R_{LOAD} = 240Ω TO 140Ω)



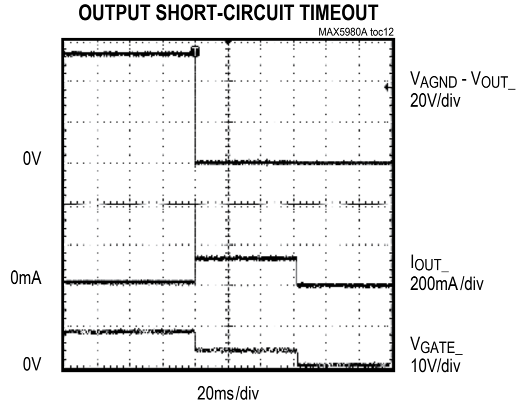
CURRENT-LIMIT TIMEOUT (R_{LOAD} = 240Ω TO 75Ω)



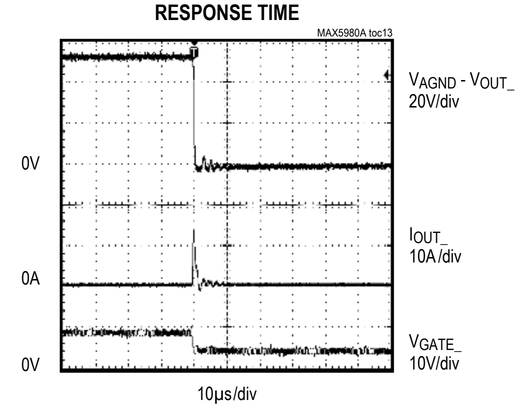
CURRENT-LIMIT TRANSIENT RESPONSE (R_{LOAD} = 240Ω TO 75Ω)



OUTPUT SHORT-CIRCUIT TIMEOUT



OUTPUT SHORT-CIRCUIT RESPONSE TIME



Typical Operating Characteristics (continued)

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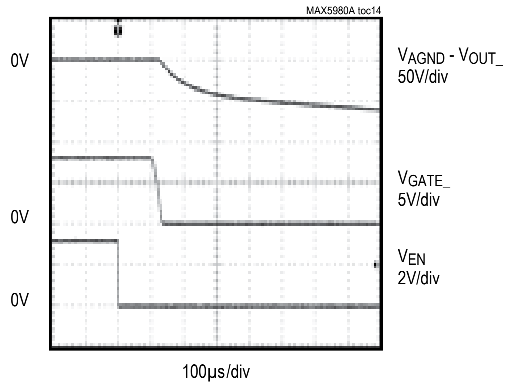
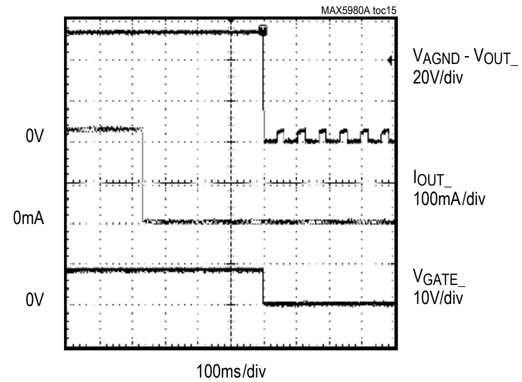
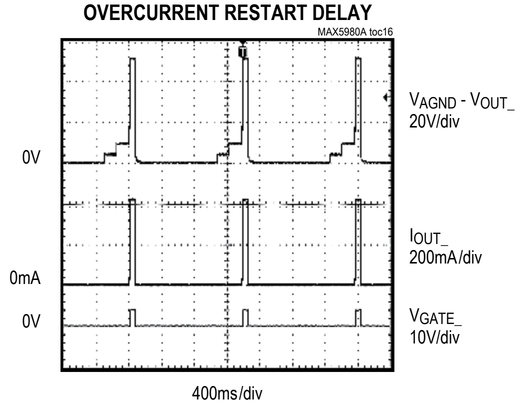
EN TO HARDWARE POWER-DOWN DELAY



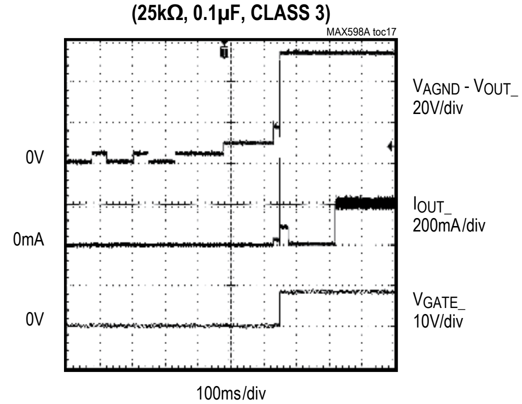
ZERO CURRENT DETECTION



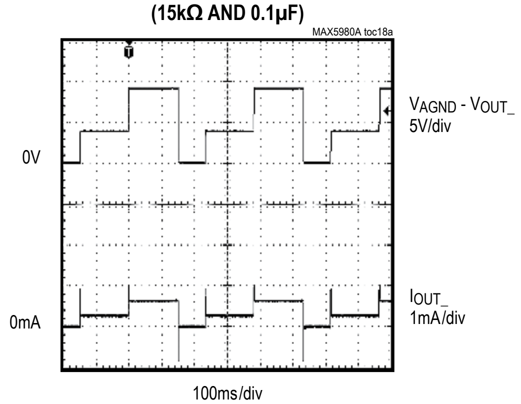
OVERCURRENT RESTART DELAY



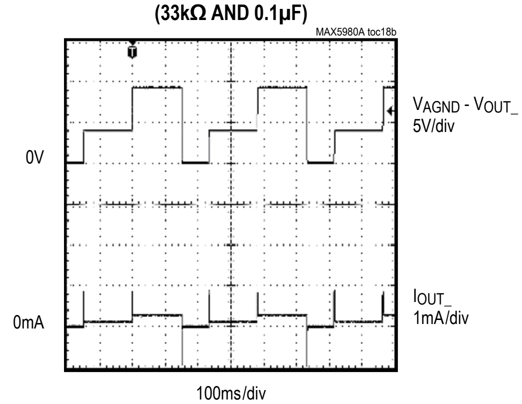
STARTUP WITH VALID PD (25kΩ, 0.1µF, CLASS 3)



DETECTION WITH INVALID PD (15kΩ AND 0.1µF)



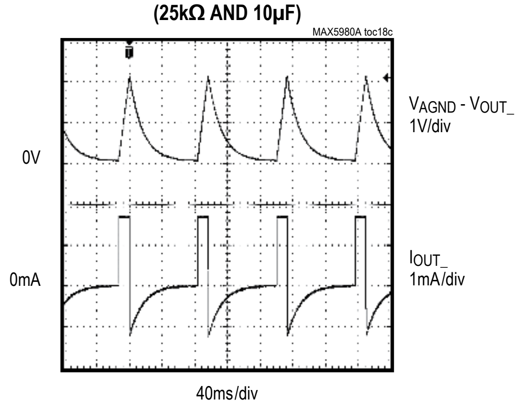
DETECTION WITH INVALID PD (33kΩ AND 0.1µF)



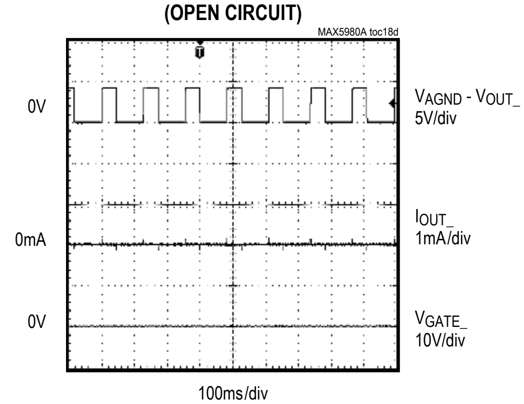
Typical Operating Characteristics (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, ENDPOINT mode, and default register settings with a Class 0 PD, unless otherwise noted.)

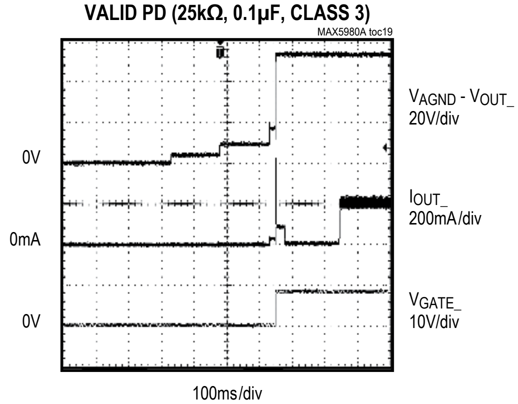
DETECTION WITH INVALID PD (25kΩ AND 10µF)



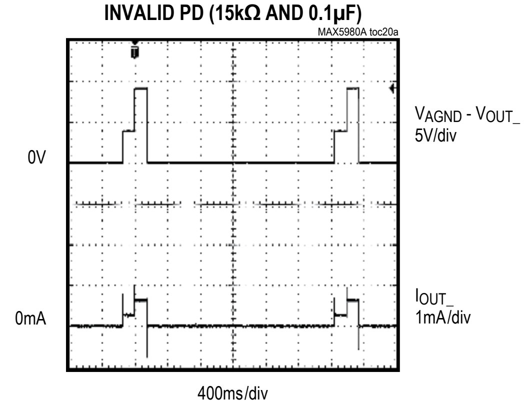
DETECTION WITH INVALID PD (OPEN CIRCUIT)



STARTUP IN MIDSPAN MODE WITH VALID PD (25kΩ, 0.1µF, CLASS 3)



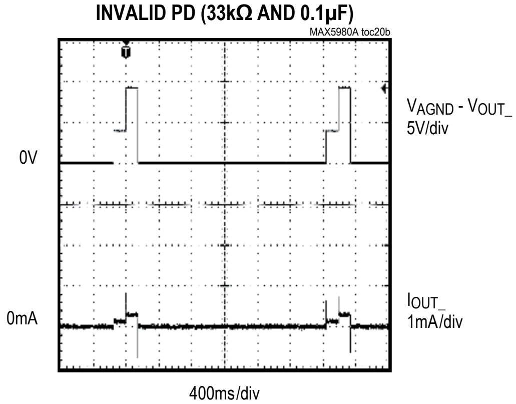
DETECTION IN MIDSPAN MODE WITH INVALID PD (15kΩ AND 0.1µF)



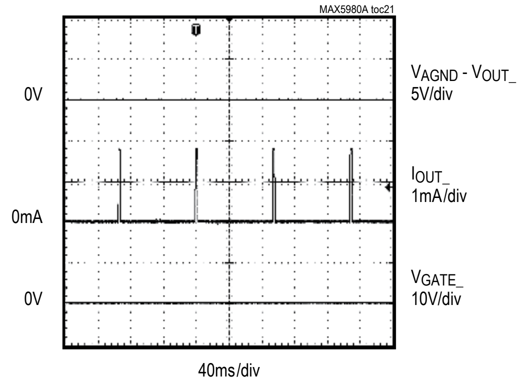
Typical Operating Characteristics (continued)

(V_{AGND} = 32V to 60V, V_{EE} = V_{DGND} = 0V, T_A = -40°C to +105°C. All voltages are referenced to V_{EE}, unless otherwise noted. Typical values are at V_{AGND} = 54V, T_A = +25°C, ENDPOINT mode, and default register settings with a Class 0 PD, unless otherwise noted.)

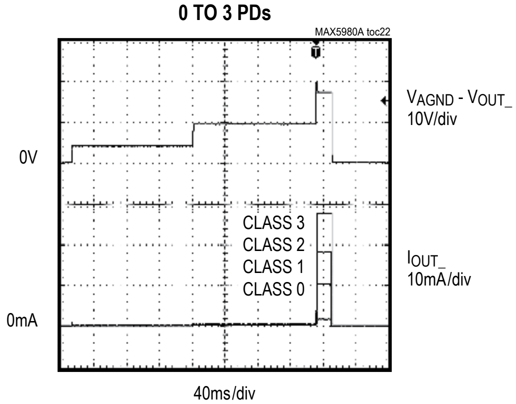
DETECTION IN MIDSPAN MODE WITH INVALID PD (33kΩ AND 0.1µF)



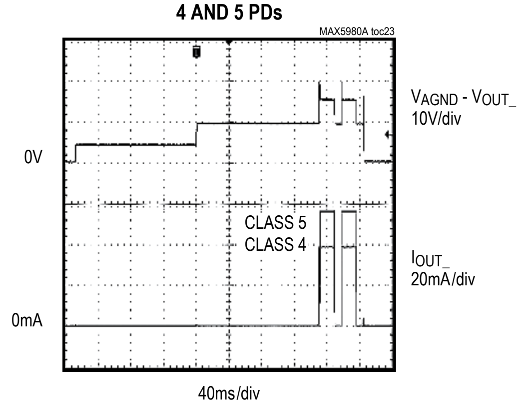
DETECTION WITH OUT_ SHORTED TO AGND



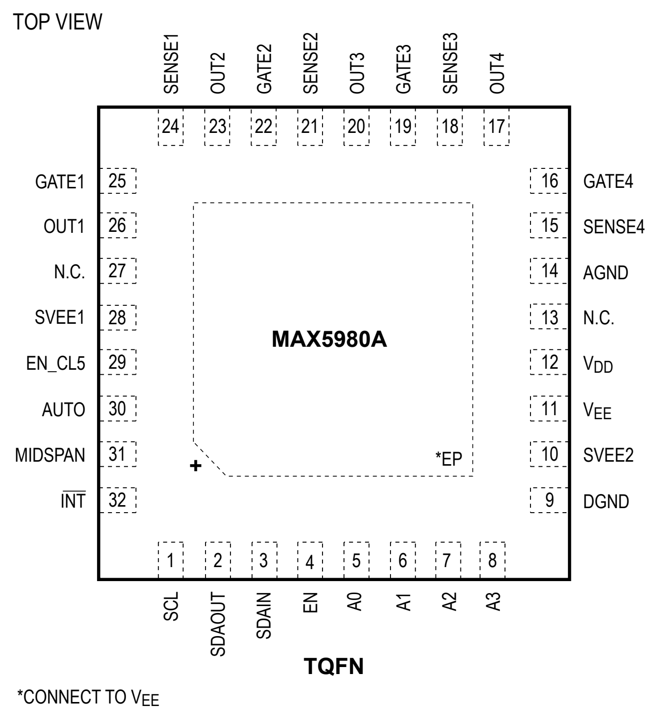
CLASSIFICATION WITH CLASS 0 TO 3 PDs



2-EVENT CLASSIFICATION WITH CLASS 4 AND 5 PDs



Pin Configuration



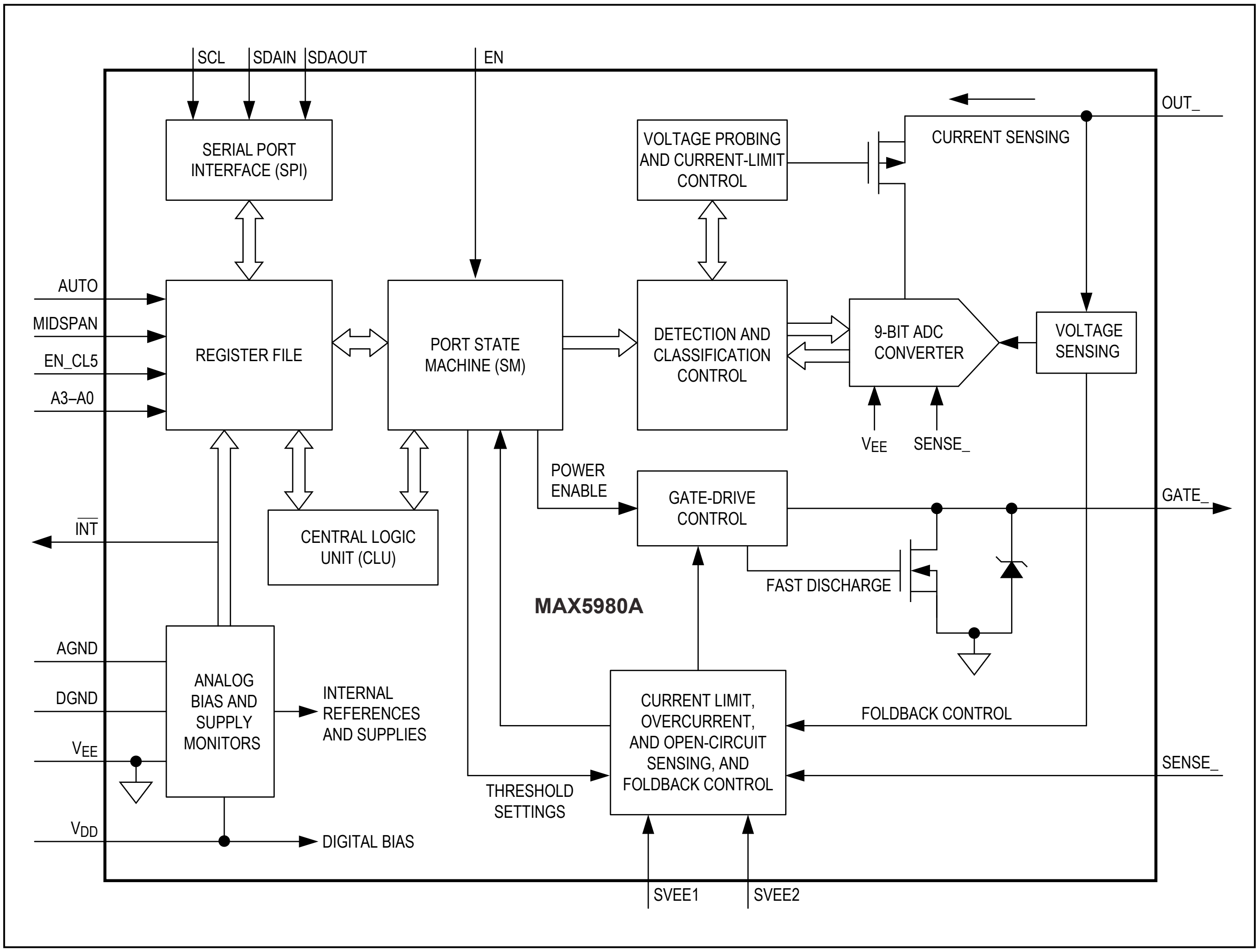
Pin Description

PIN	NAME	FUNCTION
1	SCL	3-Wire Serial Interface Input Clock Line. Referenced to DGND. Connect to DGND if the I^2C interface is not used. A 50Ω resistor is needed when push-pull I^2C driver is connected.
2	SDAOUT	Serial Interface Data Line Output. Referenced to DGND. Connect to DGND if the I^2C interface is not used.
3	SDAIN	Serial Interface Data Line Input. Referenced to DGND. Connect to DGND if the I^2C interface is not used. A 50Ω resistor is needed when push-pull I^2C driver is connected.
4	EN	EN Input. Referenced to DGND. Connect EN to V_{DD} externally through a pullup resistor to enable normal operation. See the *Hardware Power-Down* section for details.
5, 6, 7, 8	A0, A1, A2, A3	Slave Address Bits 0, 1, 2, 3 (Respectively). Referenced to DGND. The slave address bits are used to form bits 3, 2, 1, and 0 of the device address (0:1:0:A3:A2:A1:A0; see Table 3). The slave address bits are internally pulled up to V_{DD}. Leave them unconnected to use the default device address (0101111). Connect one or more to DGND to change the device address. The slave address is latched-in after the device is powered up or after a reset condition.
9	DGND	Digital Low-Side Supply Input. Connect to V_{EE} externally.
10	SVEE2	Port 3/4 Current-Sense Negative Terminal Input. Use Kelvin-sensing technique in PCB layout for best accuracy current sensing.

Pin Description (continued)

PIN	NAME	FUNCTION
11	V_{EE}	Analog Low-Side Supply Input. Bypass with an external 100V, 0.1µF ceramic capacitor between AGND and V_{EE}.
12	V_{DD}	Digital High-Side Supply Output. Bypass with an external RC network; see the *V_{DD} Power Supply* section for details.
13, 27	N.C.	No Connection. Not internally connected. Leave N.C. unconnected.
14	AGND	Analog High-Side Supply Input
15, 18, 21, 24	SENSE4, SENSE3, SENSE2, SENSE1	Current-Sense Positive Terminal Inputs. Connect to the source of the external power MOSFET and connect a 0.25Ω current-sense resistor between SENSE_ and SVEE_. Use Kelvin-sensing technique in PCB layout for best accuracy current sensing.
16, 19, 22, 25	GATE4, GATE3, GATE2, GATE1	Port_ MOSFET Gate Drivers. Connect GATE_ to the gate of the external power MOSFET (see the *Typical Operating Circuit*).
17, 20, 23, 26	OUT4, OUT3, OUT2, OUT1	Port Output Voltage Senses. Connect OUT_ to the port output through a 20Ω resistor.
28	SVEE1	Port 1/2 Current-Sense Negative Terminal Input. Use Kelvin sensing technique in PCB layout for best accuracy current sensing.
29	EN_CL5	Class 5 Enable Input. Referenced to DGND. EN_CL5 is internally pulled down to DGND. Leave unconnected to disable the classification for Class 5 devices (IEEE 802.3at-compliant mode). Connect EN_CL5 to V_{DD} to enable the classification of Class 5 devices. EN_CL5 is latched in after the device is powered up or after a reset condition.
30	AUTO	Auto/Shutdown Mode Input. Referenced to DGND. AUTO is internally pulled up to V_{DD}. Leave unconnected to put the device into auto mode by default. Connect AUTO to DGND instead to set the default mode to shutdown. In either configuration, the software can change the operating mode of the device. AUTO is latched in after the device is powered up or after a reset condition.
31	MIDSPAN	Detection Collision Avoidance Logic Input. Referenced to DGND. MIDSPAN is internally pulled up to V_{DD}. Leave unconnected to activate midspan mode, or connect to DGND to disable this function. MIDSPAN is latched in after the device is powered up or after a reset condition.
32	$\overline{INT}$	Open-Drain Interrupt Output. Referenced to DGND. $\overline{INT}$ is pulled low whenever an interrupt is sent to the microcontroller. See the *Interrupt* section for details. Connect to DGND if the I^2C interface is not used.
—	EP	Exposed Pad. EP is internally connected to V_{EE}. Connect EP to V_{EE} externally.

Functional Diagram



Detailed Description

The MAX5980A is a quad PSE power controller designed for use in IEEE 802.3at/af-compliant PSE. This device provides PD discovery, classification, current limit, and load disconnect detections. The device supports both fully automatic operation and software programmability. The device also supports new 2-Event classification and Class 5 for detection and classification of high-power PDs. The device supports single-supply operation, provides up to 70W to each port (Class 5 enabled), and still provides high-capacitance detection for legacy PDs.

The device features an I^2C-compatible, 3-wire serial interface, and is fully software configurable and programmable. The device provides instantaneous readout of port current and voltage through the I^2C interface. The device provides input undervoltage lockout (UVLO), input overvoltage lockout (OVLO), overtemperature protection, and output voltage slew-rate limit during startup.

Reset

The device is reset by any of the following conditions:

1) Power-up/down. Reset condition is asserted once V_{EE} falls below the UVLO threshold.
2) Hardware reset. To initiate a hardware reset, pull EN low to DGND for at least 100µs. Hardware reset clears once, EN returns high to V_{DD}, and all registers are set to their default states.
3) Software reset. To initiate a software reset, write a logical 1 to the RESET_IC register (R1Ah[4]) any time after power-up. Reset clears automatically, and all registers are set to their default states.
4) Thermal shutdown. The device enters thermal shutdown at +140°C. The device exits thermal shutdown and is reset once the temperature drops below 120°C.

During normal operation, changes to the address inputs, MIDSPAN, EN_CL5, and AUTO are ignored, and they can be changed at any time prior to a reset state. At the end of a reset event, the device latches in the state of these inputs.

Port Reset

Set RESET_P_ (R1Ah[3:0]) high anytime during normal powered operation to turn off port_, disable detection and classification, and clear the Port_ Event and Status registers. If a port is not powered, setting RESET_P_ high for that port has no effect. Individual port reset does not initiate a global device reset.

Midspan Mode

In midspan mode, the device adopts cadence timing during the detection phase. When cadence timing is enabled and a failed detection occurs, the ports wait at least 2s before attempting to detect again. Midspan mode is activated by setting MIDSPAN high and then powering or resetting the device. Alternatively, midspan mode can be software programmed individually for each port by setting MIDSPAN_ (R15h[3:0], Table 23) to a logical 1. By default, the MIDSPAN input is internally pulled high, enabling cadence timing. Force MIDSPAN low to disable this function.

Operation Modes

The device provides four operating modes to suit different system requirements. By default, auto mode allows the device to operate automatically at its default settings without any software. Semiautomatic mode automatically detects and classifies devices connected to the ports, but does not power a port until instructed to by software. Manual mode allows total software control of the device and is useful for system diagnostics. Shutdown mode terminates all activities and securely turns off power to the ports.

Switching between auto, semiautomatic, and manual mode does not interfere with the operation of an output port. When a port is set into shutdown mode, all port operations are immediately stopped and the port remains idle until shutdown mode is exited.

Auto (Automatic) Mode

By default, when the auto input is unconnected, the device enters auto mode after power-up or when the reset condition is cleared. To manually place a port into auto mode from any other mode, set the corresponding port mode bits (R12h[7:0]) to [11] (Table 19).

In auto mode, the device performs detection, classification, and powers up the port automatically if a valid PD is connected to the port. If a valid PD is not connected at the port, the device repeats the detection routine continuously until a valid PD is connected.

When entering auto mode after a reset condition (state of AUTO input), the DET_EN_ and CLASS_EN_ bits (R14h[7:0], Table 22) are set to high and stay high, unless changed by software. When entering auto mode from any other mode due to a software command (programmed with R12h[7:0], Table 19, the DET_EN_ and CLASS_EN_ bits retain their previous state.

Semiautomatic (Semi) Mode

Enter semiautomatic mode by setting the port operating mode (R12h, Table 19) to [10]. When entering semi mode, the DET_EN_ and CLASS_EN_ bits retain their previous states. When the DET_EN_ and/or CLASS_EN_ bits are set to 1, the MAX5980A performs detection and/or classification repeatedly, but do not power up the port(s) automatically.

Setting R19h[3:0] (PWR_ON_, Table 26) high turns on power to the port(s) if detection and classification has successfully completed. If a port is powered down while in semiautomatic mode, the corresponding DET_EN_ and CLASS_EN_ bits are reset to 0.

Manual Mode

Enter manual mode by setting the port operating mode (R12h, Table 19) to [01]. Manual mode allows the software to dictate any sequence of operation. In manual mode, the Detection/Classification register (R14h, Table 22) is set to 00h, and DET_EN_/CLASS_EN_ become pushbutton bits. A port will only perform a single detection/classification cycle when DET_EN_/CLASS_EN_ are set high, and they are reset low after execution.

PWR_ON_ (R19h[3:0], Table 26) has the highest priority, and setting PWR_ON_ high at any time causes the device to immediately enter the powered mode. Setting DET_EN_ and CLASS_EN_ high at the same time causes detection to be performed first. Once in the powered state, the device ignores DET_EN_ and CLASS_EN_ commands.

Shutdown Mode

To put a port into shutdown mode, set the corresponding port mode bits (R12h, Table 19) to [00]. Putting a port into shutdown mode immediately turns off port power, clears the event and status bits, and halts all port operations. In shutdown mode the serial interface is still fully active; however, all DET_EN_, CLASS_EN_, and PWR_ON_ commands are ignored.

PD Detection

During normal operation, the device probes the output for a valid PD. A valid PD has a 25kΩ discovery signature characteristic as specified in the IEEE 802.3at/af standard. Table 1 shows the IEEE 802.3at specification for a PSE detecting a valid PD signature.

After each detection cycle, the device sets DET_ (R04h[3:0] and R05h[3:0], Table 9) to 1 and reports the detection results in the detection status bits (see Table 13). The DET_ bits are reset to 0 when read through the CoR (clear on read) register (R05h), or after a reset event.

During detection, the device keeps the external MOSFET off and forces two probe voltages through OUT_. The current through OUT_ is measured, as well as the voltage difference from AGND to OUT_. A two-point slope measurement is used, as specified by the IEEE 802.3at/af standard, to verify the device connected to the port. The device implements appropriate settling times to reject 50Hz/60Hz power-line noise coupling.

Table 1. PSE PI Detection Modes Electrical Requirements (IEEE 802.3at)

PARAMETER	SYMBOL	MIN	MAX	UNITS	ADDITIONAL INFORMATION
Open-Circuit Voltage	V_{OC}	—	30	V	In detection mode only
Short-Circuit Current	I_{SC}	—	5	mA	In detection mode only
Valid Test Voltage	V_{VALID}	2.8	10	V	—
Voltage Difference Between Test Points	ΔV_{TEST}	1	—	V	—
Time Between Any Two Test Points	t_{BP}	2	—	ms	This timing implies a 500Hz maximum probing frequency
Slew Rate	V_{SLEW}	—	0.1	V/µs	—
Accept Signature Resistance	R_{GOOD}	19	26.5	kΩ	—
Reject Signature Resistance	R_{BAD}	< 15	> 33	kΩ	—
Open-Circuit Resistance	R_{OPEN}	500	—	kΩ	—
Accept Signature Capacitance	C_{GOOD}	—	150	nF	—
Reject Signature Capacitance	C_{BAD}	10	—	µF	—
Signature Offset Voltage Tolerance	V_{OS}	0	2.0	V	—
Signature Offset Current Tolerance	I_{OS}	0	12	µA	—

To prevent damage to non-PD devices, and to protect itself from an output short circuit, the device limits the current into OUT_ to less than 2mA (max) during PD detection. In midspan mode, after every failed detection cycle, the device waits at least 2.0s before attempting another detection cycle.

High-Capacitance Detection

High-capacitance detection for legacy PDs is software programmable. To use the software to enable high-capacitance detection, set LEG_EN_ (Port GPMD registers, Table 39) to 1 during normal operation. If high-capacitance detection is enabled, PD signature capacitances up to 100μF (typ) are accepted.

Power Device Classification (PD Classification)

During PD classification, the device forces a probe voltage between 15V and 20V at OUT_ and measures the current into OUT_. The measured current determines the class of the PD.

After each classification cycle, the device sets CLS_ (R04h[7:4] and R05h[7:4], Table 9) to 1 and reports the classification results in the classification status bits (see Table 13). The CLS_ bits are reset to 0 when read through the CoR (clear on read) register (R05h) or after a reset event.

If EN_CL5 is left unconnected, the device will classify the PD based on Table 33-9 of the IEEE 802.3at standard (see Table 2). If the measured current exceeds 51mA, the device will not power the PD, but will report an overcurrent classification result and will return to IDLE state before attempting a new detection cycle.

Class 5 PD Classification

The device supports high power beyond the IEEE 802.3at standard by providing an additional classification (Class 5) if needed. To enable Class 5, connect EN_CL5 to V_{DD} and initiate a global reset or use the software to individually enable Class 5 classification for each port (R1Ch[3:0], Table 29). Once Class 5 is enabled, during classification, if the device detects currents in excess of the Class 4 upper-limit threshold, the PD will be classified as a Class 5 powered device. The PD is guaranteed to be classified as a Class 5 device for any classification current from 51mA up to the classification current-limit threshold. The Class 5 overcurrent threshold and current limit will be set automatically with ICUT_[5:0] and ILIM_ (see Tables 40 and 41). Leave EN_CL5 unconnected to disable Class 5 detection and to be fully compliant to IEEE 802.3at standard classification.

Table 2. PSE Classification of a PD (Table 33-9 of the IEEE 802.3at Standard)

MEASURED I_{CLASS} (mA)	CLASSIFICATION
0 to 5	Class 0
> 5 and < 8	May be Class 0 or 1
8 to 13	Class 1
> 13 and < 16	Either Class 1 or 2
16 to 21	Class 2
> 21 and < 25	Either Class 2 or 3
25 to 31	Class 3
> 31 and < 35	Either Class 3 or 4
35 to 45	Class 4
> 45 and < 51	Either Class 4 or Invalid

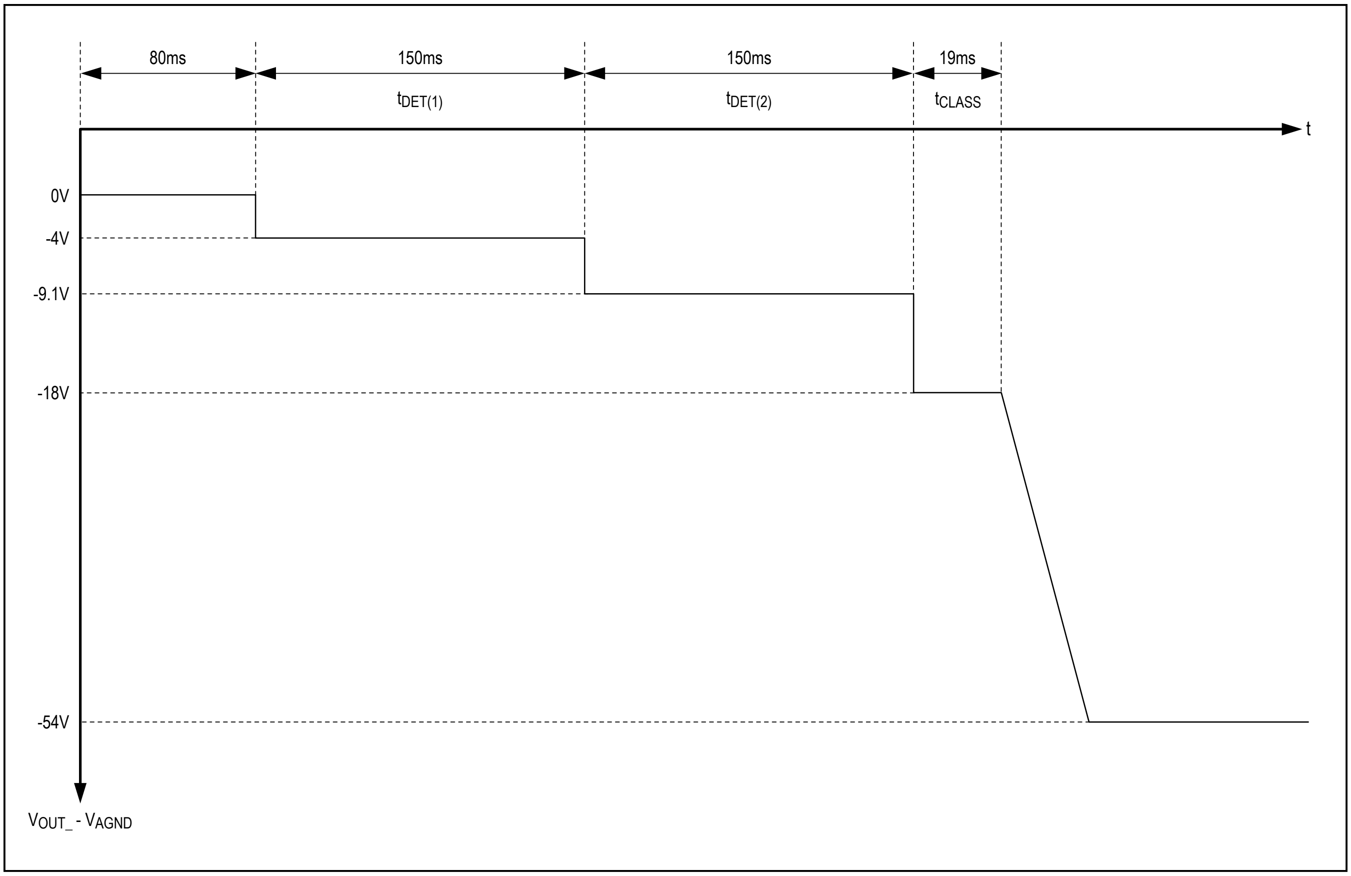


Figure 1. Detection, Classification, and Port Power-Up Sequence

2-Event PD Classification

If the result of the first classification event is Class 0 to 3, then only a single classification event occurs as shown in Figure 1. However, if the result is Class 4 (or Class 5), the device will perform a second classification event as shown in Figure 2. Between the classification cycles, the device performs a first and second mark event as required by the IEEE 802.3at standard, forcing a -9.3V probing voltage at OUT_.

Powered State

When the device enters a powered state, the t_{FAULT} timer is reset and power is delivered to the PD. PGOOD_ (R10h[7:4], Table 16) is set to 1 when the device enters the normal power condition. PGOOD_ immediately resets to 0 whenever the power to the port is turned off. The power-good change bits, PG_CHG_ (R02h[3:0], Table 8) are set both when the port powers up and when it powers down.

Overcurrent Protection

A sense resistor, $R_{SENSE\_}$, connected between SENSE_ and SVEE_ monitors the load current. Under normal operating conditions, the voltage across $R_{SENSE\_}$ ($V_{RSENSE\_}$) never exceeds the current-limit threshold, V_{SU_LIM}. If $V_{RSENSE\_}$ exceeds V_{SU_LIM}, an internal current-limiting circuit regulates the GATE_ voltage, limiting the current to $I_{LIM} = V_{SU\_LIM}/R_{SENSE\_}$. During transient conditions, if $V_{RSENSE\_}$ exceeds V_{SU_LIM} by more than 500mV, a fast pulldown circuit activates to quickly recover from the current overshoot. During startup, if the current-limit condition persists, when the startup timer, t_{START}, times out, the port shuts off, and the TSTART_ bit is set (R08h[3:0] and R09h[3:0], Table 11).

In the normal powered state, the device checks for overcurrent conditions as determined by V_{CUT}. The t_{FAULT} counter sets the maximum allowed continuous overcurrent period. The t_{FAULT} counter increases when

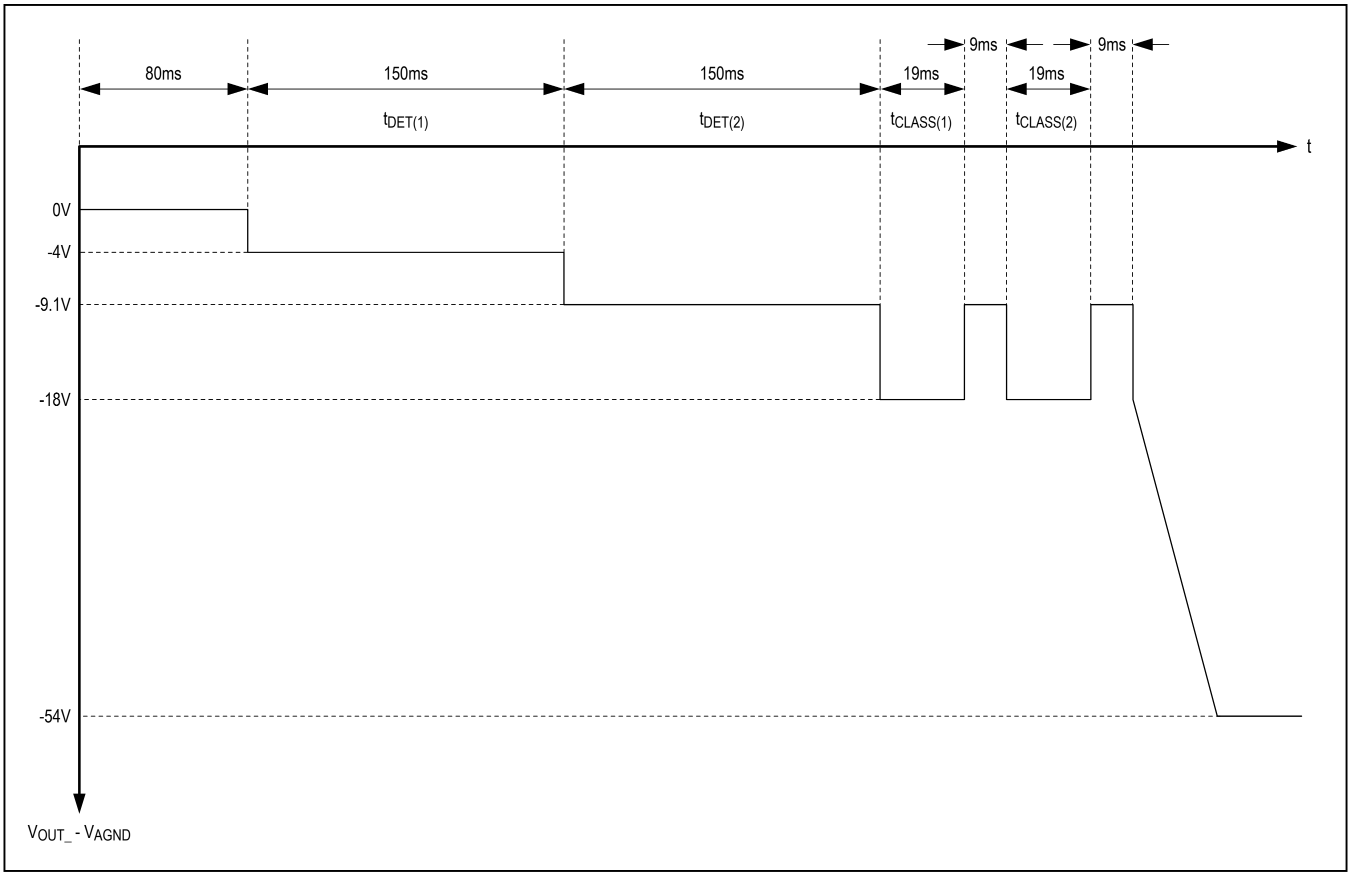


Figure 2. Detection, 2-Event Classification, and Port Power-Up Sequence

$V_{RSENSE\_}$ exceeds V_{CUT} and decreases at a slower pace when $V_{RSENSE\_}$ drops below V_{CUT}. A slower decrement for the t_{FAULT} counter allows for detecting repeated short-duration overcurrent conditions. When the counter reaches the t_{FAULT} limit, the device powers the port down and asserts the corresponding TCUT_ bit (R06h[3:0] and R07h[3:0], Table 10). For a continuous overstress, a fault latches exactly after a period of t_{FAULT}. V_{CUT} is programmable through the ICUT_ registers (Table 40). If a port is powered down due to a current-limit condition, during normal operation, the device asserts the corresponding ICV_ bit (R08h[7:4] and R09h[7:4], Table 11)

After power-off due to an overcurrent fault, the t_{FAULT} timer is not immediately reset but starts decrementing at the same slower pace. The device allows a port to be powered on only when the t_{FAULT} counter is at zero. This feature sets an automatic duty-cycle protection to the external MOSFET to avoid overheating.

High-Power Mode

The device features individual, port programmable high-power settings. To enable the high-power configuration for a port, set the corresponding HP_EN_ bit (R44h[3:0], Table 38) to 1. By default, if AUTO = 1, the HP_EN_ bits will be set to 1 automatically after a reset event. When enabled, each port's high-power settings can be individually configured using the corresponding Port GPMD, Port Overcurrent (ICUT), Port Current-Limit (ILIM_), and Port High-Power Status registers (see the *Register Map and Description* section, Tables 39–42).

Foldback Current

During startup and normal operation, an internal circuit senses the voltage at OUT_ and when necessary reduces the current-limit clamp voltage (V_{SU_LIM}) to help reduce the power dissipation through the external FET. When $I_{LIM\_}$ = 80h (Classes 0–3), foldback begins when $V_{OUT\_} - V_{EE}$ > 32V; and when $I_{LIM\_}$ = C0h (Classes 4

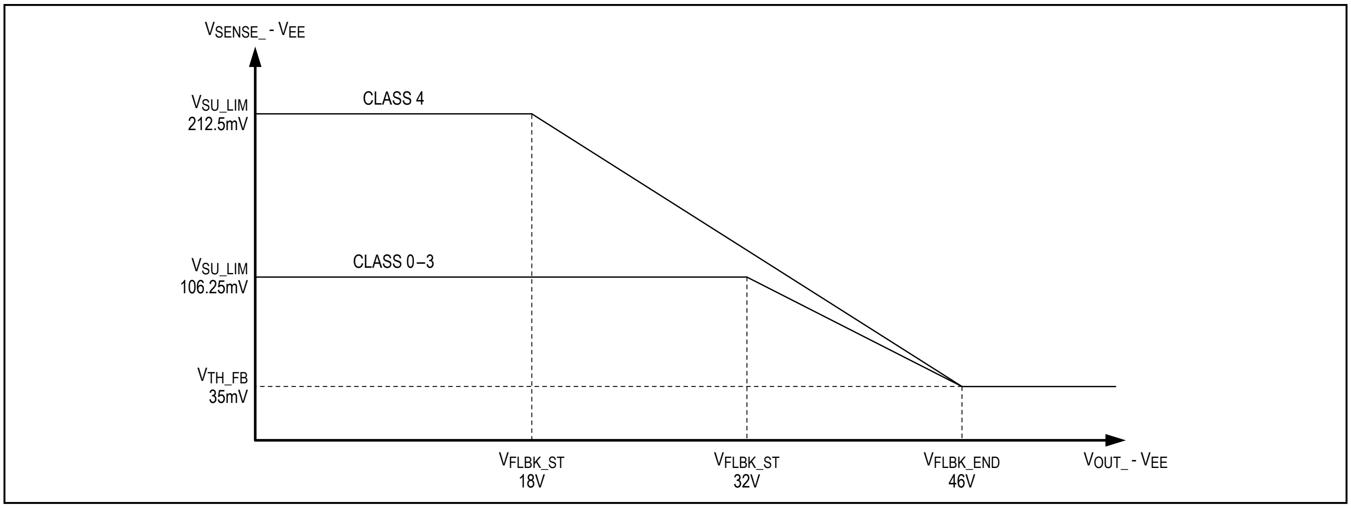


Figure 3. Foldback Current Characteristics

and 5), foldback begins when $V_{OUT\_}$ - V_{EE} > 18V. The V_{SU_LIM} eventually reduces down to the minimum current-limit threshold (V_{TH_FB} = 35mV) when $V_{OUT\_}$ - V_{EE} > 46V (Figure 3).

MOSFET Gate Driver

Connect the gate of the external n-channel MOSFET to GATE_. An internal 50µA current source pulls GATE_ to (V_{EE} + 10V) to turn on the MOSFET. An internal 40µA current source pulls down GATE_ to V_{EE} to turn off the MOSFET.

The pullup and pulldown current controls the maximum slew rate at the output during turn-on or turn-off. Use the following equation to set the maximum slew rate:

$$\frac{\Delta V_{OUT\_}}{\Delta t} = \frac{I_{GATE\_}}{C_{GD}}$$

where C_{GD} is the total capacitance between the gate and the drain of the external MOSFET. The current limit and the capacitive load at the drain control the slew rate during startup. During current-limit regulation, the device manipulates the GATE_ voltage to control the voltage at SENSE_ ($V_{RSENSE\_}$). A fast pulldown activates if $V_{RSENSE\_}$ overshoots the limit threshold (V_{SU_LIM}). The fast pulldown current increases with the amount of overshoot, and the maximum fast pulldown current is 50mA.

During turn-off, when the GATE_ voltage reaches a value lower than 1.2V, a strong pulldown switch is activated to keep the MOSFET securely off.

Interrupt

The device contains an open-drain logic output ($\overline{INT}$) that goes low when an interrupt condition exists. The Interrupt register (R00h, Table 6) contains the interrupt flag bits and the Interrupt Mask register (R01h, Table 7) determines which events can trigger an interrupt. When an event occurs, the appropriate Interrupt Event register bits (in R02h to R0Bh) and the corresponding interrupt (in R00h) are set to 1 and $\overline{INT}$ is asserted low (unless masked). If the master device on the I^2C bus sends out an Alert Response Address, any MAX5980A device on the bus that has $\overline{INT}$ asserted will respond (see the *Global Addressing and the Alert Response Address (ARA)* section).

As a response to an interrupt, the controller can read the status of the event register(s) to determine the cause of the interrupt and take appropriate action. Each interrupt event register is paired with a Clear-on-Read (CoR) register. When an interrupt event register is read through the corresponding CoR register, the corresponding event register is reset to 0 (clearing that interrupt event). $\overline{INT}$ remains low and the interrupt is not reset when the Interrupt Event register is read through the read-only address. For example, to clear a supply event fault read R0Bh (CoR) not R0Ah (read-only, see Table 12). Use the INT_CLR bit (R1Ah[7], Table 27) to clear an interrupt, or the RESET_IC bit (R1Ah[4]) to initiate software resets.

Undervoltage and Overvoltage Protection

The device contains undervoltage and overvoltage protection features, and the flag bits can be found in the Supply Event register (R0Ah and R0Bh, Table 12) and the Watchdog register (R42h, Table 36). An internal V_{EE} undervoltage lockout circuit keeps the MOSFET off and the device in reset until V_{AGND} - V_{EE} exceeds 28.5V for more than 3ms. An internal V_{EE} overvoltage circuit shuts down the ports when V_{AGND} - V_{EE} exceeds 62.5V. The digital supply also contains an undervoltage lockout that triggers when V_{DD} - V_{EE} ≤ 2V.

DC Disconnect Monitoring

The DC disconnect monitoring settings are found in the Disconnect Enable register (R13h, Table 21). To enable DC disconnect, set either the ACD_EN_ or DCD_EN_ bit for the corresponding port to 1. To disable the DC disconnect monitoring, both the ACD_EN_ and DCD_EN_ bit for that port must be set to 0. When enabled, if $V_{RSENSE\_}$ (the voltage across $R_{SENSE\_}$) falls below the DC load disconnect threshold, V_{DCTH}, for more than t_{DISC}, the device turns off power and asserts the DIS_ bit for the corresponding port (R06h[7:4] and R07h[7:4], Table 10).

V_{DD} Power Supply

The device has an internally regulated, 3.3V digital supply that powers the internal logic circuitry. V_{DD} has an undervoltage lockout (V_{DD_UVLO}) of 2V, and an undervoltage condition on V_{DD} keeps the device in reset and the ports shut off. When V_{DD} has recovered and the reset condition clears, the VDD_UVLO bit in the Supply Event registers is set to 1 (R0Ah[5] and R0Bh[5], Table 12). The digital address inputs, AUTO, and MIDSPAN are internally pulled up to V_{DD}, and all digital inputs are referenced to DGND. V_{DD} can also be used to source up to 10mA for external circuitry. For internal regulator stability, connect a 1.8kΩ resistor in parallel with a 33nF capacitor at the V_{DD} output (Figure 4). If an external load is to be shared among multiple MAX5980A devices, isolate the external supply bus with a series resistor (50Ω for 3 devices, 75Ω for 4 devices), and place a single 1µF capacitor on the bus.

Hardware Power-Down

The EN digital input is referenced to DGND and is used for hardware level control of device power management. During normal operation, EN should be externally pulled directly up to V_{DD}, the 3.3V internal regulator output (see the *Typical Operating Circuit*).

To initiate a hardware reset and port power-down, pull EN to DGND for at least 100µs. While EN is held low, the device remains in reset and the ports remain securely powered down. Normal device operation resumes once EN is pulled up to the V_{DD}.

Thermal Shutdown

If the device's die temperature reaches +140°C (typ), an overtemperature fault is generated and the device shuts down. The die temperature must cool down below +120°C (typ) to remove the overtemperature fault condition. After a thermal shutdown condition clears, the device is reset and the TSD event bit is set to a logical 1 (R0Ah[7]/R0Bh[7], Table 12).

Watchdog

The Watchdog register (R42h, Table 36) is used to monitor device status, and to enable and monitor the watchdog functionality. On a power-up or after a reset condition, this register is set to a default value of 16h. WD_DIS[3:0] is set by default to 1011, disabling the watchdog timeout. Set WD_DIS[3:0] to any other value to enable the watchdog. The watchdog monitors the SCL line for activity. If there are no transitions for 2.5s (typ), the WD_STAT bit is set to 1 and all ports are powered down (using the individual port reset protocol). WD_STAT must be reset before any port can be reenabled.

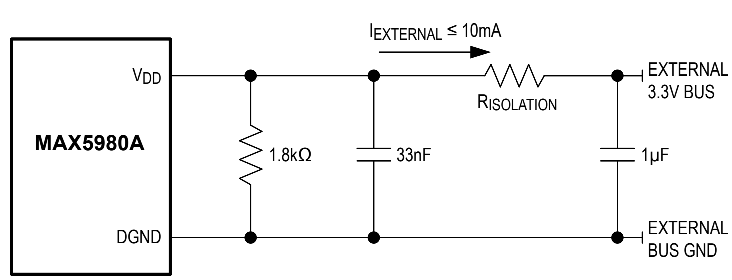


Figure 4. V_{DD} External Power Sourcing

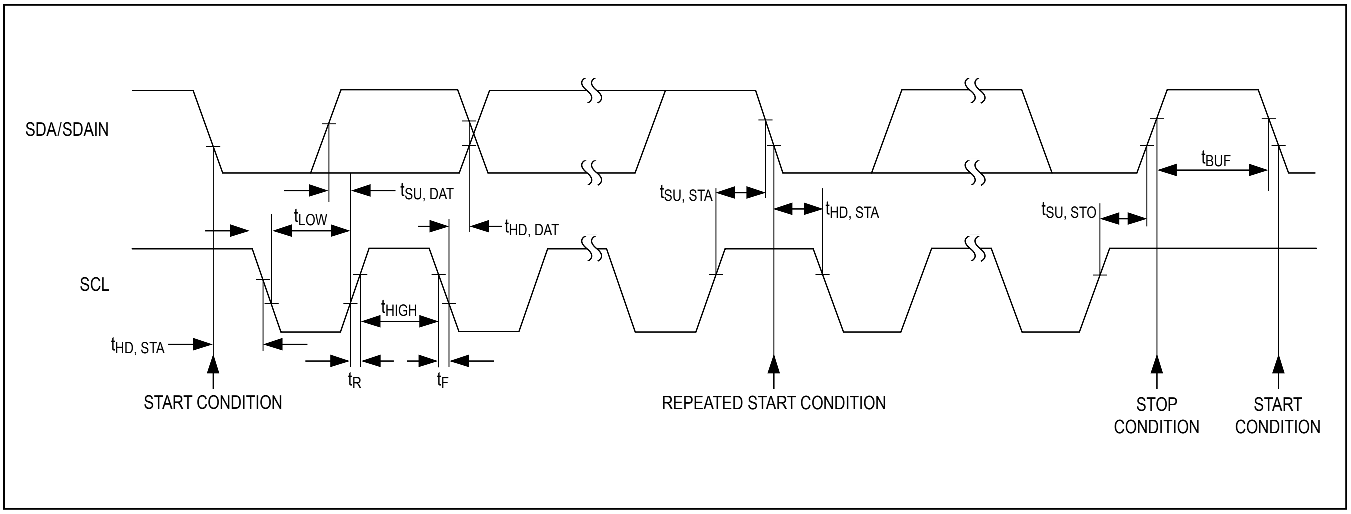


Figure 5. Serial Interface Timing Details

Table 3. Programmable Device Address Settings

DEVICE ADDRESS						
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**
0	1	0	A3	A2	A1	A0

Device Address

The MAX5980A is programmable to 1 of 16 unique slave device addresses. The three MSBs of the device address are always [010]. The 4 LSBs of the device address are programmable, and are formed by the states of the Slave Address Inputs (A0, A1, A2, and A3; see Table 3). To program the device address, connect A0, A1, A2, and A3 to a combination of V_{DD} (logical 1) and DGND (logical 0), and initiate a device reset.

I²C-Compatible Serial Interface

The device operates as a slave that sends and receives data through an I²C-compatible, 2-wire or 3-wire interface. The interface uses a serial-data input line (SDAIN), a serial-data output line (SDAOUT), and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the device, and generates the SCL clock that synchronizes the data transfer. In most applications, connect the SDAIN and the SDAOUT lines together to form the serial-data line (SDA). Most of the figures shown label the bus as SDA.

Using the separate input and output data lines allows optocoupling with the controller bus when an isolated supply powers the microcontroller.

The device's SDAIN line operates as an input and SDAOUT operates as an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDAOUT (3-wire mode) or SDA (2-wire mode). The SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters, or if the master in a single-master system has an open-drain SCL output.

Serial Addressing

Each transmission consists of a START condition sent by a master, followed by the device's 7-bit slave address plus R/W bit, a register address byte, 1 or more data bytes, and finally a STOP condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master finishes communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The STOP condition frees the bus for another transmission (see Figure 6).

Bit Transfer

Each clock pulse transfers one data bit (Figure 7). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 8) that the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master transmits to the MAX5980A, the device generates the acknowledge bit. When the device transmits to the master, the master generates the acknowledge bit.

Slave Address

The device has a 7-bit long slave address (Figure 9). The bit following the 7-bit slave address (bit 8) is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. 010 always represents the first three bits (MSBs) of the MAX5980A slave address. Slave address bits A[3:0] represent the state of the device's A3–A0 inputs, allowing up to 16 MAX5980A devices to share the bus. The states of A3–A0 latch in upon the reset of the device into register R11h. The device monitors the bus continuously, waiting for a START condition followed by the MAX5980A slave address. When the device recognizes its slave address, it acknowledges and is then ready for continued communication.

Global Addressing and the Alert Reponse Address (ARA)

The global address call is used in write mode to write to the same register to multiple devices (address 60h). The global address call can also be used in read mode (61h) in the same way as the alert response address (ARA). The actual

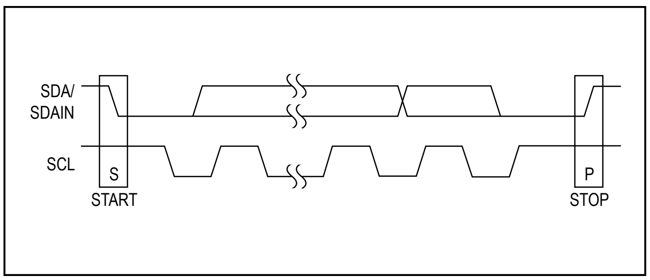


Figure 6. START and STOP Conditions

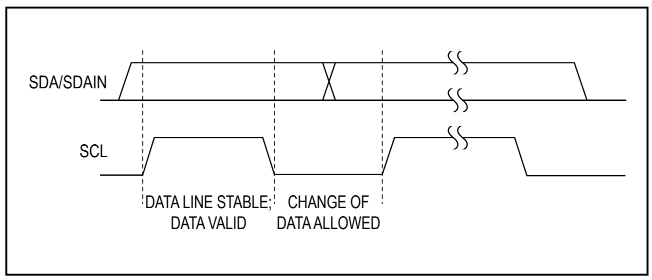


Figure 7. Bit Transfer

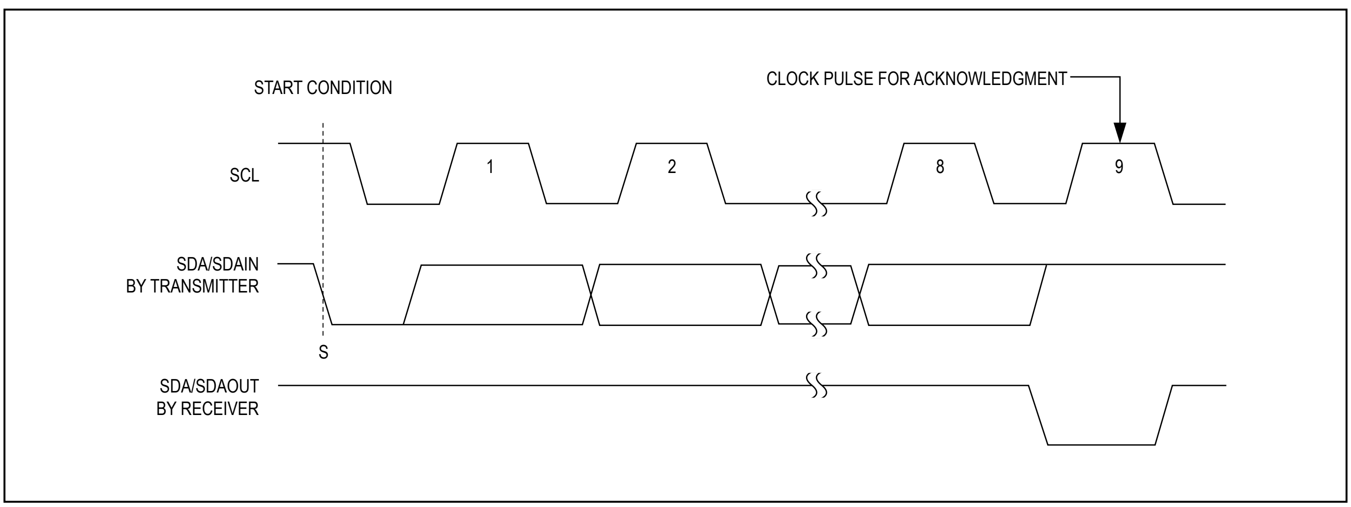


Figure 8. Acknowledge

alert response address (ARA) is 0Ch. The MAX5980A slave device only responds to the ARA if its $\overline{INT}$ (interrupt) output is asserted. All MAX5980A devices in which the $\overline{INT}$ output is not asserted ignore the ARA.

When responding to the ARA, the device transmits a byte of data on SDAOUT containing its own address in the top 7 bits, and a 1 in the LSB (as does every other device connected to the SDAIN line that has an active interrupt). As each bit in the byte is transmitted, the device determines whether to continue transmitting the remainder of the byte or terminate transmission. The device terminates the transmission if it sees a 0 on SDA at a time when it is attempting to send a 1; otherwise it continues transmitting bits until the entire byte has been sent. This litigation protocol always allows the part with the lowest address to complete the transmission, and the microcontroller can respond to that interrupt. The device deasserts $\overline{INT}$ if it completes the transmission of the entire byte. If the device did not have the lowest address, and terminates the transmission early, the $\overline{INT}$ output remains asserted. In this way, the microcontroller can continue to send ARA read cycles until all slave devices successfully transmit their addresses, and all interrupt requests are resolved.

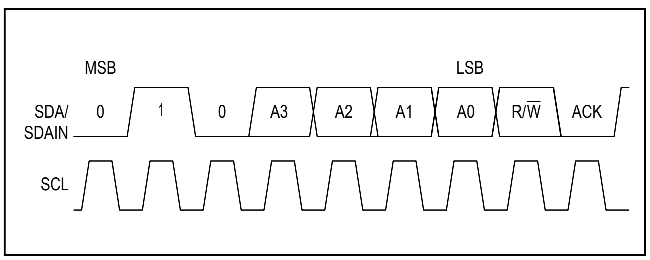


Figure 9. Slave Address

General Call

In compliance with the I²C specification, the device responds to the general call through global address 30h.

Message Format for Writing to the MAX5980A

A write to the device comprises the device slave address transmission with the R$\overline{W}$ bit set to 0, followed by at least 1 byte of information. The first byte of information is the command byte (Figure 10). The command byte determines which register of the device is written to by the next byte, if received. If the device detects a STOP condition after receiving the command byte but before receiving any data, then the device takes no further action beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the device selected by the command byte (Figure 11). The control byte address then autoincrements (if possible; see Table 4) and then waits for the next data byte or a STOP condition.

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are stored in subsequent MAX5980A internal registers as the control byte address autoincrements (Figure 12). If the control byte address can no longer increment, any subsequent data sent continues to write to that address.

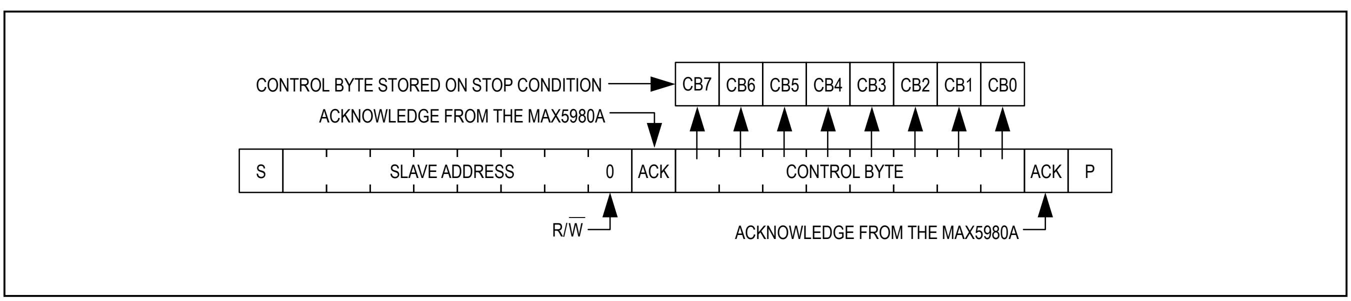


Figure 10. Write Format, Control Byte Received

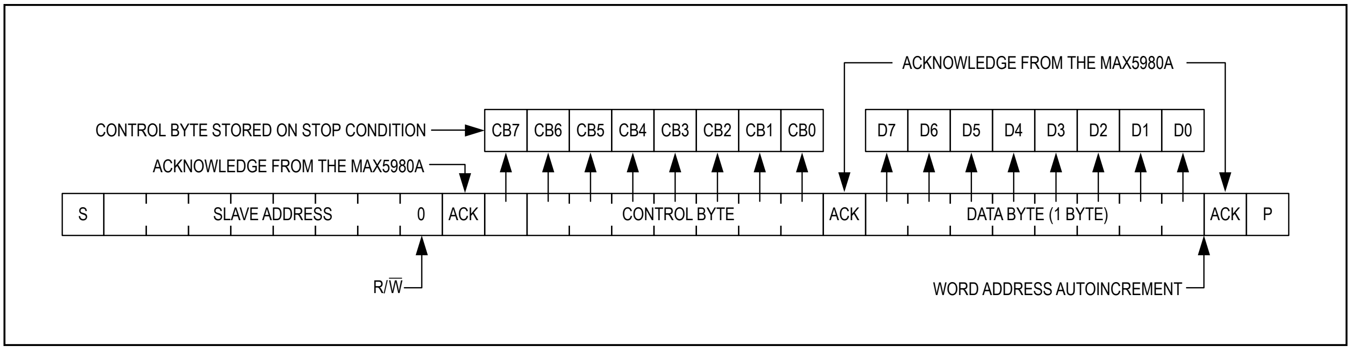


Figure 11. Write Format, Control, and Single Data Byte Written

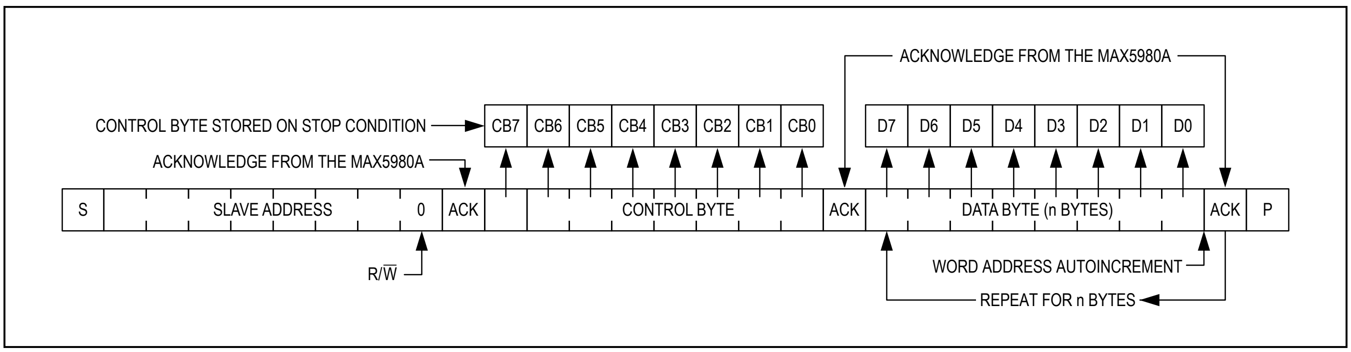


Figure 12. Write Format, Control, and n Data Bytes Written

Message Format for Reading

The MAX5980A supports the standard I2C Read formats. Since the device autoincrements the control byte address pointer when data is written or read from the device, all read commands should be preceded with a write command to reset the control byte address. The read instruction can comprise either a repeated start (standard combined-read) or a stop-start command transition, as shown in Figure 13. The device then reads using the internally stored control byte as an address pointer, the same way the stored control byte is used as an address pointer for a write command. This pointer autoincrements after reading each data byte using the same rules as for a write, though the master now sends the acknowledge bit after each received data byte (Figure 13). The read command ends when the device receives a NACK and stop instruction from the master.

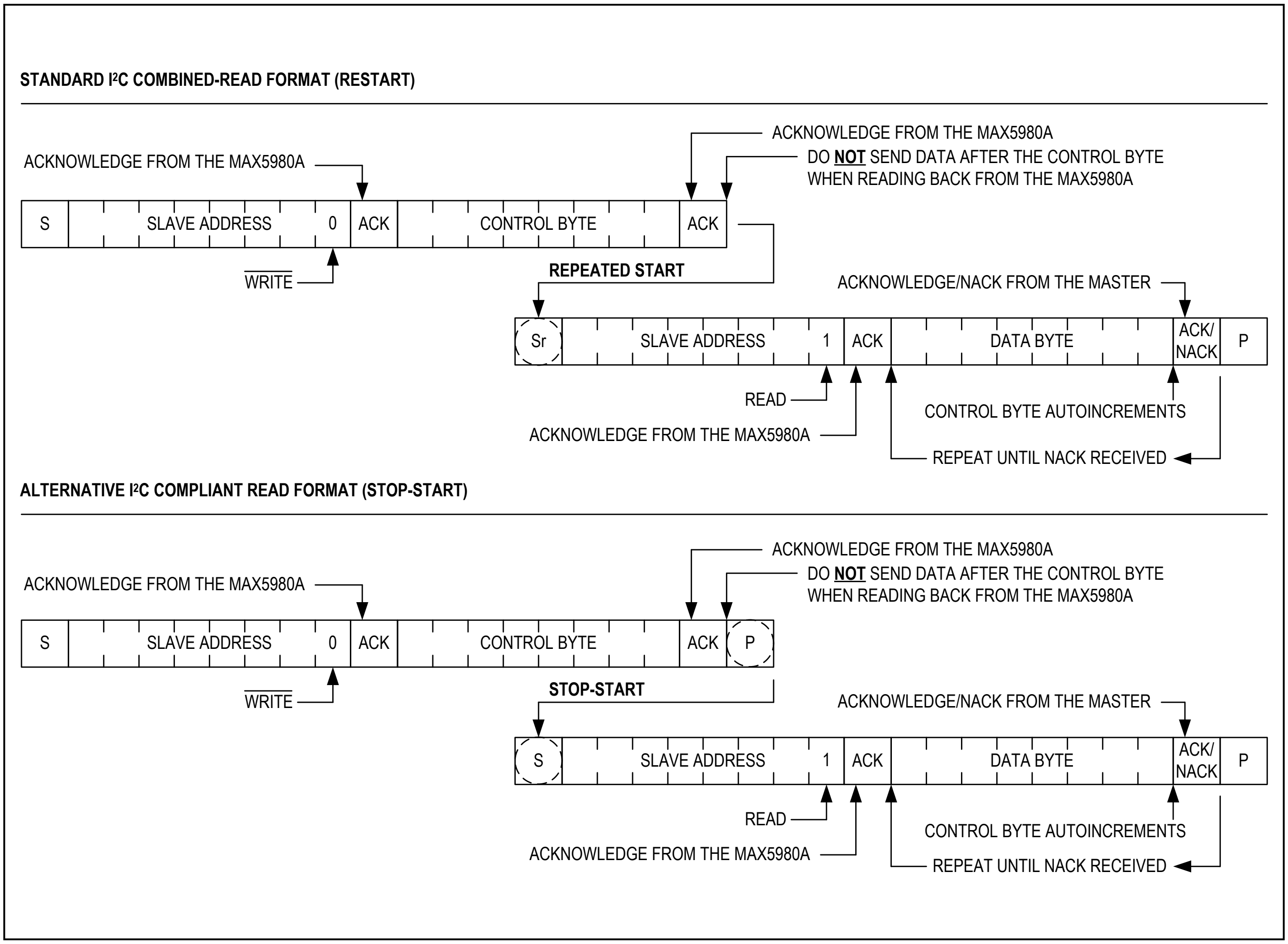


Figure 13. Read Format, Control, and n Data Bytes Read

Operation with Multiple Masters

When the device operates on a 3-wire interface with multiple masters, a master reading the device should use repeated starts between the write that sets the device's address pointer, and the read(s) that take the data from the location(s). It is possible for master 2 to take over the bus after master 1 has set up the device's address pointer but before master 1 has read the data. If master 2 subsequently resets the device's address pointer, then master 1's read may be from an unexpected location.

Command Address Autoincrementing

Address autoincrementing allows the device to be configured with fewer transmissions by minimizing the number of times the command address needs to be sent. The command address stored in the device generally increments after each data byte is written or read (Table 4). The device is designed to prevent overwrites on unavailable register addresses and unintentional wraparound of addresses.

Register Map and Description

The device contains a bank of volatile registers that store its settings and status. The device features an I^2C-compatible, 3-wire serial interface, allowing the registers to be fully software configurable and programmable. In addition, several registers are also pin-programmable to allow the device to operate in auto mode and still be partially configurable even without the assistance of software.

Table 4. Autoincrement Rules

COMMAND BYTE ADDRESS RANGE	AUTOINCREMENT BEHAVIOR
0x00 to 0x71	Command address autoincrements after byte read or written
0x71	Command address remains at 0x71 after byte written or read

Table 5. Register Map Summary

ADDR	REGISTER NAME	TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET STATE
INTERRUPTS											
00h	Interrupt	R	SUP_INT	TST_INT	TCUT_INT	CLS_INT	DET_INT	DIS_INT	PG_INT	PE_INT	1000–0000
01h	Interrupt Mask	R/W	SUP_MASK	TST_MASK	TCUT_MASK	CLS_MASK	DET_MASK	DIS_MASK	PG_MASK	PE_MASK	1XX0–0X00
EVENTS											
02h	Power Event	R	PG_CHG4	PG_CHG3	PG_CHG2	PG_CHG1	PE_CHG4	PE_CHG3	PE_CHG2	PE_CHG1	0000–0000
03h	Power Event CoR	CoR									
04h	Detect Event	R	CLS4	CLS3	CLS2	CLS1	DET4	DET3	DET2	DET1	0000–0000
05h	Detect Event CoR	CoR									
06h	Fault Event	R	DIS4	DIS3	DIS2	DIS1	TCUT4	TCUT3	TCUT2	TCUT1	0000–0000
07h	Fault Event CoR	CoR									
08h	Startup Event	R	ICV4	ICV3	ICV2	ICV1	TSTART4	TSTART3	TSTART2	TSTART1	0000–0000
09h	Startup Event CoR	CoR									
0Ah	Supply Event	R	TSD	FETBAD	V_{DD_UVLO}	V_{EE_UVLO}	—	—	—	—	0000–0010
0Bh	Supply Event CoR	CoR									

Table 5. Register Map Summary (continued)

ADDR	REGISTER NAME	TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET STATE
STATUS											
0Ch	Port 1 Status	R	—	CLASS1[2]	CLASS1[1]	CLASS1[0]	—	DET_ST1[2]	DET_ST1[1]	DET_ST1[0]	0000–0000
0Dh	Port 2 Status	R	—	CLASS2[2]	CLASS2[1]	CLASS2[0]	—	DET_ST2[2]	DET_ST2[1]	DET_ST2[0]	0000–0000
0Eh	Port 3 Status	R	—	CLASS3[2]	CLASS3[1]	CLASS3[0]	—	DET_ST3[2]	DET_ST3[1]	DET_ST3[0]	0000–0000
0Fh	Port 4 Status	R	—	CLASS4[2]	CLASS4[1]	CLASS4[0]	—	DET_ST4[2]	DET_ST4[1]	DET_ST4[0]	0000–0000
10h	Power Status	R	PGOOD4	PGOOD3	PGOOD2	PGOOD1	PWR_EN4	PWR_EN3	PWR_EN2	PWR_EN1	0000–0000
11h	Pin Status	R	—	—	SLAVE[1]	SLAVE[0]	ID[1]	ID[0]	—	AUTO	00XX–XX0X
CONFIGURATION											
12h	Operating Mode	R/W	P4_M[1]	P4_M[0]	P3_M[1]	P3_M[0]	P2_M[1]	P2_M[0]	P1_M[1]	P1_M[0]	XXXX–XXXX
13h	Disconnect Enable	R/W	ACD_EN4	ACD_EN3	ACD_EN2	ACD_EN1	DCD_EN4	DCD_EN3	DCD_EN2	DCD_EN1	XXXX–0000
14h	Detection and Classification Enable	R/W	CLASS_ EN4	CLASS_EN3	CLASS_EN2	CLASS_EN1	DET_EN4	DET_EN3	DET_EN2	DET_EN1	XXXX–XXXX
15h	Midspan Enable	R/W	—	—	—	—	MIDSPAN4	MIDSPAN3	MIDSPAN2	MIDSPAN1	0000–XXXX
16h	Reserved	R/W	—	—	—	—	—	—	—	—	—
17h	Miscellaneous Configuration 1	R/W	INT_EN	DET_CHG	—	—	—	—	—	—	1010–0000
PUSHBUTTONS											
18h	Detection/ Classification Pushbutton	W	CLS_PB4	CLS_PB3	CLS_PB2	CLS_PB1	DET_PB4	DET_PB3	DET_PB2	DET_PB1	0000–0000
19h	Power-Enable Pushbutton	W	PWR_OFF4	PWR_OFF3	PWR_OFF2	PWR_OFF1	PWR_ON4	PWR_ON3	PWR_ON2	PWR_ON1	0000–0000
1Ah	Global Pushbutton	W	INT_CLR	PIN_CLR	—	RESET_IC	RESET_P4	RESET_P3	RESET_P2	RESET_P1	0000–0000
GENERAL											
1Bh	ID	R	ID_CODE[4]	ID_CODE[3]	ID_CODE[2]	ID_CODE[1]	ID_CODE[0]	REV[2]	REV[1]	REV[0]	1101–0000
1Ch	Class 5 Enable	R/W	—	—	—	—	CL5_EN4	CL5_EN3	CL5_EN2	CL5_EN1	0000–0000
1Dh	Reserved	—	—	—	—	—	—	—	—	—	—
1Eh	TLIM1/2 Programming	R/W	TLIM2[3]	TLIM2[2]	TLIM2[1]	TLIM2[0]	TLIM1[3]	TLIM1[2]	TLIM1[1]	TLIM1[0]	0000–0000
1Fh	TLIM3/4 Programming	R/W	TLIM4[3]	TLIM4[2]	TLIM4[1]	TLIM4[0]	TLIM3[3]	TLIM3[2]	TLIM3[1]	TLIM3[0]	0000–0000

Table 5. Register Map Summary (continued)

ADDR	REGISTER NAME	TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET STATE
MAXIM RESERVED											
20h	Reserved	—	—	—	—	—	—	—	—	—	—
21h	Reserved	—	—	—	—	—	—	—	—	—	—
22h	Reserved	—	—	—	—	—	—	—	—	—	—
23h	Reserved	—	—	—	—	—	—	—	—	—	—
24h	Reserved	—	—	—	—	—	—	—	—	—	—
25h	Reserved	—	—	—	—	—	—	—	—	—	—
26h	Reserved	—	—	—	—	—	—	—	—	—	—
27h	Reserved	—	—	—	—	—	—	—	—	—	—
28h	Reserved	—	—	—	—	—	—	—	—	—	—
29h	Miscellaneous Configuration 2	R/W	—	—	—	LSC_EN	VEE_R4	VEE_R3	VEE_R2	VEE_R1	0000–0000
2Ah	Reserved	—	—	—	—	—	—	—	—	—	—
2Bh	Reserved	—	—	—	—	—	—	—	—	—	—
2Ch	Reserved	—	—	—	—	—	—	—	—	—	—
2Dh	Reserved	—	—	—	—	—	—	—	—	—	—
2Eh	Reserved	—	—	—	—	—	—	—	—	—	—
2Fh	Reserved	—	—	—	—	—	—	—	—	—	—
CURRENT/VOLTAGE											
30h	Port 1 Current	R	IP1[7]	IP1[6]	IP1[5]	IP1[4]	IP1[3]	IP1[2]	IP1[1]	IP1[0]	0000–0000
31h	Port 1 Current	R	IP1[15]	IP1[14]	IP1[13]	IP1[12]	IP1[11]	IP1[10]	IP1[9]	IP1[8]	0000–0000
32h	Port 1 Voltage	R	VP1[7]	VP1[6]	VP1[5]	VP1[4]	VP1[3]	VP1[2]	VP1[1]	VP1[0]	0000–0000
33h	Port 1 Voltage	R	VP1[15]	VP1[14]	VP1[13]	VP1[12]	VP1[11]	VP1[10]	VP1[9]	VP1[8]	0000–0000
34h	Port 2 Current	R	IP2[7]	IP2[6]	IP2[5]	IP2[4]	IP2[3]	IP2[2]	IP2[1]	IP2[0]	0000–0000
35h	Port 2 Current	R	IP2[15]	IP2[14]	IP2[13]	IP2[12]	IP2[11]	IP2[10]	IP2[9]	IP2[8]	0000–0000
36h	Port 2 Voltage	R	VP2[7]	VP2[6]	VP2[5]	VP2[4]	VP2[3]	VP2[2]	VP2[1]	VP2[0]	0000–0000
37h	Port 2 Voltage	R	VP2[15]	VP2[14]	VP2[13]	VP2[12]	VP2[11]	VP2[10]	VP2[9]	VP2[8]	0000–0000
38h	Port 3 Current	R	IP3[7]	IP3[6]	IP3[5]	IP3[4]	IP3[3]	IP3[2]	IP3[1]	IP3[0]	0000–0000
39h	Port 3 Current	R	IP3[15]	IP3[14]	IP3[13]	IP3[12]	IP3[11]	IP3[10]	IP3[9]	IP3[8]	0000–0000
3Ah	Port 3 Voltage	R	VP3[7]	VP3[6]	VP3[5]	VP3[4]	VP3[3]	VP3[2]	VP3[1]	VP3[0]	0000–0000
3Bh	Port 3 Voltage	R	VP3[15]	VP3[14]	VP3[13]	VP3[12]	VP3[11]	VP3[10]	VP3[9]	VP3[8]	0000–0000
3Ch	Port 4 Current	R	IP4[7]	IP4[6]	IP4[5]	IP4[4]	IP4[3]	IP4[2]	IP4[1]	IP4[0]	0000–0000
3Dh	Port 4 Current	R	IP4[15]	IP4[14]	IP4[13]	IP4[12]	IP4[11]	IP4[10]	IP4[9]	IP4[8]	0000–0000
3Eh	Port 4 Voltage	R	VP4[7]	VP4[6]	VP4[5]	VP4[4]	VP4[3]	VP4[2]	VP4[1]	VP4[0]	0000–0000
3Fh	Port 4 Voltage	R	VP4[15]	VP4[14]	VP4[13]	VP4[12]	VP4[11]	VP4[10]	VP4[9]	VP4[8]	0000–0000
OTHER FUNCTIONS											
40h	Reserved	—	—	—	—	—	—	—	—	—	—
41h	Firmware	R/W	0	0	0	0	0	0	0	0	0000–0000
42h	Watchdog	R	—	VEE_OV	VEE_UV	WD_DIS[3]	WD_DIS[2]	WD_DIS[1]	WD_DIS[0]	WD_STAT	0001–0110

Table 5. Register Map Summary (continued)

ADDR	REGISTER NAME	TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET STATE
43h	Developer ID/Revision Number	R/W	DEV_ID[2]	DEV_ID[1]	DEV_ID[0]	—	—	DEV_REV[2]	DEV_REV[1]	DEV_REV[0]	0000–0000
44h	High-Power Enable	R/W	—	—	—	—	HP_EN4	HP_EN3	HP_EN2	HP_EN1	0000–XXXX
45h	Reserved	—	—	—	—	—	—	—	—	—	—
46h	Port 1 GPMD	R/W	—	—	—	—	—	—	LEG_EN1	PONG_EN1	0000–000X
47h	Port 1 ICUT	R/W	RDIS1	CUT_RNG1	ICUT1[5]	ICUT1[4]	ICUT1[3]	ICUT1[2]	ICUT1[1]	ICUT1[0]	XX01–0100
48h	Port 1 ILIM	R/W	1	ILIM1	0	0	0	0	0	0	1000–0000
49h	Port 1 High-Power Status	R	—	—	—	—	—	—	FET_BAD1	PONG_PD1	0000–0000
4Ah	Reserved	—	—	—	—	—	—	—	—	—	—
4Bh	Port 2 GPMD	R/W	—	—	—	—	—	—	LEG_EN2	PONG_EN2	0000–000X
4Ch	Port 2 ICUT	R/W	RDIS2	CUT_RNG2	ICUT2[5]	ICUT2[4]	ICUT2[3]	ICUT2[2]	ICUT2[1]	ICUT2[0]	XX01–0100
4Dh	Port 2 ILIM	R/W	1	ILIM2	0	0	0	0	0	0	1000–0000
4Eh	Port 2 High-Power Status	R	—	—	—	—	—	—	FET_BAD2	PONG_PD2	0000–0000
4Fh	Reserved	—	—	—	—	—	—	—	—	—	—
50h	Port 3 GPMD	R/W	—	—	—	—	—	—	LEG_EN3	PONG_EN3	0000–000X
51h	Port 3 ICUT	R/W	RDIS3	CUT_RNG3	ICUT3[5]	ICUT3[4]	ICUT3[3]	ICUT3[2]	ICUT3[1]	ICUT3[0]	XX01–0100
52h	Port 3 ILIM	R/W	1	ILIM3	0	0	0	0	0	0	1000–0000
53h	Port 3 High-Power Status	R	—	—	—	—	—	—	FET_BAD3	PONG_PD3	0000–0000
54h	Reserved	—	—	—	—	—	—	—	—	—	—
55h	Port 4 GPMD	R/W	—	—	—	—	—	—	LEG_EN4	PONG_EN4	0000–000X
56h	Port 4 ICUT	R/W	RDIS4	CUT_RNG4	ICUT4[5]	ICUT4[4]	ICUT4[3]	ICUT4[2]	ICUT4[1]	ICUT4[0]	XX01–0100
57h	Port 4 ILIM	R/W	1	ILIM4	0	0	0	0	0	0	1000–0000
58h	Port 4 High-Power Status	R	—	—	—	—	—	—	FET_BAD4	PONG_PD4	0000–0000
59h	Reserved	—	—	—	—	—	—	—	—	—	—
5Ah	Reserved	—	—	—	—	—	—	—	—	—	—
5Bh	Reserved	—	—	—	—	—	—	—	—	—	—
5Ch	Reserved	—	—	—	—	—	—	—	—	—	—
5Dh	Reserved	—	—	—	—	—	—	—	—	—	—
5Eh	Reserved	—	—	—	—	—	—	—	—	—	—
5Fh	Reserved	—	—	—	—	—	—	—	—	—	—

X Indicates that the register reset state depends on either the status of the external programming pins (A3–A0, EN_CL5, AUTO, and MIDSPAN) or that the cause of the reset condition determines the state.

— Indicates that the register is either unused or reserved. Always write a logic-low to any reserved bits when programming a register, unless otherwise indicated in the Register Map and Description section.

Interrupt Registers (R00h, R01h)

Interrupt Register (R00h)

The Interrupt register (R00h, Table 6) summarizes the Event Register status and is used to send an interrupt signal to the controller. On power-up or after a reset condition, interrupt (R00h) is set to a default value of 00h (it may almost immediately report an interrupt depending on if it was a power-up or reset condition, and in the case of reset the type/cause of reset). $\overline{INT}$ goes low to report an interrupt event if any one of the active interrupt bits is set to 1 (active-high) and it is not masked by the Interrupt Mask register (R01h, Table 7). $\overline{INT}$ does not go low to report an interrupt if the corresponding mask bit (R01h) is set. Writing a 1 to INT_CLR (R1Ah[7], Table 27) clears all interrupt and events registers (resets to low). INT_EN (R17h[7], Table 24) is a global interrupt enable and writing a 0 to INT_EN disables the $\overline{INT}$ output, putting it into a state of high impedance.

Interrupt Mask Register (R01h)

The Interrupt Mask register (R01h, Table 7) contains mask bits that suppress the corresponding interrupt bits in register R00h (active-high). Setting mask bits low individually disables the corresponding interrupt signal. When masked (set low), the corresponding bits are still set in the Interrupt register (R00h) but the masking bit (R01h) suppresses the generation of an interrupt signal ($\overline{INT}$). Supply interrupts set on a power-up or reset event cannot be masked, such as TSD, V_{DD_UVLO}, and V_{EE_UVLO}. On power-up or a reset condition, the Interrupt Mask register is set to a default state of E4h if AUTO is high, and 80h is AUTO is low.

Table 6. Interrupt Register

ADDRESS = 00h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
SUP_INT	7	R	Interrupt signal for supply faults. SUP_INT is the logic OR of all the active bits in the Supply Event register (R0Ah/R0Bh[7:4], Table 12).
TST_INT	6	R	Interrupt signal for startup failures. TST_INT is the logic OR of the TSTART_ bits in the Startup Event register (R08h/R09h[3:0], Table 11).
TCUT_INT	5	R	Interrupt signal for port overcurrent and current-limit violations. TCUT_INT is the logic OR of the TCUT_ bits in the Fault Event register (R06h/R07h, Table 10) and the ICV_ bits in the Startup Event register (R08h/R09h, Table 11).
CLS_INT	4	R	Interrupt signal for completion of classification. CLS_INT is the logic OR of the CLS_ bits in the Detect Event register (R04h/R05h, Table 9).
DET_INT	3	R	Interrupt signal for completion of detection. DET_INT is the logic OR of the DET_ bits in the Detect Event register (R04h/R05h, Table 9).
DIS_INT	2	R	Interrupt signal for a DC load disconnect. DIS_INT is the logic OR of the DIS_ bits in the Fault Event register (R06h/R07h, Table 10).
PG_INT	1	R	Interrupt signal for PGOOD_ (R10h[7:4]) status changes. PG_INT is the logic OR of the PG_CHG_ bits in the Power Event register (R02h/R03h, Table 8).
PE_INT	0	R	Interrupt signal for power enable status change. PE_INT is the logic OR of the PE_CHG_ bits in the Power Event register (R02h/R03h, Table 8).

Event Registers (R02h–R08h)

Power Event Register (R02h/R03h)

The Power Event register (R02h/R03h, Table 8) records changes in the power status of the port. On power-up or after a reset condition, the Power Event register is set to a default value of 00h. Any change in PGOOD_ (R10h[7:4]) sets PG_CHG_ to 1. Any change in PWR_EN_ (R10h[3:0]) sets PE_CHG_ to 1. PG_CHG_ and PE_CHG_ trigger on the transition edges of PGOOD_ and PWR_EN_, and do not depend on the actual logic status of the bits. The Power Event register has two addresses. When read through the R02h address, the content of the register is left unchanged. When read through the Clear on Read (CoR) R03h address, the register content is reset to the default state.

Detect Event Register (R04h/R05h)

The Detect Event register (R04h/R05h, Table 9) records detection/classification events for the port. On power-up or after a reset condition, the Detect Event register is set to a default value of 00h. DET_ and CLS_ are set high whenever detection/classification is completed on the corresponding port. As with the other event registers, the Detect Event register has two addresses. When read through the R04h address, the content of the register

Table 7. Interrupt Mask Register

ADDRESS = 01h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
SUP_MASK	7	R/W	Supply interrupt mask. A logic-high enables the SUP_INT interrupt. A logic-low disables the SUP_INT interrupts.
TST_MASK	6	R/W	Startup interrupt mask. A logic-high enables the TST_INT interrupt. A logic-low disables the TST_INT interrupts.
TCUT_MASK	5	R/W	Current interrupt mask. A logic-high enables the TCUT_INT interrupt. A logic-low disables the TCUT_INT interrupt.
CLS_MASK	4	R/W	Classification interrupt mask. A logic-high enables the CLS_INT interrupt. A logic-low disables the CLS_END interrupt.
DET_MASK	3	R/W	Detection interrupt mask. A logic-high enables the DET_INT interrupt. A logic-low disables the DET_INT interrupt.
DIS_MASK	2	R/W	DC disconnect interrupt mask. A logic-high enables the DIS_INT interrupts. A logic-low disables the DIS_INT interrupts.
PG_MASK	1	R/W	PGOOD interrupt mask. A logic-high enables the PG_INT interrupts. A logic-low disables the PG_INT interrupts.
PE_MASK	0	R/W	Power-enable interrupt mask. A logic-high enables the PE_INT interrupts. A logic-low disables the PE_INT interrupts.

Table 8. Power Event Register

ADDRESS =		02h	03h	DESCRIPTION
SYMBOL	BIT NO.	TYPE	TYPE	
PG_CHG4	7	R	CoR	PGOOD change event for port 4
PG_CHG3	6	R	CoR	PGOOD change event for port 3
PG_CHG2	5	R	CoR	PGOOD change event for port 2
PG_CHG1	4	R	CoR	PGOOD change event for port 1
PE_CHG4	3	R	CoR	Power enable change event for port 4
PE_CHG3	2	R	CoR	Power enable change event for port 3
PE_CHG2	1	R	CoR	Power enable change event for port 2
PE_CHG1	0	R	CoR	Power enable change event for port 1

is left unchanged. When read through the CoR R05h address, the register content is reset to the default state.

Fault Event Register (R06h/R07h)

The Fault Event register (R06h/R07h, Table 10) records port DC load and overcurrent disconnect timeout events. On power-up or after a reset condition, the Fault Event register is set to a default value of 00h. DIS_ is set to 1 whenever a port shuts down due to a DC load disconnect event. TCUT_ is set to 1 when a port shuts down due to an extended overcurrent event after a successful startup. As with the other events registers, the Fault Event register has two addresses. When read through the R06h address, the content of the register is left unchanged. When read through the CoR R07h address, the register content is reset to the default state.

Startup Event Register (R08h/R09h)

The Startup Event register (R08h/R09h, Table 11) records port startup failure events and current-limit disconnect timeout events. On power-up or after a reset condition, the Fault Event register is set to a default value of 00h. ICV_ is set to 1 when a port shuts down due to an extended current-limit event after startup. TSTART is set to 1 whenever a port fails startup due to an overcurrent or current-limit event during startup. As with the other event registers, the Startup Event register has two addresses. When read through the R08h address, the content of the register is left unchanged. When read through the CoR R09h address, the register content is reset to the default state.

Supply Event Register (R0Ah/R0Bh)

The device monitors die temperature, external FET status, and the analog and digital power supplies, and sets

Table 9. Detect Event Register

ADDRESS =		04h	05h	DESCRIPTION
SYMBOL	BIT NO.	TYPE	TYPE	
CLS4	7	R	CoR	Classification completed on port 4
CLS3	6	R	CoR	Classification completed on port 3
CLS2	5	R	CoR	Classification completed on port 2
CLS1	4	R	CoR	Classification completed on port 1
DET4	3	R	CoR	Detection completed on port 4
DET3	2	R	CoR	Detection completed on port 3
DET2	1	R	CoR	Detection completed on port 2
DET1	0	R	CoR	Detection completed on port 1

Table 10. Fault Event Register

ADDRESS =		06h	07h	DESCRIPTION
SYMBOL	BIT NO.	TYPE	TYPE	
DIS4	7	R	CoR	DC load disconnect timeout on port 4
DIS3	6	R	CoR	DC load disconnect timeout on port 3
DIS2	5	R	CoR	DC load disconnect timeout on port 2
DIS1	4	R	CoR	DC load disconnect timeout on port 1
TCUT4	3	R	CoR	Overcurrent disconnect timeout on port 4
TCUT3	2	R	CoR	Overcurrent disconnect timeout on port 3
TCUT2	1	R	CoR	Overcurrent disconnect timeout on port 2
TCUT1	0	R	CoR	Overcurrent disconnect timeout on port 1

the appropriate bits in the Supply Event register (R0Ah/R0Bh, Table 12). On power-up or after a reset condition, the Supply Event register is set to a default value of 02h (but may immediately change depending on the cause of the reset).

A thermal-shutdown circuit monitors the temperature of the die and resets the device if the temperature exceeds +140°C. TSD is set to 1 after the device recovers from thermal shutdown and returns to normal operation.

If a FET failure is detected on one or more ports, FETBAD is set high. To determine which port the failure was detected on, check the FET_BAD_ bit in the HP Status register of each port (Table 42). FET_BAD_ is set to 1 if the port is powered, there is no current-limit condition, and $V_{OUT\_} - V_{EE} > 2V$.

When V_{EE} or V_{DD} are below their UVLO thresholds, the device is in reset mode and securely holds the port off. When they rise above the UVLO threshold, the device comes out of reset and the appropriate V_{DD_UVLO}/V_{EE_UVLO} bit in the Supply Event register is set to 1.

Status Registers (R0Ch–R11h)

Port Status Registers (R0Ch–R0Fh)

The Port Status registers (R0Ch–R0Fh, Table 13) record the results of the port detection and classification at the end of each phase in three encoded bits. On power-up or after a reset condition, the Port Status register is set to a default value of 00h. Tables 14 and 15 are the detection and classification result decoding tables respectively. For LEG_EN = 0 (Port GPMD register, Table 39), the detection result is shown in Table 13. When LEG_EN = 1, the device allows valid detection of high capacitive loads of up to 100µF (typ), and reports the result as HIGH_CAP. If CL5_EN_ = 1, any classification current in excess of Class 4 but less than the classification current limit will return a Class 5 classification result. If CL5_EN_ = 0, any classification current in excess of Class 4 will return a current-limit classification result, and the port will not power up.

Table 11. Startup Event Register

ADDRESS =		08h	09h	DESCRIPTION
SYMBOL	BIT NO.	TYPE	TYPE	
ICV4	7	R	CoR	Current-limit disconnect timeout on port 4
ICV3	6	R	CoR	Current-limit disconnect timeout on port 3
ICV2	5	R	CoR	Current-limit disconnect timeout on port 2
ICV1	4	R	CoR	Current-limit disconnect timeout on port 1
TSTART4	3	R	CoR	Startup failure on port 4
TSTART3	2	R	CoR	Startup failure on port 3
TSTART2	1	R	CoR	Startup failure on port 2
TSTART1	0	R	CoR	Startup failure on port 1

Table 12. Supply Event Register

ADDRESS =		0Ah	0Bh	DESCRIPTION
SYMBOL	BIT NO.	TYPE	TYPE	
TSD	7	R	CoR	Overtemperature shutdown
FETBAD	6	R	CoR	FETBAD is set if a FET failure is detected on one or more ports
V_{DD_UVLO}	5	R	CoR	V_{DD} undervoltage-lockout condition
V_{EE_UVLO}	4	R	CoR	V_{EE} undervoltage-lockout condition
Reserved	3	R	CoR	Reserved
Reserved	2	R	CoR	Reserved
Reserved	1	R	CoR	Reserved
Reserved	0	R	CoR	Reserved

Power Status Register (R10h)

The Power Status register (R10h, Table 16) records the current status of port power. On power-up or after a reset condition, the port is initially unpowered and the Power Status register is set to its default value of 00h. PGOOD_ (R10h[7:4]) is set to 1 at the end of the power-up startup period if $V_{OUT\_} - V_{EE} > PG_{TH}$ for more than t_{PGOOD}.

PGOOD_ is a real-time bit and is reset to 0 whenever $V_{OUT\_} - V_{EE} \leq PG_{TH}$, or a fault condition occurs. PWR_EN_ (R10h[3:0]) is set to 1 when the port power is turned on. PWR_EN resets to 0 as soon as the port turns off. Any transition of PGOOD_ and PWR_EN_ bits set the corresponding bit in the Power Event register (R02h/R03h, Table 8).

Table 13. Port Status Register

ADDRESS = 0Ch, 0Dh, 0Eh, 0Fh			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
Reserved	7	—	Reserved
CLASS_[2:0]	6	R	Classification result for the corresponding port (Table 14)
	5	R	
	4	R	
Reserved	3	—	Reserved
DET_ST_[2:0]	2	R	Detection result for the corresponding port (Table 13)
	1	R	
	0	R	

Table 14. Detection Result Decoding Chart

DET_ST_[2:0]	DETECTED	DESCRIPTION
000	NONE	Detection status unknown (default)
001	DCP	Positive DC supply connected at the port ($V_{AGND} - V_{OUT\_} < 1V$)
010	HIGH CAP	High capacitance at the port (> 8.5µF (typ))
011	RLOW	Low resistance at the port ($R_{DET} < 15k\Omega$)
100	DET_OK	Detection pass ($15k\Omega > R_{DET} > 33k\Omega$)
101	RHIGH	High resistance at the port ($R_{DET} > 33k\Omega$)
110	OPEN	Open port ($I_{OUT\_} < 10\mu A$)
111	DCN	Low impedance to V_{EE} at the port ($V_{OUT\_} - V_{EE} < 2V$)

Table 15. Classification Result Decoding Chart

CLASS_[2:0]	CLASS RESULT
000	Unknown
001	1
010	2
011	3
100	4
101	5
110	0
111	Current limit

Pin Status Register (R11h)

The Pin Status register (R11h, Table 17) records the state of the A3, A2, A1, A0, and AUTO pins. The states of A1and A0 (into ID[1:0]), A3 and A2 (into SLAVE[1:0]), and AUTO are latched into their corresponding bits after a power-up or reset condition clears. Therefore, the default state of the Pin Status register depends on those inputs (00XX–XX0X). Changes to those inputs during normal operation are ignored and do not change the register contents. A3, A2, A1, and A0 all have internal pullups, and when left unconnected result in a default address of 0101111 (2Fh). Connect one or more low before a power-up or device reset to reprogram the slave address. SLAVE[1:0] also typically indicates which of the 16 PSE-ICM ports the slave device controls (Table 18).

Table 16. Power Status Register

ADDRESS = 10h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
PGOOD4	7	R	Power-good condition on port 4
PGOOD3	6	R	Power-good condition on port 3
PGOOD2	5	R	Power-good condition on port 2
PGOOD1	4	R	Power-good condition on port 1
PWR_EN4	3	R	Power is enabled on port 4
PWR_EN3	2	R	Power is enabled on port 3
PWR_EN2	1	R	Power is enabled on port 2
PWR_EN1	0	R	Power is enabled on port 1

Table 17. Pin Status Register

ADDRESS = 11h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
Reserved	7	—	Reserved
Reserved	6	—	Reserved
SLAVE[1:0]	5	R	Slave input (A3 and A2) latched-in status (Table 3)
	4	R	
ID[1:0]	3	R	ID input (A1 and A0) latched-in status (Table 3)
	2	R	
Reserved	1	—	Reserved
AUTO	0	R	AUTO input latched-in status

Table 18. PSE-ICM Port Control Mapping

SLAVE[1:0]	PSE-ICM PORTS CONTROLLED
00	Slave device controls ports A, B, C, and D
01	Slave device controls ports E, F, G, and H
10	Slave device controls ports I, J, K, and L
11	Slave device controls ports M, N, O, and P

Configuration Registers (R12h–R17h)

Operating Mode Register (R12h)

The Operating Mode register in the device (R12h, Table 19) contains 2 bits per port that set the port mode of operation. Table 20 details how to set the mode of operation for the device. On a power-up or after a reset condition, if AUTO = 1, the Operating Mode register is set to a default value of FFh. If AUTO = 0, the Operating Mode register is set to 00h. Use software to program the mode of operation. The software port specific reset using RESET_P_ (R1Ah[3:0]), Table 27) does not affect the mode register.

Disconnect Enable Register (R13h)

The Disconnect Enable register (R13h, Table 21) is used to enable DC load disconnect detection. On power-up or after a reset condition, if AUTO = 1, this register is reset to a default value of F0h. If AUTO = 0, it is set to 00h. Setting either ACD_EN_ (R13h[7:4]) or DCD_EN _ (R13h[3:0]) to 1 enables the DC load disconnect detection feature on the corresponding port. To disable DC load disconnect on a port, both the ACD_EN_ and DCD_EN_ bit for that port must be set low.

Table 19. Operating Mode Register

ADDRESS = 12h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
P4_M[1:0]	7	R/W	MODE[1:0] for port 4
	6	R/W	
P3_M[1:0]	5	R/W	MODE[1:0] for port 3
	4	R/W	
P2_M[1:0]	3	R/W	MODE[1:0] for port 2
	2	R/W	
P1_M[1:0]	1	R/W	MODE[1:0] for port 1
	0	R/W	

Table 20. Port Operating Mode Status

MODE[1:0]	DESCRIPTION
00	Shutdown
01	Manual
10	Semiautomatic
11	Auto (automatic)

Table 21. Disconnect Enable Register

ADDRESS = 13h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
ACD_EN4	7	R/W	Enable DC disconnect detection on port 4
ACD_EN3	6	R/W	Enable DC disconnect detection on port 3
ACD_EN2	5	R/W	Enable DC disconnect detection on port 2
ACD_EN1	4	R/W	Enable DC disconnect detection on port 1
DCD_EN4	3	R/W	Enable DC disconnect detection on port 4
DCD_EN3	2	R/W	Enable DC disconnect detection on port 3
DCD_EN2	1	R/W	Enable DC disconnect detection on port 2
DCD_EN1	0	R/W	Enable DC disconnect detection on port 1

Detection and Classification Enable Register (R14h)

The Detection and Classification Enable register (R14h, Table 22) is used to enable detection and classification routines for the ports. On a power-up or after a reset condition, if AUTO = 1, this register is set to a default value of FFh. If AUTO = 0, it is set to 00h.

While in Auto and Semiautomatic mode, setting DET_EN_ (R14h[3:0]) and CLASS_EN_ (R14h[7:4]) to 1 enables load detection, and classification (upon successful detection) respectively. In manual mode, R14h works like a pushbutton register. Setting a bit high launches a single detection or classification cycle, and at the conclusion of the cycle the bit then clears. In SHDN mode, programming this register has no effect.

Midspan Enable Register (R15h)

The Midspan Enable register (R15h, Table 23) is used to control cadence timing (midspan) for the ports. On a power-up or after a reset condition, this register is set to a default value of 0000–XXXX where X is the latched-in value of the MIDSPAN input. Setting MIDSPAN_ (R15h[3:0]) to 1 enables cadence timing where the port backs off and waits at least 2s (min) after each failed load detection. The IEEE 802.3at/af standard requires a PSE that delivers power

Table 22. Detection and Classification Enable Register

ADDRESS = 14h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
CLASS_EN4	7	R/W	Enable classification on port 4
CLASS_EN3	6	R/W	Enable classification on port 3
CLASS_EN2	5	R/W	Enable classification on port 2
CLASS_EN1	4	R/W	Enable classification on port 1
DET_EN4	3	R/W	Enable detection on port 4
DET_EN3	2	R/W	Enable detection on port 3
DET_EN2	1	R/W	Enable detection on port 2
DET_EN1	0	R/W	Enable detection on port 1

Table 23. Midspan Enable Register

ADDRESS = 15h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
Reserved	7	—	Reserved
Reserved	6	—	Reserved
Reserved	5	—	Reserved
Reserved	4	—	Reserved
MIDSPAN4	3	R/W	Enable cadence timing on port 4
MIDSPAN3	2	R/W	Enable cadence timing on port 3
MIDSPAN2	1	R/W	Enable cadence timing on port 2
MIDSPAN1	0	R/W	Enable cadence timing on port 1

through the spare pairs (midspan) to have cadence timing (see the *Midspan Mode* section for details).

Reserved Register (R16h)

Register R16h is at this time reserved. Writing to this register has no effect (the address autoincrement still updates) and any attempt to read this register returns all zeroes.

Miscellaneous Configuration 1 Register (R17h)

The Miscellaneous Configuration 1 register (R17h, Table 24) is used for several functions that do not cleanly fit within one of the other configuration categories. On a power-up or after a reset condition, this register is set to a default value of A0h. Therefore, by default, INT_EN (R17h[7]) is set to 1 enabling $\overline{INT}$ functionality. If INT_EN is set to 0, interrupt signals are disabled and $\overline{INT}$ is set to a high-impedance state. If DET_CHG is set to 1, detect events are only be generated when the result is different from previous results (by default it is set to 0).

Pushbutton Registers (R18h–R1Ah)

Detection/Classification Pushbutton Register (R18h)

The Detection/Classification Pushbutton register (R18h, Table 25) is used as a pushbutton to set the corresponding bits in the Detection and Classification Enable register (R14h, Table 22). On a power-up or after a reset condition, this register is set to a default value of 00h.

Table 24. Miscellaneous Configuration 1 Register

ADDRESS = 17h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
INT_EN	7	R/W	A logic-high enables $\overline{INT}$ functionality
DET_CHG	6	R/W	A logic-high mandates detect events are only generated when the result changes
Reserved	5	—	Reserved
Reserved	4	—	Reserved
Reserved	3	—	Reserved
Reserved	2	—	Reserved
Reserved	1	—	Reserved
Reserved	0	—	Reserved

Table 25. Detection/Classification Pushbutton Register

ADDRESS = 18h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
CLS_PB4	7	R/W	Sets CLASS_EN4 in R14h to 1
CLS_PB3	6	R/W	Sets CLASS_EN3 in R14h to 1
CLS_PB2	5	R/W	Sets CLASS_EN2 in R14h to 1
CLS_PB1	4	R/W	Sets CLASS_EN1 in R14h to 1
DET_PB4	3	R/W	Sets DET_EN4 in R14h to 1
DET_PB3	2	R/W	Sets DET_EN3 in R14h to 1
DET_PB2	1	R/W	Sets DET_EN2 in R14h to 1
DET_PB1	0	R/W	Sets DET_EN1 in R14h to 1

Power-Enable Pushbutton Register (R19h)

The Power-Enable Pushbutton register (R19h, Table 26) is used to manually power a port on or off. On a power-up or after a reset condition, this register is set to a default value of 00h. Setting PWR_OFF_ (R19h[7:4]) to 1 turns off power to the corresponding port. PWR_OFF_ commands are ignored when the port is already off and during shutdown. In manual mode, setting PWR_ON_ (R19h[3:0]) to 1 turns on power to the corresponding port. PWR_ON_ commands are ignored in auto/semiautomatic mode, when the port is already powered, and during shutdown. After the appropriate command is executed (port power on or off), the register resets back to 00h.

Global Pushbutton Register (R1Ah)

The Global Pushbutton register (R1Ah, Table 27) is used to manually clear interrupts and to initiate global and port resets. On a power-up or after a reset condition, this register is set to a default value of 00h. Writing a 1 to INT_CLR (R1Ah[7]) clears all the event registers and the corresponding interrupt bits in the Interrupt register (R00h, Table 5). Writing a 1 to PIN_CLR (R1Ah[6]) clears the status of the $\overline{INT}$ output. RESET_IC (R1Ah[4]) causes a global software reset, after which all registers are set back to default values (after reset condition clears). Writing a 1 to RESET_P_ (R1Ah[3:0]) turns off power to the corresponding port and resets only the port status and event registers. If a port is powered when a RESET_P_ command is initiated, the port mode is also placed into SHDN, and the classification and detection enable bits are cleared. After the appropriate command is executed, the bits in the Global Pushbutton register all reset to 0.

Table 26. Power-Enable Pushbutton Register

ADDRESS = 19h			DESCRIPTION
SYMBOL	**BIT NO.**	**TYPE**	
PWR_OFF4	7	R/W	Power off port 4
PWR_OFF3	6	R/W	Power off port 3
PWR_OFF2	5	R/W	Power off port 2
PWR_OFF1	4	R/W	Power off port 1
PWR_ON4	3	R/W	Power on port 4
PWR_ON3	2	R/W	Power on port 3
PWR_ON2	1	R/W	Power on port 2
PWR_ON1	0	R/W	Power on port 1

Table 27. Global Pushbutton Register

ADDRESS = 1Ah			DESCRIPTION
SYMBOL	**BIT NO.**	**TYPE**	
INT_CLR	7	R/W	A logic-high clears all interrupts in event registers (R02h to R0bh)
PIN_CLR	6	R/W	A logic-high clears the $\overline{INT}$ pin
Reserved	5	—	Reserved
RESET_IC	4	R/W	A logic-high initiates a global device reset
RESET_P4	3	R/W	A logic-high resets port 4
RESET_P3	2	R/W	A logic-high resets port 3
RESET_P2	1	R/W	A logic-high resets port 2
RESET_P1	0	R/W	A logic-high resets port 1

General Registers (R1Bh–R1Fh)

ID Register (R1Bh)

The ID register (R1Bh, Table 28) keeps track of the device ID number and revision. The device's ID code is stored in ID_CODE[4:0] (R1Bh[7:3]) and is 11010. Contact the factory for the value of the revision code stored in REV[2:0] (R1Bh[2:0]) that corresponds to the device lot number.

Class 5 Enable Register (R1Ch)

The Class 5 Enable register (R1Ch, Table 29) is used to enable the classification of Class 5 devices. On a power-up or after a reset condition, if EN_CL5 = 0. this register is set to a default value of 00h. If EN_CL5 = 1, this register is set to 0Fh. Class 5 classification can be enabled or disabled individually for each port in auto mode by programming the corresponding bit directly using the software.

Reserved Register (R1Dh)

Register R1Dh is at this time reserved. Writing to this register is not recommended as it is internally connected. If the software needs to do a large batch write command using the address autoincrement function, write a code of 00h to this register to safely autoincrement past it, and then continue the write commands as normal.

Table 28. ID Register

ADDRESS = 1Bh			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
ID_CODE	7	R	ID_CODE[4]
	6	R	ID_CODE[3]
	5	R	ID_CODE[2]
	4	R	ID_CODE[1]
	3	R	ID_CODE[0]
REV	2	R	REV[2]
	1	R	REV[1]
	0	R	REV[0]

Table 29. Class 5 Enable Register

ADDRESS = 1Ch			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
Reserved	7	—	Reserved
Reserved	6	—	Reserved
Reserved	5	—	Reserved
Reserved	4	—	Reserved
CL5_EN4	3	R/W	Set to 1 to enable Class 5 classification on port 4
CL5_EN3	2	R/W	Set to 1 to enable Class 5 classification on port 3
CL5_EN2	1	R/W	Set to 1 to enable Class 5 classification on port 2
CL5_EN1	0	R/W	Set to 1 to enable Class 5 classification on port 1

TLIM Programming Registers (R1Eh and R1Fh)

The TLIM Programming registers (R1Eh/R1Fh, Table 30) are used to adjust the t_{LIM} current-limit timeout duration. On a power-up or after a reset condition, this register is set to a default value of 00h. When TLIM_[3:0] is set to 0000 the default t_{LIM} timeout is 60ms (typ). When set to any other value, the t_{LIM} timeout is set to 1.71ms times the decimal value of TLIM_[3:0].

Maxim Reserved Registers (R20h–R2Fh)

Maxim Reserved Registers (R20h–R28h, R2Ah–R2Fh)

These registers are reserved. Writing to these registers is not recommended as they are internally connected. If the software needs to do a large batch write command using the address autoincrement function, write a code of 0x00h to these registers to safely autoincrement past them, and then continue the write commands as normal.

Miscellaneous Configuration 2 Register (R29h)

The Miscellaneous Configuration 2 register (Table 31) is used for several functions that do not cleanly fit within one of the other configuration categories. On a power-up or after a reset condition, this register is set to a default value of 00h. When LSC_EN is set to 1, the load stability safety check is enabled and the detection phase is more immune to load variation. When VEE_R_ are set to 1, V_{EE} voltage conversion is enabled for the respective port, and the result overwrites the port voltage result in the corresponding port voltage registers.

Table 30. TLIM Programming Registers

ADDRESS = 1Eh/1Fh			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
TLIM2/4[3:0]	7	R/W	TLIM timer setting for port 2/4 (1Eh/1Fh)
	6	R/W	
	5	R/W	
	4	R/W	
TLIM1/3[3:0]	3	R/W	TLIM timer setting for port 1/3 (1Eh/1Fh)
	2	R/W	
	1	R/W	
	0	R/W	

Table 31. Miscellaneous Configuration 2 Register

ADDRESS = 29h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
Reserved	7	—	Reserved
Reserved	6	—	Reserved
Reserved	5	—	Reserved
LSC_EN	4	R/W	Set to 1 to enable the load stability safety check
VEE_R4	3	R/W	Enable V_{EE} voltage readout for port 4
VEE_R3	2	R/W	Enable V_{EE} voltage readout for port 3
VEE_R2	1	R/W	Enable V_{EE} voltage readout for port 2
VEE_R1	0	R/W	Enable V_{EE} voltage readout for port 1

Current/Voltage Readout Registers (R30h–R3Fh)

Port Current Registers (R30h, R31h, R34h, R35h, R38h, R39h, and R3Ch, R3Dh)

The Port Current registers (Tables 32 and 33) provide port current readout when a port is powered on. On a power-up or after a reset condition, these registers are both set to a default value of 00h. The Port Current Readout registers have 16 total bits, but the 3 highest bits (MSBs) and the 4 lowest bits (LSBs) are hardwired to 0. The port current readout has 9 bits of overall actual resolution. To avoid the LSB register changing while reading the MSB, the register contents are frozen if addressing byte points to either of the current readout registers. During normal operation, the port output current can be calculated as:

$$I_{OUT\_} = N_{IP\_} \times 122.07\mu A/count$$

where $N_{IP\_}$ is the decimal value of the 16-bit port current readout. The ADC saturates both at full scale and at zero, resulting in poor current readout accuracy near the top and bottom codes.

Table 32. Port Current Register (LSB)

ADDRESS = 30h, 34h, 38h, 3Ch			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
IP_[7:0]	7	R	IP_[7:0] (LSB). Lower 8 bits of the 16-bit port current readout. IP_[3:0] are configured to be hardwired to 0.
	6	R	
	5	R	
	4	R	
	3	R	
	2	R	
	1	R	
	0	R	

Table 33. Port Current Register (MSB)

ADDRESS = 31h, 35h, 39h, 3Dh			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
IP_[15:8]	7	R	IP_[15:8] (MSB). Lower 8 bits of the 16-bit port current readout. IP_[15:13] are configured to be hardwired to 0.
	6	R	
	5	R	
	4	R	
	3	R	
	2	R	
	1	R	
	0	R	

Port Voltage Registers (R32h, R33h, R36h, R37h, R3Ah, R3Bh, R3Eh, and R3Fh)

The Port Voltage registers (Tables 34 and 35) provide port voltage readout when a port is powered on. On a power-up or after a reset condition, these registers are both set to a default value of 00h. The Port Voltage Readout registers have 16 total bits, but the 2 highest bits (MSBs) and the 5 lowest bits (LSBs) are hardwired to 0. The port voltage readout has 9 bits of overall actual resolution. To avoid the LSB register changing while reading the MSB, the register contents are frozen if addressing byte points to either of the Voltage Readout registers. During normal operation, the port output voltage can be calculated as:

$$V_{OUT\_} = N_{VP\_} \times 5.835\text{mV/count}$$

where $N_{VP\_}$ is the decimal value of the 16-bit port voltage readout. The ADC saturates both at full scale and at zero, resulting in poor voltage readout accuracy near the top and bottom codes.

Other Functions Registers (R00h, R01h)

Reserved Registers (R40h, R45h, R4Ah, R4Fh, R54h, R59h, R5Ah, R5Bh, R5Ch, R5Dh, R5Eh, R5Fh)

These registers are at this time reserved. Writing to these registers will have no effect (the address autoincrement will still update) and any attempt to read these registers will return all zeroes.

Table 34. Port Voltage Register (LSB)

ADDRESS = 32h, 36h, 3Ah, 3Eh			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
VP_[7:0]	7	R	VP_[7:0] (LSB). Lower 8 bits of the 16-bit port current readout. VP_[4:0] are configured to be hardwired to 0.
	6	R	
	5	R	
	4	R	
	3	R	
	2	R	
	1	R	
	0	R	

Table 35. Port Voltage Register (MSB)

ADDRESS = 33h, 37h, 3Bh, 3Fh			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
VP_[15:8]	7	R	VP_[15:8] (MSB). Lower 8 bits of the 16-bit port current readout. VP_[15:13] are configured to be hardwired to 0.
	6	R	
	5	R	
	4	R	
	3	R	
	2	R	
	1	R	
	0	R	

Firmware Register (R41h)

The Firmware register (R41h) is at this time set by default set to 00h. This register is provided so that it can be reprogrammed as needed by the software to indicate the version of the device firmware.

Watchdog Register (R42h)

The Watchdog register (R42h, Table 36) is used to monitor device status, and to enable and monitor the watchdog functionality. On a power-up or after a reset condition, this register is set to a default value of 16h. V_{EE_OV} and V_{EE_UV} provide supply status independent of the Power Status register. WD_DIS[3:0] is set by default to 1011, disabling the watchdog timeout. Set WD_DIS[3:0] to any other value to enable the watchdog. The watchdog monitors the SCL line for activity. If there are no transitions for 2.5s (typ) the WDSTAT bit is set to 1 and all ports are powered down (using the individual port reset protocol). WD_STAT must be reset before any port can be reenabled.

Developer ID/Revision Number Register (R43h)

The Developer ID/Revision Number register (R43h, Table 37) is provided to allow developers using this device to assign the design an ID and revision version number unique to their software/design. On a power-up or after a reset condition, this register is set to a default value of 00h.

Table 36. Watchdog Register

ADDRESS = 42h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
Reserved	7	R/W	Reserved.
VEE_OV	6	R/W	VEE_OV is set if $V_{AGND} - V_{EE} > 62V$.
VEE_UV	5	R/W	VEE_UV is set if $V_{AGND} - V_{EE} < 40V$.
WD_DIS[3:0]	4	R/W	Watchdog Disable. When WD_DIS[3:0] is set to 1011 (default), the watchdog is disabled. Any other setting enables the watchdog.
	3	R/W	
	2	R/W	
	1	R/W	
WD_STAT	0	R/W	WD_STAT is set to 1 when the watchdog timer expires.

Table 37. Developer ID/Revision Number Register

ADDRESS = 43h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
DEV_ID[2:0]	7	R/W	Developer software-assigned ID number
	6	R/W	
	5	R/W	
Reserved	4	—	Reserved
Reserved	3	—	Reserved
DEV_REV[2:0]	2	R/W	Developer software-assigned revision number
	1	R/W	
	0	R/W	

High-Power Enable Register (R44h)

The High-Power Enable register (R44h, Table 38) is used to enable the high-power features on the ports. On power-up or after a reset condition, if AUTO = 1, this register is set to a default value of 0Fh. If AUTO = 0, it is set to 00h. Set HP_EN_ to 1 to enable the use of the high-power features found in R46h–R58h.

Port GPMD Register (R46h, R4Bh, R50h, and R55h)

The Port GPMD registers (Table 39) are used to enable the legacy high-capacitance PD detection and to enable 2-Event classification for the corresponding port. On a power-up or after a reset condition, these registers are set to a default value of 94h. The status of the LEGACY input on power-up or reset is latched into the LEG_EN_ bit. Set LEG_EN_ to 1 to enable, and 0 to disable, the legacy high-capacitance detection for the corresponding port. Set PONG_EN_ to 1 to enable, and 0 to disable, 2-Event classification.

Port Overcurrent Register (R47h, R4Ch, R51h, and R56h)

The Port ICUT registers (Table 40) are used to set the overcurrent SENSE_ voltage threshold for the corresponding port. On power-up or after a reset condition, if AUTO = 1, these registers are set to a default value of D4h. If AUTO = 0, it is set to 14h. To calculate the overcurrent setting, take decimal value of ICUT[5:0] multiplied times 37.5mA for CUTRNG = 0, and multiplied times 18.75mA for CUTRNG = 1 (default). Multiply the result by the value of the SENSE_ resistor (0.25Ω) to find the overcurrent SENSE_ voltage threshold. Double the resulting values when calculating Class 5 overcurrent thresholds.

Table 38. High-Power Enable Register

ADDRESS = 44h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
Reserved	7	R/W	Reserved
Reserved	6	R/W	Reserved
Reserved	5	R/W	Reserved
Reserved	4	R/W	Reserved
HP_EN4	3	R/W	Set to 1 to enable high-power features on port 4
HP_EN3	2	R/W	Set to 1 to enable high-power features on port 3
HP_EN2	1	R/W	Set to 1 to enable high-power features on port 2
HP_EN1	0	R/W	Set to 1 to enable high-power features on port 1

Table 39. Port GPMD Register

ADDRESS = 46h, 4Bh, 50h, 55h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
Reserved	7	R/W	Reserved
Reserved	6	R/W	Reserved
Reserved	5	R/W	Reserved
Reserved	4	R/W	Reserved
Reserved	3	R/W	Reserved
Reserved	2	R/W	Reserved
LEG_EN_	1	R/W	Set to 1 to enable legacy capacitance detection on the corresponding port
PONG_EN_	0	R/W	Set to 1 to enable 2-Event classification on the corresponding port

Port Current-Limit Register (R48h, R4Dh, R52h, and R57h)

The Port Current-Limit registers (Table 41) are used to set the current-limit SENSE_ voltage threshold for the corresponding port. On a power-up or after a reset condition, these registers are set to a default value of 80h. Bit 7 is hardwired to 1, while bits 5 to 0 are hardwired to 0. ILIM_ (bit 6) is set to 0 for a Class 0–3 PD, and to 1 for a Class 4 or 5 PD. The state of ILIM and the classification result (in the case of Class 5) determine the current limit (see the *Electrical Characteristics* table, V_{SU_LIM} for details).

Port High-Power Status Register (R49h, R4Eh, R53h, and R58h)

The Port High-Power Status registers (Table 42) are used to external FET failures and successful 2-Event classification results. On a power-up or after a reset condition, these registers are set to a default value of 00h. FET_BAD_ is set to 1 if the port is powered, there is no current-limit condition, and $V_{OUT\_}$ - V_{EE} > 2V. PONG_PD_ is set to 1 every time a successful 2-Event classification occurs on the corresponding port.

Table 40. Port Overcurrent Register

ADDRESS = 47h, 4Ch, 51h, 56h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
RDIS_	7	R/W	Sets the current-sense scale on the corresponding port; always set to 1
CUT_RNG_	6	R/W	ICUT is doubled when set to 0
ICUT_[5:0]	5	R/W	Sets the overcurrent SENSE_ voltage threshold (V_{CUT}) for the corresponding port
	4	R/W	
	3	R/W	
	2	R/W	
	1	R/W	
	0	R/W	

Table 41. Port Current-Limit Register

ADDRESS = 48h, 4Dh, 52h, 57h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
1	7	—	Hardwired to 1
ILIM_	6	R/W	Current-limit setting for the corresponding port
0	5	—	Hardwired to 0
0	4	—	
0	3	—	
0	2	—	
0	1	—	
0	0	—	

Table 42. Port High-Power Status Register

ADDRESS = 49h, 4Eh, 53h, 58h			DESCRIPTION
SYMBOL	BIT NO.	TYPE	
Reserved	7	R/W	Reserved
Reserved	6	R/W	Reserved
Reserved	5	R/W	Reserved
Reserved	4	R/W	Reserved
Reserved	3	R/W	Reserved
Reserved	2	R/W	Reserved
FET_BAD_	1	R/W	Set to 1 if a FET failure is detected on the corresponding port
PONG_PD_	0	R/W	Set to 1 when a 2-Event classification has occurred

Applications Information

Layout Procedure

Careful PCB layout is critical to achieve high efficiency and low EMI. Follow these layout guidelines for optimal performance:

1) Place the high-frequency input bypass capacitor (0.1µF ceramic capacitor from AGND to V_{EE}) and the output bypass capacitors (0.1µF ceramic capacitors from AGND to OUT_) as close to the device as possible.
2) Use large SMT component pads for power dissipating devices such as the MAX5980A and the external MOSFETs and sense resistors in the high-power path.
3) For the best accuracy current sensing, use Kelvin-sense techniques for the SENSE_ and SVEE_ inputs in the PCB layout. The device provides individual high-side SENSE_ inputs for each port, and two separate shared low-side sense returns, SVEE1 (ports 1 and 2 low-side sense input) and SVEE2 (ports 3 and 4 low-side sense input). The high-side sensing should be done from the end of the high-side sense resistor pad, and the SVEE_ pairs should be routed from the end of the low-side sense resistor pads. To minimize the impact from additional series resistance, the two end points should be as close as possible, and sense trace length should be minimized (see Figure 14 for a layout diagram, and refer to the MAX5980A Evaluation Kit for a design example).
4) Use short, wide traces whenever possible for high-power paths.
5) Use the MAX5980A Evaluation Kit as a design and layout reference.
6) The exposed pad (EP) must be soldered evenly to the PCB ground plane (V_{EE}) for proper operation and power dissipation. Use multiple vias beneath the exposed pad for maximum heat dissipation. A 1.0mm to 1.2mm pitch is the recommended spacing for these vias and they should be plated (1oz copper) with a small barrel diameter (0.30mm to 0.33mm).

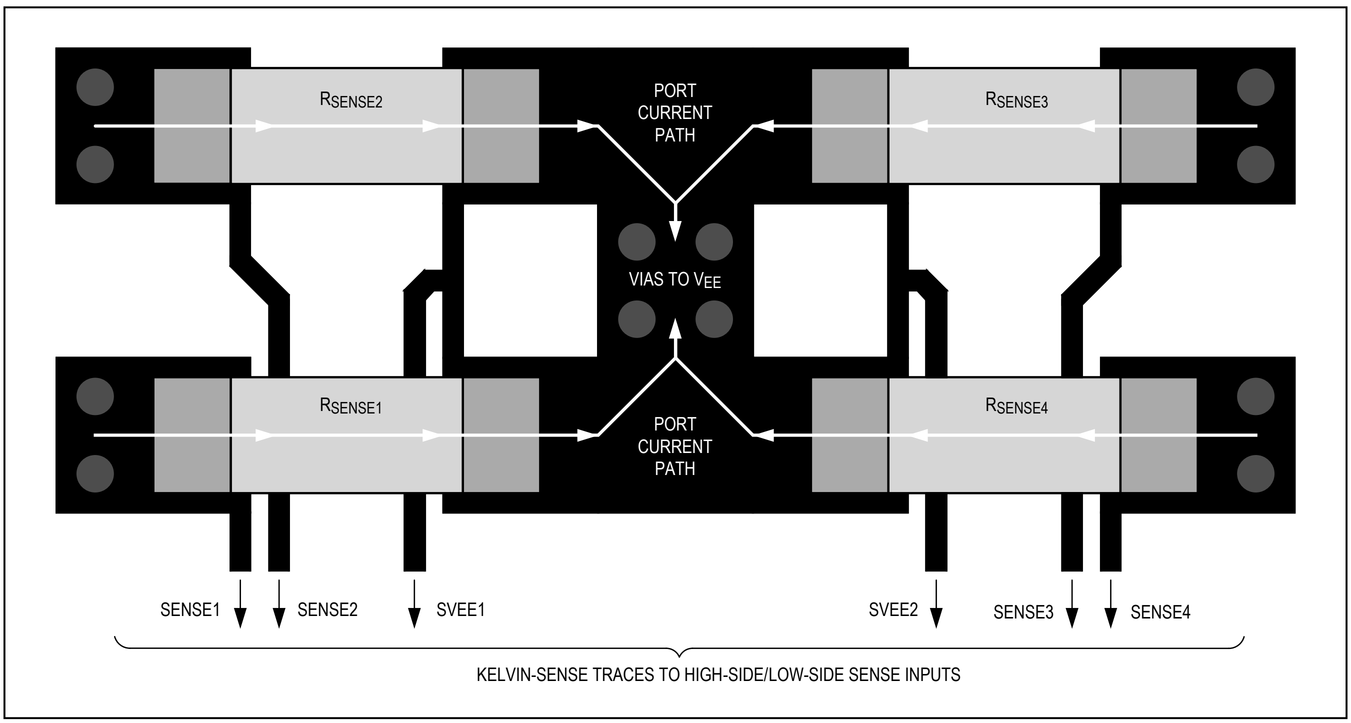
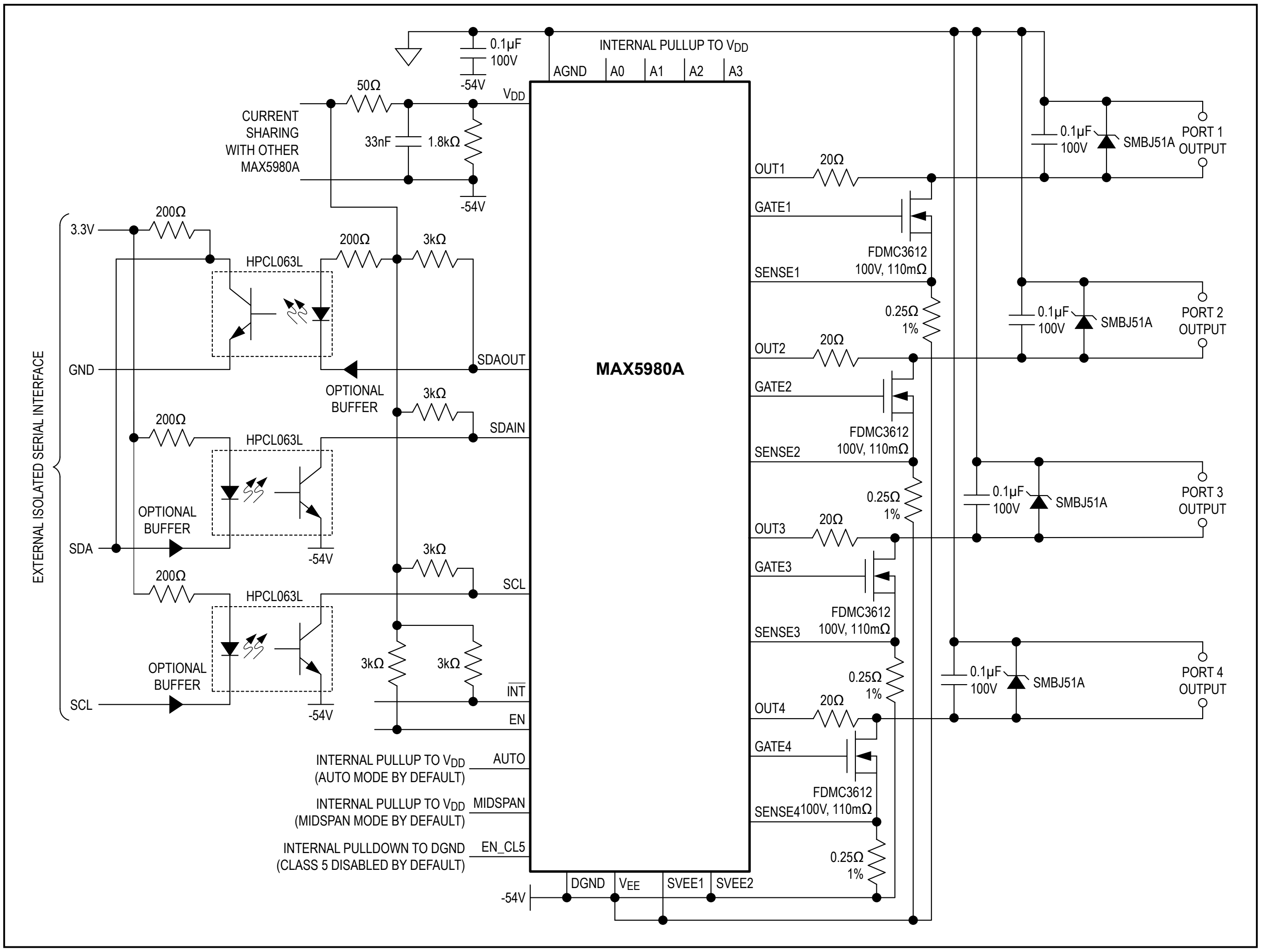


Figure 14. Kelvin-Sense Layout Diagram

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5980AGTJ+	-40°C to +105°C	32 TQFN-EP*

+Denotes lead(Pb)-free/RoHS-compliant package.

***EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+4	21-0140	90-0012

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/14	Initial release	—
1	4/15	Added application fix to *Pin Description* table and *Typical Operating Circuit*	12, 13, 49

