

FEATURES

- 5 MHz to 16 MHz external clock input rate
- 16 bits, no missing codes
- Signal-to-noise ratio (SNR): 88 dB typical
- Effective number of bits (ENOB): 14.2 bits typical
- Offset drift vs. temperature: 1.6 $\mu\text{V}/^\circ\text{C}$ typical
- On-board digital isolator
- On-board reference
- Full-scale analog input range: ± 320 mV
- High common-mode transient immunity: >25 kV/ μs
- Wide-body SOIC with increased creepage package
- Slew rate limited output for low EMI
- Safety and regulatory approvals**

UL recognition

- 5000 V rms for 1 minute per UL 1577
- CSA Component Acceptance Notice 5A
- VDE Certificate of Conformity
- DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
- $V_{\text{IORM}} = 1250 V_{\text{PEAK}}$

ENHANCED PRODUCT FEATURES

- Defense and aerospace applications (AQEC standard)
- Military temperature range: -55°C to $+125^\circ\text{C}$
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Shunt current monitoring
- AC motor controls
- Power and solar inverters
- Wind turbine inverters
- Data acquisition systems
- Analog-to-digital and optoisolator replacements

GENERAL DESCRIPTION

The AD7403-EP¹ is a high performance, second-order, Σ - Δ modulator that converts an analog input signal into a high speed, single-bit data stream, with on-chip digital isolation based on Analog Devices, Inc., iCoupler[®] technology. The device operates from a 5 V (V_{DD1}) power supply and accepts a differential input signal of ± 250 mV (± 320 mV full-scale). The differential input is ideally suited to shunt voltage monitoring in high voltage applications where galvanic isolation is required.

¹ Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

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FUNCTIONAL BLOCK DIAGRAM

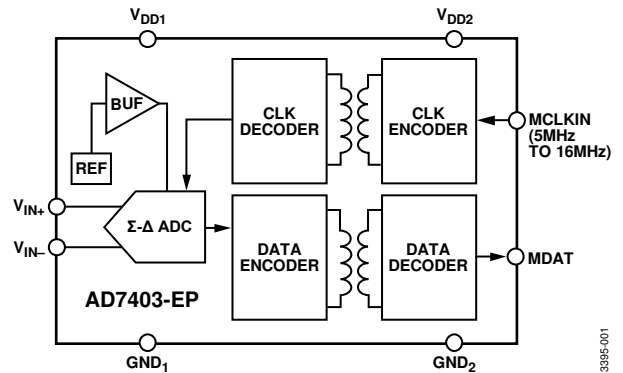


Figure 1.

13395-001

The analog input is continuously sampled by a high performance analog modulator, and converted to a one's density digital output stream with a data rate of up to 16 MHz. The original information can be reconstructed with an appropriate digital filter to achieve 88 dB signal to noise ratio (SNR) at 78.1 kSPS.

The serial interface is digitally isolated. High speed complementary metal oxide semiconductor (CMOS) technology, combined with monolithic transformer technology, means the on-chip isolation provides outstanding performance characteristics, superior to alternatives such as optocoupler devices. The AD7403-EP device is offered in a 16-lead, wide-body SOIC package and has an operating temperature range of -55°C to $+125^\circ\text{C}$.

Additional application and technical information can be found in the AD7403 data sheet.

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REVISION HISTORY

4/16—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD1} = 4.5\text{ V to }5.5\text{ V}$, $V_{DD2} = 4.5\text{ V to }5.5\text{ V}$, $V_{IN+} = -250\text{ mV to }+250\text{ mV}$, $V_{IN-} = 0\text{ V}$, $T_A = -55^\circ\text{C to }+125^\circ\text{C}$, $f_{MCLKIN} = 5\text{ MHz to }16\text{ MHz}$, tested with sinc3 filter, 256 decimation rate, as defined by Verilog code, unless otherwise noted. All voltages are relative to their respective ground.

Table 1.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|----------------------|--------------|----------------------|--------|--|
| STATIC PERFORMANCE | | | | | |
| Resolution | 16 | | | Bits | Filter output truncated to 16 bits |
| Integral Nonlinearity (INL) ¹ | | ±2 | ±12 | LSB | |
| Differential Nonlinearity (DNL) ¹ | | | ±0.99 | LSB | Guaranteed no missed codes to 16 bits |
| Offset Error ¹ | | ±0.2 | ±0.9 | mV | |
| Offset Drift vs. Temperature ² | | 1.6 | 3.8 | μV/°C | |
| | | 1.3 | 3.1 | μV/°C | 0°C to 85°C |
| Offset Drift vs. V_{DD1} ² | | 50 | | μV/V | |
| Gain Error ¹ | | ±0.2 | ±0.95 | % FSR | |
| Gain Error Drift vs. Temperature ² | | 65 | 95 | ppm/°C | |
| | | 40 | 60 | μV/°C | |
| Gain Error Drift vs. V_{DD1} ² | | ±0.6 | | mV/V | |
| ANALOG INPUT | | | | | |
| Input Voltage Range | -320 | | +320 | mV | Full-scale range |
| | -250 | | +250 | mV | For specified performance |
| Input Common-Mode Voltage Range | | -200 to +300 | | mV | |
| Dynamic Input Current | | ±45 | ±50 | μA | $V_{IN+} = \pm 250\text{ mV}$, $V_{IN-} = 0\text{ V}$ |
| | | 0.05 | | μA | $V_{IN+} = 0\text{ V}$, $V_{IN-} = 0\text{ V}$ |
| DC Leakage Current | | ±0.01 | ±0.6 | μA | |
| Input Capacitance | | 14 | | pF | |
| DYNAMIC SPECIFICATIONS¹ | | | | | |
| Signal-to-Noise-and-Distortion Ratio (SINAD) | 82 | 87 | | dB | $V_{IN+} = 1\text{ kHz}$ |
| Signal-to-Noise Ratio (SNR) | 86 | 88 | | dB | |
| Total Harmonic Distortion (THD) | | -94 | | dB | |
| Peak Harmonic or Spurious Noise (SFDR) | | -95 | | dB | |
| Effective Number of Bits (ENOB) | 13.1 | 14.2 | | Bits | |
| Noise Free Code Resolution | 14 | | | Bits | |
| ISOLATION TRANSIENT IMMUNITY¹ | | | | | |
| | 25 | 30 | | kV/μs | |
| LOGIC INPUTS | | | | | |
| Input Voltage | | | | | CMOS with Schmitt trigger |
| High (V_{IH}) | $0.8 \times V_{DD2}$ | | | V | |
| Low (V_{IL}) | | | $0.2 \times V_{DD2}$ | V | |
| Input Current (I_{IN}) | | | ±0.6 | μA | |
| Input Capacitance (C_{IN}) | | | 10 | pF | |
| LOGIC OUTPUTS | | | | | |
| Output Voltage | | | | | |
| High (V_{OH}) | $V_{DD2} - 0.1$ | | | V | $I_O = -200\text{ μA}$ |
| Low (V_{OL}) | | | 0.4 | V | $I_O = 200\text{ μA}$ |
| POWER REQUIREMENTS | | | | | |
| V_{DD1} | 4.5 | | 5.5 | V | |
| V_{DD2} | 4.5 | | 5.5 | V | |
| I_{DD1} | | 30 | 36 | mA | $V_{DD1} = 5.5\text{ V}$ |
| I_{DD2} | | 12 | 18 | mA | $V_{DD2} = 5.5\text{ V}$ |
| Power Dissipation | | 231 | 297 | mW | $V_{DD1} = V_{DD2} = 5.5\text{ V}$ |

¹ See the Terminology section of the AD7403 datasheet.

² Not production tested. Sample tested during initial release to ensure compliance.

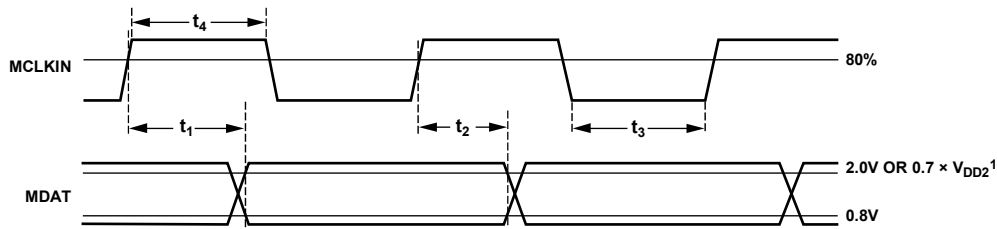
TIMING SPECIFICATIONS

$V_{DD1} = 4.5\text{ V to }5.5\text{ V}$, $V_{DD2} = 4.5\text{ V to }5.5\text{ V}$, $T_A = -55^\circ\text{C to }+125^\circ\text{C}$, unless otherwise noted. Sample tested during initial release to ensure compliance. It is recommended to read MDAT on the MCLKIN rising edge.

Table 2.

| Parameter | Limit at T_{MIN} , T_{MAX} | | | Unit | Description |
|--------------|--------------------------------|-----|-----|------|---|
| | Min | Typ | Max | | |
| f_{MCLKIN} | 5 | | 16 | MHz | Master clock input frequency |
| t_1^1 | | | 45 | ns | Data access time after MCLKIN rising edge |
| t_2^1 | 12 | | | ns | Data hold time after MCLKIN rising edge |
| t_3 | $0.45 \times t_{MCLKIN}$ | | | ns | Master clock low time |
| t_4 | $0.45 \times t_{MCLKIN}$ | | | ns | Master clock high time |

¹ Defined as the time required from an 80% MCLKIN input level to when the output crosses 0.8 V or 2.0 V for $V_{DD2} = 3\text{ V to }3.6\text{ V}$ or when the output crosses 0.8 V or $0.7 \times V_{DD2}$ for $V_{DD2} = 4.5\text{ V to }5.5\text{ V}$ as outlined in Figure 2. Measured with a $\pm 200\ \mu\text{A}$ load and a 25 pF load capacitance.



¹SEE NOTE 1 OF TABLE 3 FOR FURTHER DETAILS.

Figure 2. Data Timing

133895-002

PACKAGE CHARACTERISTICS

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------------------|-----|------------------|-----|------|---|
| Resistance (Input to Output) ¹ | R _{I-O} | | 10 ¹² | | Ω | |
| Capacitance (Input to Output) ¹ | C _{I-O} | | 2.2 | | pF | f = 1 MHz |
| IC Junction to Ambient Thermal Resistance | θ _{JA} | | 45 | | °C/W | Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces |

¹ The device is considered a 2-terminal device. For AD7403-EP, Pin 1 to Pin 8 are shorted together and Pin 9 to Pin 16 are shorted together.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4.

| Parameter | Symbol | Value | Unit | Test Conditions/Comments |
|--|------------------|-------------------------|------|--|
| Input to Output Momentary Withstand Voltage | V _{ISO} | 5000 min | V | 1 minute duration |
| Minimum External Air Gap (Clearance) | L(I01) | 8.3 min ^{1, 2} | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 8.3 min ¹ | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.034 min | mm | Distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | V | DIN IEC 112/VDE 0303 Part 1 ³ |
| Isolation Group | | II | | Material Group (DIN VDE 0110, 1/89, Table I) ³ |

¹ In accordance with IEC 60950-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

² Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

³ CSA CTI rating for the AD7403-EP is >575 V and therefore Material Group II isolation group.

REGULATORY INFORMATION

Table 5.

| UL ¹ | CSA | VDE ² |
|--|--|---|
| Recognized under 1577 Component Recognition Program ¹ | Approved under CSA Component Acceptance Notice 5A | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ² |
| 5000 V rms Isolation Voltage Single Protection | Basic insulation per CSA 60950-1-07 and IEC 60950-1, 830 V rms (1173 V _{PEAK}), maximum working voltage ³ Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 415 V rms (586 V _{PEAK}) maximum working voltage ³ Reinforced insulation per IEC 60601-1, 250 V rms (353 V _{PEAK}) maximum working voltage | Reinforced insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, 1250 V _{PEAK} |
| File E214100 | File 205078 | File 2471900-4880-0001 |

¹ In accordance with UL 1577, each AD7403-EP is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 15 μA).

² In accordance with DIN V VDE V 0884-10, each AD7403-EP is proof tested by applying an insulation test voltage ≥ 2344 V_{PEAK} for 1 second (partial discharge detection limit = 5 pC).

³ Rating is calculated for a pollution degree of 2 and a Material Group III. The AD7403-EP RI-16-2 package material is rated by CSA to a CTI of >575 V and therefore Material Group II.

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

Table 6.

| Description | Symbol | Characteristic | Unit |
|--|-----------------------------------|--|--|
| INSTALLATION CLASSIFICATION PER DIN VDE 01 10 For Rated Mains Voltage ≤300 V rms For Rated Mains Voltage ≤450 V rms For Rated Mains Voltage ≤600 V rms For Rated Mains Voltage ≤1000 V rms | | I to IV I to IV I to IV I to IV | |
| CLIMATIC CLASSIFICATION | | 40/105/21 | |
| POLLUTION DEGREE (DIN VDE 01 10, TABLE 1) | | 2 | |
| MAXIMUM WORKING INSULATION VOLTAGE | V _{IORM} | 1250 | V _{PEAK} |
| INPUT TO OUTPUT TEST VOLTAGE, METHOD B1 V _{IORM} × 1.875 = V _{PR} , 100% Production Test, t _m = 1 Second, Partial Discharge < 5 pC | V _{PD(M)} | 2344 | V _{PEAK} |
| INPUT TO OUTPUT TEST VOLTAGE, METHOD A After Environmental Test Subgroup 1 V _{IORM} × 1.6 = V _{PR} , t _m = 60 Seconds, Partial Discharge < 5 pC After Input and/or Safety Test Subgroup 2/ Safety Test Subgroup 3 V _{IORM} × 1.2 = V _{PR} , t _m = 60 Seconds, Partial Discharge < 5 pC | V _{PR(M)} | 2000 1500 | V _{PEAK} V _{PEAK} |
| HIGHEST ALLOWABLE OVERVOLTAGE (TRANSIENT OVERVOLTAGE, t _{TR} = 10 Seconds) | V _{IOTM} | 8000 | V _{PEAK} |
| SURGE ISOLATION VOLTAGE 1.2 μs Rise Time, 50 μs, 50% Fall Time | V _{IOSM} | 7500 | V _{PEAK} V _{PEAK} |
| SAFETY LIMITING VALUES (MAXIMUM VALUE ALLOWED IN THE EVENT OF A FAILURE, SEE Figure 3) Case Temperature Side 1 (P _{VDD1}) and Side 2 (P _{VDD2}) Power Dissipation | T _S P _{SO} | 150 2.78 | °C W |
| INSULATION RESISTANCE AT T _S , V _{IO} = 500 V | R _{IO} | >10 ⁹ | Ω |

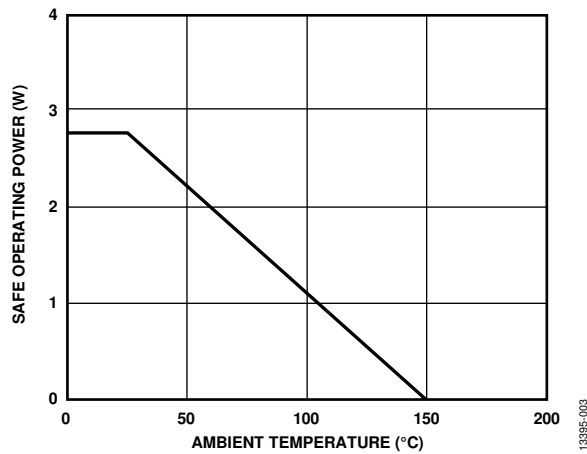


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted. All voltages are relative to their respective ground.

Table 7.

| Parameter | Rating |
|---|---|
| V_{DD1} to GND_1 | -0.3 V to +6.5 V |
| V_{DD2} to GND_2 | -0.3 V to +6.5 V |
| Analog Input Voltage to GND_1 | -1 V to $V_{DD1} + 0.3$ V |
| Digital Input Voltage to GND_2 | -0.3 V to $V_{DD2} + 0.5$ V |
| Output Voltage to GND_2 | -0.3 V to $V_{DD2} + 0.3$ V |
| Input Current to Any Pin Except Supplies ¹ | ± 10 mA |
| Operating Temperature Range | -55°C to $+125^\circ\text{C}$ |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Junction Temperature | 150°C |
| Pb-Free Temperature, Soldering | |
| Reflow | 260°C |
| ESD | 2 kV |
| FICDM ² | ± 1250 V |
| HBM ³ | ± 4000 V |

¹ Transient currents of up to 100 mA do not cause SCR to latch up.

² JESD22-C101; RC network: 1 Ω , Cpkg; Class: IV.

³ ESDA/JEDEC JS-001-2011; RC network: 1.5 k Ω , 100 pF; Class: 3A.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 8. Maximum Continuous Working Voltage¹

| Parameter | Max | Unit | Constraint |
|-------------------|------|------------|---|
| AC Voltage | | | |
| Bipolar Waveform | 1250 | V_{PEAK} | 20-year minimum lifetime (VDE approved working voltage) |
| Unipolar Waveform | 1250 | V_{PEAK} | 20-year minimum lifetime |
| DC Voltage | 1250 | V_{PEAK} | 20-year minimum lifetime |

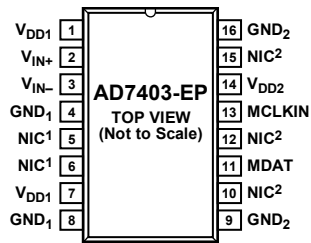
¹ Maximum continuous working voltage refers to continuous voltage magnitude imposed across the isolation barrier.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



¹NIC = NOT INTERNALLY CONNECTED. CONNECT TO V_{DD1} , GND_1 , OR LEAVE FLOATING.
²NIC = NOT INTERNALLY CONNECTED. CONNECT TO V_{DD2} , GND_2 , OR LEAVE FLOATING.

13395-004

Figure 4. Pin Configuration

Table 9. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|------------|-----------|---|
| 1, 7 | V_{DD1} | Supply Voltage, 4.5 V to 5.5 V. This is the supply voltage for the isolated side of the AD7403-EP and is relative to GND_1 . For device operation, connect the supply voltage to both Pin 1 and Pin 7. Decouple each supply pin to GND_1 with a 10 μ F capacitor in parallel with a 1 nF capacitor. |
| 2 | V_{IN+} | Positive Analog Input. |
| 3 | V_{IN-} | Negative Analog Input. Normally connected to GND_1 . |
| 4, 8 | GND_1 | Ground 1. This pin is the ground reference point for all circuitry on the isolated side. |
| 5, 6 | NIC | Not Internally Connected. These pins are not internally connected. Connect to V_{DD1} , GND_1 , or leave floating. |
| 9, 16 | GND_2 | Ground 2. This pin is the ground reference point for all circuitry on the nonisolated side. |
| 10, 12, 15 | NIC | Not Internally Connected. These pins are not internally connected. Connect to V_{DD2} , GND_2 , or leave floating. |
| 11 | MDAT | Serial Data Output. The single bit modulator output is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the MCLKIN input and are valid on the following MCLKIN rising edge. |
| 13 | MCLKIN | Master Clock Logic Input. 5 MHz to 20 MHz frequency range. The bit stream from the modulator is propagated on the rising edge of the MCLKIN. |
| 14 | V_{DD2} | Supply Voltage, 3 V to 5.5 V. This is the supply voltage for the nonisolated side and is relative to GND_2 . Decouple this supply to GND_2 with a 100 nF capacitor. |

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD1} = 5\text{ V}$, $V_{DD2} = 5\text{ V}$, $V_{IN+} = -250\text{ mV}$ to $+250\text{ mV}$, $V_{IN-} = 0\text{ V}$, $f_{MCLKIN} = 16\text{ MHz}$, using a sinc3 filter with a 256 oversampling ratio (OSR), unless otherwise noted.

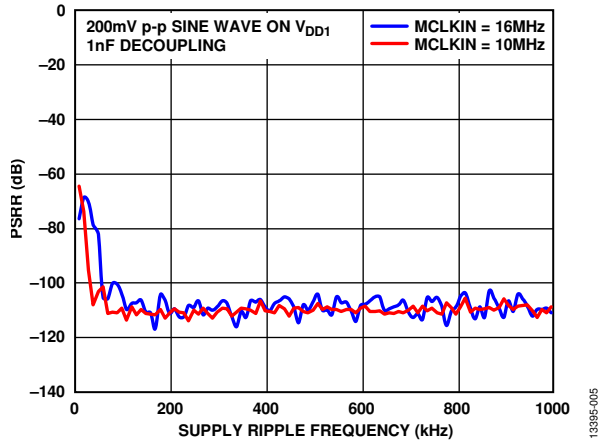


Figure 5. PSRR vs. Supply Ripple Frequency

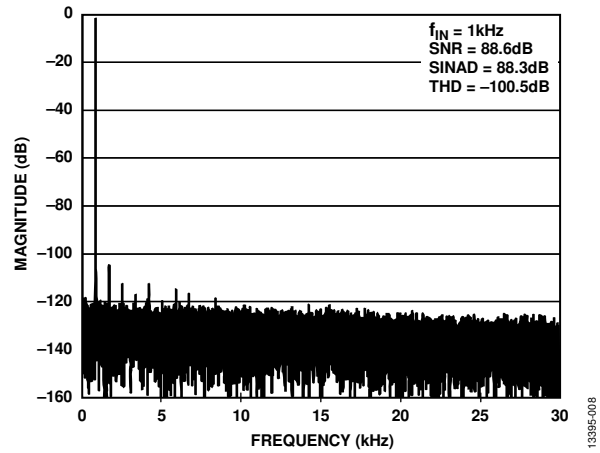


Figure 8. Typical Fast Fourier Transform (FFT)

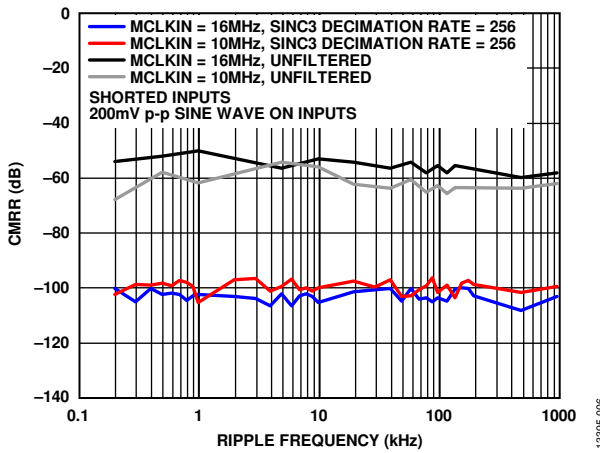


Figure 6. CMRR vs. Common-Mode Ripple Frequency

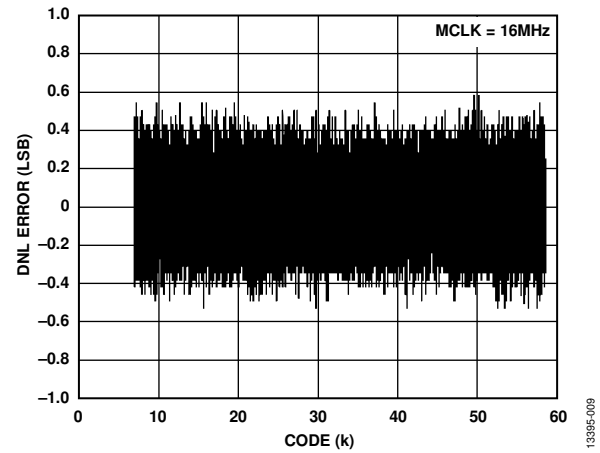


Figure 9. Typical DNL Error

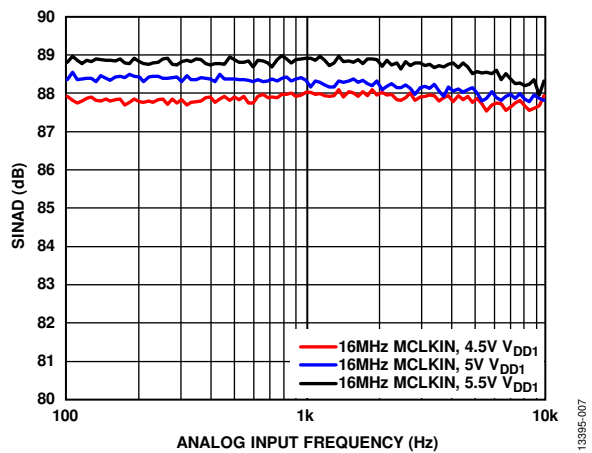


Figure 7. SINAD vs. Analog Input Frequency

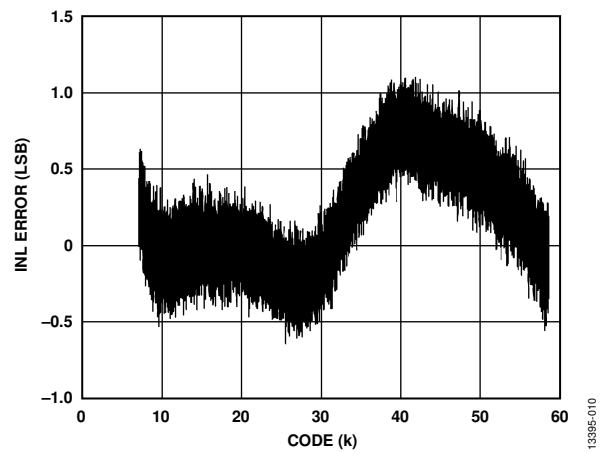


Figure 10. Typical INL Error

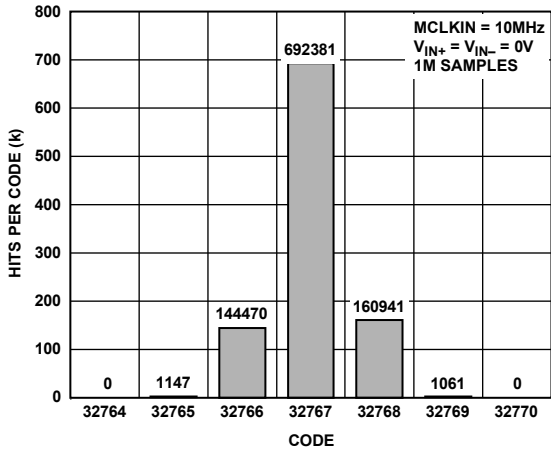


Figure 11. Histogram of Codes at Code Center

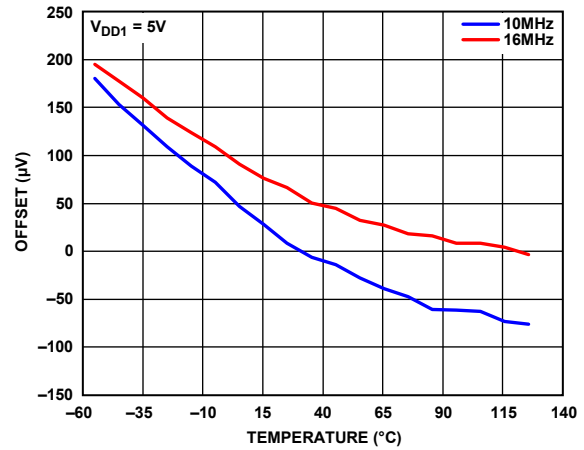


Figure 14. Offset vs. Temperature

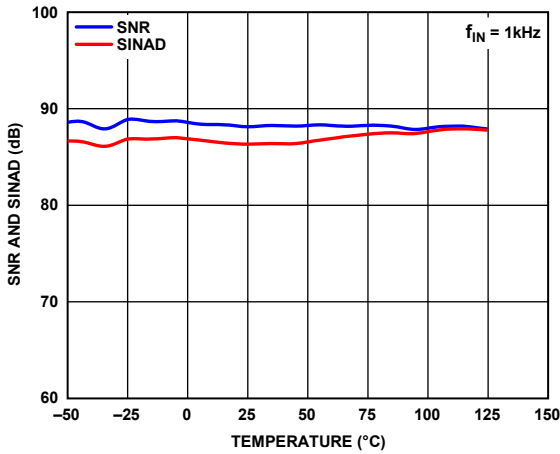


Figure 12. SNR and SINAD vs. Temperature

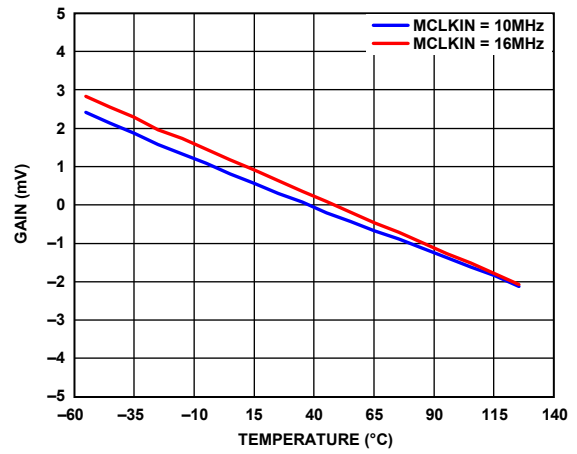


Figure 15. Gain Error vs. Temperature

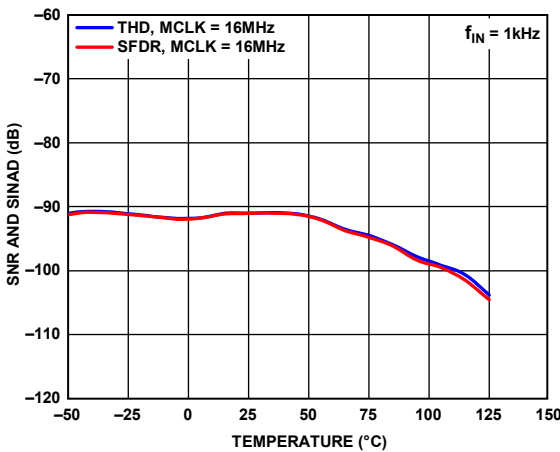


Figure 13. THD and SFDR vs. Temperature

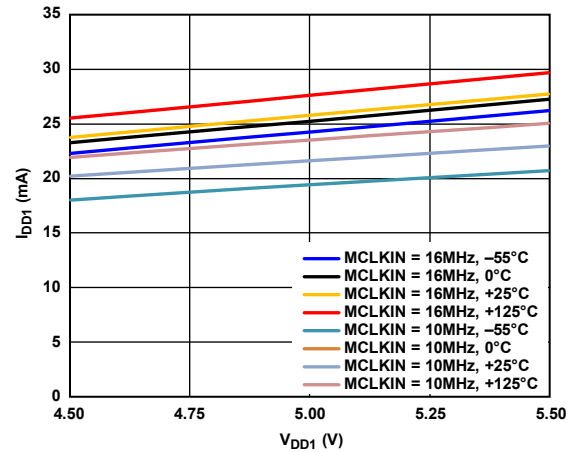


Figure 16. I_{DD1} vs. V_{DD1} at Various Temperatures and Clock Rates

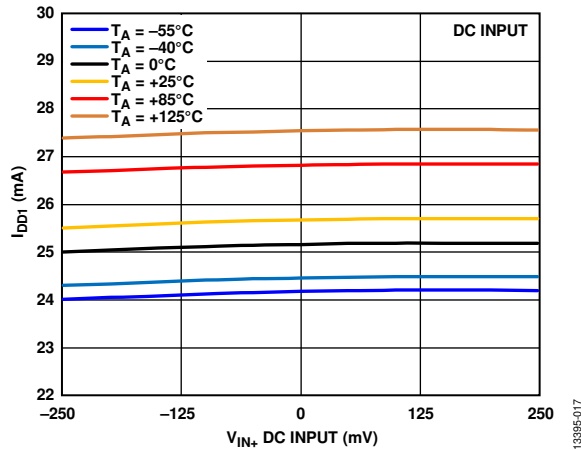


Figure 17. I_{DD1} vs. V_{IN+} DC Input at Various Temperatures

13395-017

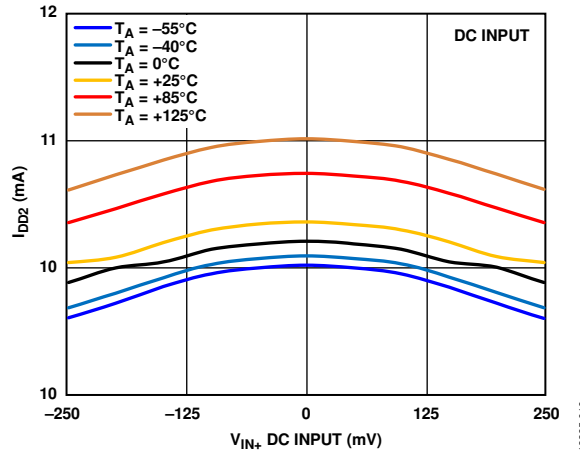


Figure 19. I_{DD2} vs. V_{IN+} DC Input at Various Temperatures

13395-019

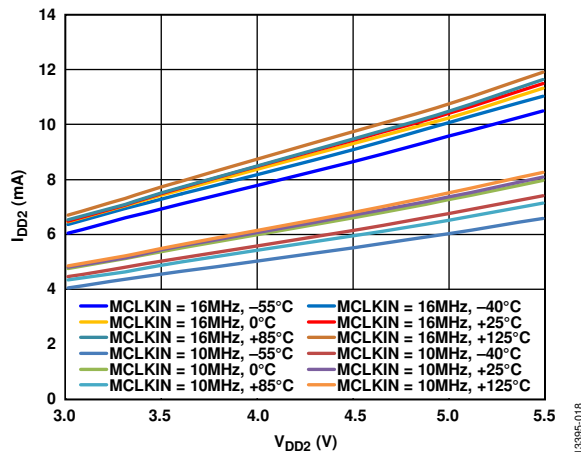


Figure 18. I_{DD2} vs. V_{DD2} at Various Temperatures and Clock Rates

13395-018

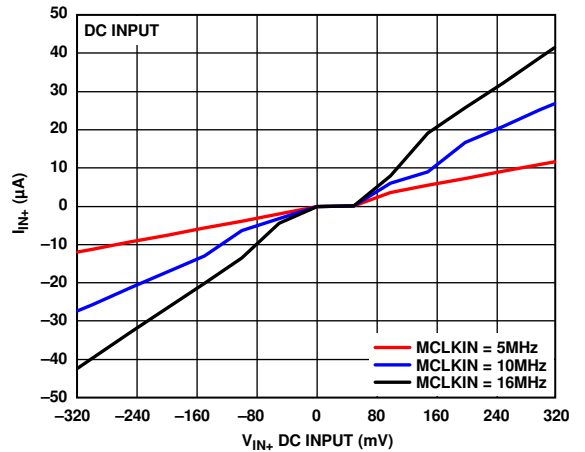
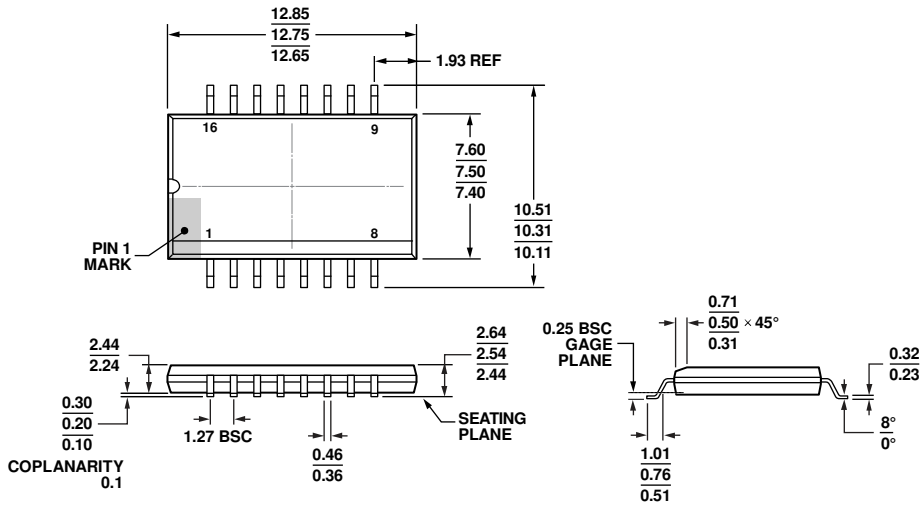


Figure 20. I_{IN+} vs. V_{IN+} DC Input at Various Clock Rates

13395-020

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AC
 Figure 21. 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
 Wide Body
 (RI-16-2)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| AD7403TRIZ-EP | -55°C to +125°C | 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC] | RI-16-2 |
| AD7403TRIZ-EP-RL7 | -55°C to +125°C | 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC] | RI-16-2 |
| EVAL-AD7403FMCZ | | AD7403 Evaluation Board | |
| EVAL-SDP-CH1Z | | System Demonstration Platform | |

¹ Z = RoHS Compliant Part.