HIP0080, HIP0081

Quad Inverting Power Drivers with Serial Diagnostic Interface

FN3018
Rev 5.00
November 2000

The HIP0080/0081 Quad Power Drivers contain four individually protected NDMOS power output transistor switches to drive inductive and resistive loads such as: relays, solenoids, injectors, AC and DC motors, heaters and incandescent lamp displays. The 4 Power Drivers are low-side switches driven by CMOS logic input control stages. Each Output Power Driver is protected against over-current, over-temperature and over-voltage. An internal drain-to-gate zener diode provides the clamping protection for over-voltage. Diagnostic circuits provide ground short, supply short, open load and thermal overload detection for each of the 4 output stages. Each of the 4 input drivers and their respective diagnostic filters are controlled by one ENABLE input.

The inputs are CMOS logic compatible and individually control the output drivers with an active high state for turn-on. All other control inputs are active high with the exception of the Chip Select ($\overline{CS}$) which is active low. The DATAIN (DI) and DATAOUT (DO) are positive logic and the Clock (CLK) input for the Serial Interface is active on the rising edge of the CLK pulse. All Inputs except the HIP0080 ENABLE have a nominal level of hysteresis. IN1, IN2, IN3, IN4 and ENABLE have pull-down resistors of approximately 100kΩ. This switches off any channel that has an unterminated input.

Filters are used on the outputs of the fault sensing comparators to avoid the detection of short duration transient spikes. The on-chip oscillator is used to clock an internal shift register in each filter. If the fault condition is longer than a preset number of clock cycles, the fault condition is recognized and the respective bit is set in the diagnostic register. No filter is used in the thermal-overload feedback circuit and the bit is set when thermal shutdown occurs.

For normal operating conditions, a Reset turns off all outputs when the V_{CC} level drops below 3.5V. The internal bandgap and bias supply function includes a 5V regulated supply for the low voltage signal and logic circuits.

Features

- Low Side Power MOSFET Output Drivers
- Output Driver Protection
  - Over-Current Shutdown
  - Over-Temperature Shutdown with Hysteresis
  - Over-Voltage Internal Clamp
- HIP0081 Output Current Switching Capability:
  - Each Output, I_{OUT} . . . . . 2.2A DC
  - All Outputs ON, Equal I_{OUT} . . . . . .6A DC
  - All Outputs ON, Equal I_{OUT} . . . . . 8A PK, 500ms
- HIP0080 Output Current Switching Capability:
  - Each Output, I_{OUT} . . . . . 1.3A DC
  - All Outputs ON, Unequal I_{OUT} . . . . . .3A DC
  - All Outputs ON, Unequal I_{OUT} . . . . . 4A PK, 500ms
- HIP0080 - Low Idle Current Shutdown Mode
- Regulated Interface for 5V CMOS Logic Inputs
- Open Drain High Z DATAOUT
- Fault Mode Output for Shorts, Opens and Over-Temperature
- 16-Bit Serial Diagnostic Register
- SPI Bus Compatible Data Readout
- HIP0081 - Low θ_{JC} Power Package . . . . . $3^oC/W$
- -40^oC to 125^oC Operating Temperature Range

Applications

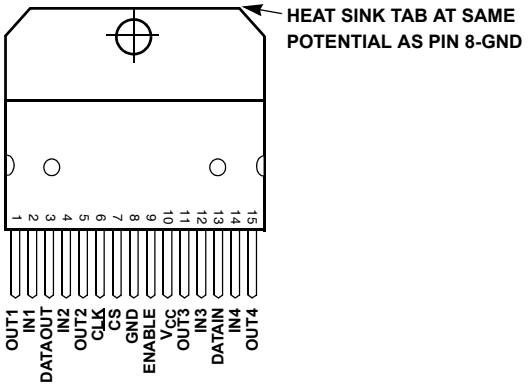
- Drivers For:
  - Solenoids
  - Relays
  - Power Output
  - Lamps
  - Injectors
  - Steppers
  - Motors
  - Displays
- System Use:
  - Automotive
  - Appliances
  - Industrial
  - Robotics

Ordering Information

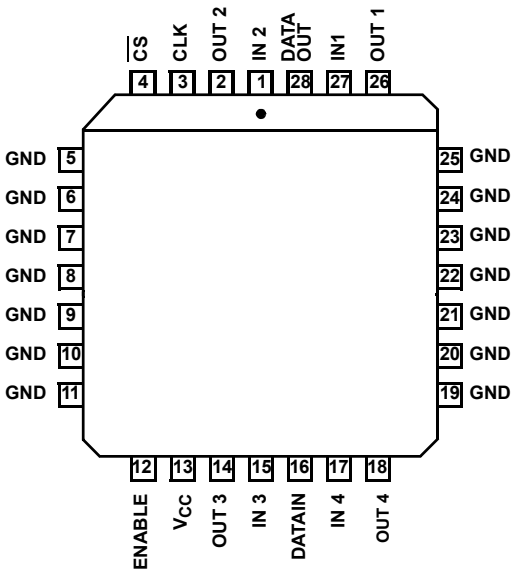
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HIP0081AS1	-40 to 125	15 Ld SIP	Z15.05A
HIP0081AS2	-40 to 125	15 Ld SIP	Z15.05B
HIP0080AM	-40 to 125	28 Ld PLCC	N28.45

Pinouts

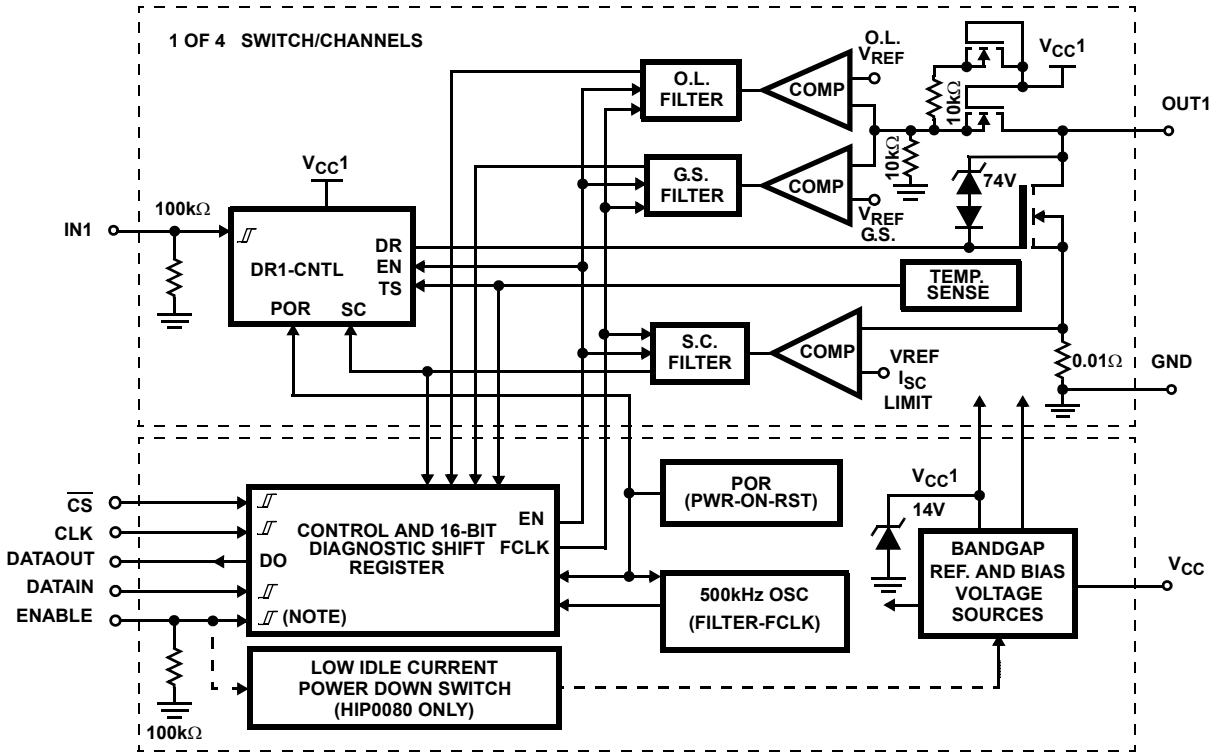
HIP0081 (SIP)
TOP VIEW



HIP0080 (PLCC)
TOP VIEW

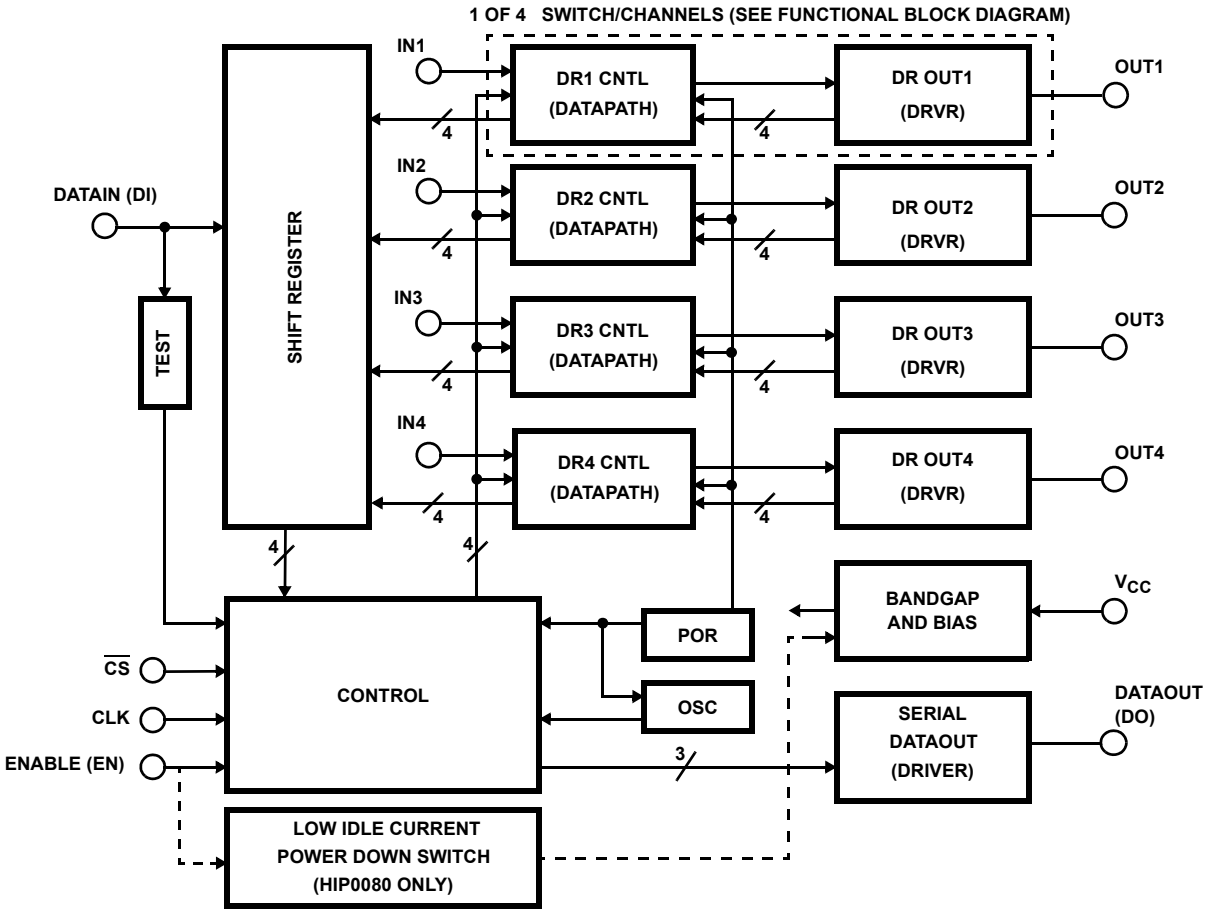


Functional Block Diagram



NOTE: HIP0080 - No enable hysteresis.

Functional Signal Flow Diagram



Absolute Maximum Ratings

Supply Voltage (Logic and Control), V_{CC} . . . . . -16 to 45V
Power MOSFET Drain Voltage, V_O (Note 1) . . . . . -0.5 to V_{CLAMP}
Maximum Output Clamp Energy, E_{OK} (HIP0080) . . . . . Note 4
Maximum Output Clamp Energy, E_{OK} (HIP0081) . . . . . Note 4
Input Voltage (Logic and Driver Inputs), V_{IN} . . . . . -0.5 to 7V
Output Voltage, DATAOUT . . . . . -0.5 to 7V
HIP0080 Output Current
- Each Output, $I_{OUT(PEAK)}$, (Note 2) . . . . . -1.5A to $I_{OUT(SC)}$
- Each Output, $I_{OUT(DC)}$ . . . . . +1.3A
- Total of 4 Outputs ON, Unequal I_{OUT} . . . . . +3A
- Total of 4 Outputs ON, Unequal I_{OUT} . . . . . +4A/500ms (Max)

HIP0081 Output Current
- Each Output, $I_{OUT(PEAK)}$, (Note 2) . . . . . -2 to $I_{OUT(SC)}$
- Each Output, $I_{OUT(DC)}$ . . . . . +2.2A
- Total of 4 Outputs, ON, Unequal I_{OUT} . . . . . +6A
- Total of 4 Outputs ON, Unequal I_{OUT} . . . . . +8A/500ms (Max)

Operating Conditions

Ambient Temperature Range . . . . . -40^oC to 125^oC
Junction Temperature Range . . . . . -40^oC to 150^oC

Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}(^oC/W)$	$\theta_{JC}(^oC/W)$
HIP0080	43	N/A
HIP0080 (on 2 sq. in. PC Board)	33	N/A
HIP0081	45	3

HIP0080 Power Dissipation with a 2 sq. in. PC Board Heat Sink:
- At 85^oC 1.95W
- Above 85^oC: . . . . . Derate Linearly at $30mW/^oC$

HIP0081 Power Dissipation with Infinite Heat Sink:
- At 125^oC 8.33W
- Above 125^oC . . . . . Derate Linearly at $333\ mW/^oC$

Maximum Storage Temperature Range, T_{STG} . . . . -55^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Die Characteristics

HIP0080 Back Side Potential . . . . . Frame, GND Leads
HIP0081 Back Side Potential . . . . . Heat Sink Tab, GND Lead

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The MOSFET Output Drain is internally Clamped with a Drain-to-Gate zener diode that turns-on the MOSFET to hold the Drain at the V_{CLAMP} voltage. Refer to the Electrical Characteristic Tables for the V_{CLAMP} voltage limits.
2. Each Output has Over-Current Shutdown protection in the positive current direction. The maximum peak current rating is determined by the minimum Over-Current Shutdown as detailed in the Electrical Specification Table. In the event of an Over-Current Shutdown the input drive is latched OFF. The output short must be removed and the input toggled OFF and ON to restore the output drive.
3. Effective Heat Sinking for the HIP0080 PLCC package requires a PC Board solder mount or equivalent. The HIP0080 θ_{JA} junction-to-air thermal resistance is given for a PC Board with 2 sq. in. of 1 oz. surface mount ground copper extending away from the package. For additional Power Dissipation Derating information, see Figure 8 curves.
4. Refer to Figures 4 and 5 Single Pulse Output Clamp Energy vs. Time Capability of the HIP0080 and HIP0081. The safe margin for single pulse energy operation is below the dotted line shown in Figures 4 and 5.

Electrical Specifications

V_{CC} = 5.5V to 25V ±5%, T_A = -40^oC to 125^oC, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HIP0080			HIP0081			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER OUTPUTS									
Output ON Resistance (HIP0081)	r_{ON}	V_{CC} = 10 to 25V, All Outputs ON $I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4}$ = 1A	-	-	-	-	-	0.5	Ω
		V_{CC} = 5.5 to 10V, All Outputs ON $I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4}$ = 0.7A	-	-	-	-	-	1.0	Ω
Output ON Resistance (HIP0080)	r_{ON}	V_{CC} = 10 to 25V, All Outputs ON $I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4}$ = 0.5A	-	-	1.0	-	-	-	Ω
		V_{CC} = 5.5 to 10V, All Outputs ON $I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4}$ = 0.4A	-	-	2.0	-	-	-	Ω
HIP0081 Output Off Current	I_{OFF}	Inputs Low, Each V_{OUT} = 60V T_A = 25^oC to 125^oC	-	-	-	-	0.75	1.0	mA
		Inputs Low, Each V_{OUT} = 60V, T_A = -40^oC	-	-	-	-	0.75	1.5	mA
HIP0081 Output Leakage Current	I_{OFFLK}	Inputs Low, Each V_{OUT} = 60V, V_{CC} = 0V	-	-	-	-	1.0	10	µA

Electrical Specifications V_{CC} = 5.5V to 25V ±5%, T_A = -40°C to 125°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	HIP0080			HIP0081			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
HIP0080 Output Off Current	I_{OFF}	Inputs Low, Each V_{OUT} = 25V, ENABLE High, T_A = 25°C to 125°C	-	0.75	1.0	-	-	-	mA
		Inputs Low, Each V_{OUT} = 25V, ENABLE High, T_A = -40°C	-	0.75	1.5	-	-	-	mA
HIP0080 Output Leakage Current	I_{OFFLK}	Inputs Low, Each V_{OUT} = 25V, ENABLE Low	-	1.0	10	-	-	-	µA
Over-Voltage Clamp Range	V_{CLAMP}	IN Inputs Low (Outputs OFF), I_{OUT} = 40mA	27	-	43	73	-	89	V
Current Short Circuit Prot.	$I_{OUT(SC)}$	Note 2	1.3	-	3	2.2	-	4.8	A
Short Circuit Det. Delay	t_{SCDLY}		-	6	-	-	6	-	µs
Output ON-OFF Voltage Ramp Rate		Resistive Load	-	10	-	-	10	-	V/µs
Turn-On Delay	t_{PHL}	V_{CC} = 14V, R_{LOAD} = 14Ω	-	-	8	-	-	8	µs
Turn-Off Delay	t_{PLH}	V_{CC} = 14V, R_{LOAD} = 14Ω	-	-	8	-	-	8	µs
SUPPLY									
Power Supply Current	I_{CC}		-	20	30	-	20	30	mA
Power Supply Reset Active	V_{CC_RST}	T_A = 25°C to T_A = 125°C	3	-	4	3	-	4	V
		T_A = -40°C	2.7	-	4	2.7	-	4	V
Shut-Down Current Mode	I_{SHTDN}	Enable Low	-	130	200	-	-	-	µA
INPUTS									
Low-Level Input Voltage	V_{IL}		-	-	1	-	-	1	V
High-Level Input Voltage	V_{IH}		3.5	-	-	3.5	-	-	V
Input Hysteresis Threshold	V_{IN_HYS}	(N.A. to HIP0080 ENABLE)	0.85	-	2.25	0.85	-	2.25	V
Input Pull-Down Resistance	R_{PD}	IN1, IN2, IN3, IN4 and ENABLE	50	100	200	50	100	200	kΩ
DATAOUT (Open Drain)									
Leakage Current	I_{DO_LEAK}	V_{DO} = 7V, DO OFF (High)	-	-	10	-	-	10	µA
Logic Low Output Voltage	V_{OL}	I_{DO} = 1.6mA, DO ON (Low)	-	-	0.4	-	-	0.4	V
Max. Logic Low Current	I_{OH}	V_{DO} = 4.5V, DO ON	1.6	-	-	1.6	-	-	mA
Oscillator Frequency	f_{OSC}		-	500	-	-	500	-	kHz
Serial Interface Clock Freq.	f_{CLK}	Note 5	-	-	2	-	-	2	MHz
DIAGNOSTIC AND PROTECTION									
Over-Temperature Shutdown Threshold			150	165	-	150	165	-	°C
Shutdown Temperature Hysteresis			-	15	-	-	15	-	°C
Output Short-to-GND Threshold		V_{CC} = 5.5V to 16V	-	0.24x V_{CC}	-	-	0.24x V_{CC}	-	V
Short-to-GND Hysteresis		V_{CC} = 5.5V to 16V	-	0.02x V_{CC}	-	-	0.02x V_{CC}	-	V
Open-Load Resistance for No-Load Warning		V_{CC} = 5.5V to 16V	5	-	25	5	-	25	kΩ
Filter Delay Time for O.L. or Short-to-GND			-	12	-	-	12	-	µs

NOTE:

5. The maximum Serial Clock Frequency may be limited by the time constant of the external load network at the DATAOUT pin.

Diagnostic Interface Overview

Each Quad Inverting Power Driver IC may be used as a single power switching driver, with or without the diagnostic interface. Where more than 4 Power Driver Switches are required, the HIP0080 or HIP0081 may be used in a multiple IC cascade connection. In cascade operation, the diagnostic data from all chips is read as a single serial sequence of fault bits. As shown in the Functional Block Diagram each output stage has voltage and temperature sensors to detect fault conditions while comparators and delay filters process the data. Four bits of diagnostic information is provided as fault feedback from each of the four output stages. When detected, the diagnostic data is put in a parallel diagnostic data register. Using the diagnostic control interface to address the system (one or more ICs in cascade), the fault data is transferred from the parallel diagnostic data register to a serial diagnostic data register as a sequence of 16 bits for each IC.

All diagnostic data bits may be read using the Chip Select ($\overline{CS}$) and the Clock (CLK) inputs. The CLK input must be low, when $\overline{CS}$ goes active low. After reading the first bit at DO to determine if there is an error flag, the following 16 bits of serial diagnostic data may be clocked out of DO. Clocking the CLK input synchronously shifts the serial register data out of DO while cascaded data (from other devices or sources) is shifted into the DI input. As data is shifted out of DO, the parallel diagnostic data register is cleared on the first rising edge of the CLK input, following the $\overline{CS}$ low. After each 16 clocks, cascaded diagnostic data from the next IC in sequence is then shifted out of the DO output. Shifting the serial diagnostic data out of DO is done as a continuous sequence, reading the data from all ICs in cascade while $\overline{CS}$ remains low. New diagnostic data can be stored in the parallel diagnostic data registers on each IC while the existing serial diagnostic data is read.

Referring to Figure 1 and Figure 2, there are two sources that generate an OR'ed Fault Flag at DO when $\overline{CS}$ goes low. The two fault data sources are (1) the on-chip fault detection and (2) the off-chip DI input from front end ICs in the cascade. The fault data bit, labeled DF (Data Fault) in Figure 2, contains the OR'ed inputs from both sources. The DF bit is not part of the 16-bit serial diagnostic data sequence. In cascaded operation, the DI input for the first of the selected chips should be tied low. And, in single IC operation (no cascade), the DI input should also be tied low. In cascaded operation, the Error Flags are cascaded via the DI inputs.

The on-chip fault Error Flag goes high if any one of the 16 diagnostic data fault bits have been set HIGH. This fault Error Flag bit precedes the 16 diagnostic data fault bits and is OR'ed with all diagnostic data fault bits. The DF bit flags the presence of an Error Flag fault on the IC and in any part of the cascaded string, including DI data input. As shown in Figure 3 each IC in the cascade provides an output which is passed to the DI input of the following IC and is passed on as an OR'ed bit to the DO output of the last IC in the cascade. A fault condition is immediately evident without reading all diagnostic data bits. However, all bits must be read to determine which chip and which diagnostic bit has been set. The Fault Flag is reset by the CLK input when the bits are read. When no fault condition is detected, it is not necessary to toggle the CLK input. When a fault is detected, at least one toggle of the clock is needed to reset the parallel diagnostic register which clears the register of all detected fault states.

The last IC in the string ORs its own 16 fault bits in the parallel diagnostic register data and sends this data bit to an Error Flag register. The Error Flag register outputs the presence of a fault in one or more bits of the parallel diagnostic data register. As shown in Figure 2, the Error Flag is the first bit in front of the serial register and is input to OR Gate, U7 with the DI input. The DI input passes through AND Gate, U6 when the GATE signal is high and output via the amplifier U8 to DO. The output amplifier U8 is active only while $\overline{CS}$ is low. When $\overline{CS}$ is low, the RS Flip-Flop drives the GATE output high. When the GATE is high, the cascaded DF bits are jammed from DI to DO. All Error Flags in the cascade are cleared (by the CLK input) when the serial diagnostic data is clocked out of DO.

The GATE is an internal control signal that is forced high when the CLK input is low and $\overline{CS}$ goes low. The GATE will remain high, even when $\overline{CS}$ is returned to a high state, provided the CLK input has not changed from a low state. This condition still applies when fault data is detected. The DO output is not latched; however, the Error Flag is latched when $\overline{CS}$ goes low and will not be updated until the next time $\overline{CS}$ goes low. The fault data is preserved as long as the CLK input does not go high. If the CLK is high when $\overline{CS}$ goes low, the GATE will be disabled and no cascade data will be shifted from DI to DO. Under normal conditions, the CLK signal goes high to switch the GATE low and simultaneously shifts the first of 16 diagnostic data bits out of the serial diagnostic data register to DO. The $\overline{CS}$ low input is not latched and must be held low while all data is shifted out of DO.

The diagnostic interfaces to the HIP0080 and HIP0081 are SPI compatible. The microcontroller is programmed to control the read and respond action based on the diagnostic readout. Normally the $\overline{CS}$ input is addressed and DO is read. If a fault is indicated by the Error Flag, all data is shifted out of DO and processed to determine the diagnostic fault condition. The Error Flag bit does require a separate input back to the microcontroller to initiate the serial data shift. When the CLK signal starts, the serial sequence starting with the first of the 16 serial diagnostic bits is input to the microcontroller.

Serial Register Data Sequence

The fault data follows the Serial Register Data Sequence of Table 1 in bit sequence and, in cascade, by IC sequence. In each of the 4 power switching output channels, the diagnostic sense circuits set 1-bit in the parallel diagnostic register for each of the 4 diagnostics fault conditions. A total of 16 diagnostics data bits are shifted to the serial register when $\overline{CS}$ goes low. Table 1 shows the order and sequence of the serial bits as they are shifted out of DO. The fault action that sets

each of the diagnostics bits for each of the 4 switches is described below:

Bit 1 - indicates a thermal overload when the sensed junction temperature of the output is greater than 150^{O}C. When over-temperature is sensed, the sensor output directly gates-off the drive to the power output and the respective fault bit is set in the diagnostic register. When the chip is sufficiently cooled, the output is gated-on if the input remains ON.

Bit 2 - indicates the fault condition for an output-to-supply short (shorted load). A small value of resistance (~0.01Ω) in the source-to-ground line of the output stage is used to sense the output short. A comparator senses the voltage level and filters the output to provide an input to the control stage and to the diagnostic register. The control state directly shuts down the output when an over-current condition is sensed. Under this condition of fault, the input driver is latched off. To restore the output drive, the short must be removed and the input toggled OFF and then ON. A short to the supply is the only error condition that requires an input toggle reset.

Bit 3 - indicates the condition of an output to ground short. As shown in the Functional Block Diagram, each output stage has drain-to-supply (VCC1) and drain-to-ground pull-up and pull-down resistors of approximately 10kΩ to sense this condition. When the output is off and the sense level is low, an output-to-ground short is detected by the comparator. This condition is sensed when the output is pulled lower than 0.24xVCC (typical).

Bit 4 - indicates the condition of an open load on the output. The same divider noted for Bit 3 is used to set the output level. If the sense level is at or near the mid-range of the voltage supply, $V_{CC}1$ when the output is in the off condition, a no-load condition is detected.

TABLE 1. SERIAL REGISTER DATA SEQUENCE

CHANNEL NO.	BIT NO.	FAULT FUNCTION	FAULT SYMBOL
Switch Channel 1	1	Over-Temperature	OT1
	2	Short to Supply	SB1
	3	Short to Ground	SG1
	4	Open Load	OI1
Switch Channel 2	5	Over-Temperature	OT2
	6	Short to Supply	SB2
	7	Short to Ground	SG2
	8	Open Load	OI2
Switch Channel 3	9	Over-Temperature	OT3
	10	Short to Supply	SB3
	11	Short to Ground	SG3
	12	Open Load	OI3
Switch Channel 4	13	Over-Temperature	OT4
	14	Short to Supply	SB4
	15	Short to Ground	SG4
	16	Open Load	OI4

Serial Peripheral Interface Bus Control

Technically, the HIP0080 and HIP0081 fault data has only 16 bits. Except for the Error Flag, DF data bit shown in Figure 2, the format matches that of a normal CPOL = 0, CPHA = 1 SPI protocol (polarities, phase, etc). The DF bit from the DO output is active only until the clock starts. The best way to take advantage of it (if desired) is to connect the DO to the SPI bus, and also to a port pin, or other logic input. After CS goes low and before the SPI clocks starts, the DF bit can be read. If it is a zero, then the rest of the data does not have to be read. (The data will be all 0's = no errors). If the DF bit = 1, then the data must be read to find out which bit(s) is set.

Multiple ICs can be cascaded such that an error bit on any IC will daisy chain up to the last DO; this allows the microcontroller to "wire-OR" all of the devices automatically. Other than bidirectional data IC types, different IC types may be cascaded. The HIP0080 or HIP0081 should be closest to the microcontroller to use the DF bit feature. ICs that do not have an OR'ed means of passing fault bit would require all data be clocked to check the diagnostic bits.

Clamp Energy Ratings for the HIP0080 and HIP0081

Figures 4 and 5 define the Single Pulse Energy ratings for the HIP0080 and HIP0081. Refer to Application Note AN9416 for further information on Single Pulse Energy ratings for inductive load operation and Dissipation capability for the 15 pin Power SIP Package. The Device Under Test conducts when the zener over voltage clamp turns on the output. While drain-to-source voltage, VDS and drain current, ID are monitored, the current drive pulse width, t_{ON} in seconds is varied to determine the Single Pulse Energy capability. The energy in Joules is calculated from the following equation:

Single Pulse Energy = VDS x ID x t_{ON}.

Refer to Application Note 9416 for further information on Single Pulse Energy ratings for inductive load operation and Dissipation capability for the 15 pin Power SIP Package.

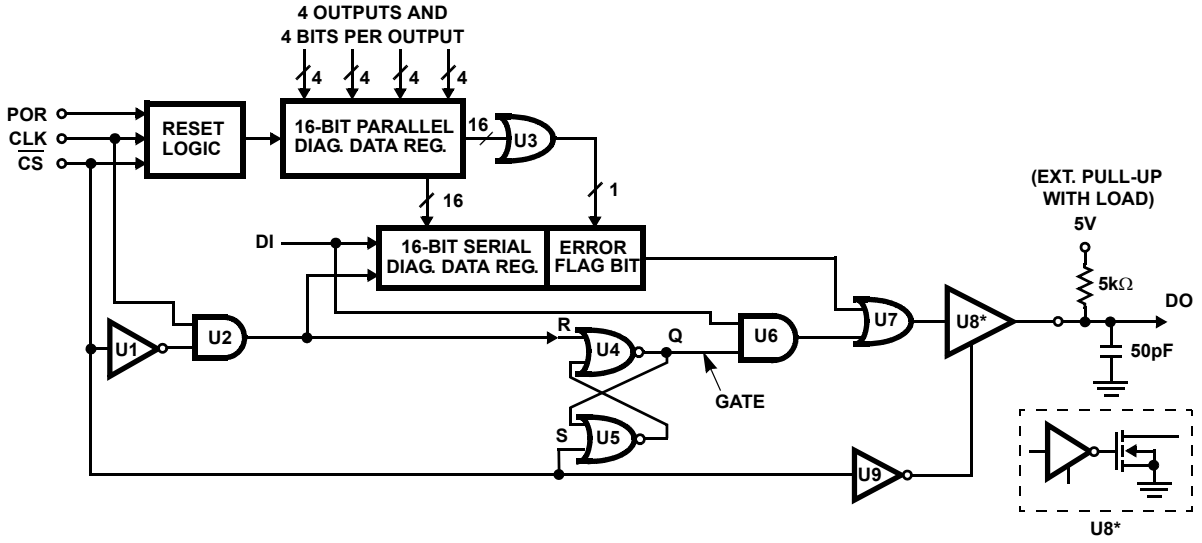


FIGURE 1. DIAGNOSTIC INTERFACE LOGIC

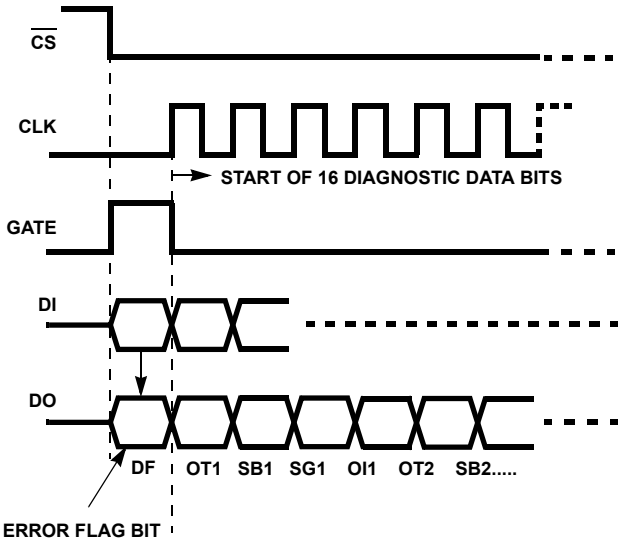


FIGURE 2. DATA AND CLOCK TIMING

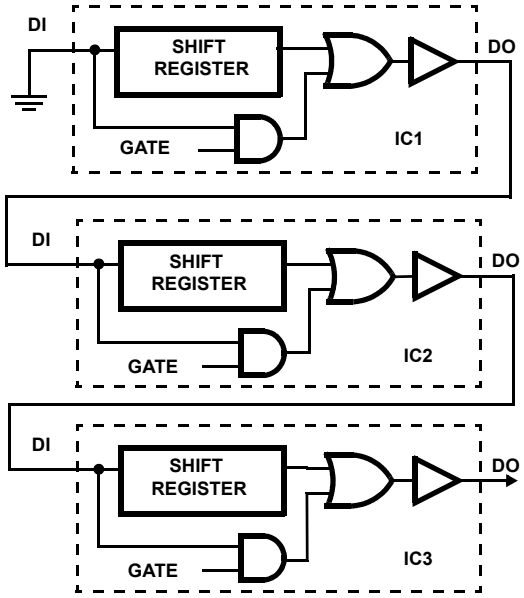


FIGURE 3. CASCADED CHIP OPERATION TO READ DIAGNOSTIC DATA

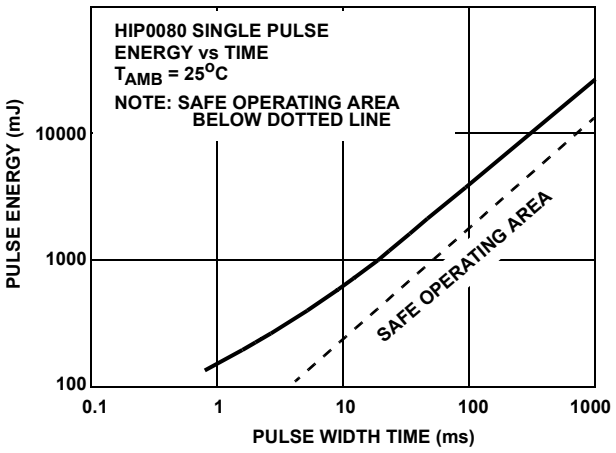


FIGURE 4. SINGLE PULSE ENERGY TEST SHOWING THE FAILURE BOUNDARY FOR EACH HIP0080 OUTPUT STRESSED TO POINT OF FAILURE

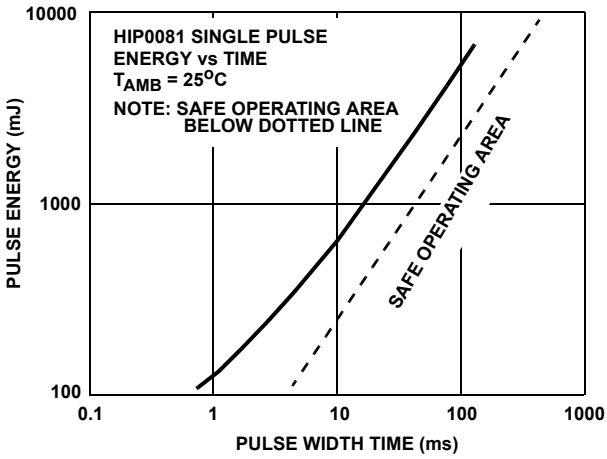


FIGURE 5. SINGLE PULSE ENERGY TEST SHOWING THE FAILURE BOUNDARY FOR EACH HIP0081 OUTPUT STRESSED TO POINT OF FAILURE

Dissipation In Multiple Outputs

The HIP0080 and HIP0081 Power Drivers have multiple MOS Output Drivers and require special consideration with regard to maximum current and dissipation ratings. While each output has a maximum current specification consistent with the device structure, all such devices on the chip can not be simultaneously rated to the same high level of peak current. The total combined current and the dissipation on the chip must be adjusted for maximum allowable ratings, given simultaneous multiple output conditions.

For the HIP0081, the maximum positive output current rating is 2.2A when one output is ON. When ALL outputs are ON, the rating is reduced to 1.5A because the total maximum current is limited to 6A. For any given application, all output drivers on a chip may or may not have a different level of loading. The discussion here is intended to provide relatively simple methods to determine the maximum dissipation and current ratings as a general solution and, as a special solution, when all switched ON outputs have the same current loading.

General Solution

A general equation for dissipation should specify that the total power dissipation in a package is the sum of all significant elements of dissipation on the chip. However, in Power BiMOS Circuits very little dissipation is needed to control the logic and predriver circuits on the chip. The overall chip dissipation is primarily the sum of the I^2R dissipation losses in each channel where the current, I is the output current and the resistance, R is the NMOS channel resistance, $r_{DS(ON)}$ of each output driver. As such, the total dissipation, P_D for n output drivers is:

$$_D = \sum_{k=1}^{n} P_k \quad \text{(EQ. 1)}$$

This expression sums the dissipation, P_k of each output driver without regard to uniformity of dissipation in each MOS channel. The dissipation loss in an NMOS channel is given in Equation 2 where the current, I, is determined by the output load when the channel is turned ON. The channel resistance, $r_{DS(ON)}$ is a function of the circuit design, level of gate voltage and the chip temperature. Other switching losses may include I^2R lost in the interconnecting metal on the chip and bond wires of the package.

$$P_k = I^2 \times r_{DS(ON)} \quad \text{(EQ. 2)}$$

The temperature rise in the package due to the dissipation is the product of the dissipation, P_D and the thermal resistance, θ_{JC} of the package (Junction-to-Case). To determine the chip junction temperature, T_J, given the case (heat sink $_{tab}$) temperature, T_C, the linear heat flow solution is:

$$T_J = T_C + P_D \times \theta_{JC} \quad \text{(EQ. 3)}$$

or:

$$T_C = T_J - P_D \times \theta_{JC} \quad \text{(EQ. 3A)}$$

Since this solution relates only to the package, further consideration must be given to a practical heat sink. The equation of linear heat flow assumes that the thermal resistance from Junction-to-Ambient (θ_{JA}) is the sum of the thermal resistance from Junction-to-Case and the thermal resistance from Case (heat sink)-to-Ambient. The Junction-to-Ambient thermal resistance, θ_{JA} is the sum of all thermal paths from the chip junction to the ambient temperature (T_A) environment and can be expressed as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad \text{(EQ. 4)}$$

The Junction-to-Ambient equivalent to Equation 3, 3A is:

$$T_J = T_A + P_D \times \theta_{JA} \quad \text{(EQ. 5)}$$

or:

$$T_A = T_J - P_D \times \theta_{JA} \quad \text{(EQ. 5A)}$$

Not all Integrated Circuit packages have a directly definable case temperature because the heat is spread through the lead frame to a PC Board which is the effective heat sink.

Calculation Example 1

For the HIP0081, θ_{JC} = 3°C/W and the worst case junction temperature, as an application design solution, should not exceed 150°C. For a given application, Equation 1 determines the dissipation, P_D.

Assume the package is mounted to a heat sink having a thermal resistance of 6°C/W and, for a given application, assume the dissipation is 3W and the ambient temperature (T_A) is 100°C. From Equation 4, θ_{JA} is 9°C/W. The solution for junction temperature (T_C) by Equation 3 is:

T_J = 100°C + 3W x 9°C/W = 127°C.

Calculation Example 2:

Assume for the HIP0080, θ_{JA} = 30°C/W mounted on a PC Board with good heat sinking characteristics. Again, the worst case junction temperature, as an application design solution, should not exceed 150°C. Assume from the application, based on Equation 1, the dissipation, P_D = 1.5W. The maximum junction temperature is known and can be used to determine the maximum allowable ambient temperature from Equation 5A as follows:

T_A = 150°C - 1.5W x 30°C/W = 105°C.

Equal Current Loading Solution

Many applications may have equal current loading in the output drivers with equal saturated turn ON and temperature conditions. As such, a convenient method to show rating boundaries is to substitute the dissipation Equation 2 into the junction temperature Equation 3. For m outputs that are ON and conducting with equal currents, where $I = I_1 = I_2 ..... = I_m$, we have the following solution for dissipation:

$$P_D = m \times P_k = m \times I^2 \times r_{DS(ON)} \quad \text{(EQ. 6)}$$

$$I = \sqrt{\frac{T_J - T_C}{m \times \theta_{JC} \times r_{DS(ON)}}} \quad \text{(EQ. 7)}$$

The number of output drivers ON and conducting (m) may be from 1 to n. (i.e., For all four output drivers of the HIP0081 ON, m = 4.) Maximum temperature, dissipation and current ratings must be observed. For a defined number of conducting Power MOS Output Drivers, we can plot the results for m devices showing I vs T_C.

Given the HIP0081 as an example, Figures 6 and Figure 7 illustrate the boundaries for temperature and current. Figure 6 shows the maximum current for a single output ON while Figure 7 shows the maximum current for all four outputs ON with equal current plotted versus Case Temperature, T_C. Boundary conditions relate to the Absolute Maximum Ratings as defined in the Data Sheet.

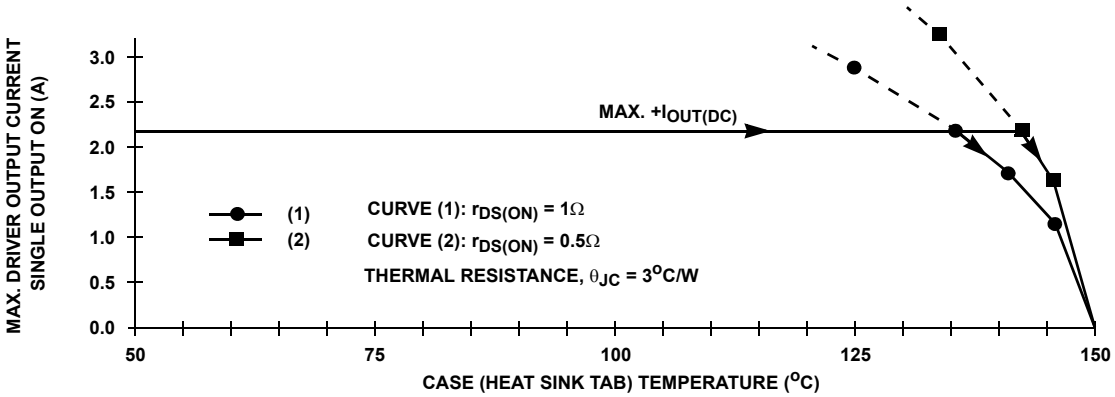


FIGURE 6. HIP0081 MAXIMUM SINGLE OUTPUT CURRENT vs CASE (TAB) TEMPERATURE

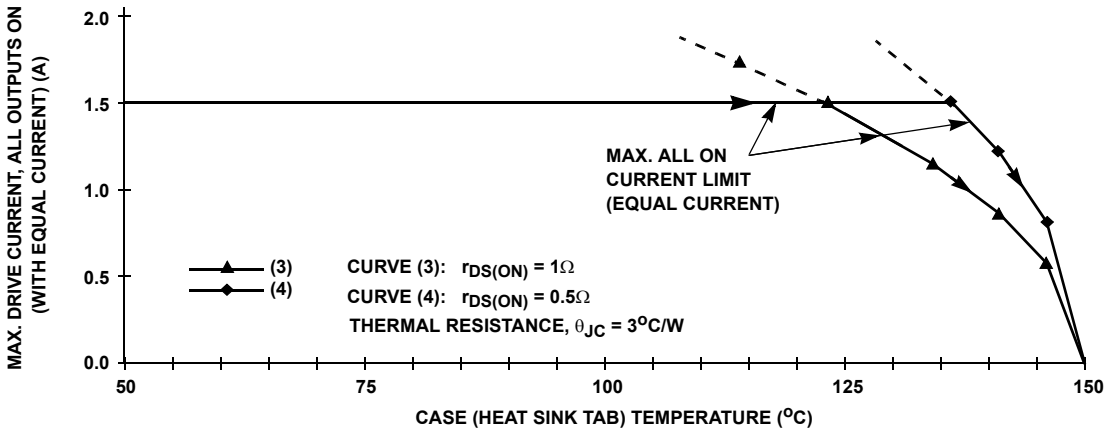


FIGURE 7. HIP0081 CURRENT vs CASE (TAB) TEMPERATURE, ALL OUTPUTS ON WITH EQUAL CURRENT

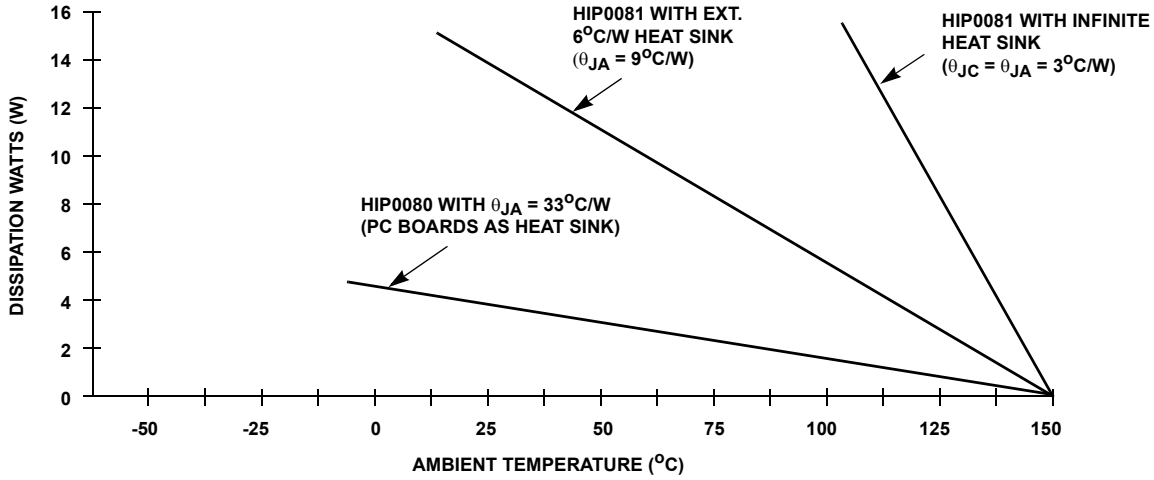
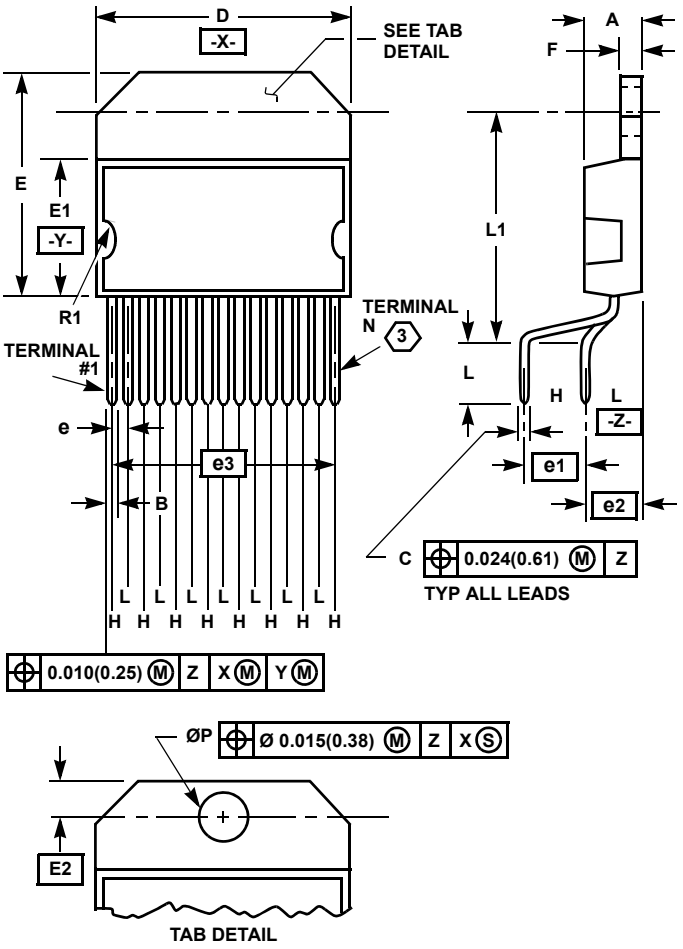


FIGURE 8. DISSIPATION DERATING CURVES

Single-In-Line Plastic Packages (SIP)



Z15.05A (JEDEC MO-048 AB ISSUE A)
15 LEAD PLASTIC SINGLE-IN-LINE PACKAGE STAGGERED VERTICAL LEAD FORM

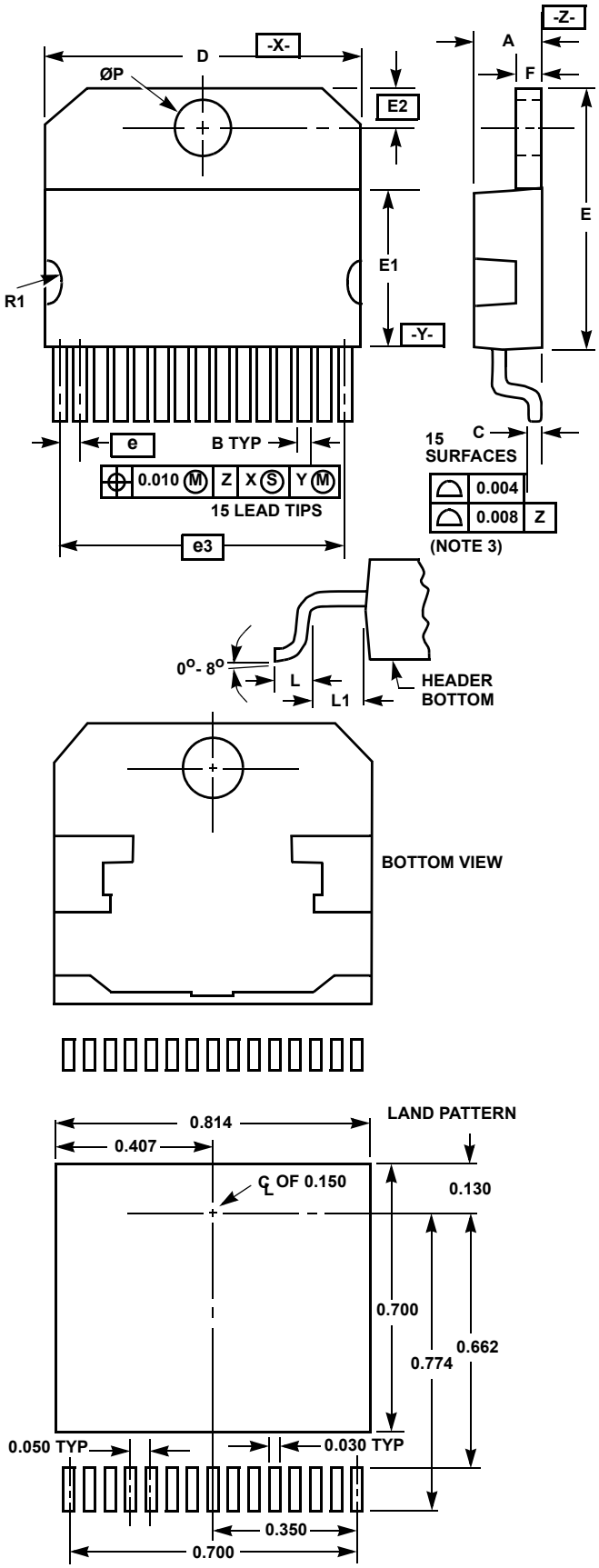
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.172	0.182	4.37	4.62
B	0.024	0.031	0.61	0.79
C	0.014	0.024	0.36	0.61
D	0.778	0.798	19.76	20.27
E	0.684	0.694	17.37	17.63
E1	0.416	0.426	10.57	10.82
E2	0.110 BSC		2.79 BSC	
e	0.050 BSC		1.27 BSC	
e1	0.200 BSC		5.08 BSC	
e2	0.169 BSC		4.29 BSC	
e3	0.700 BSC		17.78 BSC	
F	0.057	0.063	1.45	1.60
L	0.150	0.176	3.81	4.47
L_1	0.690	0.710	17.53	18.03
N	15		15	
ØP	0.148	0.152	3.76	3.86
R1	0.065	0.080	1.65	2.03

Rev. 1 4/98

NOTES:

1. Refer to series symbol list, JEDEC Publication No. 95.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. N is the number of terminals.
4. Controlling dimension: INCH.

Single-In-Line Plastic Packages (SIP)



Z15.05B

15 LEAD PLASTIC SINGLE-IN-LINE PACKAGE SURFACE MOUNT "GULLWING" LEAD FORM

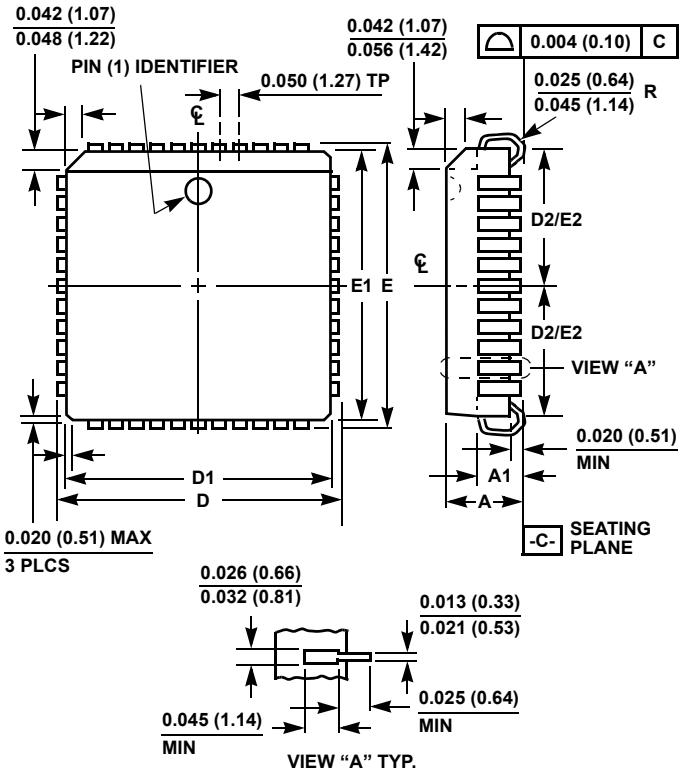
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.172	0.182	4.37	4.62
B	0.024	0.031	0.61	0.79
C	0.018	0.024	0.46	0.61
D	0.778	0.798	19.76	20.27
E	0.684	0.694	17.37	17.63
E1	0.416	0.426	10.57	10.82
E2	0.110 BSC		2.79 BSC	
e	0.050 BSC		1.27 BSC	
e3	0.700 BSC		17.78 BSC	
F	0.057	0.063	1.45	1.60
L	0.065	0.080	1.66	2.03
L1	0.098	0.108	2.49	2.74
N	15		15	
ØP	0.148	0.152	3.76	3.86
R1	0.065	0.080	1.65	2.03

Rev. 1 11/97

NOTES:

1. Dimensioning and Tolerancing per ANSI Y14.5M - 1982.
2. N is the number of terminals.
3. All lead surfaces are within 0.004 inch of each other. No lead can be more than 0.004 inch above or below the header plane, (-Z- Datum).
4. Controlling dimension: INCH.

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

Rev. 2 11/97

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.