

Am9016

16,384 x 1 Dynamic RAM

DISTINCTIVE CHARACTERISTICS

- Replacement for MK4116
- High-speed operation - 150ns access, 320ns cycle (COM'L); 200ns access, 375ns cycle (MIL)
- Three-state output
- $\overline{\text{RAS}}$ only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output

GENERAL DESCRIPTION

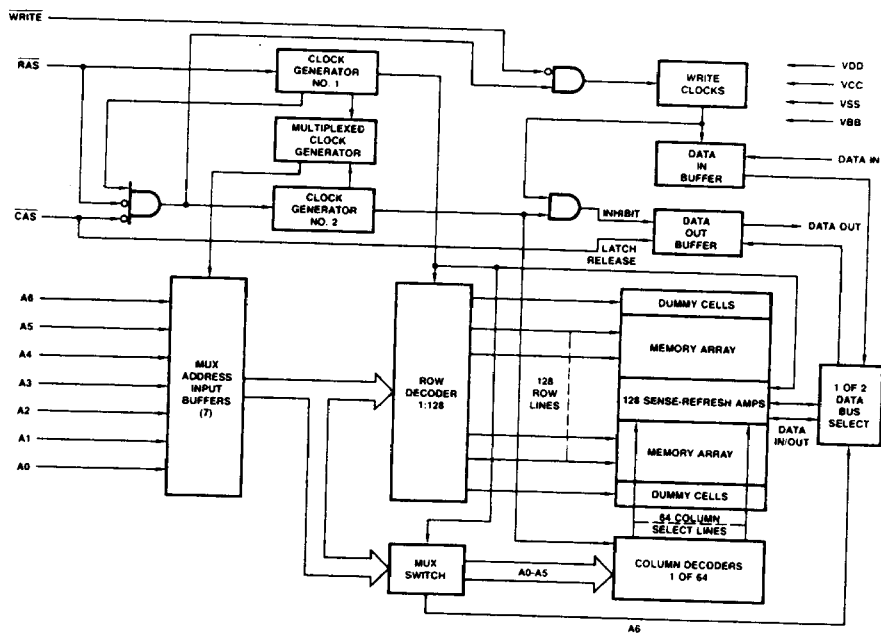
The Am9016 is a high-speed, 16K-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP or 18-pin leadless chip carrier. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{\text{RAS}}$) loads the row address and the Column Address Strobe ($\overline{\text{CAS}}$) loads the column

address. The row and column address signals share seven input lines. Active cycles are initiated when $\overline{\text{RAS}}$ goes low, and standby mode is entered when $\overline{\text{RAS}}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance and power dissipation.

The 3-state output buffer turns on when the column access time has elapsed and turns off after $\overline{\text{CAS}}$ goes high. Input and output data are the same polarity.

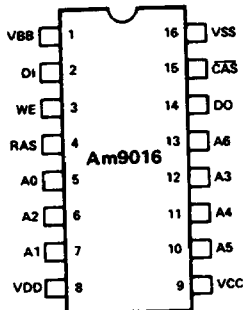
BLOCK DIAGRAM



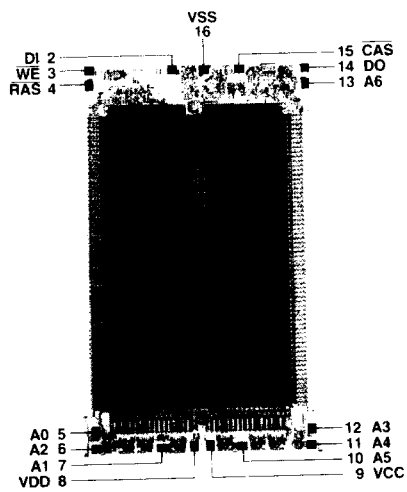
BD000240

**CONNECTION DIAGRAM
Top View**

DIP



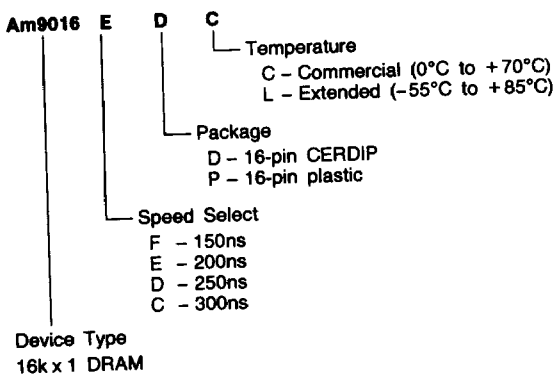
Metallization and Pad Layout



DIE SIZE 0.107" x 0.205"

4

ORDERING INFORMATION



Valid Combinations	
C, D, E	DC, PC, DL
F	DC, PC

APPLICATION INFORMATION

The Am9016 electrical connections are such that if power is applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

OPERATING CYCLES

Random read operations from any location hold the \overline{WE} line high and follow this sequence of events:

1. The row address is applied to the address inputs and \overline{RAS} is switched low.
2. After the row address hold time has elapsed, the column address is applied to the address inputs and \overline{CAS} is switched low.
3. Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as \overline{CAS} is low.
4. \overline{CAS} and \overline{RAS} are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the \overline{WE} line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have \overline{WE} low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds \overline{WE} high until a valid read is established and then strobes new data in with the falling edge of \overline{WE} .

After the power is first applied to the device, the internal circuit requires execution of at least eight initialization cycles which exercise \overline{RAS} before valid memory accesses are begun.

ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe (\overline{RAS}) enters the row address bits and the Column Address Strobe (\overline{CAS}) enters the column address bits.

When \overline{RAS} is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain \overline{RAS} low while \overline{CAS} is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that \overline{RAS} can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column

address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

REFRESH

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be " \overline{RAS} -only" cycles. Since only the rows need to be addressed, \overline{CAS} may be held high while \overline{RAS} is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of \overline{WE} and \overline{CAS} while \overline{RAS} is low. The later negative transition of \overline{WE} or \overline{CAS} strobes the data into the internal register. In a write cycle, if the \overline{WE} input is brought low prior to \overline{CAS} , the data is strobed by \overline{CAS} , and the set-up and hold times are referenced to \overline{CAS} . If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of \overline{WE} .

In the read cycle the data is read by maintaining \overline{WE} in the high state throughout the portion of the memory cycle in which \overline{CAS} is low. The selected valid data will appear at the output within the specified access time.

DATA OUTPUT CONTROL

Any time \overline{CAS} is high the data output will be off (after tOFF). The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until \overline{CAS} is returned to the high state. The output data is the same polarity as the input data.

The user can control the output state during write operations by controlling the placement of the \overline{WE} signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

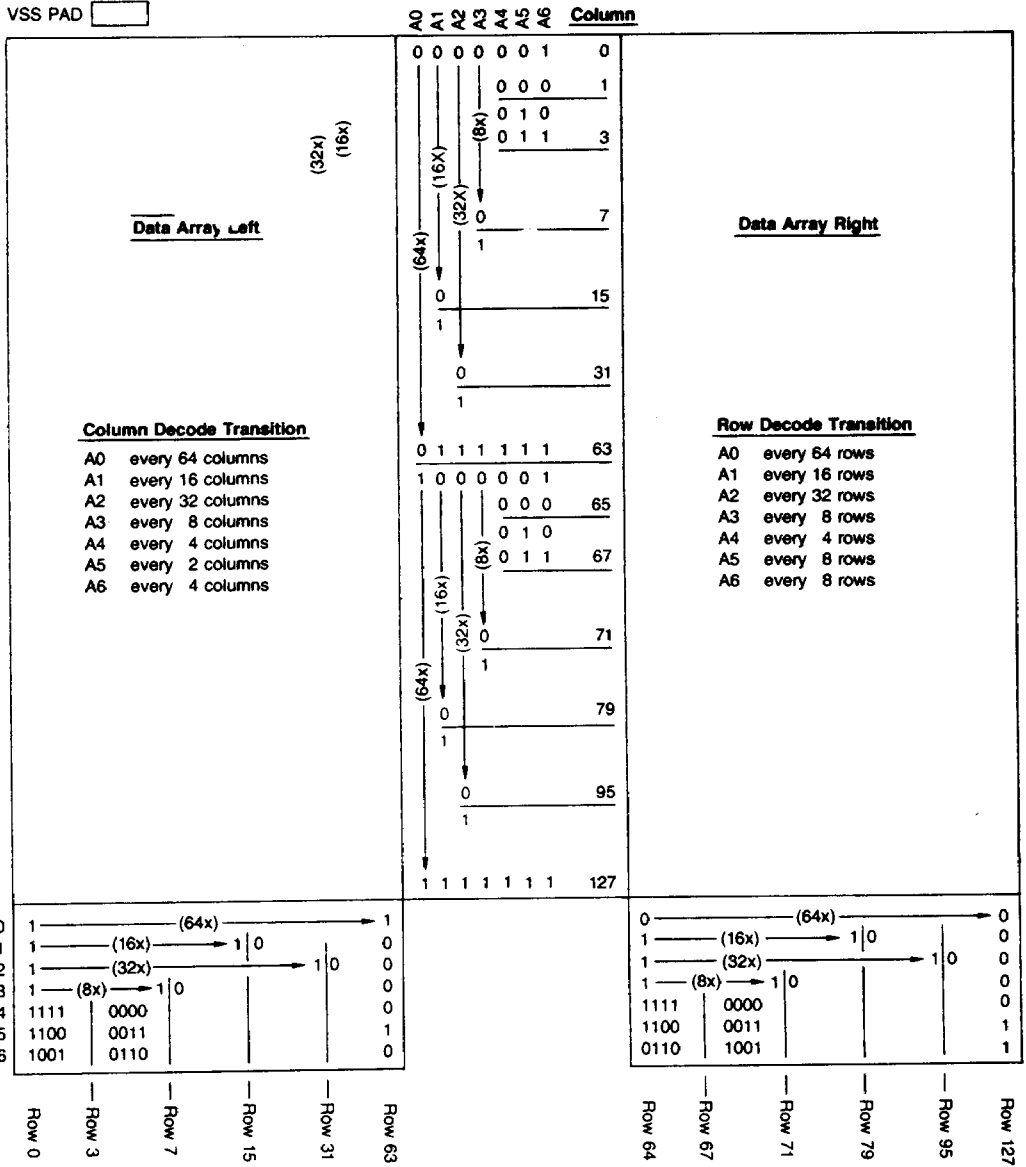
POWER CONSIDERATIONS

\overline{RAS} and/or \overline{CAS} can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if \overline{RAS} is used for this purpose. The devices which do not receive \overline{RAS} will be in low power standby mode regardless of the state of \overline{CAS} .

At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.

VSS PAD

Y-Address Lines



Data Array Left

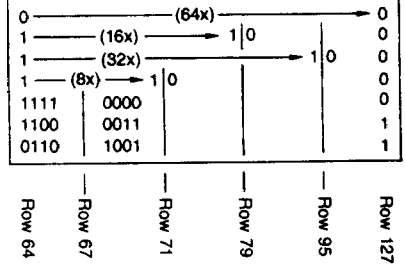
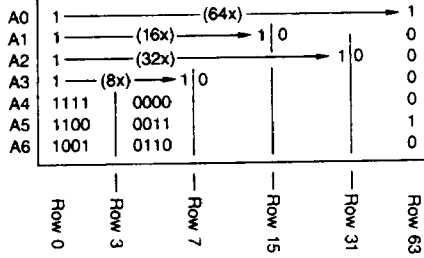
Data Array Right

Column Decode Transition

- A0 every 64 columns
- A1 every 16 columns
- A2 every 32 columns
- A3 every 8 columns
- A4 every 4 columns
- A5 every 2 columns
- A6 every 4 columns

Row Decode Transition

- A0 every 64 rows
- A1 every 16 rows
- A2 every 32 rows
- A3 every 8 rows
- A4 every 4 rows
- A5 every 8 rows
- A6 every 8 rows



X-Decode Left

X-Decode Right

TOPOLOGICAL BIT MAP

AF000080

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +85°C
Voltage on any pin with respect to V_{BB}	-0.5V to +20V
Positive Supply Voltages with respect to ground	-1.0V to +15.0V
DC Layout Voltage	-0.5V to +7.0V
$V_{BB} - V_{SS}$ Differentials given $V_{DD} - V_{SS} > 0V$	0W
Power Dissipation	1.0W
Short Circuit Output Current	50mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES

Commercial (C) Devices	Temperature	0°C to +70°C
Positive Supply Voltage V_{DD}	+10.8V to +13.2V	
V_{CC}	+4.5V to +5.5V	
Negative Supply Voltage V_{BB}	-4.5V to -5.5V	
Extended (L) Devices	Temperature	-55°C to +85°C
Positive Supply Voltage V_{DD}	+10.8V to +13.2V	
V_{CC}	+4.5V to +5.5V	
Negative Supply Voltage V_{BB}	-4.5V to -5.5V	

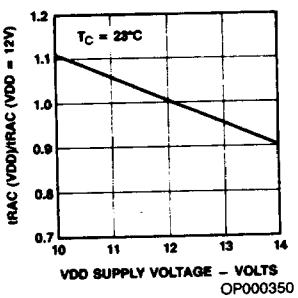
Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

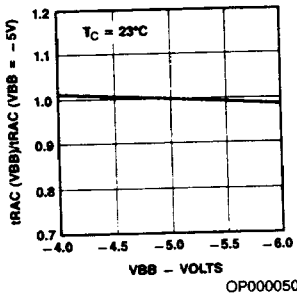
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -5.0mA$	2.4		V_{CC}	Volts
V_{OL}	Output LOW Voltage	$I_{OL} = 4.2mA$			0.40	Volts
V_{IH}	Input HIGH Voltage for Address, Data In		2.4		7.0	Volts
V_{IHC}	Input HIGH Voltage for \overline{CAS} , \overline{RAS} , \overline{WE}		2.7		7.0	Volts
V_{IL}	Input LOW Voltage		-1.0		0.80	Volts
I_x	Input Load Current	$V_{SS} \leq V_i \leq 7V$	-10		10	μA
I_{OZ}	Output Leakage Current	$V_{SS} \leq V_O \leq V_{CC}$, Output OFF	-10		10	μA
I_{CC}	V_{CC} Supply Current	Output OFF (Note 4)	-10		10	μA
I_{BB}	Supply Current, Average	Standby, $\overline{RAS} \geq V_{IHC}$	$0^\circ C \leq T_A \leq +70^\circ C$		100	μA
			$-55^\circ C \leq T_A \leq +85^\circ C$		200	
I_{DD}	V_{DD} Supply Current Average	Operating, Minimum Cycle Time	$0^\circ C \leq T_A \leq +70^\circ C$		200	mA
			$-55^\circ C \leq T_A \leq +85^\circ C$		400	
		\overline{RAS} Cycling, \overline{CAS} Cycling, Minimum Cycle Times, Operating I_{DD1}			35	
		$\overline{RAS} \leq V_{IL}$, \overline{CAS} Cycling, Minimum Cycle Times, Page Mode I_{DD4}			27	
C_1	Input Capacitance	Inputs at 0V, $f = 1MHz$, Nominal Supply Voltages	\overline{RAS} Cycling, $\overline{CAS} \geq V_{IHC}$, Minimum Cycle Times, \overline{RAS} Only Refresh I_{DD3}		27	pF
			$\overline{RAS} \leq V_{IHC}$, Standby I_{DD2}	$0^\circ C \leq T_A \leq +70^\circ C$	1.5	
C_0	Output Capacitance	Output OFF	$-55^\circ C \leq T_A \leq +85^\circ C$		2.25	
			\overline{RAS} , \overline{CAS} , \overline{WE} Address, Data In		10	
					5.0	
					7.0	

DC OPERATING CHARACTERISTICS

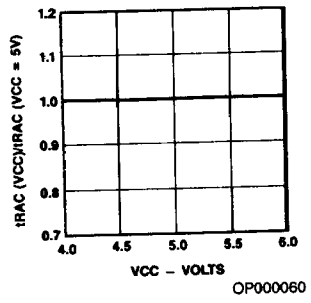
Typical Access Time (Normalized) t_{RAC} Versus V_{DD}



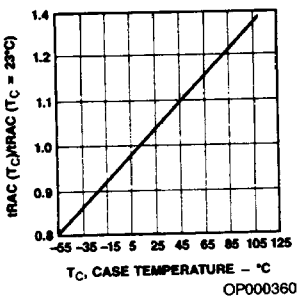
Typical Access Time (Normalized) t_{RAC} Versus V_{BB}



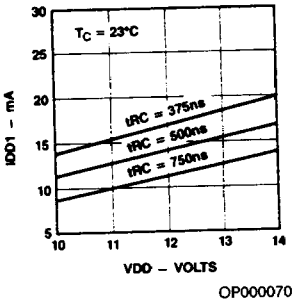
Typical Access Time (Normalized) t_{RAC} Versus V_{CC}



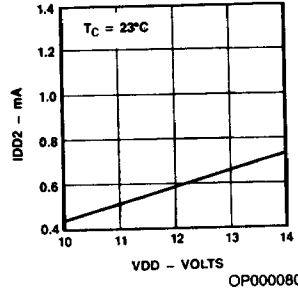
Typical Access Time (Normalized) t_{RAC} Versus Case Temperature



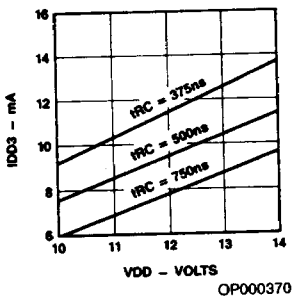
Typical Operating current I_{DD1} Versus V_{DD}



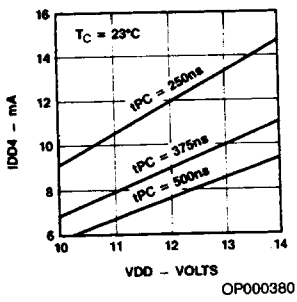
Typical Standby Current I_{DD2} Versus V_{DD}



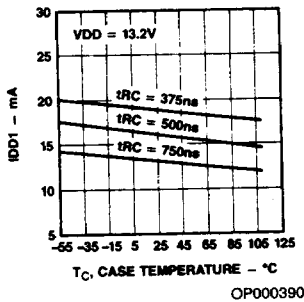
Typical Refresh Current I_{DD3} Versus V_{DD}



Typical Page Mode Current I_{DD4} Versus V_{DD}

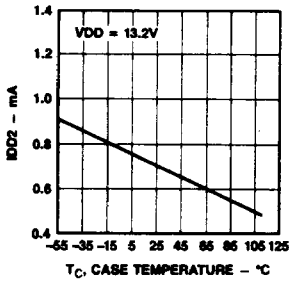


Typical Operating Current I_{DD1} Versus Case Temperature



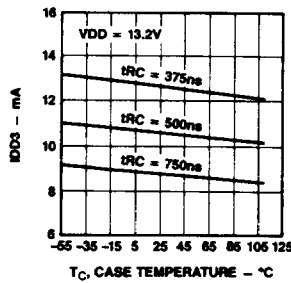
DC OPERATING CHARACTERISTICS (Cont.)

Typical Standby Current
IDD2 Versus
Case Temperature



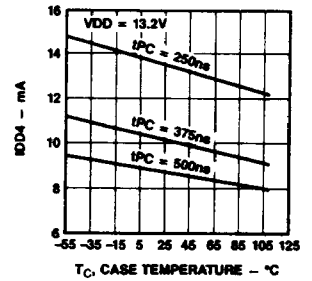
OP000400

Typical Refresh Current
IDD3 Versus
Case Temperature



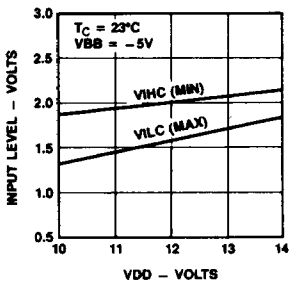
OP000410

Typical Page Mode Current IDD4
Versus Case Temperature



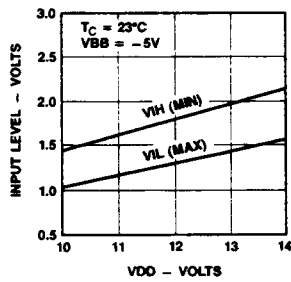
OP000420

Input Voltage Levels
Versus VDD



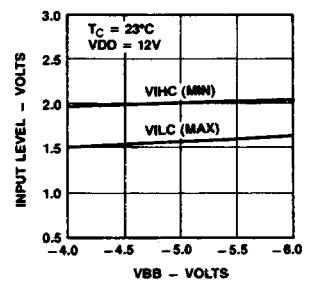
OP000470

Input Voltage Levels
Versus VDD



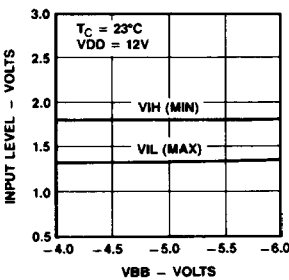
OP000480

Input Voltage Levels
Versus VBB



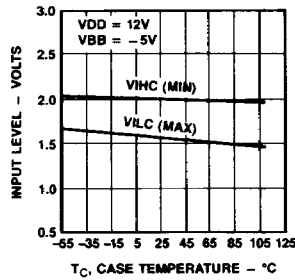
OP000490

Input Voltage Levels
Versus VBB



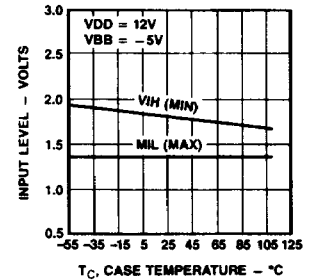
OP000500

Input Voltage Levels
Versus
Case Temperature



OP000510

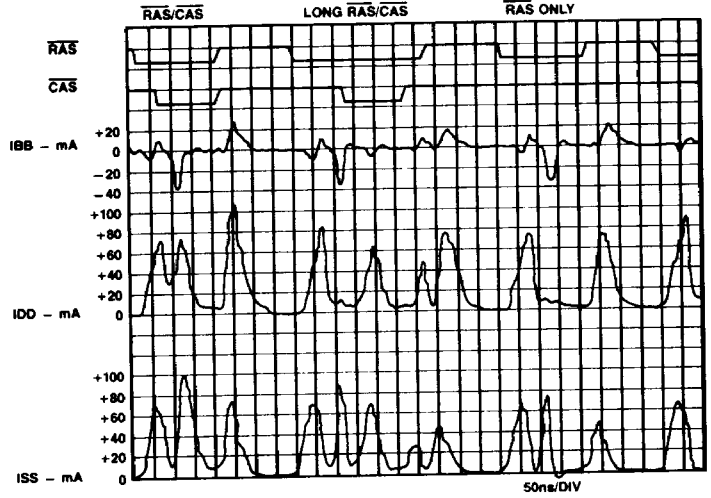
Input Voltage Levels
Versus
Case Temperature



OP000520

DC OPERATING CHARACTERISTICS (Cont.)

TYPICAL CURRENT WAVEFORMS



WF000310

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Symbol	Description	Am9016C		Am9016D		Am9016E		Am9016F		Units		
			Min	Max	Min	Max	Min	Max	Min	Max			
1	tAR	RAS LOW to Column Address Hold Time	200		160		120		95		ns		
2	tASC	Column Address Setup Time	0°C ≤ T _A ≤ +70°C		-10		-10		-10		ns		
			-55°C ≤ T _A ≤ +85°C		0		0		0		NA	ns	
3	tASR	Row Address Setup Time	0		0		0		0		ns		
4	tCAC	Access Time from CAS (Note 6)		185		165		135		100	ns		
5	tCAH	CAS LOW to Column Address Hold Time	85		75		55		45		ns		
6	tCAS	CAS Pulse Width	0°C ≤ T _A ≤ +70°C		185	10,000	165	10,000	135	10,000	100	10,000	ns
			-55°C ≤ T _A ≤ +85°C		185	5000	165	5000	135	5000	NA	NA	ns
7	tCP	Page Mode CAS Precharge Time	100		100		80		60		ns		
8	tCRP	CAS to RAS Precharge Time	0°C ≤ T _A ≤ +70°C		-20		-20		-20		-20	ns	
			-55°C ≤ T _A ≤ +85°C		0		0		0		NA	ns	
9	tCSH	CAS Hold Time	300		250		200		150		ns		
10	tCWD	CAS LOW to WE LOW Delay (Note 9)	145		125		95		70		ns		
11	tCWL	WE LOW to CAS HIGH Setup Time	100		85		70		50		ns		
12	tDH	CAS LOW or WE LOW to Data In Valid Hold Time (Note 7)	85		75		55		45		ns		
13	tDHR	RAS LOW to Data In Valid Hold Time	200		160		120		95		ns		
14	tDS	Data in Stable to CAS LOW or WE LOW Setup Time (Note 7)	0		0		0		0		ns		
15	tOFF	CAS HIGH to Output OFF Delay	0	60	0	60	0	50	0	40	ns		
16	tPC	Page Mode Cycle Time	295		275		225		170		ns		
17	tRAC	Access Time from RAS (Note 6)		300		250		200		150	ns		
18	tRAH	RAS LOW to Row Address Hold Time	45		35		25		20		ns		
19	tRAS	RAS Pulse Width	0°C ≤ T _A ≤ +70°C		300	10,000	250	10,000	200	10,000	150	10,000	ns
			-55°C ≤ T _A ≤ +85°C		300	5000	250	5000	200	5000	NA	NA	ns
20	tRC	Random Read or Write Cycle Time	460		410		375		320		ns		
21	tRCD	RAS LOW to CAS LOW Delay (Note 6)	35	115	35	85	25	65	20	50	ns		
22	tRCH	Read Hold Time	0		0		0		0		ns		
23	tRCS	Read Setup Time	0		0		0		0		ns		
24	tREF	Refresh Interval		2		2		2		2	ms		
25	tRMW	Read Modify Write Cycle Time	600		500		405		320		ns		

No.	Symbol	Description	Am9016C		Am9016D		Am9016E		Am9016F		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
26	tRP	RAS Precharge Time	150		150		120		100		ns
27	tRSH	CAS LOW to RAS HIGH Delay	185		165		135		100		ns
28	tRWC	Read/Write Cycle Time	525		425		375		320		ns
29	tRWD	RAS LOW to WE LOW Delay (Note 9)	260		210		160		120		ns
30	tRWL	WE LOW to RAS HIGH Setup Time	100		85		70		50		ns
31	tT	Transition Time	3	50	3	50	3	50	3	35	ns
32	tWCH	Write Hold Time	85		75		55		45		ns
33	tWCR	RAS LOW to Write Hold Time	200		160		120		95		ns
34	tWCS	WE LOW to CAS LOW Setup Time (Note 9)	0°C ≤ T _A ≤ +70°C		-20		-20		-20		ns
			-55°C ≤ T _A ≤ +85°C		0		0		0		NA
35	tWP	Write Pulse Width	85		75		55		45		ns

Notes:

- All voltages referenced to V_{SS}.
- Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
- Timing reference levels for both input and output signals are the specified worst-case logic levels.
- V_{CC} is used in the output buffer only. I_{CC} will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, V_{CC} is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode V_{CC}

may be reduced to zero without affecting stored data or refresh operations.

- Output loading is two standard TTL loads plus 100pF capacitance.
- Both RAS and CAS must be low read data. Access timing will depend on the relative positions of their falling edges. When t_{RCD} is less than the maximum value shown, access time depends on RAS and t_{RAC} governs. When t_{RCD} is more than the maximum value shown access time depends on CAS and t_{CAC} governs. The maximum value listed for t_{RCD} is shown for reference purposes only and does not restrict operation of the part.

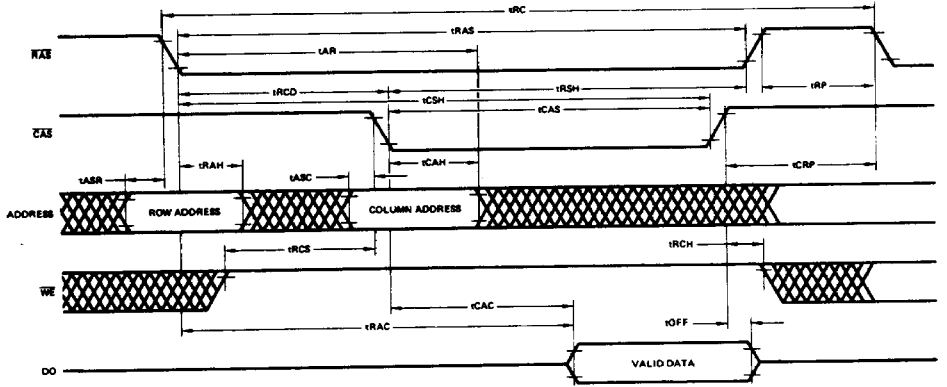
SWITCHING CHARACTERISTICS (Cont.)

7. Timing reference points for data input setup and hold times will depend on what type of write cycle is being performed and will be the later falling edge of \overline{CAS} or \overline{WE} .
8. At least eight initialization cycles that exercise \overline{RAS} should be performed after power-up and before valid operations are begun.
9. The t_{WCS} , t_{RPD} and t_{CWD} parameters are shown for reference purposes only and do not restrict the operating

flexibility of the part. When the falling edge of \overline{WE} follows the falling edge of \overline{CAS} by at most t_{WCS} , the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of \overline{WE} follows the falling edges of \overline{RAS} and \overline{CAS} by at least t_{RPD} and t_{CWD} respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of \overline{WE} may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.

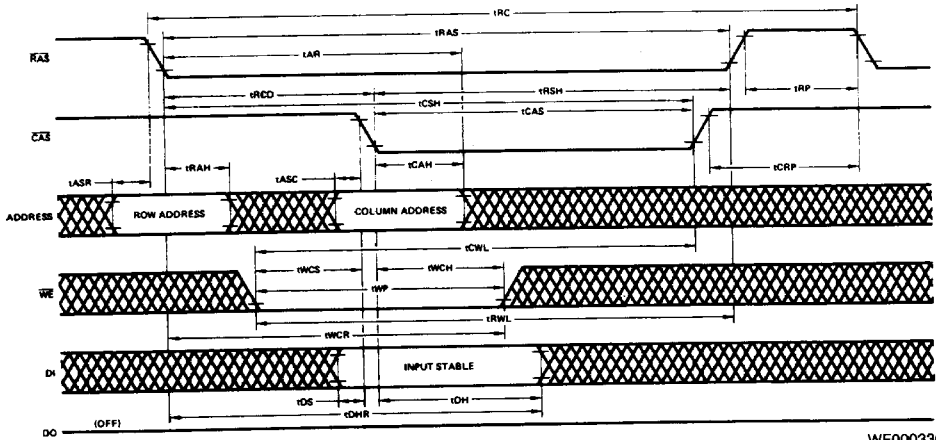
SWITCHING WAVEFORMS

READ CYCLE



WF000320

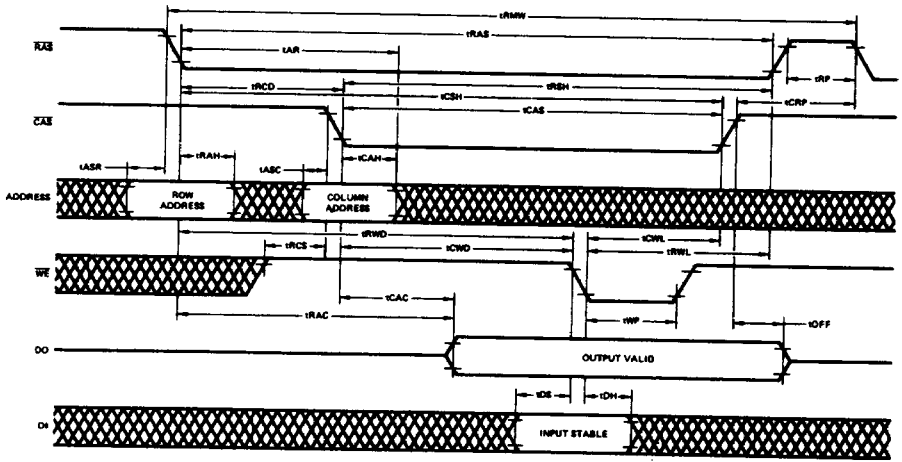
WRITE CYCLE (EARLY WRITE)



WF000330

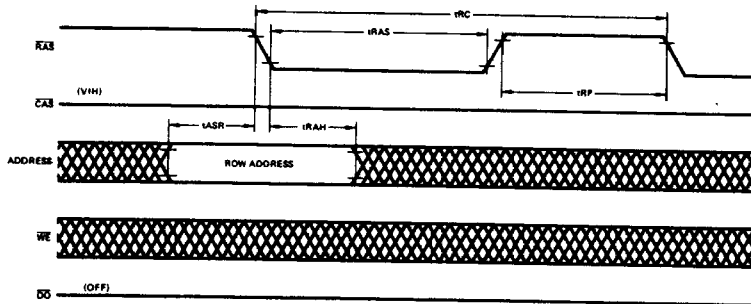
SWITCHING WAVEFORMS (Cont.)

READ-WRITE/READ-MODIFY-WRITE CYCLE



WF000340

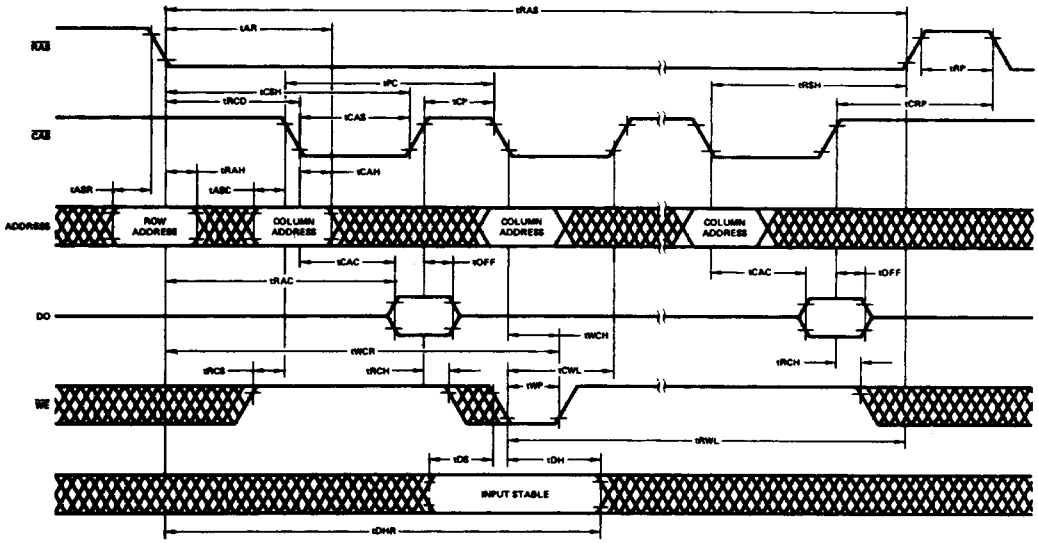
RAS ONLY REFRESH CYCLE



WF000350

SWITCHING WAVEFORMS (Cont.)

PAGE MODE CYCLE



WF000360