Rochester Electronics®

Datasheet

PM7224

8-Bit CMOS D/A Converter with Voltage Output

The PM-7224 is an improved version of the AD7224, which is an 8-bit, double-buffered, voltage output, CMOS digital-to-analog converter. It consists of a CMOS output amplifier, two 8-bit registers, interface control logic, and an R-2R resistor ladder network on a single monolithic chip.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

8-Bit CMOS D/A Converter with Voltage Output

PM-7224

FEATURES

- Internal Output Amplifier
- Double-Buffered Data Inputs
- Microprocessor Compatible
- Adjustment Free (±1/2 LSB Total Error)
- Guaranteed Monotonicity
- Single or Dual Supply Operation
- Space Saving 0.3" Wide 18-Pin DIP
- TTL/5V CMOS Compatible
- Fast Data Load, t_{WR} = 90ns (All Temperatures)
- Single Specification Table for Both Dual and Single Power Supply Operation
- Available In Die Form

APPLICATIONS

- Process/Industrial Controls
- Automatic Test Equipment
- Op Amp Offset Adjust
- Gain Adjust
- Attenuation
- Medical Equipment

ORDERING INFORMATION †

TOTAL UNADJUSTED ERROR	PACKAGE: MILITARY* TEMPERATURE	PACKAGE: EXTENDED INDUSTRIAL TEMPERATURE	PACKAGE: COMMERCIAL TEMPERATURE
±1/2 LSB	PM7224AX	PM7224EX	PM7224GP
±1 LSB	PM7224BX	PM7224FX	–
±1 LSB	PM7224BRC/883	PM7224FS	–
±1 LSB	–	PM7224FPC	–
±1 LSB	–	PM7224FP	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

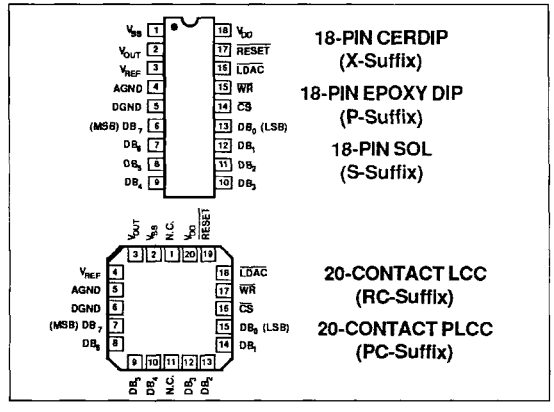
CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7224AX PM7224BX	AD7224UQ AD7224TQ	MIL
PM7224EX PM7224FX	AD7224CQ AD7224BQ	IND
PM7224GP PM7224FPC PM7224FP	AD7224LN AD7224KP AD7224KN	COM

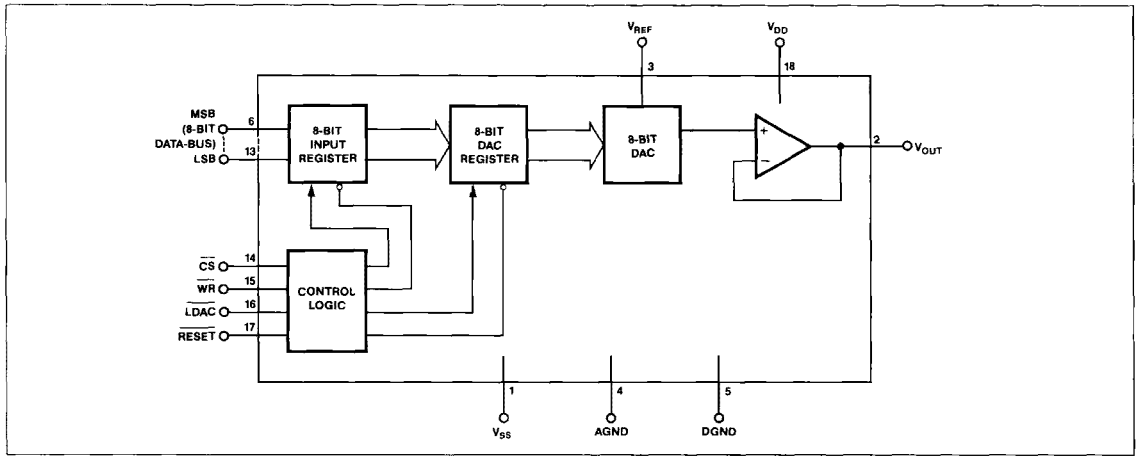
GENERAL DESCRIPTION

The PM-7224 is an improved version of the AD7224, which is an 8-bit, double-buffered, voltage output, CMOS digital-to-analog converter. It consists of a CMOS output amplifier, two 8-bit registers, interface control logic, and an R-2R resistor ladder network on a single monolithic chip.

PIN CONNECTIONS



FUNCTIONAL BLOCK DIAGRAM



PC board-space and costs are greatly reduced by eliminating the need for an external amplifier and associated trim circuitry.

Excellent zero code error is achieved for both single and dual supply operation by laser trimming the offset during manufacturing. The internal amplifier can deliver up to 5mA into a 2kΩ load and can drive a 3300pF capacitive load.

A reset pin simplifies system power-up and/or calibration cycles. It allows the DAC to momentarily be reset to 0V and function like a zero-override when both registers are transparent; however, the DAC output will remain at 0V when both registers are latched.

The PM-7224 can be operated with either a single or dual supply; however, zero code error can be improved using dual supplies.

PMI's advanced oxide-isolated, silicon-gate, CMOS process allows the PM-7224's analog and digital circuitry to be manufactured on the same chip. This, coupled with PMI's highly-stable thin-film R-2R resistor ladder, aids in the PM-7224's excellent full-scale and zero-code error temperature coefficients. It also results in an inherently reliable DAC and output amplifier.

The PM-7224 is a CMOS monolithic chip that fits into a space saving 18-pin, 0.3" wide, DIP package. With faster AC timing and tighter single and dual supply operation specifications, it is an improved replacement for the AD7224.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

V_{DD} to AGND or DGND ..... −0.3V, +17V
V_{SS} to AGND or DGND ..... −7V, V_{DD}
V_{DD} to V_{SS} ..... −0.3V, +24V
AGND to DGND ..... −0.3, V_{DD}
Digital Input Voltage to DGND ..... −0.3V, V_{DD}
V_{REF} to AGND ..... −0.3V, V_{DD}
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}
Operating Temperature
Military, AX/BX ..... −55°C to +125°C
Extended Industrial, EX/FX/FP/FPC/FS ..... −40°C to +85°C
Commercial, GP ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 5)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (X)	84	15	°C/W
18-Pin Plastic DIP (P)	75	33	°C/W
20-Contact LCC (RC)	98	38	°C/W
18-Pin SOL (S)	89	27	°C/W
20-Contact PLCC (PC)	76	36	°C/W

NOTES:
1. Outputs may be shorted to AGND provided the package power dissipation is not exceeded. Typical output short circuit current to AGND is 50mA.
2. The digital inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high-energy electrostatic fields. Keep device in conductive foam at all times until ready for use.
3. Use proper anti-static handling procedures.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum ratings conditions for extended periods may affect device reliability.
5. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: V_{DD} = +11.4V to +16.5V; V_{SS} = −5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} − 4V); or SINGLE SUPPLY: V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; T_A = −55°C to +125°C apply for PM-7224AX/BX; T_A = −40°C to +85°C apply for PM-7224EX/FX/FP/FPC/FS; T_A = 0°C to +70°C for PM-7224GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7224 MIN	PM-7224 TYP	PM-7224 MAX	UNITS
STATIC ACCURACY						
Resolution	N		8	–	–	Bits
Total Unadjusted Error (Note 1)	TUE	PM-7224A/E/G	–	–	±1/2	LSB
		PM-7224B/F	–	–	±1	
Relative Accuracy	INL	PM-7224A/E/G	–	–	±1/2	LSB
		PM-7224B/F	–	–	±1	
Differential Nonlinearity (Note 2)	DNL	PM-7224A/E/G	–	–	±1/2	LSB
		PM-7224B/F	–	–	±1	
Full-Scale Error	G_{FSE}	PM-7224A/E/G	–	–	±1/2	LSB
		PM-7224B/F	–	–	±1	
Full-Scale Temperature Coefficient (Note 3)	T_{CGFS}		–	±1	±20	ppm/°C
Zero Error Code	V_{ZSE}	DUAL SUPPLY:				mV
		PM-7224A/E/G	–	–	±5	
		PM-7224B/F	–	–	±20	
		SINGLE SUPPLY:				
		PM-7224A/E/G	–	–	±10	
		PM-7224B/F	–	–	±20	
Zero Error Code Temperature Coefficient (Note 3)	TCV_{ZS}		–	±10	–	µV/°C

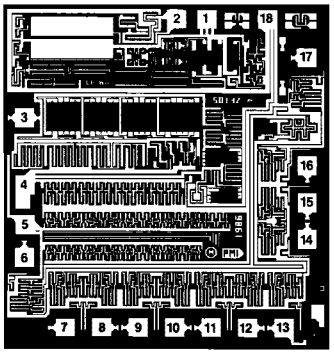
Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: V_{DD} = +11.4V to +16.5V; V_{SS} = –5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} – 4V); or SINGLE SUPPLY: V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V; T_A = –55°C to +125°C apply for PM-7224AX/BX; T_A = –40°C to +85°C apply for PM-7224EX/FX/FP/FPC/FS; T_A = 0°C to +70°C for PM-7224GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7224 MIN	PM-7224 TYP	PM-7224 MAX	UNITS
REFERENCE INPUT						
Voltage Range (Note 4)		DUAL SUPPLY ONLY	2	—	(V_{DD} – 4)	V
Input Resistance	R_{IN}		8	—	—	kΩ
Input Capacitance (Note 3)	C_{IN}	Digital Inputs = all 1's	—	—	100	pF
DIGITAL INPUTS						
Digital Input High	V_{INH}		2.4	—	—	V
Digital Input Low	V_{INL}		—	—	0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	—	—	±1	μA
Input Capacitance (Note 3)	C_{IN}		—	—	8	pF
Input Coding				BINARY		
POWER SUPPLIES						
Power Supply Rejection Ratio	PSRR		—	—	0.005%	%/%
Positive Supply Current (Note 5)	I_{DD}	T_A = +25°C T_A = Full Temp Range	— —	— —	4 6	mA
Negative Supply Current (Note 5)	I_{SS}	DUAL SUPPLY ONLY T_A = +25°C T_A = Full Temp Range	— —	— —	3 5	mA
DYNAMIC PERFORMANCE						
V_{OUT} Slew Rate (Note 3)	SR		2.5	—	—	V/μS
V_{OUT} Settling Time Positive or Negative (Note 3, 6)	t_S		—	—	5	μS
Digital Feedthrough (Note 3)	Q		—	10	—	nVs
Minimum Load Resistance	$R_{L(MIN)}$	V_{OUT} = +10V	2	—	—	kΩ
SWITCHING CHARACTERISTICS (Note 3)						
Chip Select/Load DAC Pulse-Width	t_1		90	—	—	ns
Write/Reset Pulse-Width	t_2		90	—	—	ns
Chip Select/Load DAC to Write Setup Time	t_3		0	—	—	ns
Chip Select/Load DAC to Write Hold Time	t_4		0	—	—	ns
Data Valid to Write Setup Time	t_5		90	—	—	ns
Data Valid to Write Hold Time	t_6		10	—	—	ns

NOTES:
1. Includes Full Scale Error, Relative Accuracy, and Zero Code Error.
2. All devices guaranteed monotonic over the full operating temperature range.
3. Guaranteed by design and not subject to production test.
4. V_{DD} – 4 volts is the maximum reference voltage for the above specifications.
5. V_{IN} = V_{INL} or V_{INH}; outputs unloaded.
6. V_{REF} = +10V; to where output settles to 1/2 LSB.

DICE CHARACTERISTICS



DIE SIZE 0.094 × 0.099 inch, 9306 sq. mils
(2.39 × 2.52 mm, 6.0 sq. mm)

1. V_{SS}
2. V_{OUT}
3. V_{REF}
4. AGND
5. DGND
6. DB7(MSB)
7. DB6
8. DB5
9. DB4
10. DB3
11. DB2
12. DB1
13. DB0(LSB)
14. $\overline{CS}$
15. $\overline{WR}$
16. $\overline{LDAC}$
17. $\overline{RESET}$
18. V_{DD}

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

WAFER TEST LIMITS: DUAL SUPPLY: $V_{DD} = +11.4V$ to $+16.5V$; $V_{SS} = -5V \pm 10\%$; AGND = DGND = 0V; $V_{REF} = +2V$ to $(V_{DD} - 4V)$. SINGLE SUPPLY: $V_{DD} = +15V \pm 5\%$; V_{SS} = AGND = DGND = 0V; $V_{REF} = +10V$; unless otherwise noted.

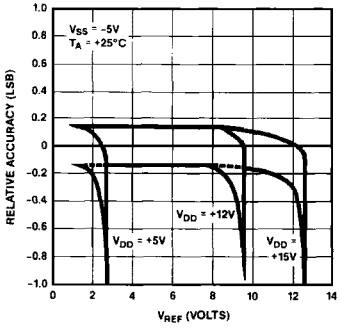
PARAMETER	SYMBOL	CONDITIONS	PM-7224GBC LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits
Total Unadjusted Error (Note 1)	TUE		±1	LSB MAX
Relative Accuracy	INL		±1	LSB MAX
Differential Nonlinearity (Note 2)	DNL		±1	LSB MAX
Full Scale Error	G_{FSE}		±1	LSB MAX
Zero Code Error	V_{ZSE}		±20	mV MAX
REFERENCE INPUT				
Voltage Range (Note 3)	V_{REF}	DUAL SUPPLY ONLY	2 to $(V_{DD} - 4V)$	V
Reference Input Resistance	R_{IN}		8	kΩ MIN
DIGITAL INPUTS				
Digital Inputs High	V_{INH}		2.4	V MIN
Digital Inputs Low	V_{INL}		0.8	V MAX
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	μA MAX
Input Coding			BINARY	
POWER SUPPLIES				
Positive Supply Current (Note 4)	I_{DD}		4	mA MAX
Negative Supply Current (Note 4)	I_{SS}	DUAL SUPPLY ONLY	3	mA MAX

NOTES:
1. Includes Full Scale Error, Relative Accuracy, and Zero Code Error.
2. All dice guaranteed monotonic over the full operating temperature range.
3. $V_{DD} - 4$ volts is the maximum reference voltage for the above specifications.
4. $V_{IN} = V_{INL}$ or V_{INH}; output unloaded.

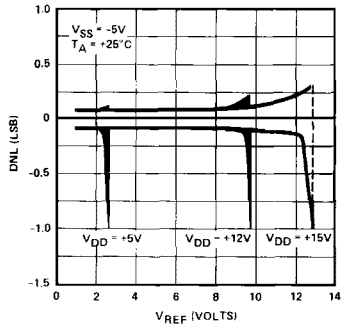
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

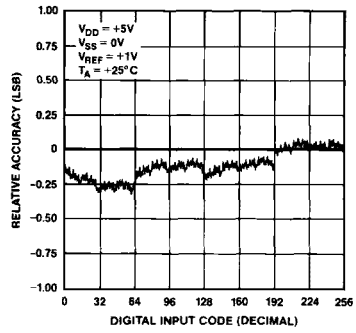
RELATIVE ACCURACY vs V_{REF}



DIFFERENTIAL NONLINEARITY vs V_{REF}



RELATIVE ACCURACY WITH SINGLE +5V SUPPLY



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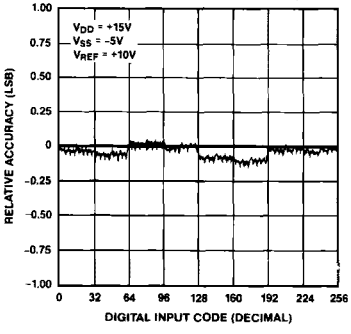
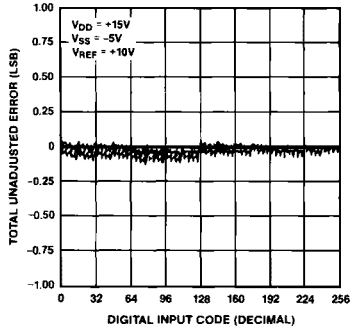
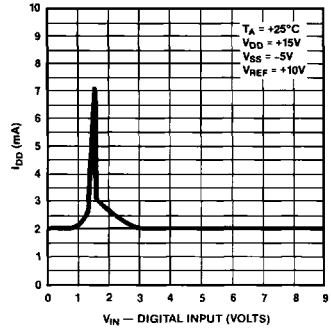
RELATIVE ACCURACY vs CODE AT T_A = -55°C, +25°C, +125°C (ALL SUPERIMPOSED)



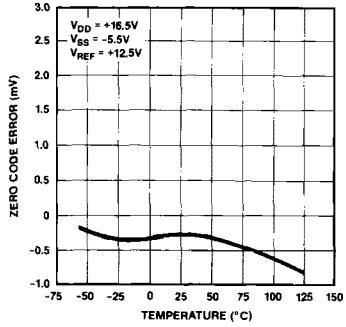
TOTAL UNADJUSTED ERROR vs CODE AT T_A = -55°C, +25°C, +125°C (ALL SUPERIMPOSED)



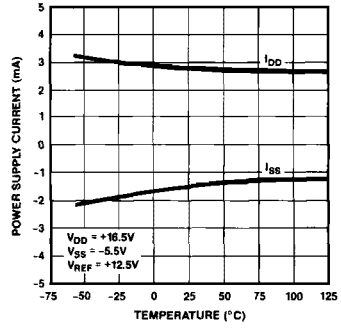
POSITIVE SUPPLY CURRENT (I_{DD}) vs LOGIC LEVEL



ZERO CODE ERROR vs TEMPERATURE

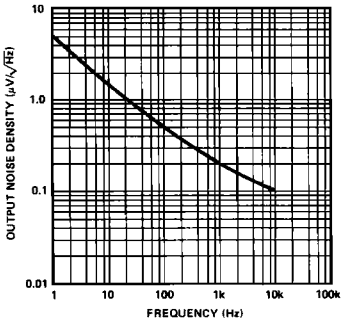


POWER SUPPLY CURRENT vs TEMPERATURE

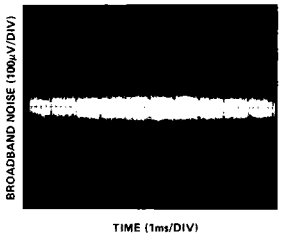


TYPICAL PERFORMANCE CHARACTERISTICS

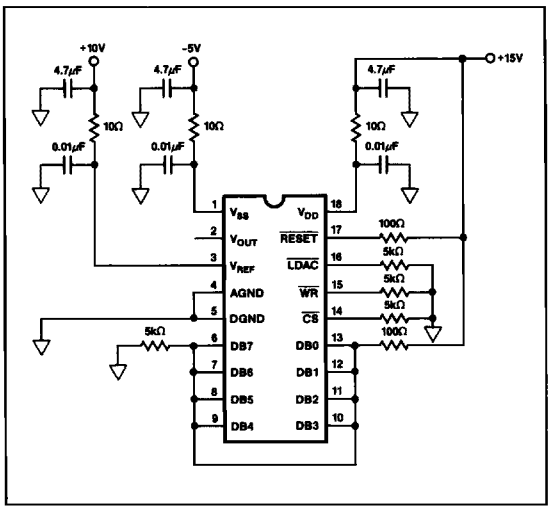
OUTPUT VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY



BROADBAND NOISE



BURN-IN CIRCUIT



PARAMETER DEFINITIONS

TOTAL UNADJUSTED ERROR

This specification includes Full-Scale-Error, Relative Accuracy, and Zero-Code-Error. Ideal full scale output is $V_{REF} - 1$ LSB, and 1 LSB is $V_{REF} \times (2^{-n})$.

DIGITAL FEEDTHROUGH

Digital feedthrough are the switching transients coupled to the output of the DAC due to a change in digital input code. It is expressed in nano-Volt-seconds and measured with $V_{REF} = 0V$.

Refer to PMI 1986 Data Book Section 11 for additional digital-to-analog converter definitions.

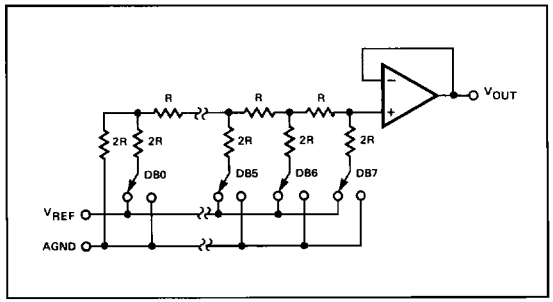
GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The PM-7224 contains an output buffer amplifier, a highly-stable, thin-film, R-2R resistor ladder network, 8-bit input and DAC registers, and interface control logic. Also included are eight single-pole double-throw NMOS transistor switches. These transistors were designed to switch between V_{REF} and AGND and are controlled by the digital input code.

A simplified circuit of the R-2R resistor ladder and output is illustrated in Figure 1. The ladder is shown connected to the amplifier in the voltage-mode configuration. The advantages gained in operating the ladder in the voltage mode are two-fold: it allows the DAC to be operated with a single supply, and the ladder resistance/capacitance modulation encountered in the current mode configuration are eliminated. The modulation (caused by the varying digital code) is now presented to the low-impedance reference voltage source (most voltage reference output-impedances are low enough so that its output voltage will not be affected by the varying digital code). The

FIGURE 1: Simplified DAC Circuit Configuration. (Switches are shown for all "1's" on the digital inputs.)



amplifier's input terminal now "sees" a constant resistance/capacitance and thus, the output offset voltage modulation is eliminated. Also, digital glitches fed through the switch capacitance to the output will be greatly reduced; it will be absorbed by the low output-impedance of the external reference resulting in a "cleaner" output voltage.

Figure 1 also shows the amplifier configured to operate as a buffer amplifier resulting in no signal inversion from input to output (V_{REF} to V_{OUT}). Also, note that analog ground (AGND) is accessible and can be biased above digital ground (DGND) for some applications; more on this in the applications section under AGND biasing.

For proper operation, maximum V_{REF} should be limited to V_{DD} minus 4 volts. This means that in order to operate the DAC with +10V at the reference input terminal, V_{DD} must be at least +14V.

The voltage output equation is given by:

$$V_{OUT} = V_{REF} \times D/256$$

where D is the digital input code integer number that is between 0 and 255.

BUFFER AMPLIFIER SECTION

The R-2R resistor ladder network has a typical resistance of 10kΩ; a 100kΩ load would cause a 23 LSB gain error. Therefore, in order to drive a 2kΩ load, the R-2R ladder was terminated with a stable CMOS buffer amplifier. The amplifier can drive 10 volts across a 2kΩ load delivering 5mA, and can easily drive a 3300pF capacitive load. The PM-7224's output can also withstand an indefinite short-circuit to AGND to typically 50mA. The output may also be shorted to any voltage between V_{DD} and V_{SS}; however, care must be taken to not exceed the device maximum power dissipation.

The amplifier's output stage is an intrinsic NPN bipolar transistor. It is derived from the P^- well and the substrate. This transistor provides a low-impedance high-output current capability using only a small part of the chip area. The emitter of this NPN transistor is loaded with a 400μA NMOS current-source referenced to V_{SS}. This current is sunk into the negative supply allowing the amplifier's output to go directly to ground.

A simplified schematic of the output amplifier is shown in Figure 2. It shows the current-source connection between the NPN output transistor's emitter and V_{SS}. Figure 3 depicts a typical plot for the dual and single supply current sink capability of the DAC versus output voltage. Let's take a closer look at what happens to its behavior by referring to Figures 2 and 3.

It can be seen that with dual supplies the current-source is still in its high impedance (saturation) state when the output reaches 0 volts. This is due to the 5 volts (V_{SS}) across the current-source that is sinking the 400μamps. When V_{SS} = 0 volts, however, the current sink capability is reduced as the output voltage approaches 0 volts; the current-source is coming out of its saturation region and starts appearing resistive.

The amplifier's current-limiting and buffering abilities are achieved with an NMOS transistor and a series resistor, see Figure 2. The transistor operates as a source follower driving the resistor and output transistor.

The amplifier's internal gain stages were designed so that they maintain sufficient gain over its common mode range; this results in good offset performance over the specified voltage range. In addition, the amplifier's offset voltage is laser-trimmed during the manufacturing process; this eliminates offset trimming by the user in most applications. The amplifier's offset is included in the data sheet under "total unadjusted error" specification.

2

FIGURE 2: Amplifier Output Stage

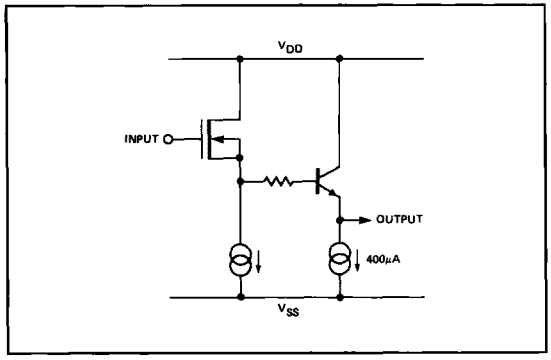
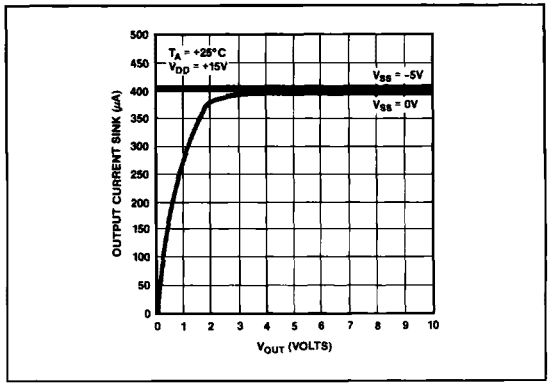


FIGURE 3: DAC Output Current Sink



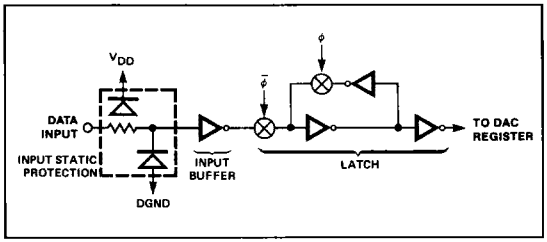
DIGITAL SECTION

The digital inputs are CMOS inverters. They were designed to convert TTL and 5V CMOS input logic levels into CMOS levels to drive the internal circuitry. A simple internal 5V regulator is used to ensure the high speed timing requirements.

The PM-7224's digital inputs are TTL and CMOS (5V) compatible between the V_{DD} range of +11.4V to +16.5V. As shown in Figure 4, these inputs are protected from electrostatic-discharge and build-up with two internal distributed-diodes; they are connected between V_{DD} and DGND. Each input has a typical input current of less than 1nA.

Figure 4 also shows the equivalent logic circuit for the digital data input register structure. This circuit drives the DAC register. The digital controls ϕ and $\bar{\phi}$ shown are controlled by the external $\overline{WR}$, and $\overline{CS}$ signals.

FIGURE 4: Input Register Structure



INTERFACE CONTROL LOGIC SECTION

Figure 5 shows the PM-7224's input control logic structure with its input register and DAC register; also shown is the equivalent logic circuitry. The $\overline{WR}$ signal is required when loading data into either register and is used in conjunction with either $\overline{CS}$ or $\overline{LDAC}$. $\overline{CS}$ loads data into the input register, and $\overline{LDAC}$ loads data into the DAC register. Data is latched in the input register on the rising edge of the $\overline{WR}$ pulse. The DAC's analog output voltage is determined by the data contained in the DAC register. See Table 1.

TABLE 1

$\overline{RESET}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	FUNCTION
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register is Transparent
H	H	↓	L	Input Register is Latched
H	L	L	H	DAC Register is Transparent
H	L	↓	H	DAC Register is Latched
L	X	X	X	Both Registers Loaded with all Zeros
↓	H	H	H	Both Registers Loaded with all Zeros and the Output Remains at Zero
↓	L	L	L	Both Registers are Transparent (output follows the input)

H = High State; L = Low State; X = Don't Care

Table 1 shows that the DAC is transparent when $\overline{WR}$, $\overline{CS}$, and $\overline{LDAC}$ are low, and the input register is transparent when $\overline{WR}$ and $\overline{CS}$ only are low. Also shown is the data being latched into the input register on the rising edge of the $\overline{WR}$ signal.

Also provided with the PM-7224 is a $\overline{RESET}$ pin as shown in Figure 5. A low $\overline{RESET}$ signal will reset both registers to zero. If the DAC is in the transparent mode, the DAC output will go to 0V for as long as the reset line remains low. If the DAC is in the latched mode, the output will go to 0V (and remain there) on the rising edge of the reset signal.

Figure 6 shows the PM-7224 write timing diagram.

FIGURE 5: Input Control Logic

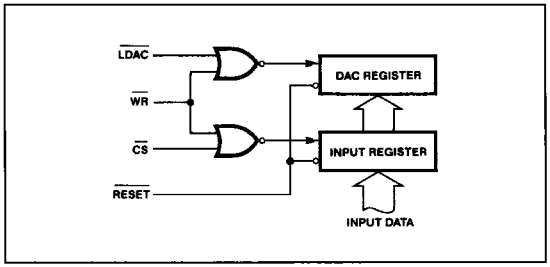
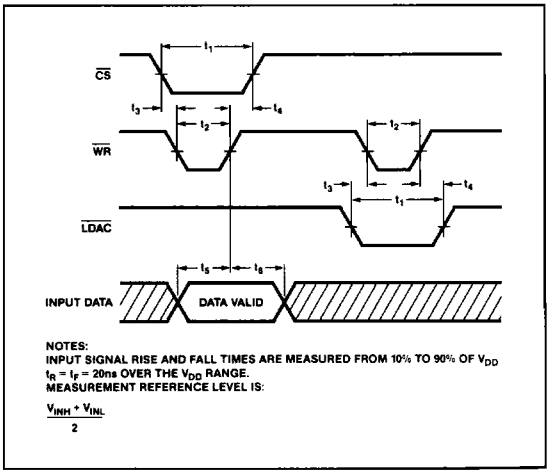


FIGURE 6: Write Timing Diagram



APPLICATIONS INFORMATION

POWER SUPPLY

The PM-7224 data sheet is specified with a dual or single power supply condition. The dual supply specifications are specified with a positive supply (V_{DD}) range of +11.4V to +16.5V and a negative supply (V_{SS}) of −5V. The specified reference voltage (V_{REF}) under these conditions range from +2V to V_{DD} − 4V. For those applications requiring +10 volts at the output (V_{REF} = +10V), V_{DD} must be +14V minimum to meet data sheet limits.

The specified V_{REF} for the single supply specifications is +10V. V_{REF} voltage limitation of V_{DD} − 4V for dual or single power supply applications must be observed. This will ensure that the PM-7224's multiplying capabilities are preserved.

Although the PM-7224 can operate well with either a single or dual power supply, improved zero-code error can be achieved by using dual supplies.

DYNAMIC PERFORMANCE

The PM-7224's settling time is limited by the internal amplifier's slew rate; however, it sports an impressive settling time of 5μs using a dual or single power supply. Settling time is not affected by the DAC's output voltage polarity, positive or negative. The PM-7224 also has minimum signal overshoot or ringing.

AGND BIASING

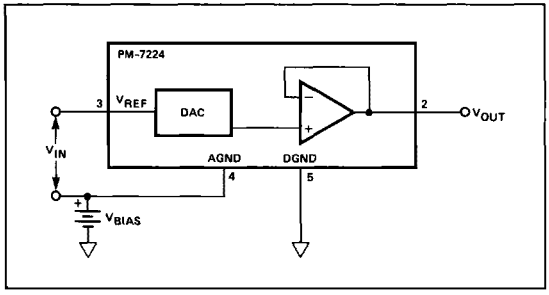
Some applications may require a DC offset voltage level at the DAC's output. This may be easily accomplished with the PM-7224; the desired DC offset voltage can be applied to the AGND pin as shown in Figure 7. The DAC's TTL/CMOS compatibility is not affected. Note that V_{DD} and V_{SS} must be referenced to DGND.

The DAC's output voltage expression under this condition is:

$$V_{OUT} = \text{AGND bias} + V_{IN} \times D/256$$

where AGND bias is the voltage level above DGND and D is the digital input code integer number that is between 0 and 255.

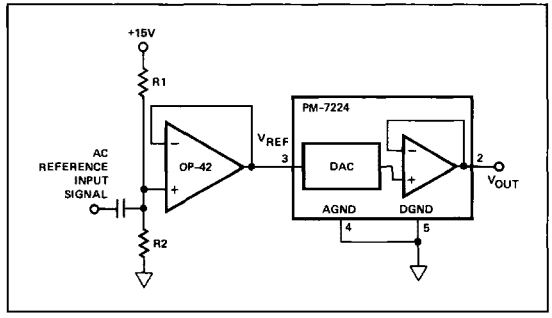
FIGURE 7: AGND Biasing Scheme



MULTIPLYING OPERATION

The PM-7224 has good multiplying capabilities if the reference input signal level is kept within +2V and V_{DD} − 4V, with V_{DD} of +16.5 V, the maximum input signal level is +12.5V; however, it is recommended that V_{DD} = +15V ±5% and the AC voltage swing between +2V and V_{DD} − 4V. The signal must be AC coupled and biased up with a voltage divider as shown in Figure 8. A buffer amplifier should be used to ensure that the DAC's V_{REF} impedance does not load the resistor divider, R1 and R2.

FIGURE 8: AC Signal Input Scheme

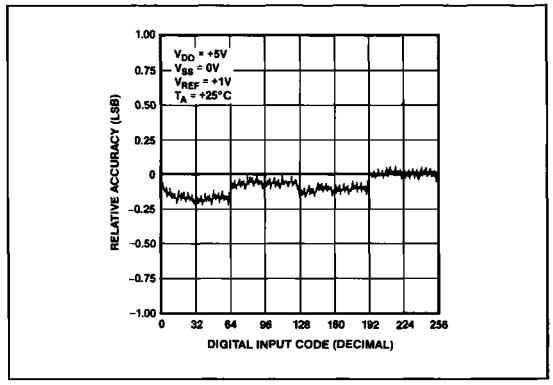


The V_{REF} small-signal frequency response (−3dB bandwidth) for the PM-7224 is typically 1.5MHz. Its small-signal harmonic distortion is less than −57dB at 1kHz and −55dB at 100kHz.

+5V SINGLE SUPPLY OPERATION

Although a +5V performance specification table is not listed, the PM-7224 can operate well with only a single +5V supply (see Figure 9). This will then limit the reference input voltage level to a maximum of +1V; the V_{DD} − 4V limitation must still be observed.

FIGURE 9: Relative Accuracy With Single +5V Operation



GENERAL GROUND MANAGEMENT

Digital transient voltages between AGND and DGND can appear as noise at the PM-7224's output. It is, therefore, recommended that AGND and DGND be tied together at the device socket; each ground is then brought out separately to their respective common ground points. A word of caution is worth mentioning here: ground loops can be created if both grounds are tied together at more than one location, i.e., at the device socket and back at the power supplies, or at any other location. These ground loops can cause noisy digital ground currents to flow through the analog ground paths and destroy its integrity. Analog ground should be maintained as a high quality ground.

If system requirements dictate the use of one common return line for each ground, then the DAC should be placed as close to the power supplies as possible. Also, for those systems that require both grounds be separated, two Schottky diodes should be tied in inverse parallel between AGND and DGND at the device socket.

POWER SUPPLY DECOUPLING

Power supply decoupling capacitors are important to suppress oscillations and noise transients from entering the system and causing system errors. Noise transients are generated from digital switching or switching power supplies; and oscillations on the power supply lines are caused by lead inductances combined with stray capacitance.

High and low frequency decoupling capacitors at the device socket is strongly recommended; a 0.01μF ceramic in parallel with a 1 to 10μF tantalum decoupling capacitors should be used.

BASIC APPLICATIONS

UNIPOLAR OPERATION

Figure 10 shows the PM-7224 configured to operate in the unipolar mode; the analog output voltage is of a single positive polarity only. Table 2 shows the code for this mode of operation.

FIGURE 10: Unipolar Operation

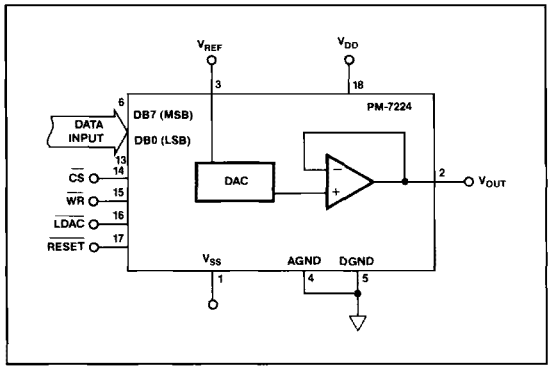


TABLE 2: Unipolar Code Table (Refer to Figure 10)

DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{225}{256}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$+V_{REF}\left(\frac{128}{256}\right) = \frac{+V_{REF}}{2}$
0	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

It shows no signal inversion between $+V_{REF}$ and V_{OUT}. Also note that the analog output voltage is equal to V_{REF} multiplied by the digital input code, hence, multiplying DAC.

The expression for 1 LSB and V_{OUT} is:

$$1\ LSB = V_{REF} \times 2^{-8}, \text{ or } V_{REF} \times 1/256$$

and

$$V_{OUT} = V_{REF} \times D/256$$

where D is the digital input integer between 0 and 255.

BIPOLAR OPERATION

Figure 11 illustrates the bipolar mode of operation for the PM-7224. This mode allows the output voltage to swing plus or minus and is determined by the digital input code; see Table 3 for R1 = R2. This configuration requires an external amplifier and two resistors.

The output voltage expression is given by:

$$V_{OUT} = ((1 + R2/R1) \times D/256 \times V_{REF}) - (R2/R1 \times V_{REF})$$

where D is the digital input code integer between 0 and 255. If R1 = R2, then V_{OUT} becomes:

$$V_{OUT} = (2 \times D/256 - 1) \times V_{REF}$$

To keep gain and offset errors at a minimum, R1 and R2 should be matched to ±0.1% and track over the operating temperature range of interest.

FIGURE 11: Bipolar Operation

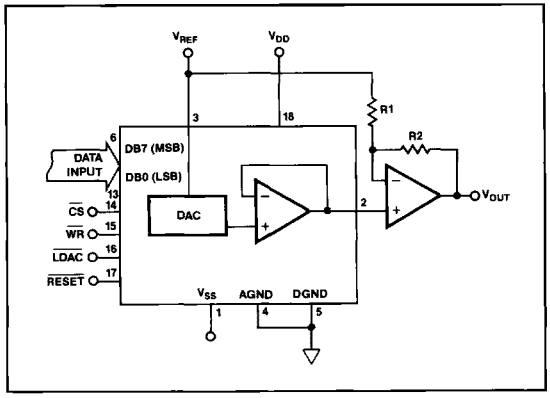


TABLE 3: Bipolar (Offset Binary) Code Table (Refer to Figure 11)

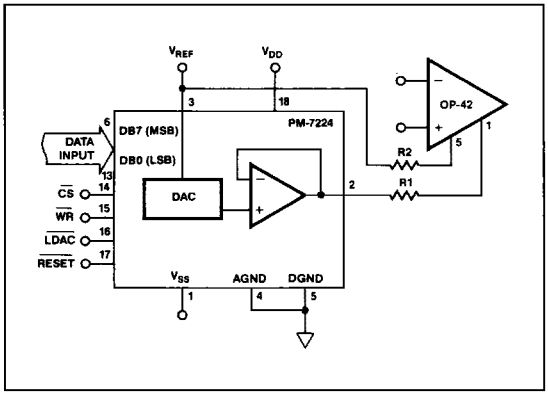
DAC DATA INPUT MSB							LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	0V
0	1	1	1	1	1	1	1	$-V_{REF}\left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	$-V_{REF}\left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

PROGRAMMABLE OP AMP OFFSET ADJUST

The PM-7224 can be used for op amp offset trim adjustments under microprocessor control. Offsets caused by temperature drifts can also be trimmed by the microprocessor during a periodic calibration cycle.

The PM-7224 uses the input offset voltage nulling pins normally provided on most amplifiers as shown in Figure 12. A fixed bias current is provided to pin 5 of the op amps offset null pin with R2, and R1 (connected to the DAC's voltage output pin) provides the variable current to pin 1.

FIGURE 12: Op Amp Offset Adjust (See Text)



For a plus or minus (±) offset adjust control, the current through R1 must equal the current through R2 when the PM-7224 is at half scale, binary code = 10000000.

The resistor values R1 and R2 should be chosen to give the required offset adjustment range desired. Lower values provide a larger range; however, resolution will be sacrificed. Reversing the op amp connections, pin 1 and 5, will reverse the offset adjustment direction.

Some op amps are not provided with offset adjustment pins. In these cases, the circuit configuration of Figure 13 can be used. Again, the current through resistor R4 must equal the current through R3 with the PM-7224 at half scale, digital code = 10000000. With the circuit components shown, the maximum adjustment range is ±5mV. Incremental adjustment resolution is 39μV per bit.

MICROPROCESSOR INTERFACING

Interfacing the PM-7224 to a microprocessor is simplified by virtue of its loading structure simplicity. Data from the processor is loaded into the DAC by use of only two control lines, the write strobe ($\overline{WR}$) and chip select ($\overline{CS}$). The data is then output with the $\overline{WR}$ and $\overline{LDAC}$ signal. Figures 14 through 17 show various popular microprocessor interface configurations.

FIGURE 14: PM-7224 to 8085A Interface (Only digital interface portion of PM-7224 shown for clarity.)

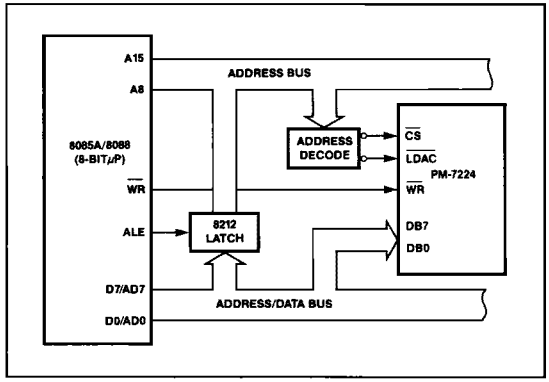


FIGURE 15: PM-7224 to Z-80 Interface (Only digital interface portion of PM-7224 shown for clarity.)

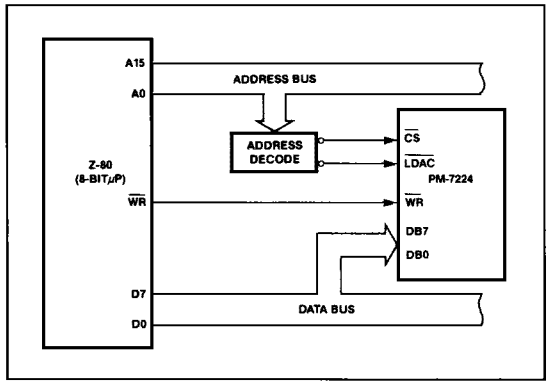


FIGURE 13: Alternate Offset Adjust (See Text)

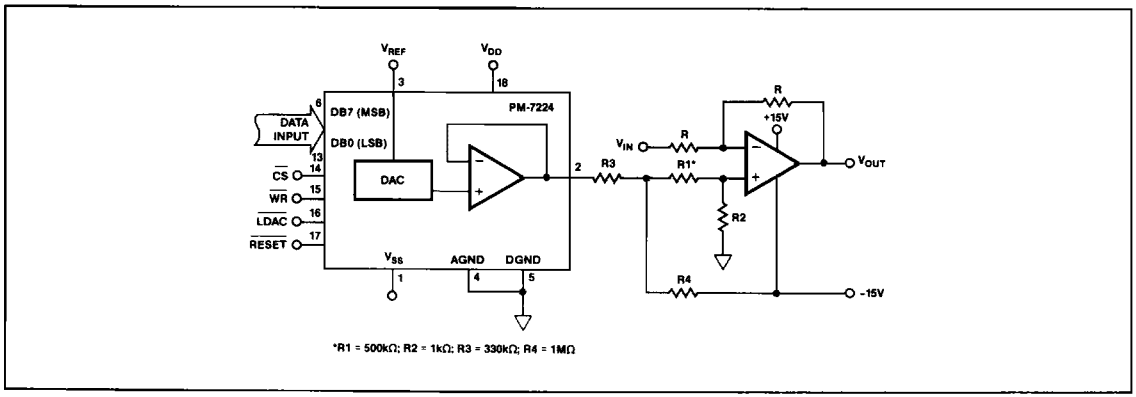


FIGURE 16: PM-7224 to 6809 Interface (Only digital interface portion of PM-7224 shown for clarity.)

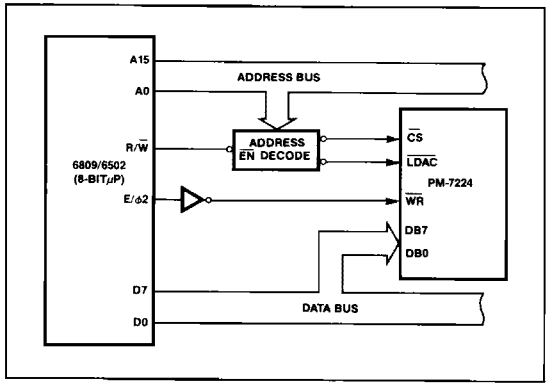


FIGURE 17: PM-7224 to 68008 Microprocessor (Only digital interface portion of PM-7224 shown for clarity.)