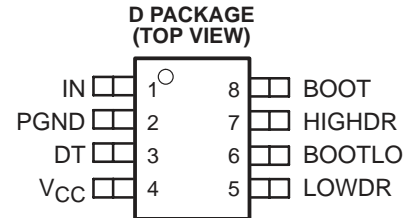


# TPS2836, TPS2837 SYNCHRONOUS-BUCK MOSFET DRIVER WITH DEAD-TIME CONTROL

SLVS224B – NOVEMBER 1999 – REVISED AUGUST 2002

- Floating Bootstrap or Ground-Reference High-Side Driver
- Adaptive Dead-Time Control
- 50-ns Max Rise/Fall Times With 3.3-nF Load
- 2.4-A Typical Output Current
- 4.5-V to 15-V Supply Voltage Range
- TTL-Compatible Inputs
- Internal Schottky Bootstrap Diode
- Low Supply Current...3 mA Typical
- Ideal for High-Current Single or Multiphase Power Supplies
- – 40°C to 125°C Operating Virtual Junction-Temperature Range



## description

The TPS2836 and TPS2837 are MOSFET drivers for synchronous-buck power stages. These devices are ideal for designing a high-performance power supply using switching controllers that do not have MOSFET drivers. The drivers are designed to deliver minimum 2-A peak currents into large capacitive loads. The high-side driver can be configured as ground-reference or as floating-bootstrap. An adaptive dead-time control circuit eliminates shoot-through currents through the main power FETs during switching transitions and provides high efficiency for the buck regulator.

The TPS2836 has a noninverting input, while the TPS2837 has an inverting input. These drivers, available in 8-terminal SOIC packages, operate over a junction temperature range of – 40°C to 125°C.

### AVAILABLE OPTIONS

T <sub>J</sub>	PACKAGED DEVICES
	SOIC (D)
– 40°C to 125°C	TPS2836D TPS2837D

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS2836DR)

### Related Synchronous MOS FET Drivers

DEVICE NAME	ADDITIONAL FEATURES	INPUTS	
TPS2830	ENABLE, SYNC and CROWBAR	CMOS	Noninverted
TPS2831			Inverted
TPS2832	W/O ENABLE, SYNC and CROWBAR	CMOS	Noninverted
TPS2833			Inverted
TPS2834	ENABLE, SYNC and CROWBAR	TTL	Noninverted
TPS2835			Inverted



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

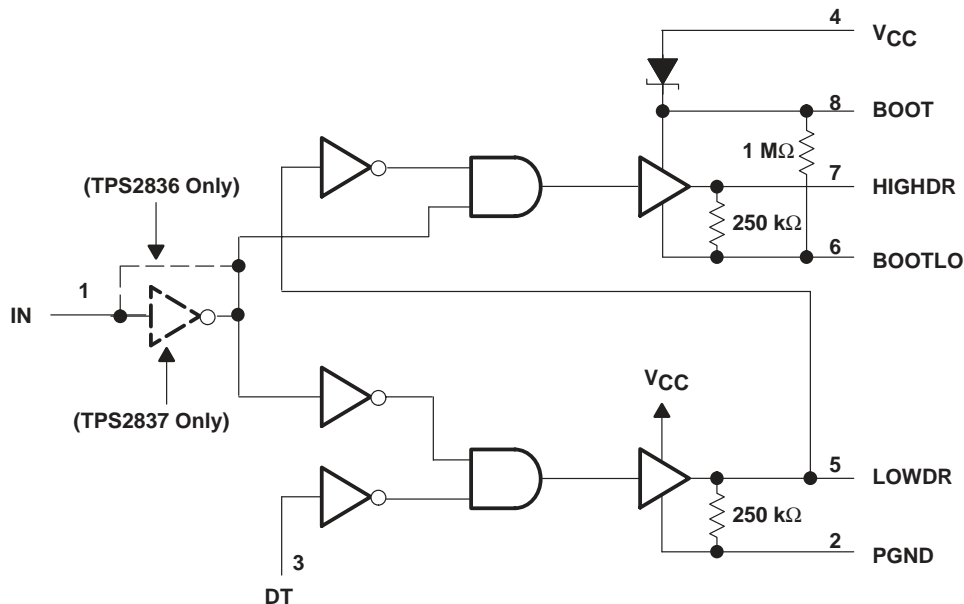
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated

# TPS2836, TPS2837 SYNCHRONOUS-BUCK MOSFET DRIVER WITH DEAD-TIME CONTROL

SLVS224B – NOVEMBER 1999 – REVISED AUGUST 2002

## functional block diagram



## Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BOOT	8	I	Bootstrap terminal. A ceramic capacitor is connected between BOOT and BOOTLO to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 $\mu\text{F}$ and 1 $\mu\text{F}$ .
BOOTLO	6	O	This terminal connects to the junction of the high-side and low-side MOSFETs.
DT	3	I	Dead-time control terminal. Connect DT to the junction of the high-side and low-side MOSFETs
HIGHDR	7	O	Output drive for the high-side power MOSFET
IN	1	I	Input signal to the MOSFET drivers (noninverting input for the TPS2836; inverting input for the TPS2837).
LOWDR	5	O	Output drive for the low-side power MOSFET
PGND	2		Power ground. Connect to the FET power ground.
VCC	4	I	Input supply. Recommended that a 1 $\mu\text{F}$ capacitor be connected from VCC to PGND.

# TPS2836, TPS2837 SYNCHRONOUS-BUCK MOSFET DRIVER WITH DEAD-TIME CONTROL

SLVS224B – NOVEMBER 1999 – REVISED AUGUST 2002

## detailed description

### low-side driver

The low-side driver is designed to drive low  $r_{DS(on)}$  N-channel MOSFETs. The current rating of the driver is 2 A, source and sink.

### high-side driver

The high-side driver is designed to drive low  $r_{DS(on)}$  N-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured as a ground-reference driver or a floating bootstrap driver. The internal bootstrap diode is a Schottky for improved drive efficiency. The maximum voltage that can be applied between the BOOT terminal and ground is 30 V.

### dead-time (DT) control

Dead-time control prevents shoot-through current from flowing through the main power FETs during switching transitions by controlling the turnon times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is low, and the low-side driver is not allowed to turn on until the voltage at the junction of the power FETs ( $V_{drain}$ ) is low; the TTL-compatible DT terminal connects to the junction of the power FETs.

### IN

The IN terminal is a TTL-compatible digital terminal that is the input control signal for the drivers. The TPS2836 has a noninverting input; the TPS2837 has an inverting input.

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 16 V
Input voltage range: BOOT to PGND (high-side driver ON)	–0.3 V to 30 V
BOOTLO to PGND	–0.3 V to 16 V
BOOT to BOOTLO	–0.3 V to 16 V
IN	–0.3 V to 16 V
DT	–0.3 V to 30 V
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$	–40°C to 125°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to PGND.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	600 mW	6.0 mW/°C	330 mW	240 mW

### recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.5		15	V
Input voltage   BOOT to PGND	4.5		28	V



# TPS2836, TPS2837 SYNCHRONOUS-BUCK MOSFET DRIVER WITH DEAD-TIME CONTROL

SLVS224B – NOVEMBER 1999 – REVISED AUGUST 2002

electrical characteristics over recommended operating virtual junction temperature range,  
 $V_{CC} = 6.5\text{ V}$ ,  $C_L = 3.3\text{ nF}$  (unless otherwise noted)

## supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		4.5		15	V
	Quiescent current	V <sub>CC</sub> = 15 V, V <sub>(ENABLE)</sub> = LOW			100	μA
	Quiescent current	V <sub>CC</sub> = 15 V, V <sub>(ENABLE)</sub> = HIGH		300	400	
	Quiescent current	V <sub>CC</sub> = 12 V, f <sub>SWX</sub> = 200 kHz, C <sub>LOWDR</sub> = 50 pF, C <sub>HIGHDR</sub> = 50 pF, BOOTLO grounded, See Note 2		3		mA

NOTE 2: Ensured by design, not production tested.

## output drivers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Peak output-current	High-side sink (see Note 4)	Duty cycle < 2%, t <sub>pw</sub> < 100 μs (see Note 3)	V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 4.5 V, V <sub>HIGHDR</sub> = 4 V	0.7	1.1	A	
		V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 6.5 V, V <sub>HIGHDR</sub> = 5 V	1.1	1.5			
		V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 12 V, V <sub>HIGHDR</sub> = 10.5 V	2	2.4			
	High-side source (see Note 4)	Duty cycle < 2%, t <sub>pw</sub> < 100 μs (see Note 3)	V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 4.5 V, V <sub>HIGHDR</sub> = 0.5 V	1.2	1.4	A	
			V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 6.5 V, V <sub>HIGHDR</sub> = 1.5 V	1.3	1.6		
			V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 12 V, V <sub>HIGHDR</sub> = 1.5 V	2.3	2.7		
	Low-side sink (see Note 4)	Duty cycle < 2%, t <sub>pw</sub> < 100 μs (see Note 3)	V <sub>CC</sub> = 4.5 V, V <sub>LOWDR</sub> = 4 V	1.3	1.8	A	
			V <sub>CC</sub> = 6.5 V, V <sub>LOWDR</sub> = 5 V	2	2.5		
			V <sub>CC</sub> = 12 V, V <sub>LOWDR</sub> = 10.5 V	3	3.5		
	Low-side source (see Note 4)	Duty cycle < 2%, t <sub>pw</sub> < 100 μs (see Note 3)	V <sub>CC</sub> = 4.5 V, V <sub>LOWDR</sub> = 0.5 V	1.4	1.7	A	
			V <sub>CC</sub> = 6.5 V, V <sub>LOWDR</sub> = 1.5 V	2	2.4		
			V <sub>CC</sub> = 12 V, V <sub>LOWDR</sub> = 1.5 V	2.5	3		
Output resistance	High-side sink (see Note 4)	V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 4.5 V, V <sub>HIGHDR</sub> = 0.5 V			5	Ω	
		V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 6.5 V, V <sub>HIGHDR</sub> = 0.5 V			5		
		V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 12 V, V <sub>HIGHDR</sub> = 0.5 V			5		
	High-side source (see Note 4)	Duty cycle < 2%, t <sub>pw</sub> < 100 μs (see Note 3)	V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 4.5 V, V <sub>HIGHDR</sub> = 4 V			75	Ω
			V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 6.5 V, V <sub>HIGHDR</sub> = 6 V			75	
			V <sub>BOOT</sub> - V <sub>BOOTLO</sub> = 12 V, V <sub>HIGHDR</sub> = 11.5 V			75	
	Low-side sink (see Note 4)	Duty cycle < 2%, t <sub>pw</sub> < 100 μs (see Note 3)	V <sub>DRV</sub> = 4.5 V, V <sub>LOWDR</sub> = 0.5 V			9	Ω
			V <sub>DRV</sub> = 6.5 V, V <sub>LOWDR</sub> = 0.5 V			7.5	
			V <sub>DRV</sub> = 12 V, V <sub>LOWDR</sub> = 0.5 V			6	
	Low-side source (see Note 4)	Duty cycle < 2%, t <sub>pw</sub> < 100 μs (see Note 3)	V <sub>DRV</sub> = 4.5 V, V <sub>LOWDR</sub> = 4 V			75	Ω
			V <sub>DRV</sub> = 6.5 V, V <sub>LOWDR</sub> = 6 V			75	
			V <sub>DRV</sub> = 12 V, V <sub>LOWDR</sub> = 11.5 V			75	

NOTES: 3. Ensured by design, not production tested.

4. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the r<sub>DS(on)</sub> of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.



**TPS2836, TPS2837**  
**SYNCHRONOUS-BUCK MOSFET DRIVER**  
**WITH DEAD-TIME CONTROL**

SLVS224B – NOVEMBER 1999 – REVISED AUGUST 2002

electrical characteristics over recommended operating virtual junction temperature range,  
 $V_{CC} = 6.5\text{ V}$ ,  $C_L = 3.3\text{ nF}$  (unless otherwise noted) (continued)

**dead-time**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH}$	High-level input voltage		LOWDR Over the $V_{CC}$ range (see Note 3)	0.7 $V_{CC}$		
$V_{IL}$	Low-level input voltage				1 V	
$V_{IH}$	High-level input voltage	DT Over the $V_{CC}$ range	2			V
$V_{IL}$	Low-level input voltage					1 V

NOTE 3: Ensured by design, not production tested.

**digital control terminals (IN)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH}$	High-level input voltage		Over the $V_{CC}$ range	2		
$V_{IL}$	Low-level input voltage				1 V	

switching characteristics over recommended operating virtual junction temperature range,  
 $C_L = 3.3\text{ nF}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rise time	HIGHDR output (see Note 3)		$V_{BOOT} = 4.5\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	60		
		$V_{BOOT} = 6.5\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	50			
		$V_{BOOT} = 12\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	50			
	LOWDR output (see Note 3)	$V_{CC} = 4.5\text{ V}$	40			ns
		$V_{CC} = 6.5\text{ V}$	30			
		$V_{CC} = 12\text{ V}$	30			
Fall time	HIGHDR output (see Note 3)	$V_{BOOT} = 4.5\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	50			ns
		$V_{BOOT} = 6.5\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	40			
		$V_{BOOT} = 12\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	40			
	LOWDR output (see Note 3)	$V_{CC} = 4.5\text{ V}$	40			ns
		$V_{CC} = 6.5\text{ V}$	30			
		$V_{CC} = 12\text{ V}$	30			
Propagation delay time	HIGHDR going low (excluding dead-time) (see Note 3)	$V_{BOOT} = 4.5\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	95			ns
		$V_{BOOT} = 6.5\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	80			
		$V_{BOOT} = 12\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	65			
	LOWDR going high (excluding dead-time) (see Note 3)	$V_{BOOT} = 4.5\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	80			ns
		$V_{BOOT} = 6.5\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	70			
		$V_{BOOT} = 12\text{ V}$ , $V_{BOOTLO} = 0\text{ V}$	60			
Propagation delay time	LOWDR going low (excluding dead-time) (see Note 3)	$V_{CC} = 4.5\text{ V}$	80			ns
		$V_{CC} = 6.5\text{ V}$	70			
		$V_{CC} = 12\text{ V}$	60			
Driver nonoverlap time	DT to LOWDR and LOWDR to HIGHDR (see Note 3)	$V_{CC} = 4.5\text{ V}$	40		170	ns
		$V_{CC} = 6.5\text{ V}$	25		135	
		$V_{CC} = 12\text{ V}$	15		85	

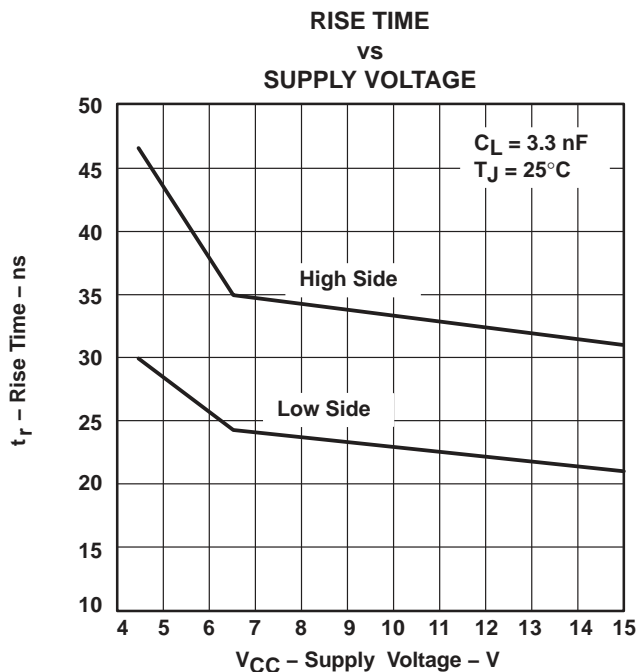
NOTE 3: Ensured by design, not production tested.



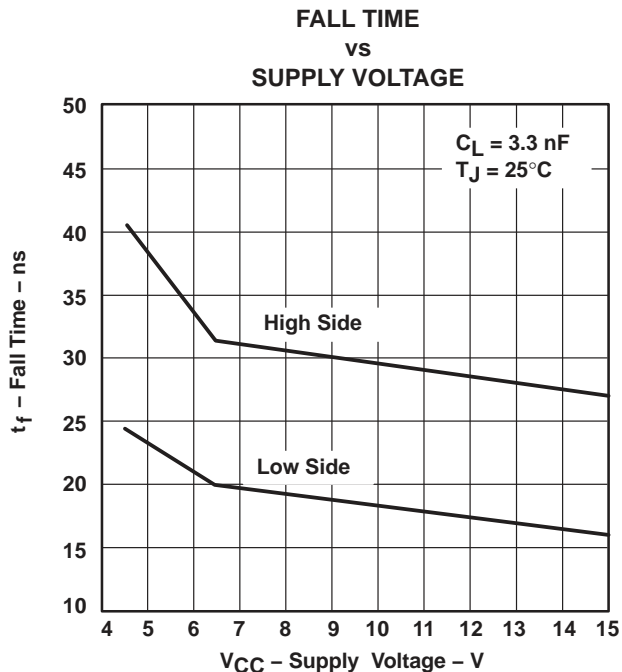
**TPS2836, TPS2837**  
**SYNCHRONOUS-BUCK MOSFET DRIVER**  
**WITH DEAD-TIME CONTROL**

SLVS224B – NOVEMBER 1999 – REVISED AUGUST 2002

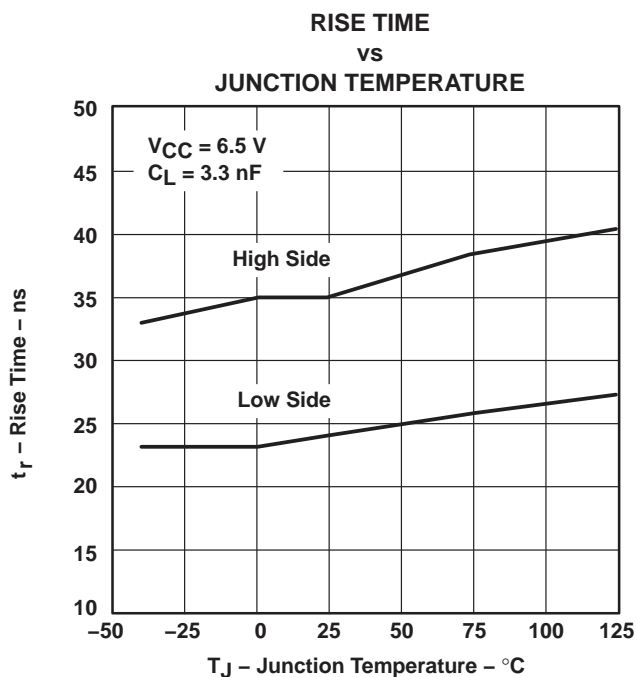
**TYPICAL CHARACTERISTICS**



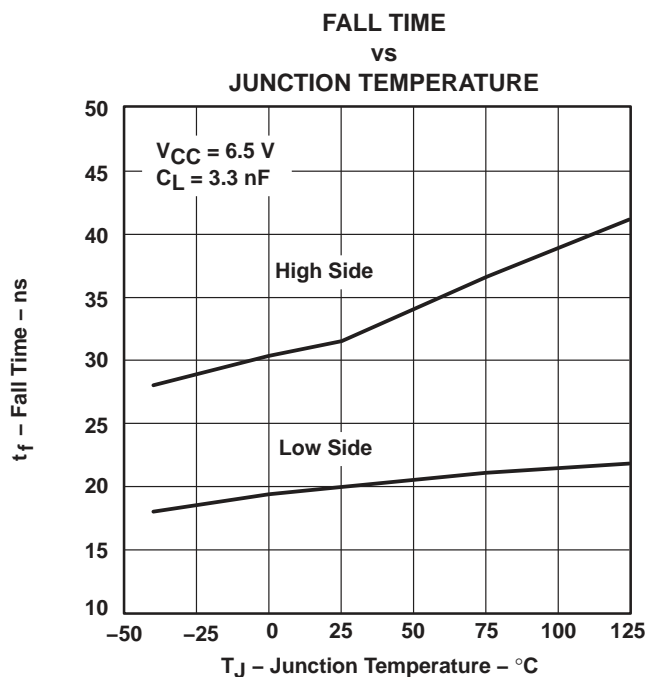
**Figure 1**



**Figure 2**



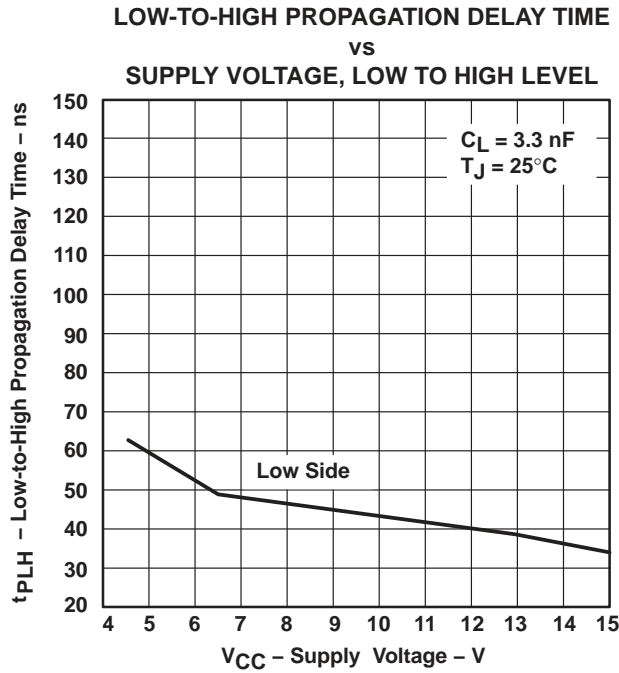
**Figure 3**



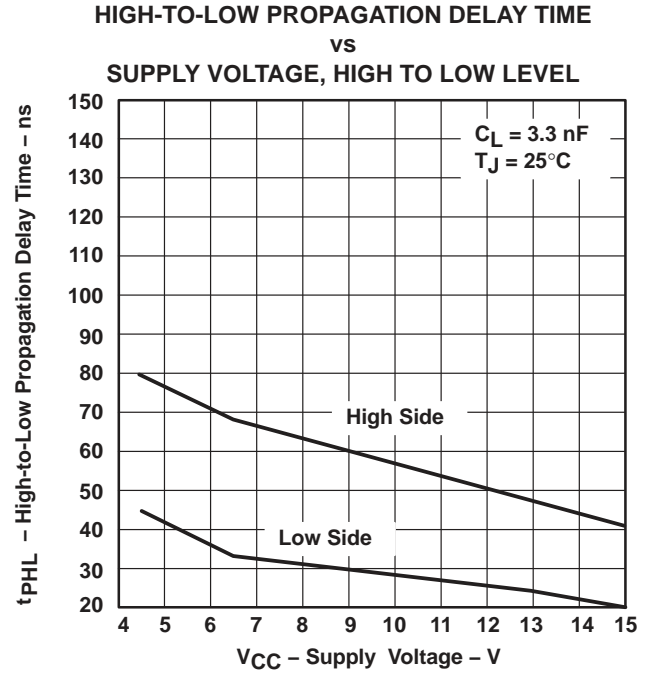
**Figure 4**



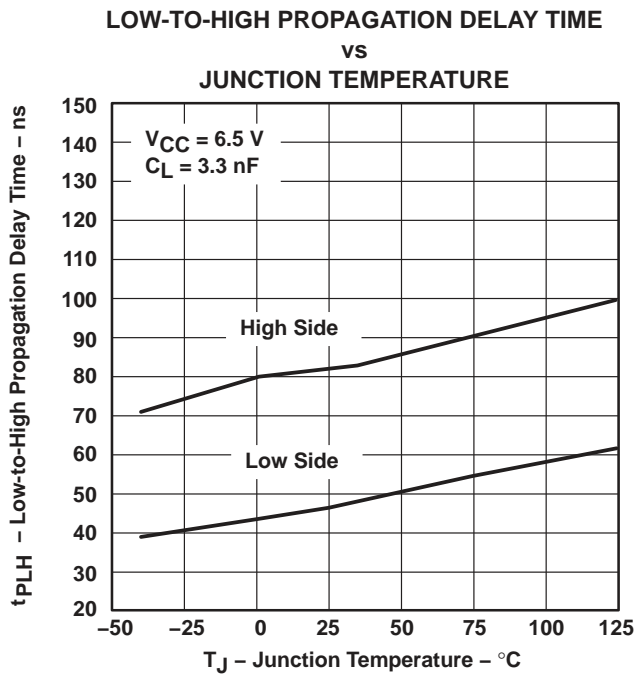
**TYPICAL CHARACTERISTICS**



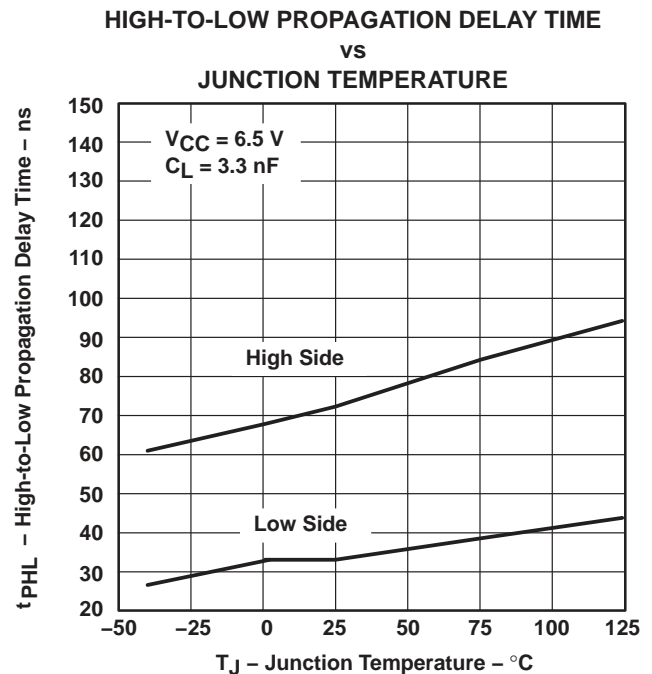
**Figure 5**



**Figure 6**



**Figure 7**



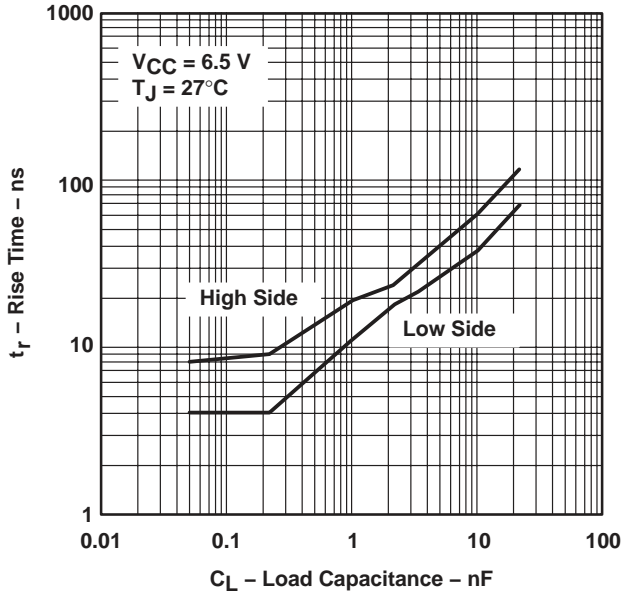
**Figure 8**

**TPS2836, TPS2837**  
**SYNCHRONOUS-BUCK MOSFET DRIVER**  
**WITH DEAD-TIME CONTROL**

SLVS224B – NOVEMBER 1999 – REVISED AUGUST 2002

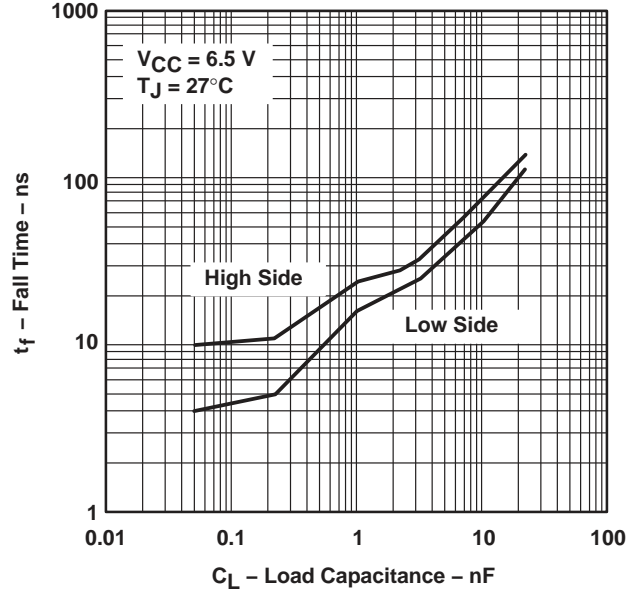
**TYPICAL CHARACTERISTICS**

**DRIVER-OUTPUT RISE TIME**  
**vs**  
**LOAD CAPACITANCE**



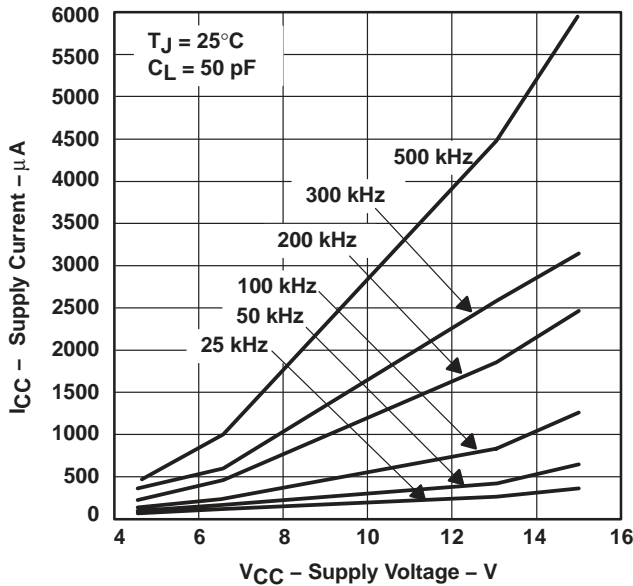
**Figure 9**

**DRIVER-OUTPUT FALL TIME**  
**vs**  
**LOAD CAPACITANCE**



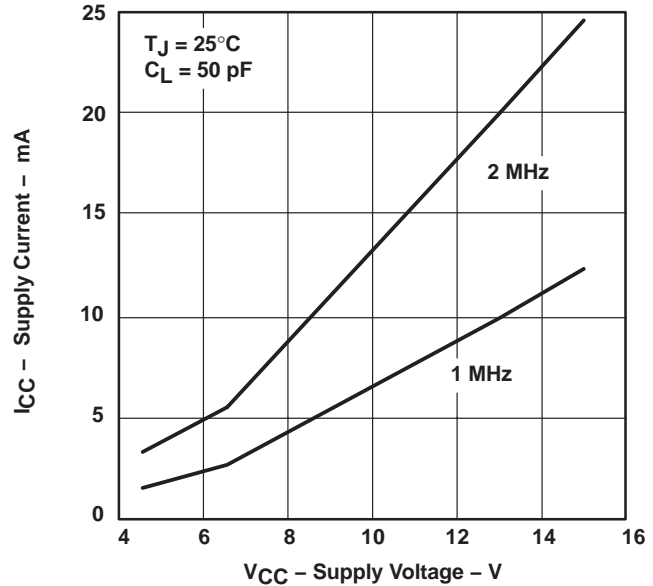
**Figure 10**

**SUPPLY CURRENT**  
**vs**  
**SUPPLY VOLTAGE**



**Figure 11**

**SUPPLY CURRENT**  
**vs**  
**SUPPLY VOLTAGE**



**Figure 12**





TYPICAL CHARACTERISTICS

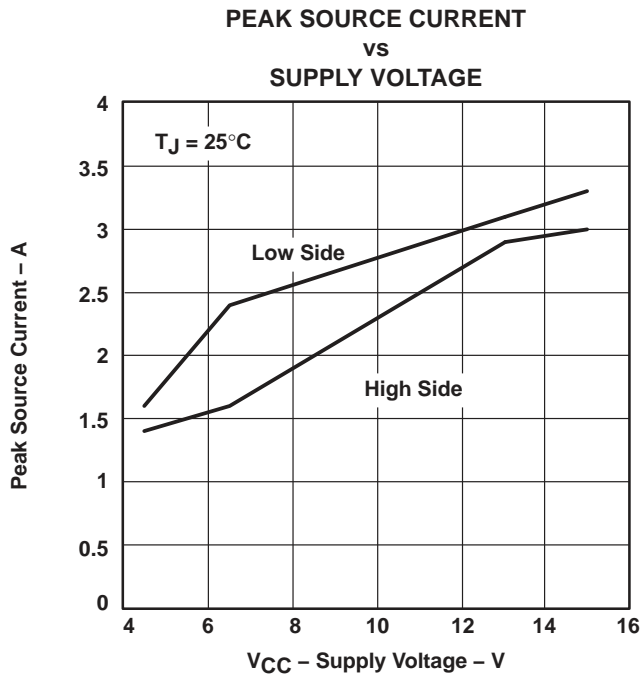


Figure 13

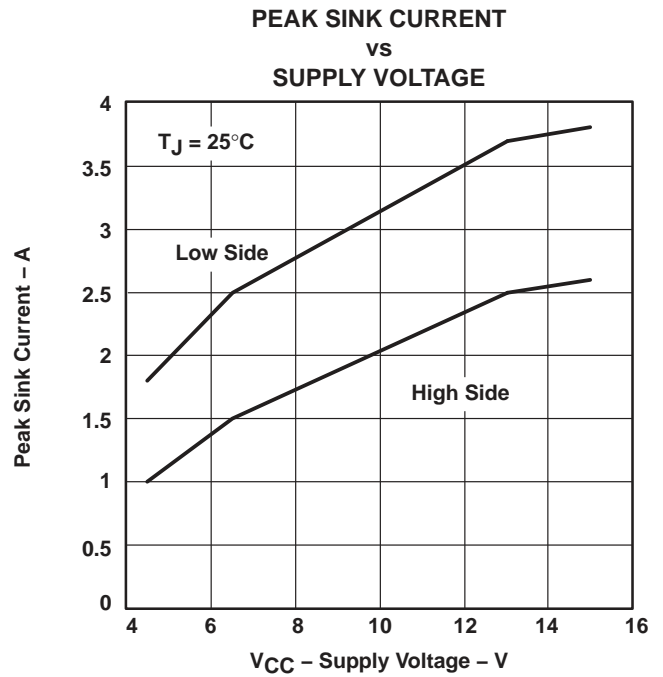


Figure 14

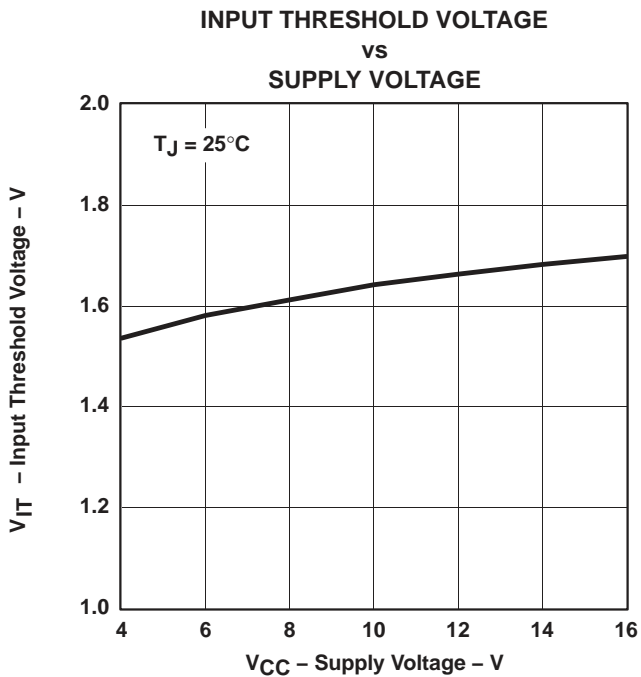


Figure 15

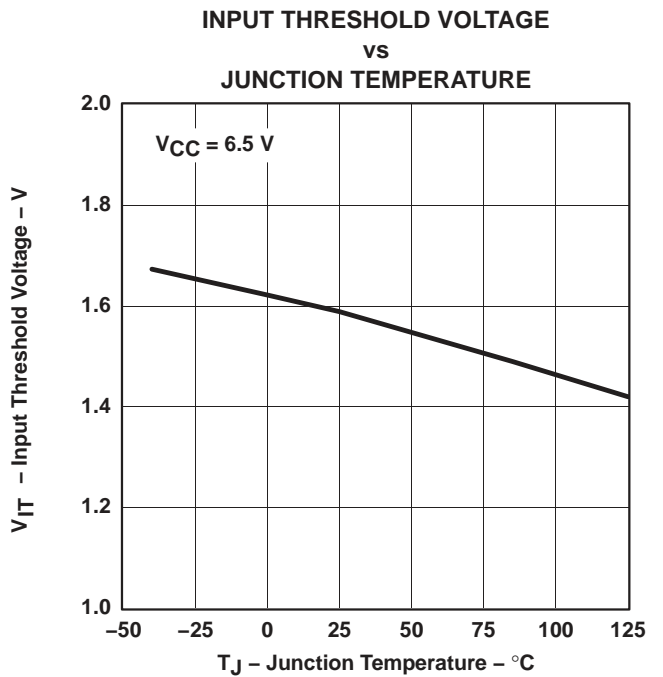


Figure 16

# TPS2836, TPS2837 SYNCHRONOUS-BUCK MOSFET DRIVER WITH DEAD-TIME CONTROL

SLVS224B – NOVEMBER 1999 – REVISED AUGUST 2002

## APPLICATION INFORMATION

Figure 17 shows the circuit schematic of a 100-kHz synchronous-buck converter implemented with a TL5001A pulse-width-modulation (PWM) controller and a TPS2837 driver. The converter operates over an input range from 4.5 V to 12 V and has a 3.3-V output. The circuit can supply 3 A continuous load and the transient load is 5 A. The converter achieves an efficiency of 94% for  $V_{IN} = 5\text{ V}$ ,  $I_{load} = 1\text{ A}$ , and 93% for  $V_{IN} = 5\text{ V}$ ,  $I_{load} = 3\text{ A}$ .

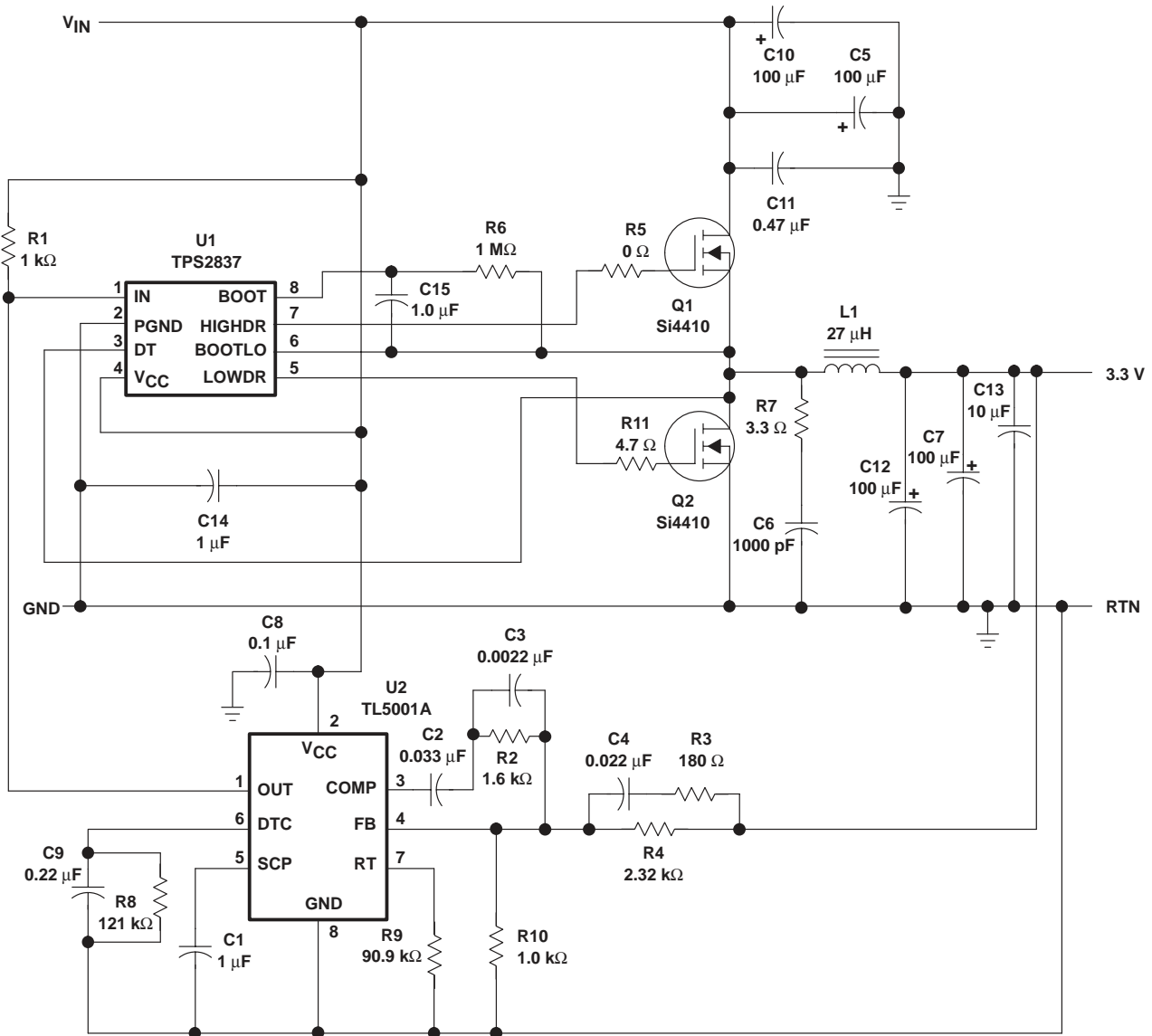


Figure 17. 3.3 V 3 A Synchronous-Buck Converter Circuit

## APPLICATION INFORMATION

Great care should be taken when laying out the PC board. The power-processing section is the most critical and will generate large amounts of EMI if not properly configured. The junction of Q1, Q2, and L1 should be very tight. The connection from Q1 drain to the positive sides of C5, C10, and C11 and the connection from Q2 source to the negative sides of C5, C10, and C11 should be as short as possible. The negative terminals of C7 and C12 should also be connected to Q2 source.

Next, the traces from the MOSFET driver to the power switches should be considered. The BOOTLO signal from the junction of Q1 and Q2 carries the large gate drive current pulses and should be as heavy as the gate drive traces. The bypass capacitor (C14) should be tied directly across  $V_{CC}$  and PGND.

The next most sensitive node is the FB node on the controller (terminal 4 on the TL5001A). This node is very sensitive to noise pickup and should be isolated from the high-current power stage and be as short as possible. The ground around the controller and low-level circuitry should be tied to the power ground as the output. If these three areas are properly laid out, the rest of the circuit should not have other EMI problems and the power supply will be relatively free of noise.

**TPS2836, TPS2837**  
**SYNCHRONOUS-BUCK MOSFET DRIVER**  
**WITH DEAD-TIME CONTROL**

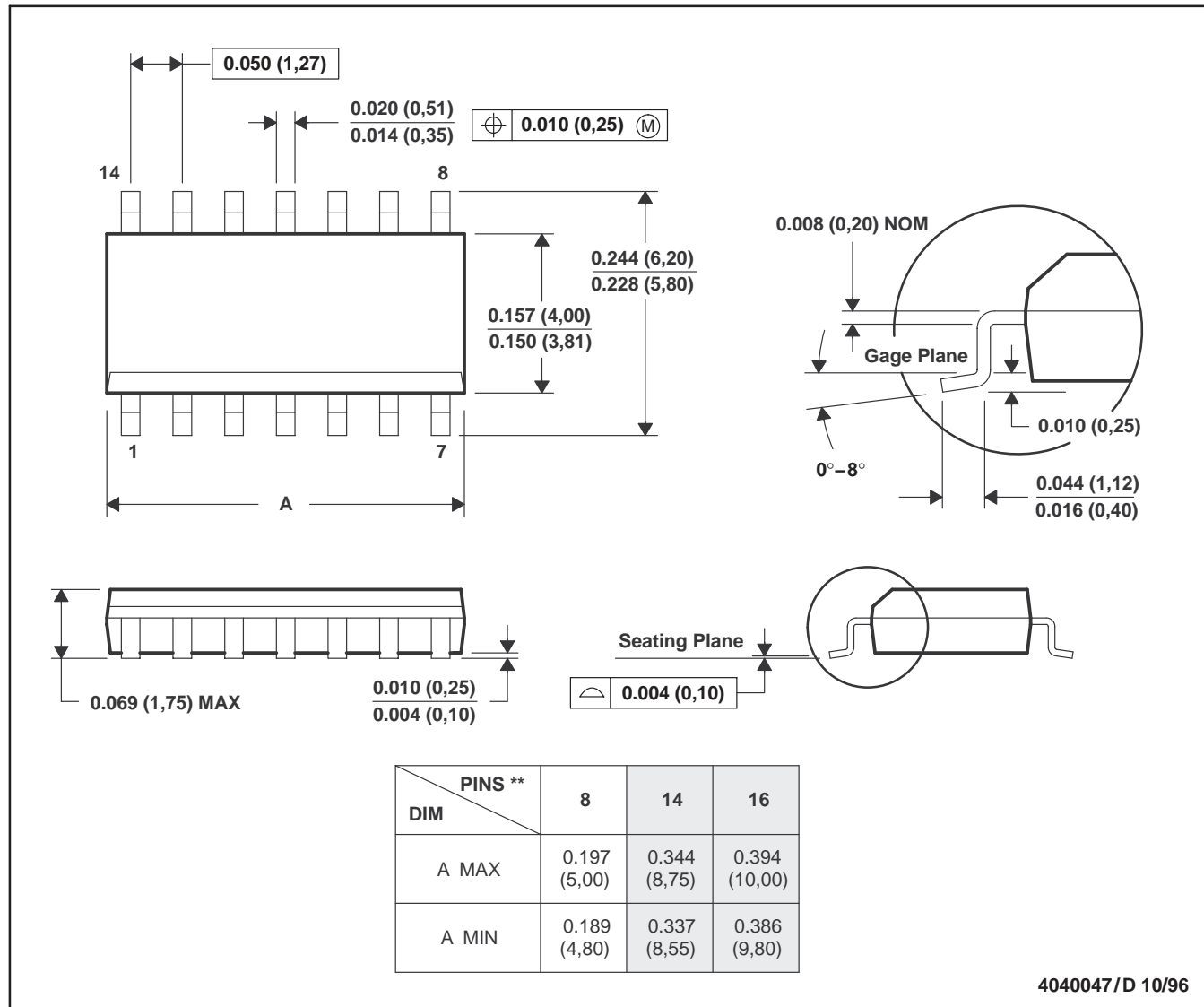
SLVS224B – NOVEMBER 1999 – REVISED AUGUST 2002

**MECHANICAL DATA**

**D (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



4040047/D 10/96

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2836D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2836	
TPS2836DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2836	Samples
TPS2837D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2837	
TPS2837DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2837	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

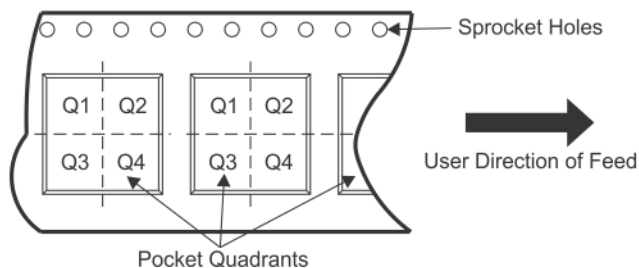
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2836DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2837DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2836DR	SOIC	D	8	2500	340.5	336.1	25.0
TPS2837DR	SOIC	D	8	2500	340.5	336.1	25.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS2836D	D	SOIC	8	75	507	8	3940	4.32
TPS2837D	D	SOIC	8	75	507	8	3940	4.32

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated