14-Bit, 125Msps ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **14-Bit Resolution**
- **125 Msps Sample Rate**
- **High SNR: 71.2 dBFS at 100-MHz f_{IN}**
- **High SFDR: 82 dBc at 100-MHz f_{IN}**
- **2.3-V_{PP} Differential Input Voltage**
- **Internal Voltage Reference**
- **3.3-V Single-Supply Voltage**
- **Analog Power Dissipation: 578 mW**
- **Serial Programming Interface**
- **TQFP-64 PowerPAD™ Package**
- **Recommended Amplifiers: OPA695, OPA847, THS3201, THS3202, THS4503, THS4509, THS9001**

APPLICATIONS

- **Wireless Communication**
  - **Communication Receivers**
  - **Base Station Infrastructure**
- **Test and Measurement Instrumentation**
- **Single and Multichannel Digital Receivers**
- **Communication Instrumentation**
  - **Radar, Infrared**
- **Video and Imaging**
- **Medical Equipment**

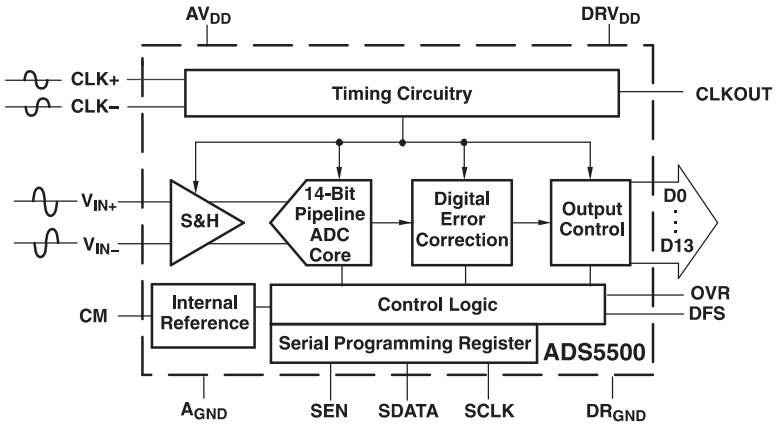
DESCRIPTION

The ADS5500 is a high-performance, 14-bit, 125 Msps analog-to-digital converter (ADC). To provide a complete converter solution, it includes a high-bandwidth linear sample-and-hold stage (S&H) and internal reference. Designed for applications demanding the highest speed and highest dynamic performance in little space, the ADS5500 has excellent power consumption of 578 mW at 3.3-V single-supply voltage. This allows an even higher system integration density. The provided internal reference simplifies system design requirements. Parallel CMOS-compatible output ensures seamless interfacing with common logic.

The ADS5500 is available in a 64-pin TQFP PowerPAD™ package and in both a commercial and industrial temperature grade device.

ADS5500 PRODUCT FAMILY

	80 Msps	105 Msps	125 Msps
12 Bit	ADS5522	ADS5521	ADS5520
14 Bit	ADS5542	ADS5541	ADS5500



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5500	HTQFP-64(2) PowerPAD	PAP	–40°C to 85°C	ADS5500I	ADS5500IPAP	Tray, 160
					ADS5500IPAPR	Tape and Reel, 1000R
			0°C to 70°C	ADS5500C	ADS5500CPAP	Tray, 160
					ADS5500CPAPR	Tape and Reel, 100

(1) For the most current product and ordering information, see the Package Option Addendum located at the end of this data sheet.
(2) Thermal pad size: 3,5 mm × 3,5 mm (min), 4 mm × 4 mm (max). θ_{JA} = 21.47°C/W and θ_{JC} = 2.99°C/W, when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard four layer 3 in × 3 in PCB.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		ADS5500	UNIT
Supply voltage	AV_{DD} to A_{GND}, DRV_{DD} to DR_{GND}		V
	A_{GND} to DR_{GND}		V
Analog input to A_{GND} (2) (2)		–0.3 to Min (AV_{DD} + 0.3 V, 3.6 V)	V
Logic input to DR_{GND}		– 0.3 to DRV_{DD}	V
Digital data output to DR_{GND}		–0.3 to DRV_{DD}	V
Operating temperature range		0 to 70	°C
		–40 to 85	
Junction temperature		105	°C
Storage temperature range		–65 to 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) If the input signal can exceed 3.6 V, then a resistor greater than or equal to 25 Ω should be added in series with each of the analog input pins to support input voltages up to 3.8 V. For input voltages above 3.8 V, the device can only handle transients and the duty cycle of the overshoot should be limited to less than 5% for inputs up to 3.9 V.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
SUPPLIES						
AV_{DD}	Analog supply voltage		3	3.3	3.6	V
DRV_{DD}	Output driver supply voltage		3	3.3	3.6	V
ANALOG INPUT						
	Differential input range			2.3		V_{PP}
V_{CM}	Input common-mode voltage (1)		1.45	1.55	1.65	V
DIGITAL OUTPUT						
	Maximum output load			10		pF
CLOCK INPUT						
	ADCLK input sample rate (sine wave) $1/t_C$	DLL ON	60		125	Msps
		DLL OFF	2		80	
	Clock amplitude, sine wave, differential (see Figure 50 for more information)		1	3		V_{PP}

(1) Input common-mode should be connected to CM.

RECOMMENDED OPERATING CONDITIONS (continued)

	MIN	NOM	MAX	UNIT
Clock duty cycle (see Figure 49 for more information)		50%		
Open free-air temperature range	0		70	°C
	–40		85	

ELECTRICAL CHARACTERISTICS

Typ values given at T_A = 25°C, min and max specified over the full recommended operating temperature range, AVDD = DRV_{DD} = 3.3 V, sampling rate = 125 Msps, 50% clock duty cycle, DLL On, 3-V_{PP} differential clock, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resolution					14		Bits
ANALOG INPUTS							
	Differential input range				2.3		V_{PP}
	Differential input impedance	See Figure 41			6.6		Ω
	Differential input capacitance	See Figure 41			4		pF
	Analog input common-mode current (per input)				300		µA
	Analog input bandwidth	Source impedance = 50Ω			750		MHz
	Voltage overload recovery time				4		Clock Cycles
INTERNAL REFERENCE VOLTAGES							
V_{REFM}	Reference bottom voltage				0.97		V
V_{REFP}	Reference top voltage				2.11		V
	Reference error			– 4%	±0.9%	4%	
V_{CM}	Common-mode voltage output				1.55 ±0.05		V
DYNAMIC DC CHARACTERISTICS AND ACCURACY							
	No missing codes				Tested		
DNL	Differential linearity error	f_{IN} = 10 MHz		–0.9	±0.75	1.1	LSB
INL	Integral linearity error	f_{IN} = 10 MHz		–5	±2.5	5	LSB
	Offset error			–11	±1.5	11	mV
	Offset temperature coefficient 0.02						mV/°C
	DC power supply rejection ratio, DC PSRR	Δoffset error/ΔAV_{DD} from AV_{DD} = 3 V to AV_{DD} = 3.6 V			0.25		mV/V
	Gain error (1)			–2	±0.45	2	%FS
	Gain temperature coefficient				0.01		Δ%/°C
DYNAMIC AC CHARACTERISTICS							
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz	25°C to T_{MAX}	71.5	73.2		dBFS
			Full temp range	70.5	72.8		
		f_{IN} = 30 MHz			72.7		
		f_{IN} = 55 MHz			71.9		
		f_{IN} = 70 MHz	25°C to T_{MAX}	70.8	72.3		
			Full temp range	69.8	72		
		f_{IN} = 100 MHz			71.2		
		f_{IN} = 150 MHz			70.1		
		f_{IN} = 225 MHz			69.1		
	RMS output noise	Input tied to common-mode			1.1		LSB

(1) Gain error is specified by design and characterization; it is not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

Typ values given at T_A = 25°C, min and max specified over the full recommended operating temperature range, AVDD = DRV_{DD} = 3.3 V, sampling rate = 125 Msps, 50% clock duty cycle, DLL On, 3-V_{PP} differential clock, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz	25°C	82	84		dBc
			Full temp range	78	84		
		f_{IN} = 30 MHz			84		
		f_{IN} = 55 MHz			79		
		f_{IN} = 70 MHz	25°C	80	83		
			Full temp range	77	82		
		f_{IN} = 100 MHz			82		
		f_{IN} = 150 MHz			78		
		f_{IN} = 225 MHz			74		
HD2	Second-harmonic	f_{IN} = 10 MHz	25°C	82	91		dBc
			Full temp range	78	86		
		f_{IN} = 30 MHz			86		
		f_{IN} = 55 MHz			84		
		f_{IN} = 70 MHz	25°C	80	87		
			Full temp range	77	83		
		f_{IN} = 100 MHz			84		
		f_{IN} = 150 MHz			78		
		f_{IN} = 225 MHz			74		
HD3	Third-harmonic	f_{IN} = 10 MHz	25°C	82	89		dBc
			Full temp range	78	88		
		f_{IN} = 30 MHz			90		
		f_{IN} = 55 MHz			79		
		f_{IN} = 70 MHz	25°C	80	85		
			Full temp range	77	82		
		f_{IN} = 100 MHz			82		
		f_{IN} = 150 MHz			80		
		f_{IN} = 225 MHz			76		
	Worst-harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz	25°C		88		dBc
		f_{IN} = 70 MHz	25°C		86		
SINAD	Signal-to-noise + distortion	f_{IN} = 10 MHz	25°C to T_{MAX}	71	72.8		dBFS
			Full temp range	69.5	72.2		
		f_{IN} = 30 MHz			72.3		
		f_{IN} = 55 MHz			70.7		
		f_{IN} = 70 MHz	25°C to T_{MAX}	70.3	71.6		
			Full temp range	69	71.3		
		f_{IN} = 100 MHz			70.5		
		f_{IN} = 150 MHz			69.1		
		f_{IN} = 225 MHz			67.4		

ELECTRICAL CHARACTERISTICS (continued)

Typ values given at T_A = 25°C, min and max specified over the full recommended operating temperature range, AVDD = DRV_{DD} = 3.3 V, sampling rate = 125 Msps, 50% clock duty cycle, DLL On, 3-V_{PP} differential clock, and –1-dBFS differential input, unless otherwise noted

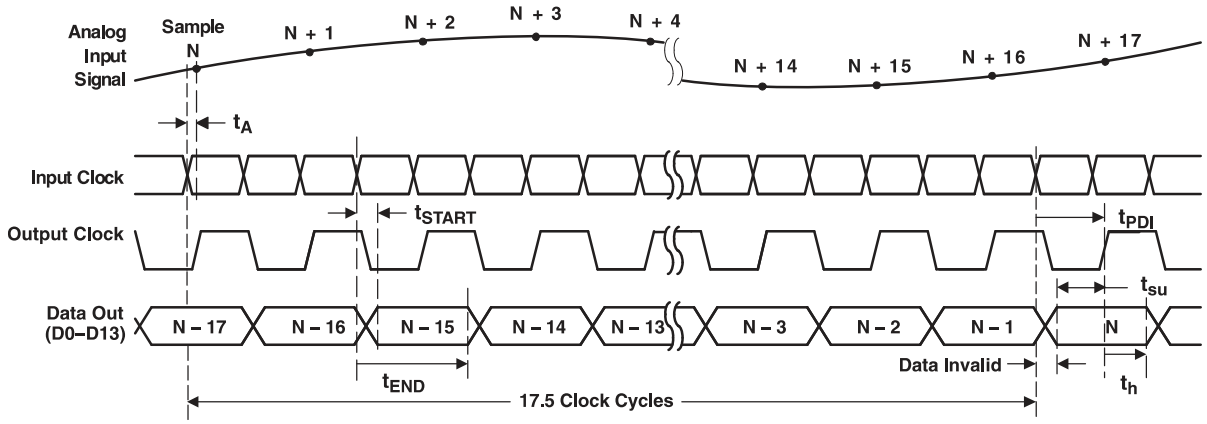
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f_{IN} = 10 MHz	25°C	80	85		dBc
			Full temp range	78	83		
		f_{IN} = 30 MHz			82		
		f_{IN} = 55 MHz			77		
		f_{IN} = 70 MHz	25°C	77.5	81		
			Full temp range	76	79.5		
		f_{IN} = 100 MHz			79		
		f_{IN} = 150 MHz			75		
		f_{IN} = 225 MHz			71.8		
ENOB	Effective number of bits	f_{IN} = 70 MHz			11.3		Bits
IMD	Two-tone intermodulation distortion	f = 10.1 MHz, 15.1 MHz (–7 dBFS each tone)			95		dBFS
		f = 30.1 MHz, 35.1 MHz (–7 dBFS each tone)			94		
		f = 50.1 MHz, 55.1 MHz (–7 dBFS each tone)			94		
ACPSRR	AC power supply rejection ratio	Supply noise frequency ≤ 100 MHz			35		dB
POWER SUPPLY							
I_{CC}	Total supply current	f_{IN} = 70 MHz			236	265	mA
I_{AVDD}	Analog supply current	f_{IN} = 70 MHz			175	190	mA
I_{DRVDD}	Output buffer supply current	f_{IN} = 70 MHz, 10-pF load from digital outputs to ground			61	75	mA
	Power dissipation	Analog only			578	627	mW
		Output buffer power with 10-pF load on digital output to ground			202	248	mW
	Standby power	With clocks running			181	250	mW

DIGITAL CHARACTERISTICS

Valid over the full recommended operating temperature range, AV_{DD} = DRV_{DD} = 3.3 V, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current				10	µA
Low-level input current				–10	µA
Input current for RESET			–20		µA
Input capacitance			4		pF
DIGITAL OUTPUTS					
Low-level output voltage	C_{LOAD} = 10 pF		0.3		V
High-level output voltage	C_{LOAD} = 10 pF	2.8	3		V
Output capacitance			3		pF

TIMING CHARACTERISTICS



NOTE: It is recommended that the loading at CLKOUT and all data lines are accurately matched to ensure that the above timing matches closely with the specified values.

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Figure 1. Timing Diagram

TIMING CHARACTERISTICS(1)(2)

Typ values given at T_A = 25°C, min and max specified over the full recommended operating temperature range, sampling rate = 125 Msps, 50% clock duty cycle, AV_{DD} = DRV_{DD} = 3.3 V, 3-V_{PP} differential clock, and C_{LOAD} = 10 pF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING SPECIFICATION						
t_A	Aperture delay	Input CLK falling edge to data sampling point		1		ns
	Aperture jitter (uncertainty)	Uncertainty in sampling instant		300		fs
t_{su}	Data setup time	Data valid(3) to 50% of CLKOUT rising edge	2.1	2.5		ns
t_h	Data hold time	50% of CLKOUT rising edge to data becoming invalid(3)	1.7	2.1		ns
t_{START}	Input clock to output data valid start(4)(5)	Input clock rising edge to Data valid start delay		2.2	2.9	ns
t_{END}	Input clock to output data valid end(4)(5)	Input clock rising edge to Data valid end delay	5.8	6.9		ns
t_{JIT}	Output clock jitter	Uncertainty in CLKOUT rising edge, peak-to-peak		150	210	ps
t_r	Output clock rise time	Rise time of CLKOUT measured from 20% to 80% of DRVDD		1.7	1.9	ns
t_f	Output clock fall time	Fall time of CLKOUT measured from 80% to 20% of DRVDD		1.5	1.7	ns
t_{PDI}	Input clock to output clock delay	Input clock rising edge, zero crossing, to output clock rising edge 50%	4.2	4.8	5.5	ns
t_r	Data rise time	Data rise time measured from 20% to 80% of DRVDD		3.6	4.6	ns
t_f	Data fall time	Data fall time measured from 80% to 20% of DRVDD		2.8	3.7	ns
	Output enable (OE) to data output delay	Time required for outputs to have stable timings w.r.t input clock(after OE is activated			1000	Clock Cycles

(1) Timing parameters are ensured by design and characterization and not tested in production.
(2) See Table 5 through Table 8 in the *Application Information* section for timing information at additional sampling frequencies.
(3) Data valid refers to 2 V for LOGIC high and 0.8 V for LOGIC low.
(4) See the *Output Information* section for details on using the input clock for data capture.
(5) These specifications apply when the CLKOUT polarity is set to rising edge (according to Table 3). Add ½ clock period for the valid number for a falling edge CLKOUT polarity.

TIMING CHARACTERISTICS (continued)

Typ values given at T_A = 25°C, min and max specified over the full recommended operating temperature range, sampling rate = 125 Msps, 50% clock duty cycle, AV_{DD} = DRV_{DD} = 3.3 V, 3-V_{PP} differential clock, and C_{LOAD} = 10 pF, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wake-up time	Time to valid data after coming out of software power down			1000	Clock Cycles
	Time to valid data after stopping and restarting the clock			1000	
Latency Time for a sample to propagate to the ADC outputs 17.5 Clock Cycles			17.5		Clock Cycles

RESET TIMING CHARACTERISTICS

Typ values given at T_A = 25°C, min and max specified over the full recommended operating temperature range, AV_{DD} = DRV_{DD} = 3.3 V, 3-V_{PP} differential clock(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING SPECIFICATION						
t_1	Power-on delay	Delay from power on of AV_{DD} and DRV_{DD} to RESET pulse	10			ms
t_2	Reset pulse width	Pulse width of active RESET signal	2			µs
t_3	Register write delay	Delay from RESET disable to SEN active	2			µs
	Power-up time	Delay from power-up of AV_{DD} and DRV_{DD} to output stable		40		ms

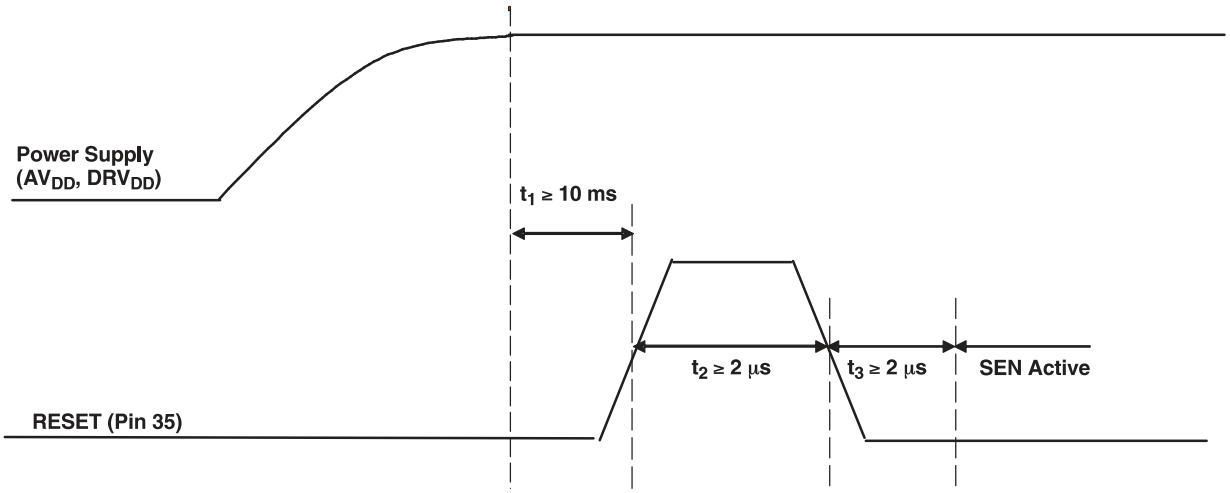


Figure 2. Reset Timing Diagram

SERIAL PROGRAMMING INTERFACE CHARACTERISTICS

The device has a three-wire serial interface. The device latches the serial data SDATA on the falling edge of serial clock SCLK when SEN is active.

- Serial shift of bits is enabled when SEN is low. SCLK shifts serial data at falling edge.
- Minimum width of data stream for a valid loading is 16 clocks.
- Data is loaded at every 16th SCLK falling edge while SEN is low.
- In case the word length exceeds a multiple of 16 bits, the excess bits are ignored.
- Data can be loaded in multiple of 16-bit words within a single active SEN pulse.
- The first 4-bit nibble is the address of the register while the last 12 bits are the register contents.

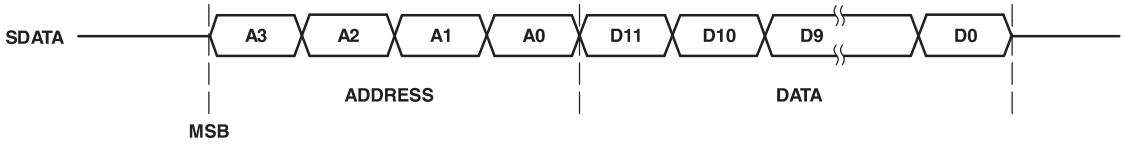


Figure 3. DATA Communication is 2-Byte, MSB First

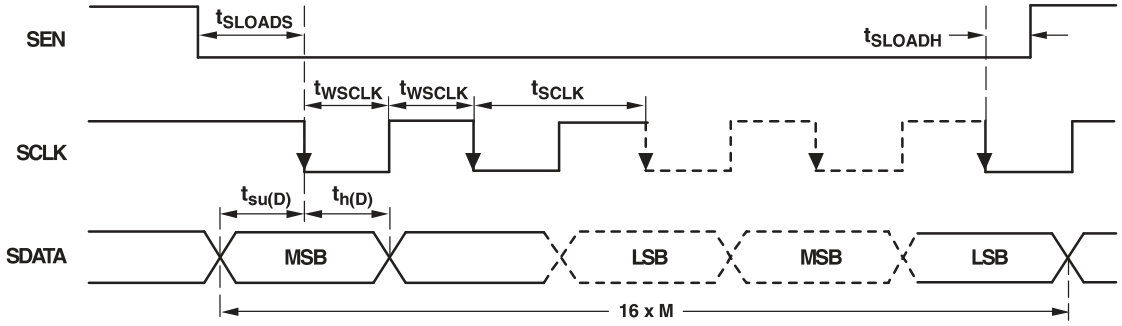


Figure 4. Serial Programming Interface Timing Diagram

Table 1. Serial Programming Interface Timing Characteristics

PARAMETER		MIN(1)	TYP(1)	MAX(1)	UNIT
t_{SCLK}	SCLK period	50			ns
t_{WSCLK}	SCLK duty cycle	25%	50%	75%	
t_{SLOADS}	SEN to SCLK setup time	8			ns
t_{SLOADH}	SCLK to SEN hold time	6			ns
t_{DS}	Data setup time	8			ns
t_{DH}	Data hold time	6			ns

(1) Min, typ, and max values are characterized, but not production tested.

Table 2. Serial Register Table(1)

A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
														DLL CTRL		Clock DLL
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Internal DLL is on, recommended for 60–125 Msps clock speed
1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	Internal DLL is off, recommended for 2-80 Msps clock speed
TP<1> TP<0>																Test Mode
1	1	1	0	0	0	0	0	0	0	0	0	0	0	X	0	Normal mode of operation
1	1	1	0	0	0	1	0	0	0	0	0	0	0	X	0	All outputs forced to 0.(2)
1	1	1	0	0	1	0	0	0	0	0	0	0	0	X	0	All outputs forced to 1. (2)
1	1	1	0	0	1	1	0	0	0	0	0	0	0	X	0	Each output bit toggles between 0 and 1. (2)(3)
PDN																Power Down
1	1	1	1	0	0	0	0	0	0	0	0	0	0	X	0	Normal mode of operation
1	1	1	1	1	0	0	0	0	0	0	0	0	0	X	0	Device is put in power down (low current) mode

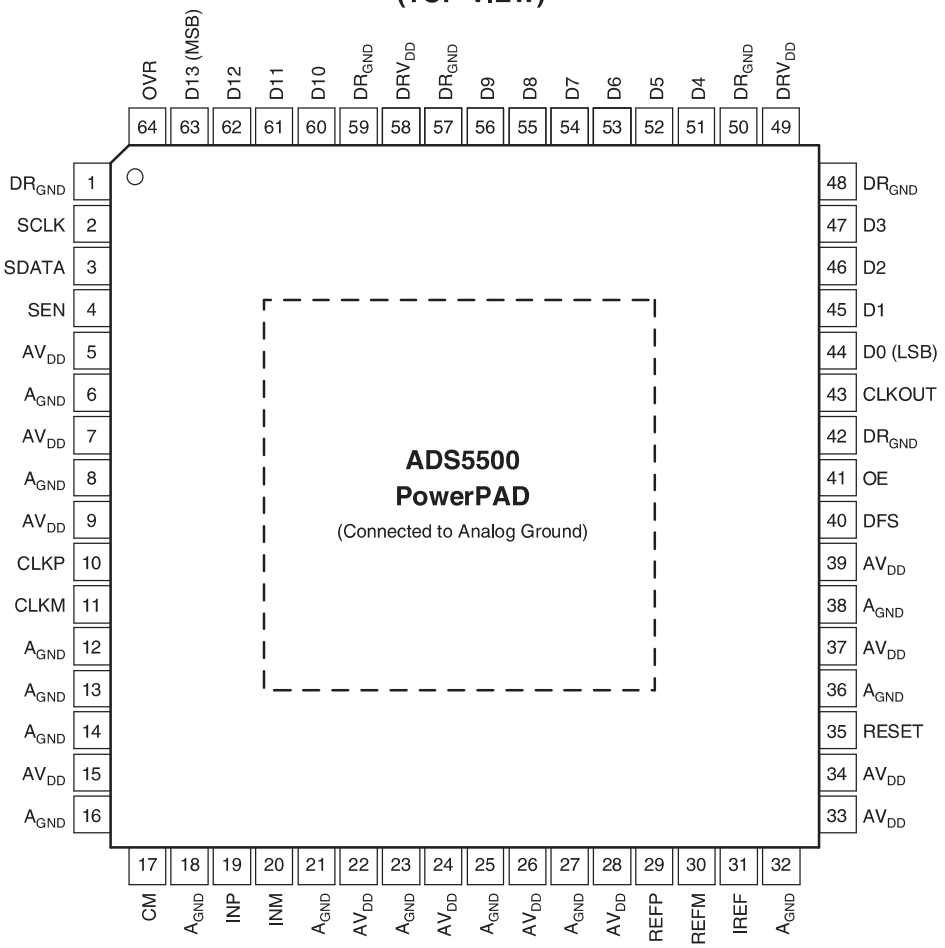
(1) The register contents default to the appropriate setting for normal operation upon RESET.
(2) The patterns given are applicable to the straight offset binary output format. If two's complement output format is selected, the test mode outputs will be the two's complement equivalent of these patterns as described in the Output Information section.
(3) While each bit toggles between 1 and 0 in this mode, there is no assured phase relationship between the data bits D0 through D13. For example, when D0 is a 1, D1 in not assured to be a 0, and vice versa.

Table 3. Data Format Select (DFS Table)

DFS-PIN VOLTAGE (V_{DFS})	DATA FORMAT	CLOCK OUTPUT POLARITY
$V_{DFS} < \frac{2}{12} \times AV_{DD}$	Straight Binary	Data valid on rising edge
$\frac{4}{12} \times AV_{DD} < V_{DFS} < \frac{5}{12} \times AV_{DD}$	Two's Complement	Data valid on rising edge
$\frac{7}{12} \times AV_{DD} < V_{DFS} < \frac{8}{12} \times AV_{DD}$	Straight Binary	Data valid on falling edge
$V_{DFS} > \frac{10}{12} \times AV_{DD}$	Two's Complement	Data valid on falling edge

PIN CONFIGURATION

PAP PACKAGE
(TOP VIEW)



PIN ASSIGNMENTS

TERMINAL		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
AV_{DD}	5, 7, 9, 15, 22, 24, 26, 28, 33, 34, 37, 39	12	I	Analog power supply
A_{GND}	6, 8, 12-14, 16, 18, 21, 23, 25, 27, 32, 36, 38	14	I	Analog ground
DRV_{DD}	49, 58	2	I	Output driver power supply

PIN CONFIGURATION (continued)

PIN ASSIGNMENTS (continued)

TERMINAL		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
DR_{GND}	1, 42, 48, 50, 57, 59	6	I	Output driver ground
INP	19	1	I	Differential analog input (positive)
INM	20	1	I	Differential analog input (negative)
REFP	29	1	O	Reference voltage (positive); 1-µF capacitor to GND
REFM	30	1	O	Reference voltage (negative); 1-µF capacitor to GND
IREF	31	1	I	Current set; 56.2-kΩ resistor to GND; do not connect capacitors
CM	17	1	O	Common-mode output voltage
RESET	35	1	I	Reset (active high), internal 200-kΩ resistor to AVDD (1)
OE	41	1	I	Output enable (active high)
DFS	40	1	I	Data format and clock out polarity select (2)(3)
CLKP	10	1	I	Data converter differential input clock (positive)
CLKM	11	1	I	Data converter differential input clock (negative)
SEN	4	1	I	Serial interface chip select (3)
SDATA	3	1	I	Serial interface data (3)
SCLK	2	1	I	Serial interface clock (3)
D0 (LSB)–D13(MSB)	44-47, 51-56, 60-63	14	O	Parallel data output
OVR	64	1	O	Over-range indicator bit
CLKOUT	43	1	O	CMOS clock out in sync with data
NOTE: PowerPAD must be connected to analog ground.				

(1) If unused, the RESET pin should be tied to AGND. See the serial programming interface section for details.
(2) Table 3 defines the voltage levels for each mode selectable via the DFS pin.
(3) Pins OE, DFS, SEN, SDATA, and SCLK have internal clamping diodes to the DRVDD supply. Any external circuit driving these pins must also run off the same supply voltage as DRVDD.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay
The delay in time between the falling edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle
The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate
The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate
The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL)
The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error
The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error does not account for variations in the internal reference voltages (see the *Electrical Specifications* section for limits on the variation of V_{REFP} and V_{REFM}).

Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference T_{MAX}-T_{MIN}.

Signal-to-Noise Ratio

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at DC and the first eight harmonics.

$$SNR = 10Log_{10}\frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log_{10}\frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (3)$$

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the power of the first eight harmonics (P_D).

$$THD = 10Log_{10}\frac{P_S}{P_D} \quad (4)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency $2f_1–f_2$ or $2f_2–f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR)

The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

Reference Error

The reference error is the variation of the actual reference voltage (V_{REFP} – V_{REFM}) from its ideal value. The reference error is typically given as a percentage.

Voltage Overload Recovery Time

The voltage overload recovery time is defined as the time required for the ADC to recover to within 1% of the full-scale range in response to an input voltage overload of 10% beyond the full-scale range.

TYPICAL CHARACTERISTICS

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 125 Msps, DLL On, and 3-V differential clock unless otherwise noted

SPECTRAL PERFORMANCE (FFT for 2-MHz Input Signal)

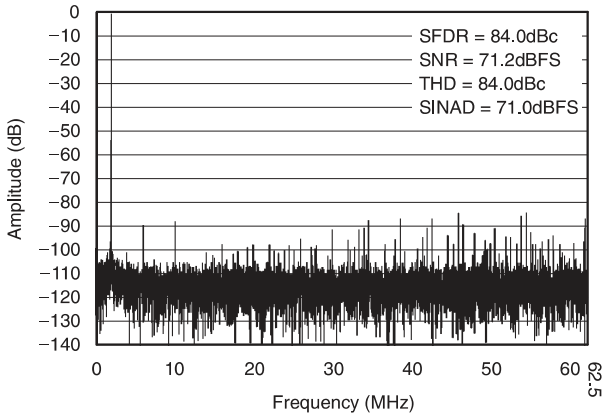


Figure 5.

SPECTRAL PERFORMANCE (FFT for 15-MHz Input Signal)

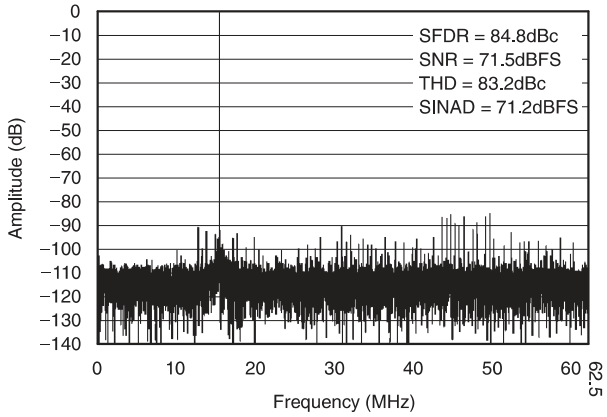


Figure 6.

SPECTRAL PERFORMANCE (FFT for 60-MHz Input Signal)

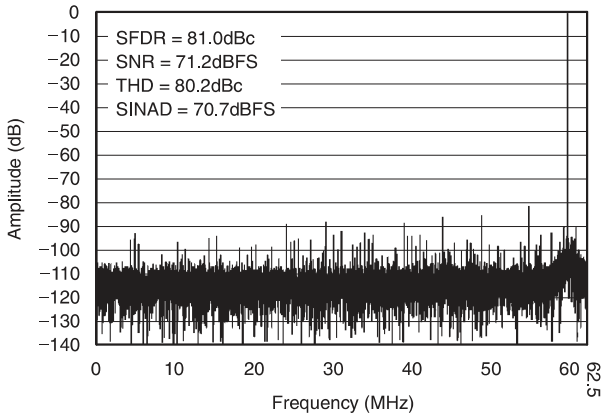


Figure 7.

SPECTRAL PERFORMANCE (FFT for 70-MHz Input Signal)

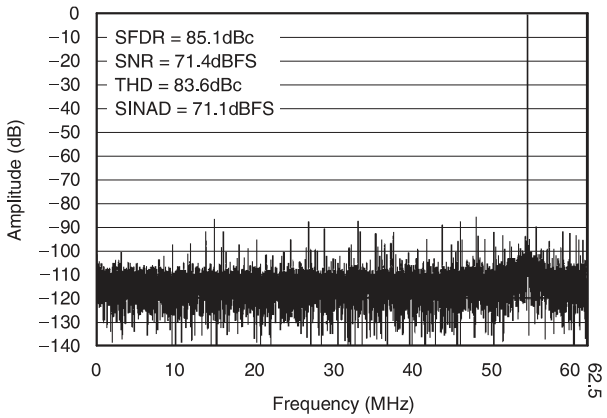


Figure 8.

SPECTRAL PERFORMANCE (FFT for 80-MHz Input Signal)

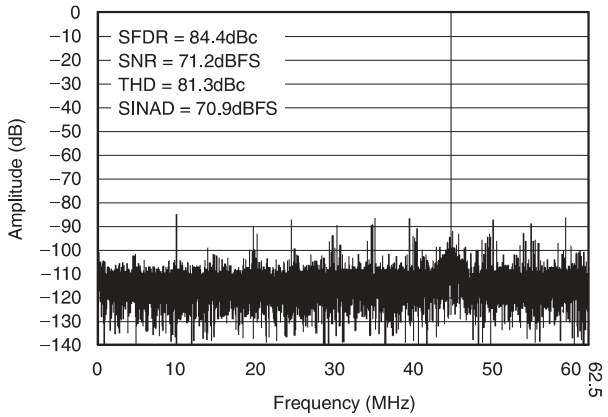


Figure 9.

SPECTRAL PERFORMANCE (FFT for 100-MHz Input Signal)

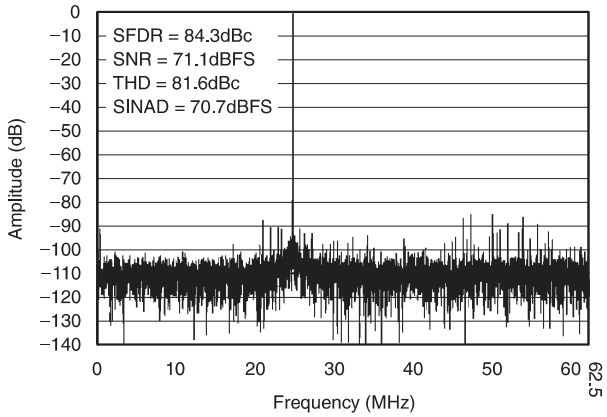


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 125 Msps, DLL On, and 3-V differential clock unless otherwise noted

SPECTRAL PERFORMANCE (FFT for 150-MHz Input Signal)

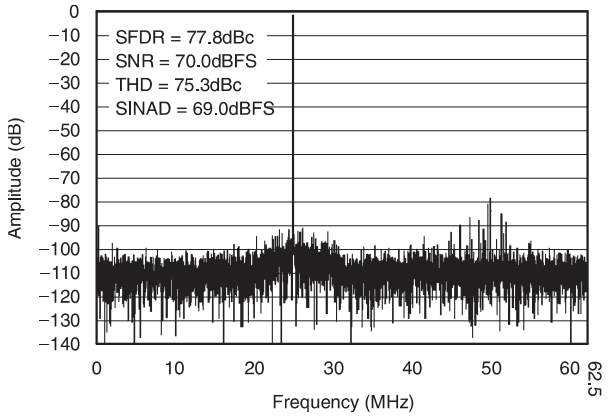


Figure 11.

SPECTRAL PERFORMANCE (FFT for 225-MHz Input Signal)

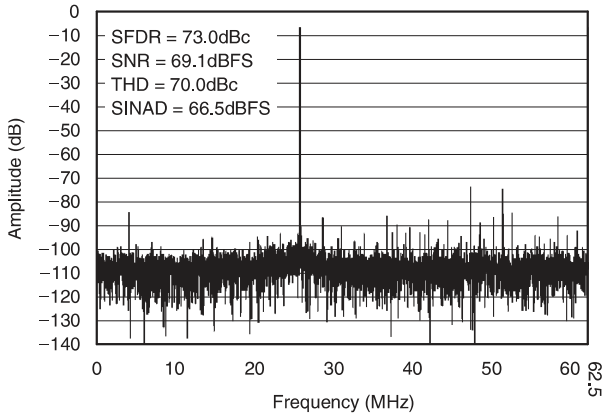


Figure 12.

SPECTRAL PERFORMANCE (FFT for 300-MHz Input Signal)

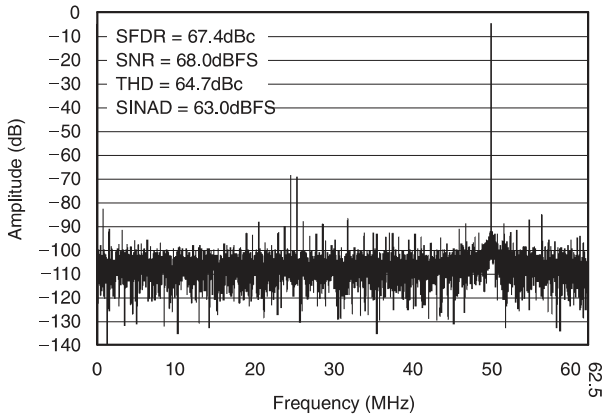


Figure 13.

TWO-TONE INTERMODULATION

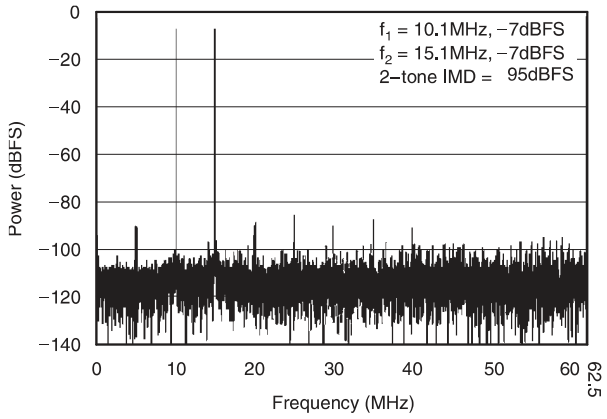


Figure 14.

TWO-TONE INTERMODULATION

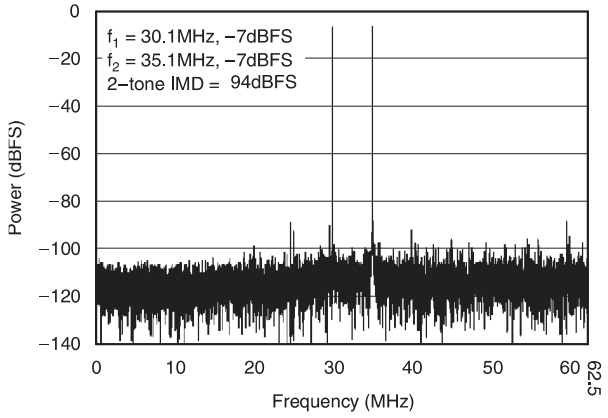


Figure 15.

TWO-TONE INTERMODULATION

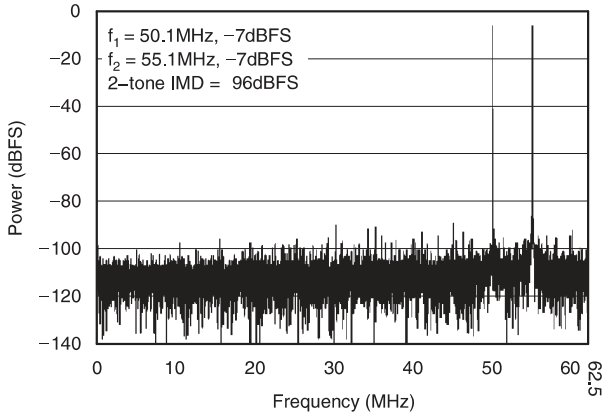


Figure 16.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 125 Msps, DLL On, and 3-V differential clock unless otherwise noted

DIFFERENTIAL NONLINEARITY (DNL)

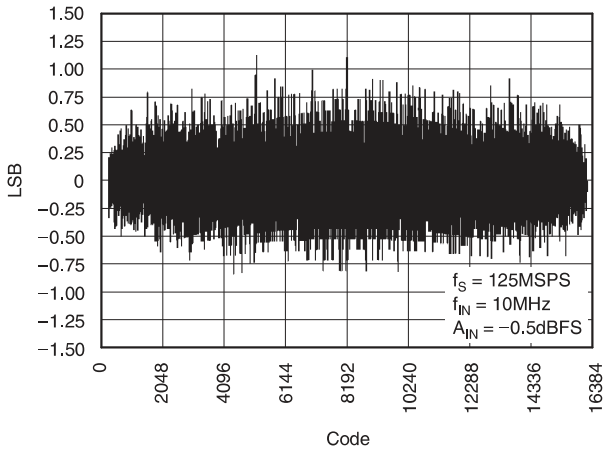


Figure 17.

INTEGRAL NONLINEARITY (INL)

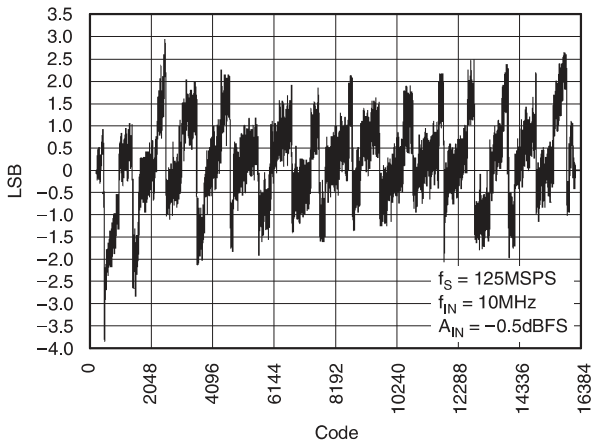


Figure 18.

SPURIOUS-FREE DYNAMIC RANGE vs INPUT FREQUENCY

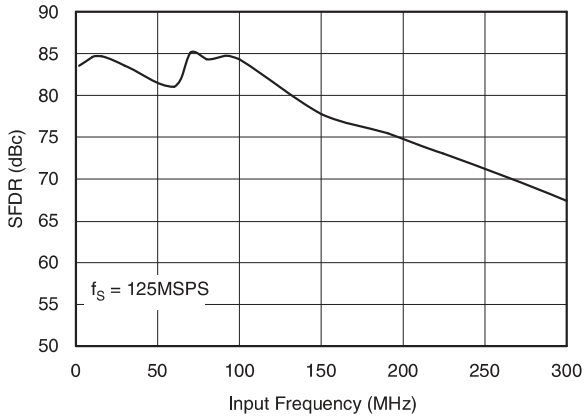


Figure 19.

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

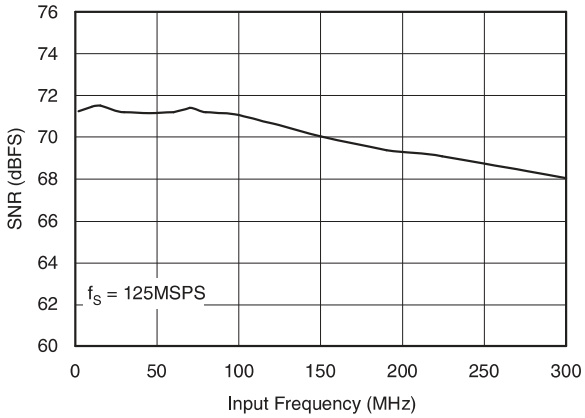


Figure 20.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 125 Msps, DLL On, and 3-V differential clock unless otherwise noted

AC PERFORMANCE vs ANALOG SUPPLY VOLTAGE

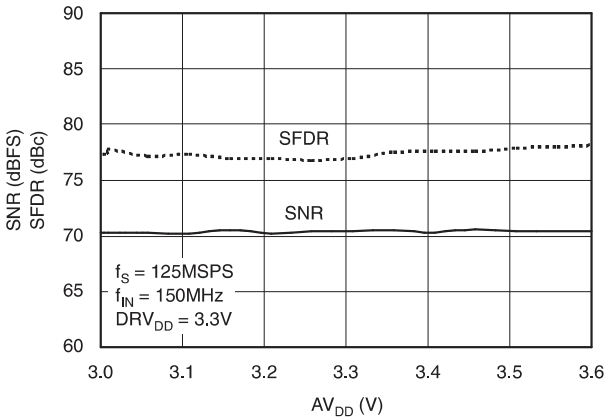


Figure 21.

AC PERFORMANCE vs ANALOG SUPPLY VOLTAGE

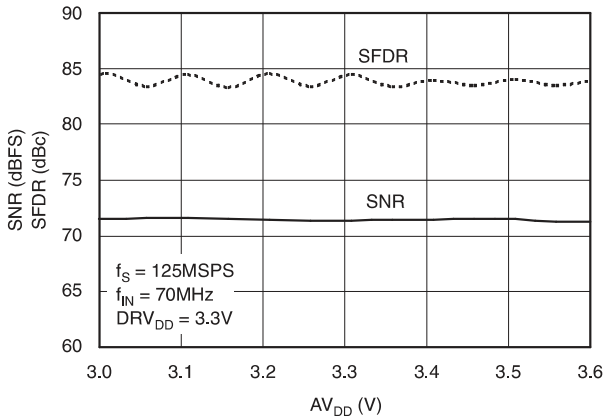


Figure 22.

AC PERFORMANCE vs DIGITAL SUPPLY VOLTAGE

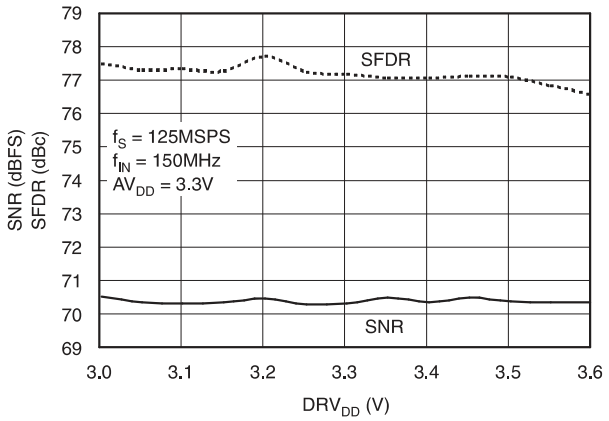


Figure 23.

AC PERFORMANCE vs DIGITAL SUPPLY VOLTAGE

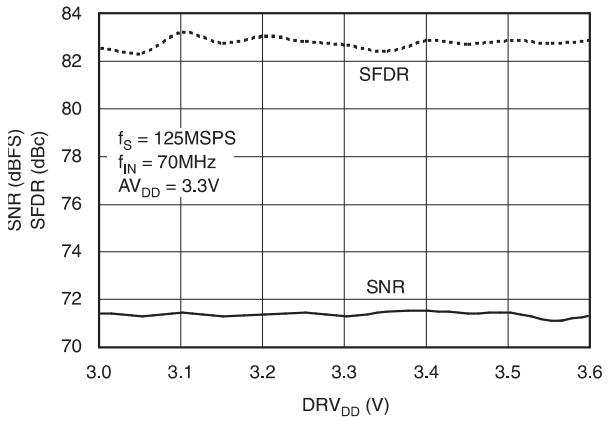


Figure 24.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 125 Msps, DLL On, and 3-V differential clock unless otherwise noted

TOTAL POWER DISSIPATION vs SAMPLING FREQUENCY

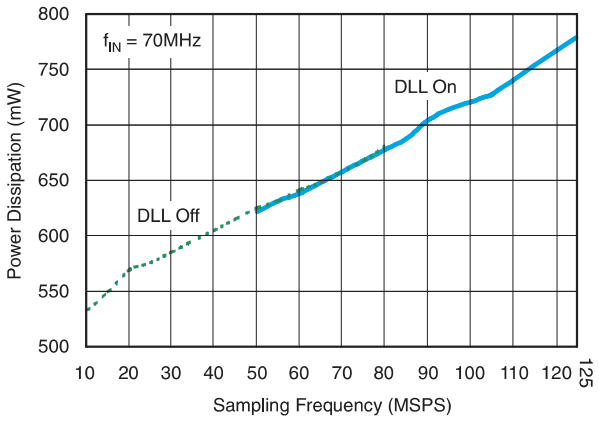


Figure 25.

SIGNAL-TO-NOISE RATIO AND SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE

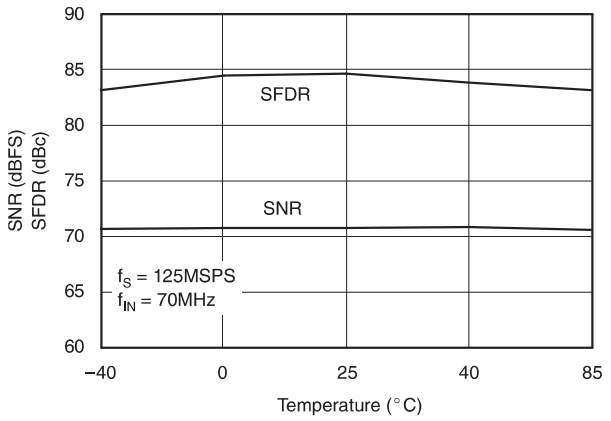


Figure 26.

AC PERFORMANCE vs INPUT AMPLITUDE

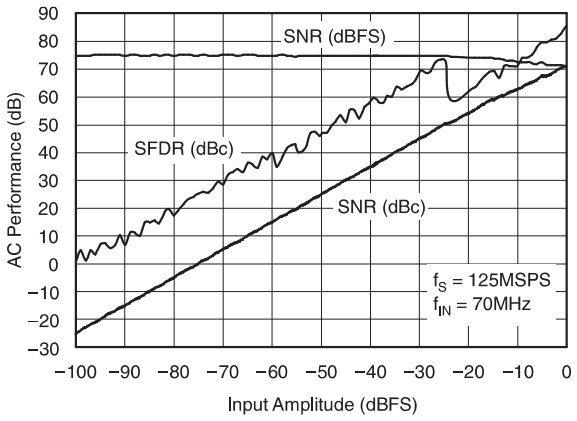


Figure 27.

AC PERFORMANCE vs INPUT AMPLITUDE

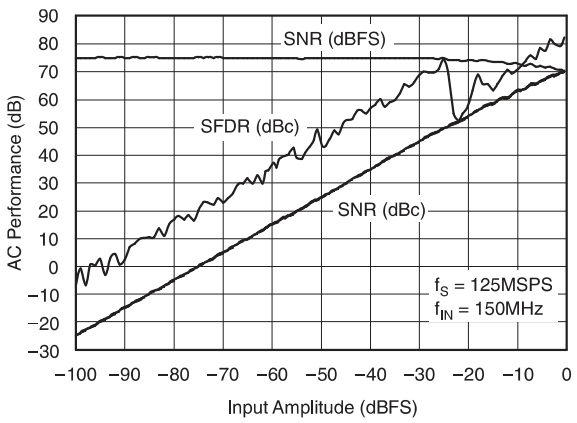


Figure 28.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 125 Msps, DLL On, and 3-V differential clock unless otherwise noted

AC PERFORMANCE vs INPUT AMPLITUDE

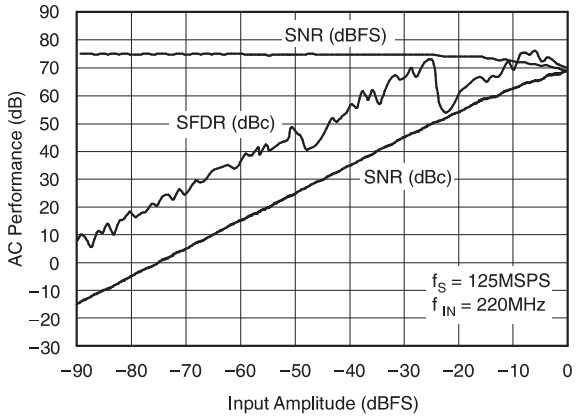


Figure 29.

OUTPUT NOISE HISTOGRAM

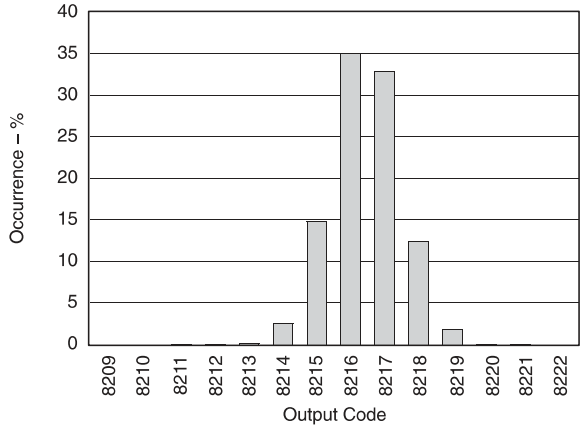


Figure 30.

AC PERFORMANCE vs CLOCK AMPLITUDE

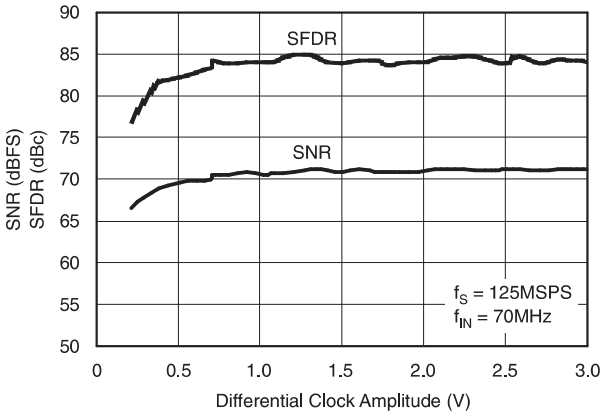


Figure 31.

WCDMA CARRIER

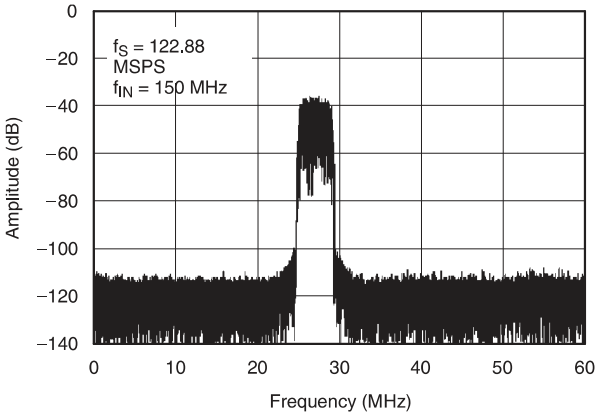


Figure 32.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 125 Msps, DLL On, and 3-V differential clock unless otherwise noted

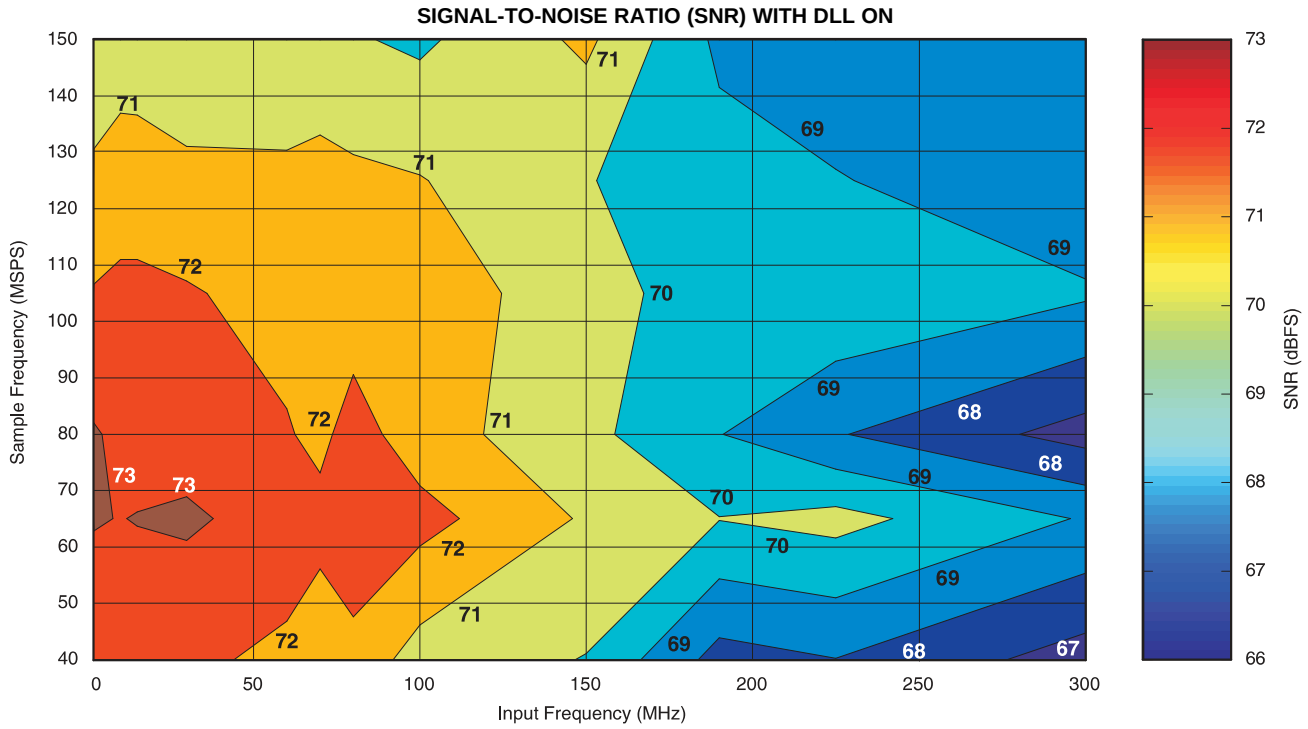


Figure 33.

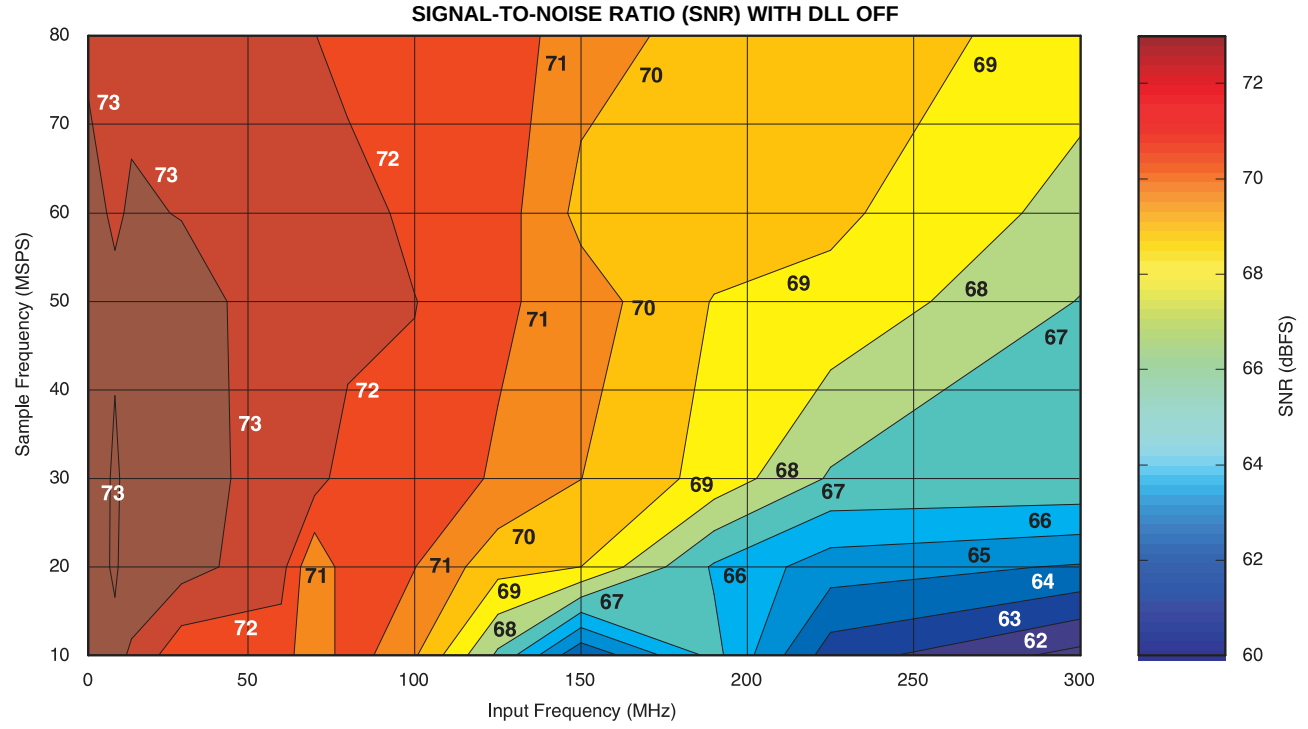


Figure 34.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 125 Msps, DLL On, and 3-V differential clock unless otherwise noted

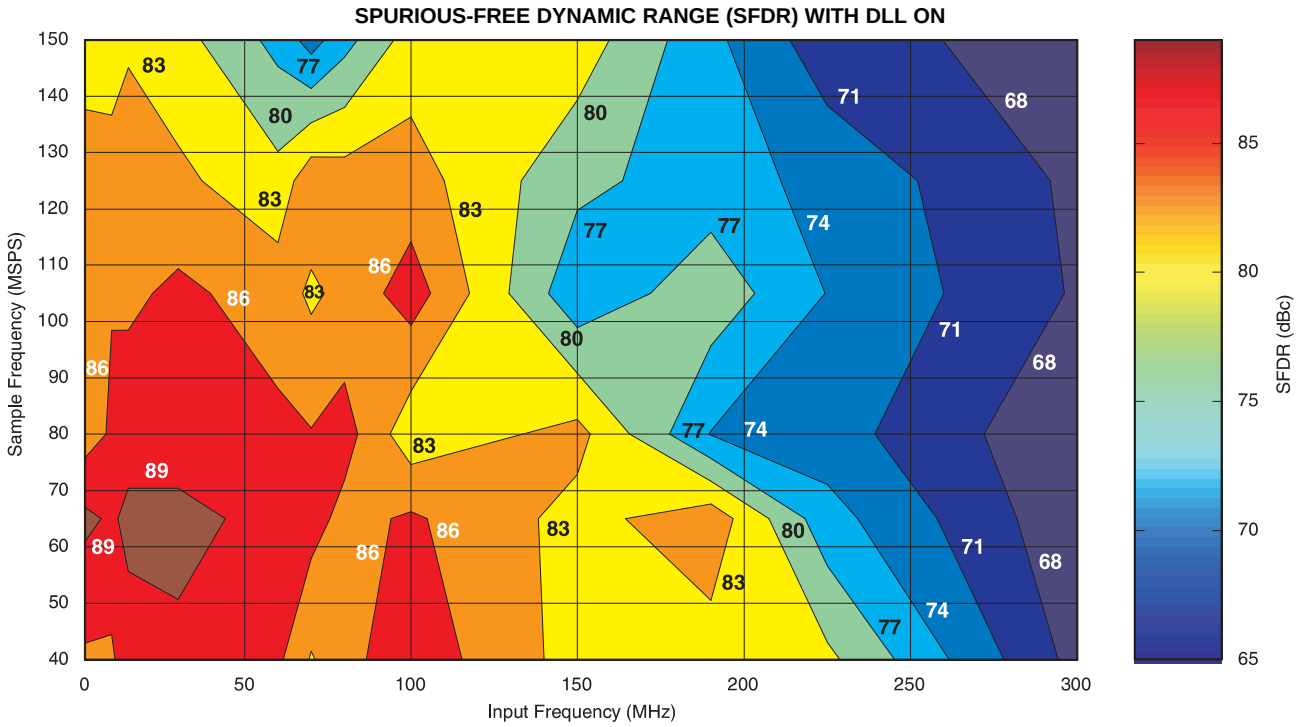


Figure 35.

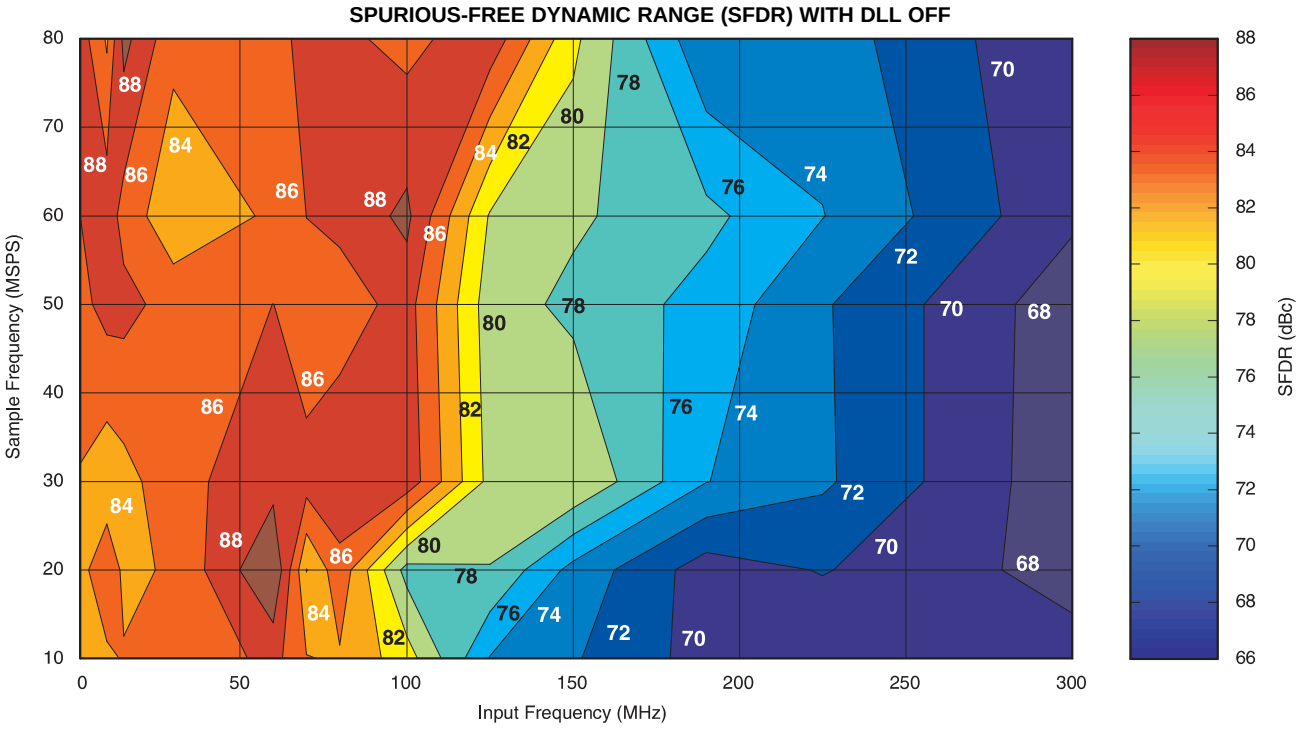


Figure 36.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 125 Msps, DLL On, and 3-V differential clock unless otherwise noted

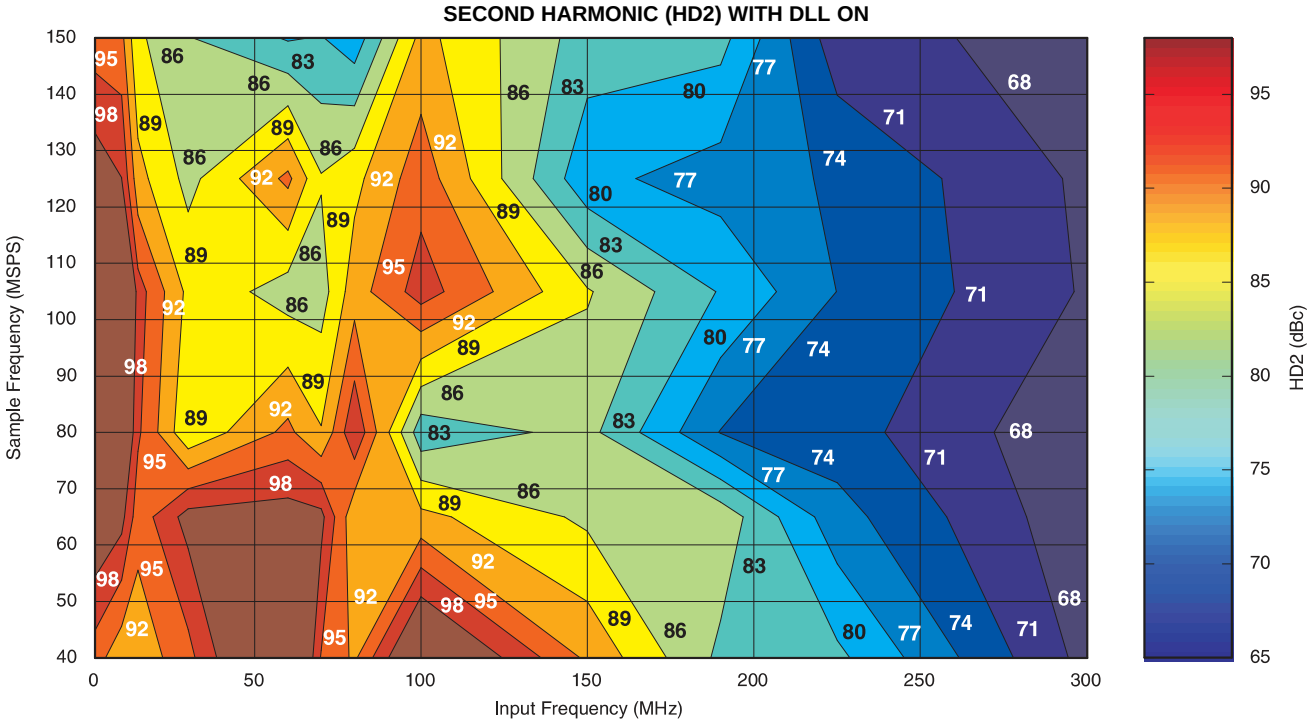


Figure 37.

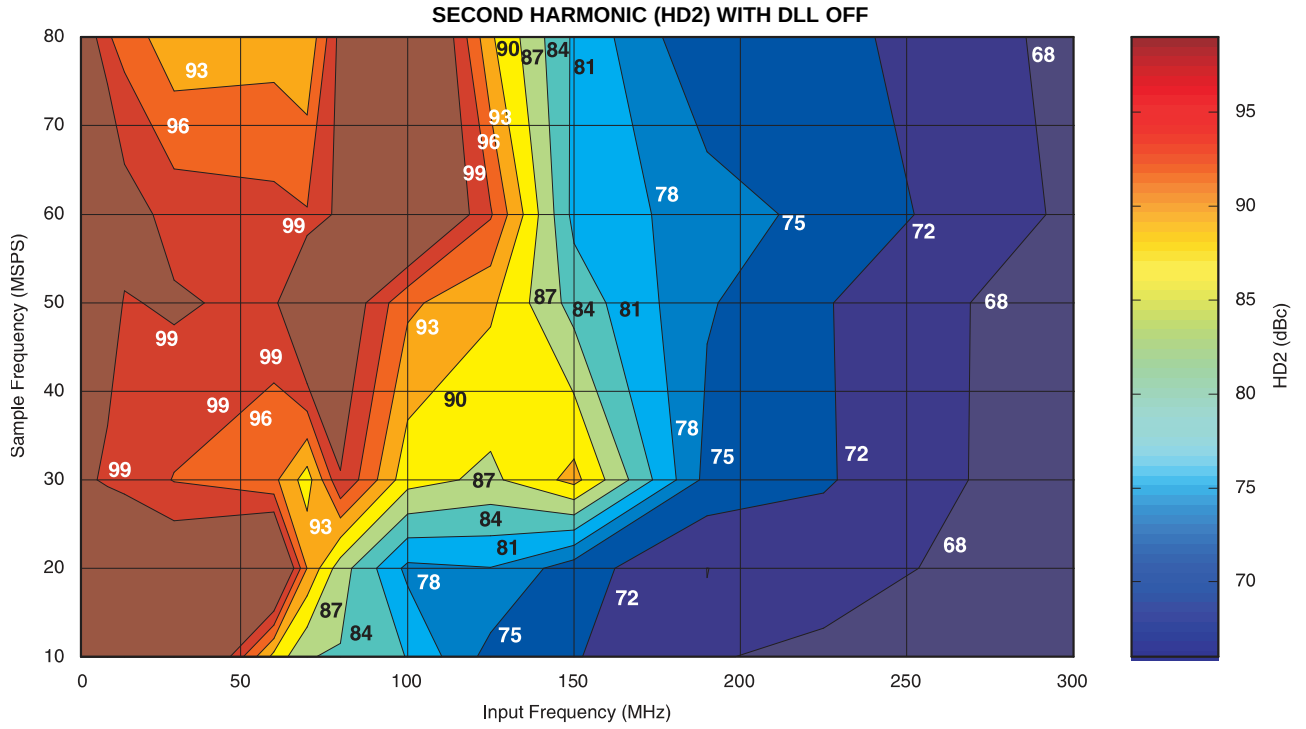


Figure 38.

TYPICAL CHARACTERISTICS (continued)

Typical values are at T_A = 25°C, AV_{DD} = DRV_{DD} = 3.3 V, differential input amplitude = –1 dBFS, sampling rate = 125 Msps, DLL On, and 3-V differential clock unless otherwise noted

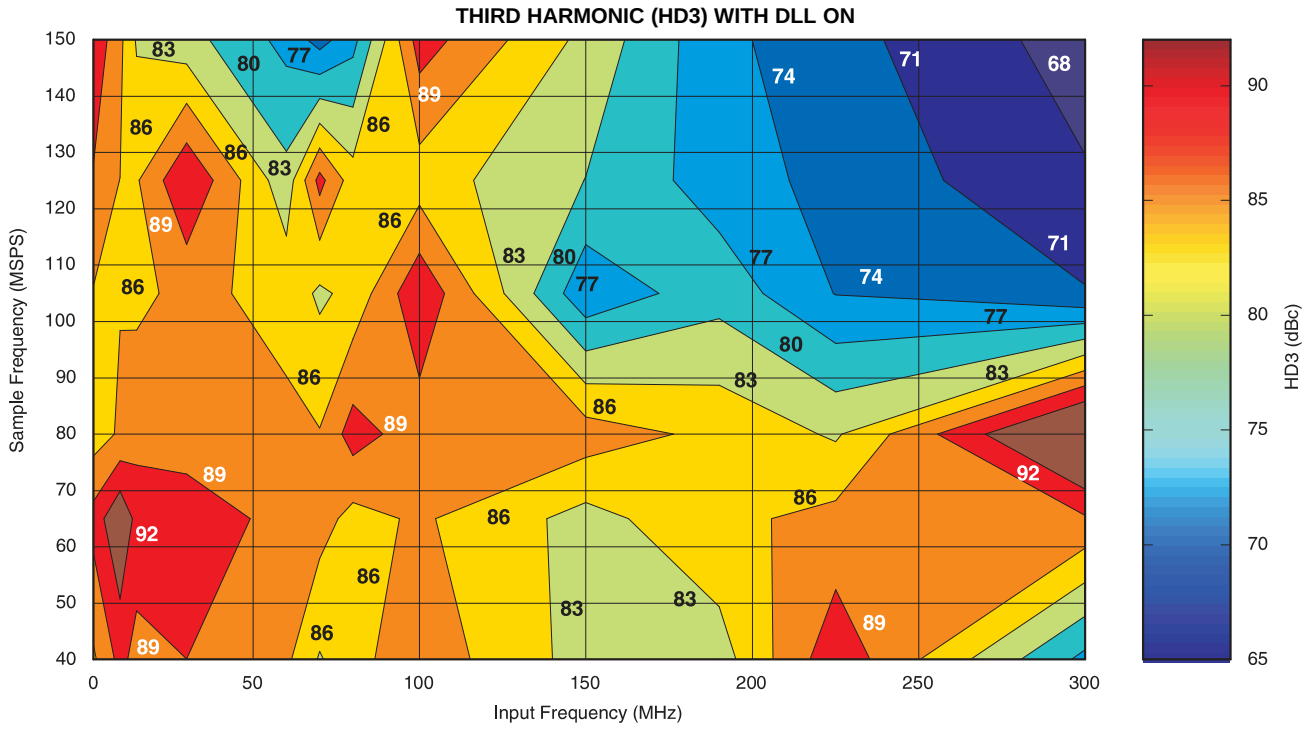


Figure 39.

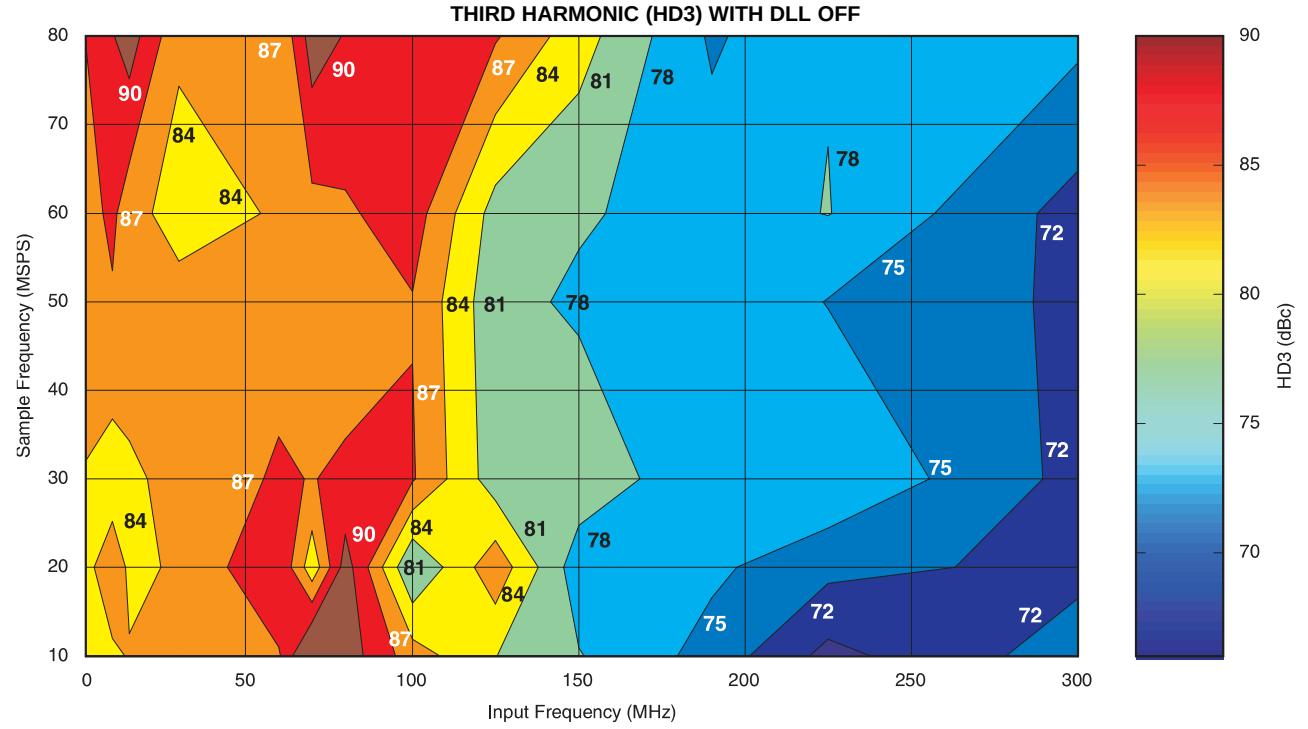


Figure 40.

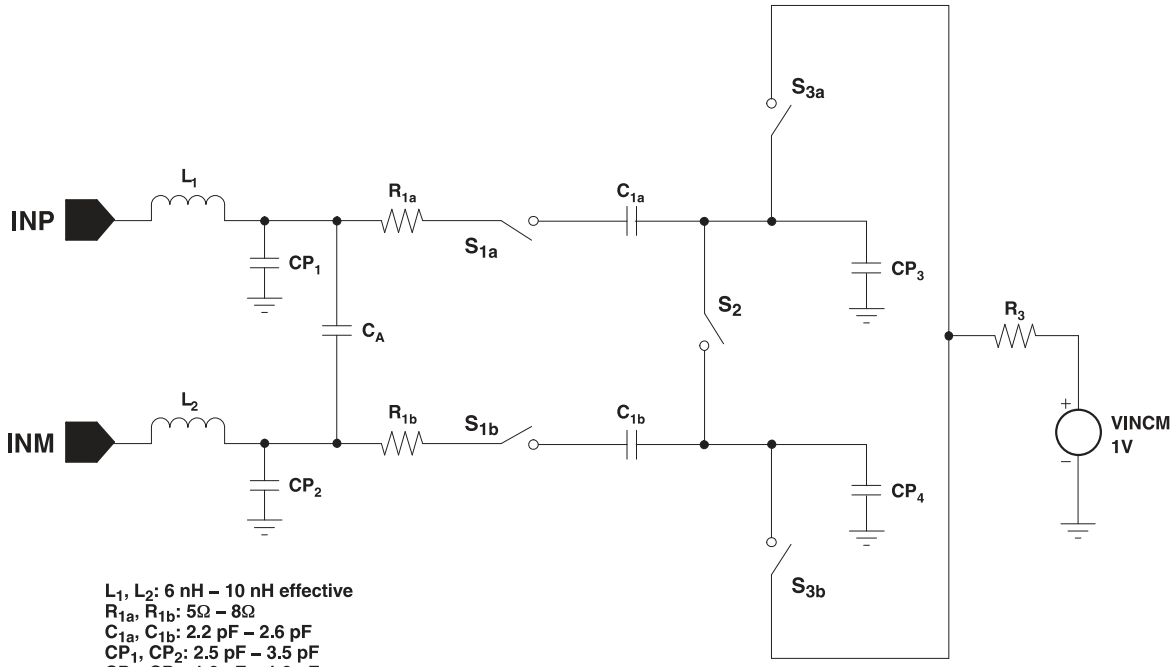
APPLICATION INFORMATION

THEORY OF OPERATION

The ADS5500 is a low-power, 14-bit, 125 Msps, CMOS, switched capacitor, pipeline ADC that operates from a single 3.3-V supply. The conversion process is initiated by a falling edge of the external input clock. Once the signal is captured by the input S&H, the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of 17.5 clock cycles, after which the output data is available as a 14-bit parallel word, coded in either straight offset binary or binary two's complement format.e sample through the pipeline every half clock cycle. This process results

INPUT CONFIGURATION

The analog input for the ADS5500 consists of a differential sample-and-hold architecture implemented using a switched capacitor technique, shown in Figure 41.



L_1, L_2: 6 nH – 10 nH effective
R_{1a}, R_{1b}: 5Ω – 8Ω
C_{1a}, C_{1b}: 2.2 pF – 2.6 pF
CP_1, CP_2: 2.5 pF – 3.5 pF
CP_3, CP_4: 1.2 pF – 1.8 pF
C_A: 0.8 pF – 1.2 pF
R_3: 80 Ω – 120 Ω
Swithches: S_{1a}, S_{1b}: On Resistance: 35 Ω – 50 Ω
S_2: On Resistance: 7.5 Ω – 15 Ω
S_{3a}, S_{3b}: On Resistance: 40 Ω – 60 Ω
All switches OFF Resistance: 10 GΩ

NOTE: All Switches are ON in sampling phase which is approximately one half of a clock period.

Figure 41. Analog Input Stage

This differential input topology produces a high level of AC performance for high sampling rates. It also results in a high usable input bandwidth, especially important for high intermediate-frequency (IF) or undersampling applications. The ADS5500 requires each of the analog inputs (INP, INM) to be externally biased around the common-mode level of the internal circuitry (CM, pin 17). For a full-scale differential input, each of the differential lines of the input signal (pins 19 and 20) swings symmetrically between CM + 0.575 V and CM – 0.575 V. This means that each input is driven with a signal of up to CM 0.575 V, so that each input has a maximum differential signal of 1.15 V_{PP} for a total differential input signal swing of 2.3 V_{PP}. The maximum swing is determined by the two reference voltages, the top reference (REFP, pin 29), and the bottom reference (REFM, pin 30).

The ADS5500 obtains optimum performance when the analog inputs are driven differentially. The circuit shown in Figure 42 shows one possible configuration using an RF transformer.

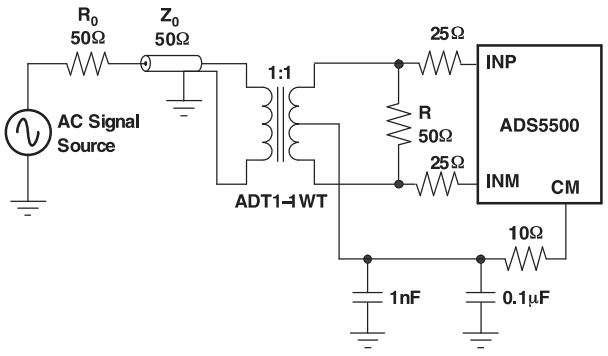


Figure 42. Transformer Input to Convert Single-Ended Signal to Differential Signal

The single-ended signal is fed to the primary winding of an RF transformer. Since the input signal must be biased around the common-mode voltage of the internal circuitry, the common-mode voltage (V_{CM}) from the ADS5500 is connected to the center-tap of the secondary winding. To ensure a steady low-noise V_{CM} reference, best performance is obtained when the CM (pin 17) output is filtered to ground with 0.1 μF and 0.001-μF low-inductance capacitors.

Output V_{CM} (pin 17) is designed to directly drive the ADC input. When providing a custom CM level, be aware that the input structure of the ADC sinks a common-mode current in the order of 600 μA (300 μA per input) at 125 Msps. Equation 5 describes the dependency of the common-mode current and the sampling frequency:

$$\frac{600\ \mu A \times f_s}{125 MSPS} \quad (5)$$

Where:

f_S > 2 Msps.

This equation helps to design the output capability and impedance of the driving circuit accordingly.

When it is necessary to buffer or apply a gain to the incoming analog signal, it is possible to combine single-ended operational amplifiers with an RF transformer, or to use a differential input/output amplifier without a transformer, to drive the input of the ADS5500. TI offers a wide selection of single-ended operational amplifiers (including the THS3201, THS3202, OPA847, and OPA695) that can be selected depending on the application. An RF gain block amplifier, such as TI's THS9001, can also be used with an RF transformer for very high input frequency applications. The THS4503 is a recommended differential input/output amplifier. Table 4 lists the recommended amplifiers.

When using single-ended operational amplifiers (such as the THS3201, THS3202, OPA847, or OPA695) to provide gain, a three-amplifier circuit is recommended with one amplifier driving the primary of an RF transformer and one amplifier in each of the legs of the secondary driving the two differential inputs of the ADS5500. These three amplifier circuits minimize even-order harmonics. For very high frequency inputs, an RF gain block amplifier can be used to drive a transformer primary; in this case, the transformer secondary connections can drive the input of the ADS5500 directly, as shown in Figure 42, or with the addition of the filter circuit shown in Figure 43.

Figure 43 illustrates how RIN and CIN can be placed to isolate the signal source from the switching inputs of the ADC and to implement a low-pass RC filter to limit the input noise in the ADC. It is recommended that these components be included in the ADS5500 circuit layout when any of the amplifier circuits discussed previously are used. The components allow fine-tuning of the circuit performance. Any mismatch between the differential lines of the ADS5500 input produces a degradation in performance at high input frequencies, mainly characterized by an increase in the even-order harmonics. In this case, special care should be taken to keep as much electrical symmetry as possible between both inputs.

Another possible configuration for lower-frequency signals is the use of differential input/output amplifiers that can simplify the driver circuit for applications requiring dc-coupling of the input. Flexible in their configurations (see Figure 44), such amplifiers can be used for single-ended-to-differential conversion, signal amplification.

Table 4. Recommended Amplifiers to Drive the Input of the ADS5500

INPUT SIGNAL FREQUENCY	RECOMMENDED AMPLIFIER	TYPE OF AMPLIFIER	USE WITH TRANSFORMER?
DC to 20 MHz	THS4503	Differential In/Out Amp	No
DC to 50 MHz	OPA847	Operational Amp	Yes
DC to 100 MHz	THS4509	Differential In/Out Amp	NO
10 MHz to 120 MHz	OPA695	Operational Amp	Yes
	THS3201	Operational Amp	Yes
	THS3202	Operational Amp	Yes
Over 100 MHz	THS90016	RF Gain Block	Yes

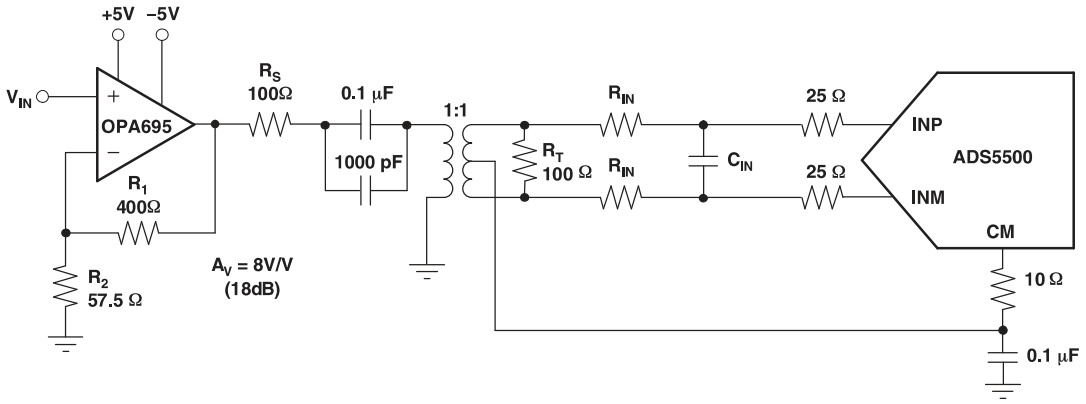


Figure 43. Converting a Single-Ended Input Signal to a Differential Signal Using an RF Transformer

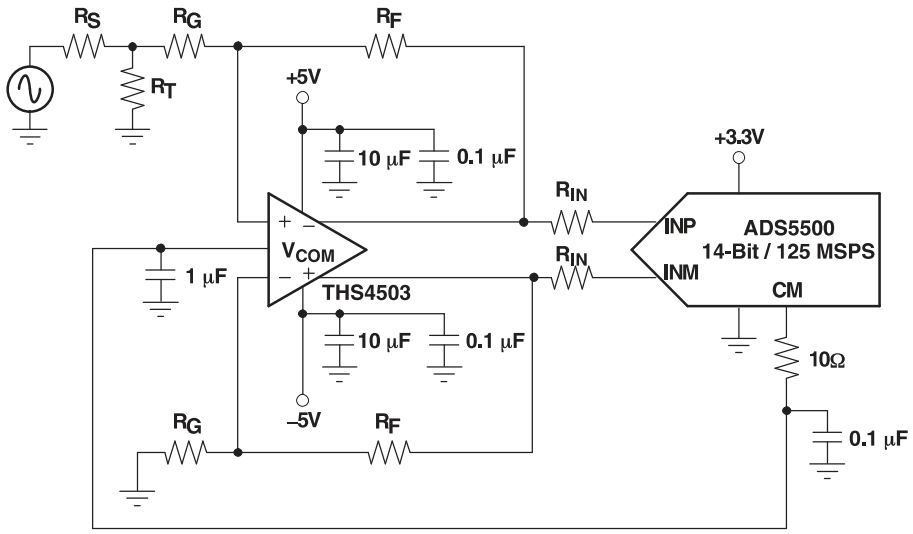


Figure 44. Using the THS4503 With the ADS5500

POWER SUPPLY SEQUENCING

The preferred power-up sequence is to ramp AV_{DD} first, followed by DRV_{DD}, including a simultaneous ramp of AV_{DD} and DRV_{DD}. In the case that DRV_{DD} ramps up first in the system, care must be taken to ensure that AV_{DD} ramps up within 10 ms.

POWER DOWN

The device enters power-down in one of two ways: either by reducing the clock speed or by setting the PDN bit through the serial programming interface. Using the reduced clock speed, power-down may be initiated for clock frequencies below 2 Msps. The exact frequency at which the power down occurs varies from device to device.

Using the serial interface PDN bit to power down the device places the outputs in a high-impedance state and only the internal reference remains on to reduce the power-up time. The power-down mode reduces power dissipation to approximately 180 mW.

REFERENCE CIRCUIT

The ADS5500 has built-in internal reference generation, requiring no external circuitry on the printed circuit board (PCB). For optimum performance, it is best to connect both REFP and REFM to ground with a 1-μF decoupling capacitor (the 1-Ω series resistor shown in Figure 45 is optional). In addition, an external 56.2-kΩ resistor should be connected from IREF (pin 31) to AGND to set the proper current for the operation of the ADC, as shown in Figure 45. No capacitor should be connected between pin 31 and ground; only the 56.2-kΩ resistor should be used.

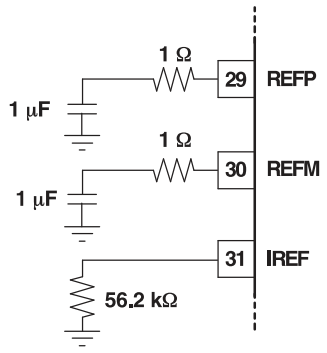


Figure 45. REFP, REFM, and IREF Connections for Optimum Performance

CLOCK INPUT

The ADS5500 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. The common-mode voltage of the clock inputs is set internally to CM (pin 17) using internal 5-kΩ resistors that connect CLKP (pin 10) and CLKM (pin 11) to CM (pin 17), as shown in Figure 46.

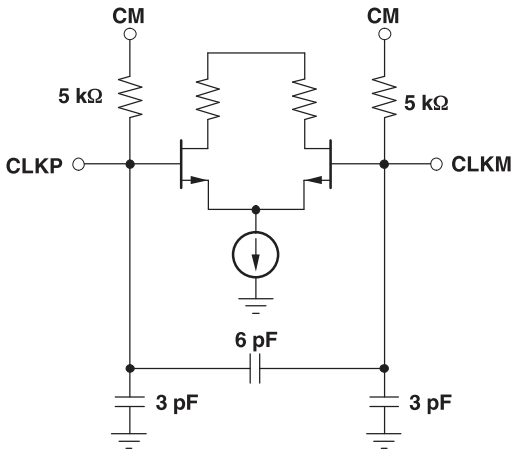


Figure 46. Clock Inputs

When driven with a single-ended CMOS clock input, it is best to connect CLKM (pin 11) to ground with a 0.01-μF capacitor, while CLKP is ac-coupled with a 0.01-μF capacitor to the clock source, as shown in Figure 47.

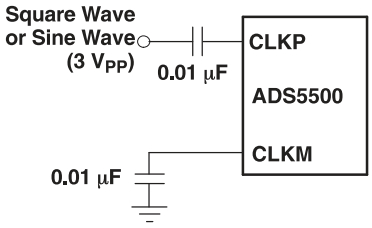


Figure 47. AC-Coupled, Single-Ended Clock Input

The ADS5500 clock input can also be driven differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.01-μF capacitors, as shown in Figure 48.

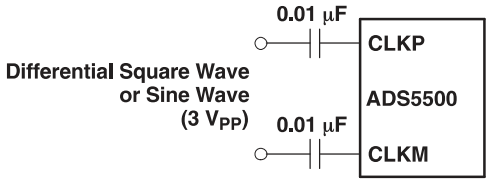


Figure 48. AC-Coupled, Differential Clock Input

For high input frequency sampling, it is recommended to use a clock source with very low jitter. Additionally, the internal ADC core uses both edges of the clock for the conversion process. This means that, ideally, a 50% duty cycle should be provided. Figure 49 shows the performance variation of the ADC versus clock duty cycle.

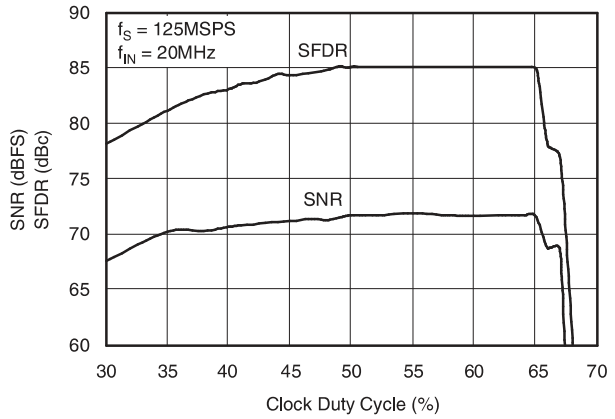


Figure 49. AC Performance vs Clock Duty Cycle

Bandpass filtering of the clock source can help produce a 50% duty cycle clock and reduce the effect of jitter. When using a sinusoidal clock, the clock jitter further improves as the amplitude is increased. In that sense, using a differential clock allows for the use of larger amplitudes without exceeding the supply rails and absolute maximum ratings of the ADC clock input. Figure 50 shows the performance variation of the device versus input clock amplitude. For detailed clocking schemes based on transformer or PECL-level clocks, see the ADS5500EVM user's guide (SLWU010), available for download from www.ti.com.

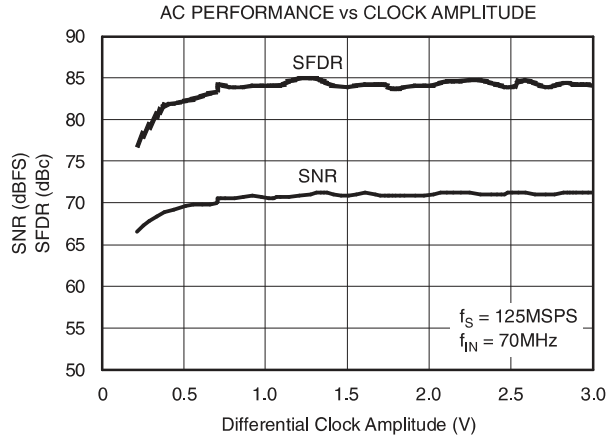


Figure 50. AC Performance vs Clock Amplitudes

INTERNAL DLL

In order to obtain the fastest sampling rates achievable with the ADS5500, the device uses an internal digital delay lock loop (DLL). Nevertheless, the limited frequency range of operation of DLL degrades the performance at clock frequencies below 60 Msps. In order to operate the device below 60 Msps, the internal DLL must be shut off using the DLL OFF mode described in the Serial Interface Programming section. The *Typical Performance Curves* show the performance obtained in both modes of operation: DLL ON (default) and DLL OFF. In either of the two modes, the device enters power-down mode if no clock or slow clock is provided. The limit of the clock frequency where the device functions properly with default settings is ensured to be over 2 MHz.

OUTPUT INFORMATION

The ADC provides 14 data outputs (D13 to D0, with D13 being the MSB and D0 the LSB), a data-ready signal (CLKOUT, pin 43), and an out-of-range indicator (OVR, pin 64) that equals one when the output reaches the full-scale limits.

Two different output formats (straight offset binary or two's complement) and two different output clock polarities (latching output data on rising or falling edge of the output clock) can be selected by setting DFS (pin 40) to one of four different voltages. Table 3 details the four modes. In addition, output enable control (OE, pin 41, active high) is provided to put the outputs into a high-impedance state.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0x3FFF in straight offset binary output format, and 0x1FFF in 2's complement output format. For a negative input overdrive, the output code is 0x0000 in straight offset binary output format and 0x2000 in two's complement output format. These outputs to an overdrive signal are ensured through design and characterization.

The output circuitry of the ADS5500, by design, minimizes the noise produced by the data switching transients and, in particular, its coupling to the ADC analog circuitry. Output D4 (pin 51) senses the load capacitance and adjusts the drive capability of all the output pins of the ADC to maintain the same output slew rate described in the timing diagram of Figure 1. Care should be taken to ensure that all output lines (including CLKOUT) have nearly the same load as D4 (pin 51). This circuit also reduces the sensitivity of the output timing versus supply voltage or temperature. Placing external resistors in series with the outputs is not recommended.

The timing characteristics of the digital outputs change for sampling rates below the 125 Msps maximum sampling frequency. Table 5 through Table 7 show the values of various timing parameters for lower sampling frequencies, both with DLL on and off.

To use the input clock as the data capture clock, it is necessary to delay the input clock by a delay (t_d) that results in the desired setup or hold time. Use either of the following equations to calculate the value of t_d.

Desired setup time = $t_d - t_{START}$

Desired hold time = $t_{END} - t_d$

Table 5. Timing Characteristics at Additional Sampling Frequencies (DLL ON)

F_S (Msps)	t_{su} (ns)			t_h (ns)			t_{START} (ns)			t_{END} (ns)			t_r (ns)			t_f (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
105	2.2	2.8		2.2	2.5			1.9	2.8	5.8	7.3			4.4	5.1		3.3	3.8
80	2.8	3.7		2.8	3.3			0.5	1.7	5.3	7.9			5.8	6.6		4.4	5.3
65	3.8	4.6		3.6	4.1			–0.5	0.8	5.3	8.5			6.7	7.2		5.5	6.4

Table 6. Timing Characteristics at Additional Sampling Frequencies (DLL OFF)

F_S (Msps)	t_{su} (ns)			t_h (ns)			t_{START} (ns)			t_{END} (ns)			t_r (ns)			t_f (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	3.2	4.2		1.8	3			3.8	5	8.4	11			5.8	6.6		4.4	5.3
65	4.3	5.7		2	3			2.8	4.5	8.3	11.8			6.6	7.2		5.5	6.4
40	8.5	11		2.6	3.5			–1	1.5	8.9	14.5			7.5	8		7.3	7.8
20	17	25.7		2.5	4.7			–9.8	2	9.5	21.6			7.5	8		7.6	8
10	27	51		4	6.5			–30	–3	11.5	31							
2	284	370		8	19			185	320	515	576			50	82		75	150

Table 7. Timing Characteristics at Additional Sampling Frequencies (DLL ON)

F_S (Msps)	CLKOUT, Rise Time t_r (ns)			CLKOUT, Fall Time t_f (ns)			CLKOUT Jitter, Peak-to-Peak t_{JIT} (ps)			Input-to-Output Clock Delay t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
105		2	2.2		1.7	1.8		175	250	4	4.7	5.5
80		2.5	2.8		2.1	2.3		210	315	3.7	4.3	5.1
65		3.1	3.5		2.6	2.9		260	380	3.5	4.1	4.8

Table 8. Timing Characteristics at Additional Sampling Frequencies (DLL OFF)

F_S (Msps)	CLKOUT, Rise Time t_r (ns)			CLKOUT, Fall Time t_f (ns)			CLKOUT Jitter, Peak-to-Peak t_{JIT} (ps)			Input-to-Output Clock Delay t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80		2.5	2.8		2.1	2.3		210	315	7.1	8	8.9
65		3.1	3.5		2.6	2.9		260	380	7.8	8.5	9.4
40		4.8	5.3		4	4.4		445	650	9.5	10.4	11.4
20		8.3	9.5		7.6	8.2		800	1200	13	15.5	18
10										16	20.7	25.5
2		31	52		36	65		2610	4400	537	551	567

SERIAL PROGRAMMING INTERFACE

The ADS5500 has internal registers for the programming of some of the modes described in the previous sections. The registers should be reset after power-up by applying a 2 µs (minimum) high pulse on RESET (pin 35); this also resets the entire ADC and sets the data outputs to low. This pin has a 200-kΩ internal pullup resistor to AV_{DD}. The programming is done through a three-wire interface. The timing diagram and serial register setting in the Serial Programing Interface section describe the programming of this register.

Table 2 shows the different modes and the bit values to be written on the register to enable them.

Note that some of these modes may modify the standard operation of the device and possibly vary the performance with respect to the typical data shown in this data sheet.

Applying a RESET signal is required to set the internal registers to their default states for normal operation. If the hardware RESET function is not used in the system, the RESET pin must be tied to ground and it is necessary to write the default values to the internal registers through the serial programming interface. The registers must be written in the following order.

Write 9000h (Address 9, Data 000)
Write A000h (Address A, Data 000)
Write B000h (Address B, Data 000)
Write C000h (Address C, Data 000)

Write D000h (Address D, Data 000)
Write E000h (Address E, Data 804)
Write 0000h (Address 0, Data 000)
Write 1000h (Address 1, Data 000)
Write F000h (Address F, Data 000).

NOTE: This procedure is only required if a RESET pulse is not provided to the device.

PowerPAD PACKAGE

The PowerPAD package is a thermally enhanced standard size IC package designed to eliminate the use of bulky heat sinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques and can be removed and replaced using standard repair procedures. AVDD. The programming is done through a three-wire interface. The timing diagram and serial register setting in the Serial Programing Interface section describe the programming of this register.

The PowerPAD package is designed so that the lead frame die pad (or thermal pad) is exposed on the bottom of the IC. This provides a low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the printed circuit board (PCB), using the PCB as a heatsink. Programming is done through a three-wire interface. The timing diagram and serial register setting in the Serial Programing Interface section describe the programming of this register.

Assembly Process

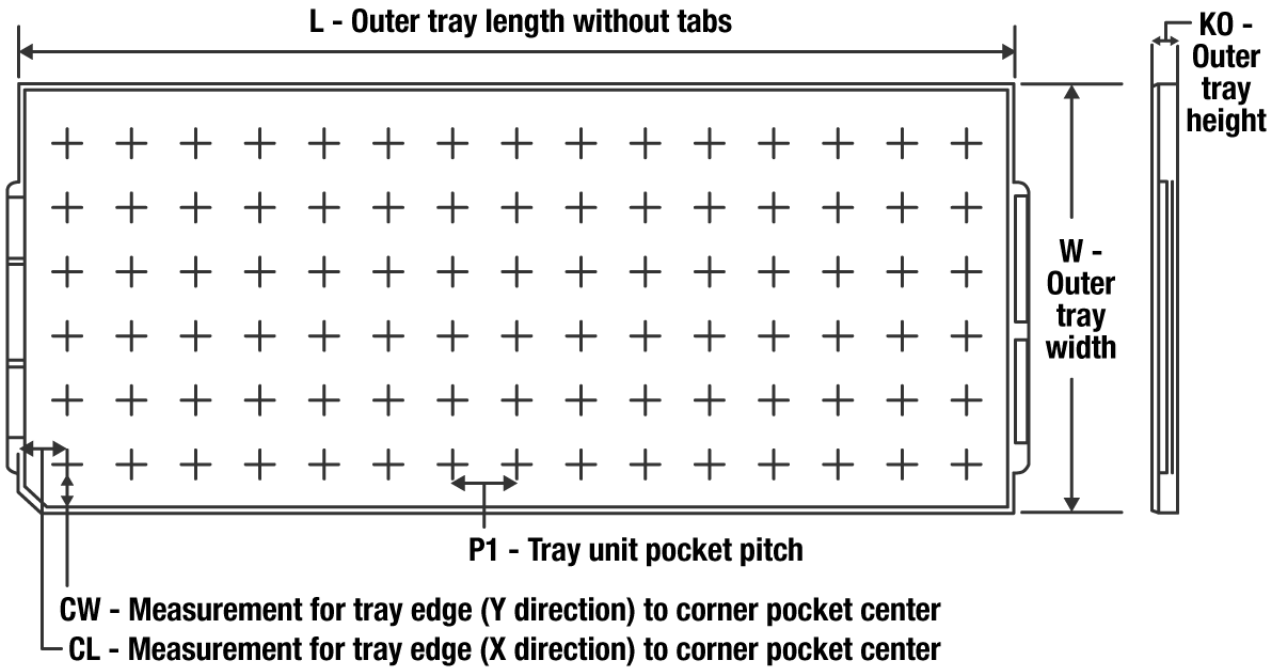
1. Prepare the PCB top-side etch pattern including etch for the leads as well as the thermal pad as illustrated in the Mechanical Data section. The recommended thermal pad dimension is 8 mm x 8 mm.
2. Place a 5-by-5 array of thermal vias in the thermal pad area. These holes should be 13 mils in diameter. The small size prevents wicking of the solder through the holes.
3. It is recommended to place a small number of 25 mil diameter holes under the package, but outside the thermal pad area to provide an additional heat path.
4. Connect all holes (both those inside and outside the thermal pad area) to an internal copper plane (such as a ground plane).
5. Do not use the typical web or spoke via connection pattern when connecting the thermal vias to the ground plane. The spoke pattern increases the thermal resistance to the ground plane.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area.
7. Cover the entire bottom side of the PowerPAD vias to prevent solder wicking.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.

For more detailed information regarding the PowerPAD package and its thermal properties, see either the SLMA004B application brief PowerPAD Made Easy or SLMA002 technical brief PowerPAD Thermally Enhanced Package.

REVISION HISTORY

REVISION	DATE	DESCRIPTION
0.0	12/03	Preliminary data sheet released
1.0	03/04	Data sheet updated to reflect RTM silicon
2.0	09/05	Added information regarding thermal pad size and thermal characteristics of the package.
		Removed input current from Absolute Maximum Ratings table. Updated specifications to AGND and DRGND. Added notes regarding the input voltage overstress requirements.
		Changed minimum recommended sampling rate to 2 Msps.
		Clarified the Electrical Characteristics measurement conditions.
		Changed analog input common-mode current specification.
		Removed maximum sampling rate from specification table.
		Added Voltage Overload Recovery Time specification.
		Changed offset temperature coefficient to units of mV/°C.
		Changed power dissipation reporting to separate analog and digital power dissipation.
		Changed two-tone intermodulation distortion units to dBFS and updated the specification values to reflect this change.
		Clarified the Digital Characteristics measurement conditions.
		Added min V_{OH} and max V_{OL} specifications.
		Added data valid with respect to the input clock, output clock jitter, wakeup time, and output clock rise and fall time parameters.
		Clarified the Timing Characteristics measurement conditions.
		Updated the timing diagram in Figure 1 to include t_{START} and t_{END} timing parameters.
		Added minimum and maximum specifications for various timing parameters.
		Added section on Reset Timing.
		Clarified serial interface data word format.
		Clarified output capture test modes.
		Simplified the information given in Table 3.
		Updated the definitions section.
		Clarified measurement conditions for the specifications plots.
		Corrected text annotations on the WCDMA signal plot.
		Added axis label to HD3 with DLL ON contour plot.
		Updated Figure 4 to correct parameter values and improve readability.
		Added 25-Ω series resistors to ADC inputs in Figure 5.
		Corrected text in Input Configuration section to accurately reflect the CM voltage decoupling depicted in Figure 5.
		Updated Equation 5 to match the new definition of common-mode input current and minimum sample rate.
		Added 25-Ω series resistors to ADC inputs in Figure 6.
		Changed Power Supply Sequence section to reduce constraints on the power-up sequence.
		Updated the Power Down section to reflect the newly specified 2 Msps minimum sampling rate.
		Updated Output Information text to include information on the output data in over-range conditions, describe data capture using the input clock, and add tables to specify timing parameters at various sampling rates.
3.0	10/05	Improved SNR performance parameters.
		Updated Reference Circuit section to reflect that the 1-Ω series resistors to REFP and REFM are now optional.
		Updated timing parameters in Table 5 through Table 8 to reflect revised silicon timing.
REV G	02/07	Added min/max specs for offset and gain errors

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS5500IPAP	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

GENERIC PACKAGE VIEW

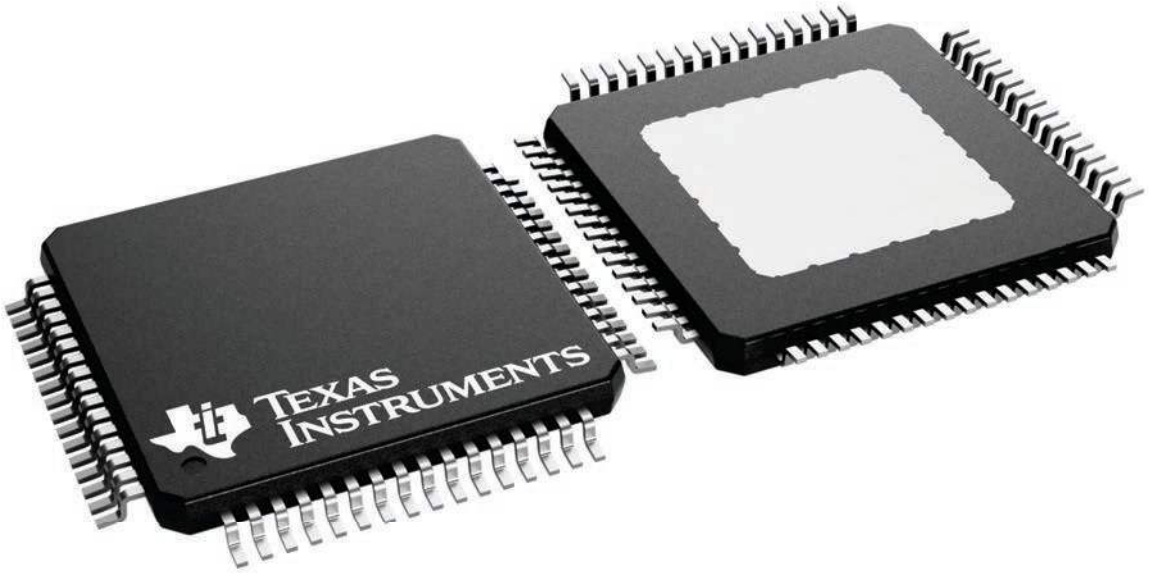
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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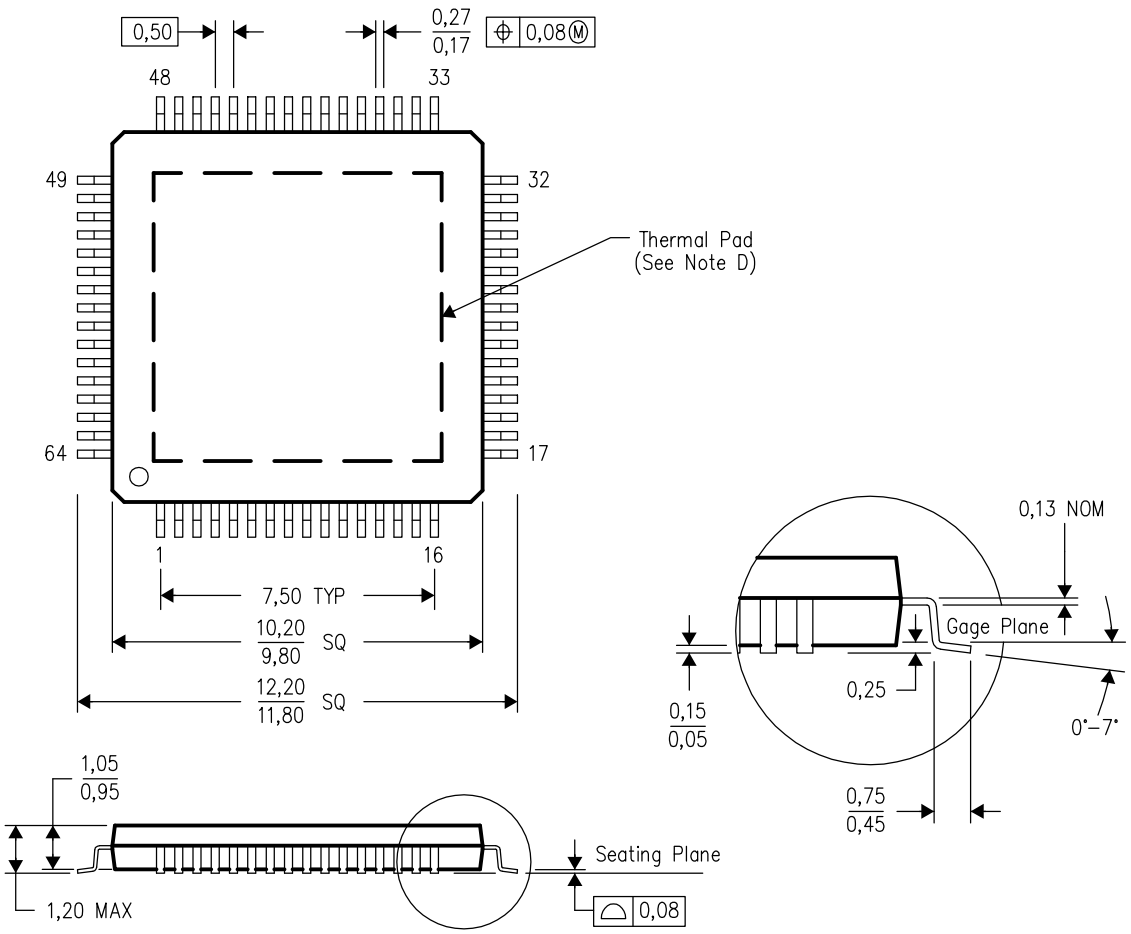
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

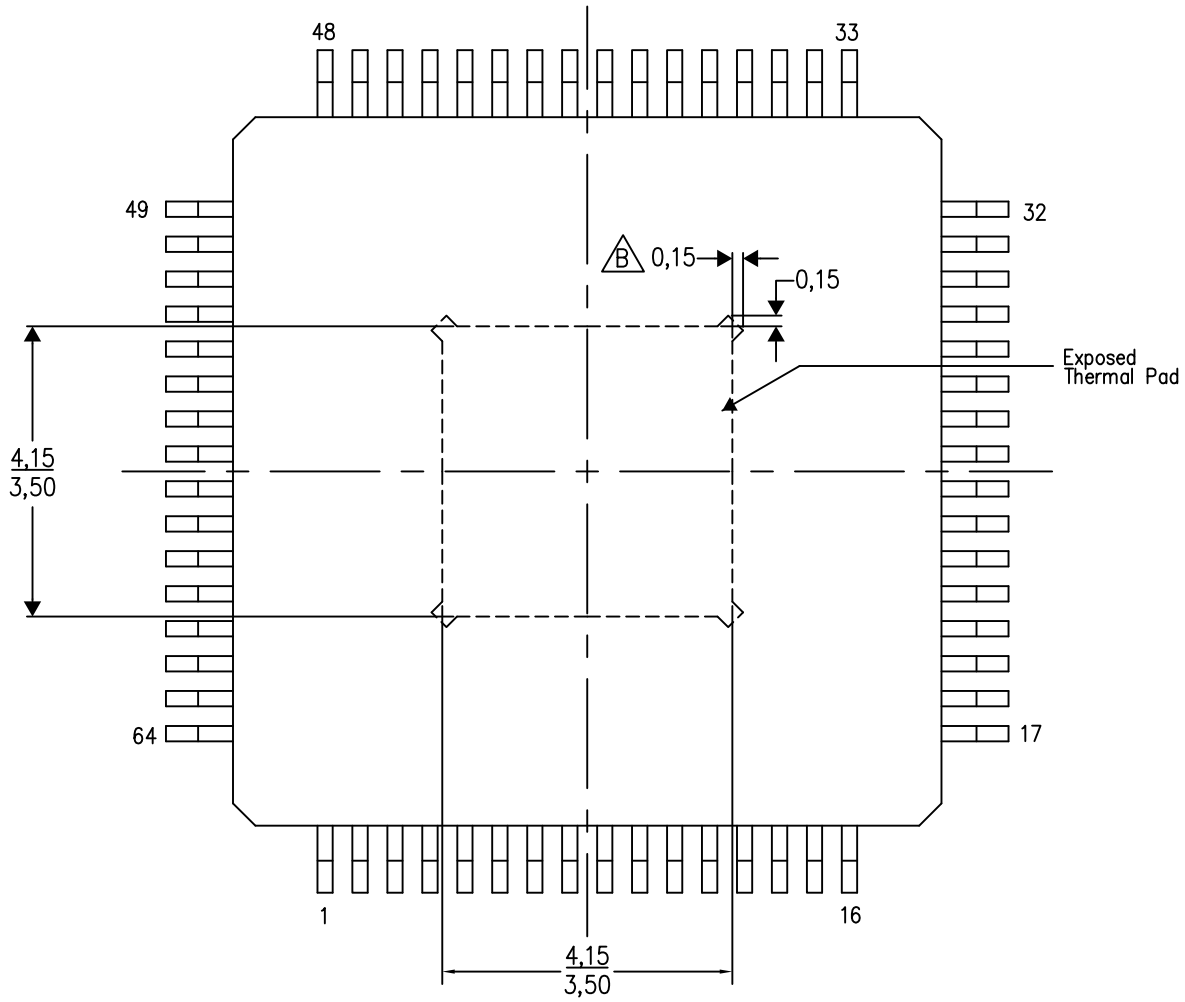
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

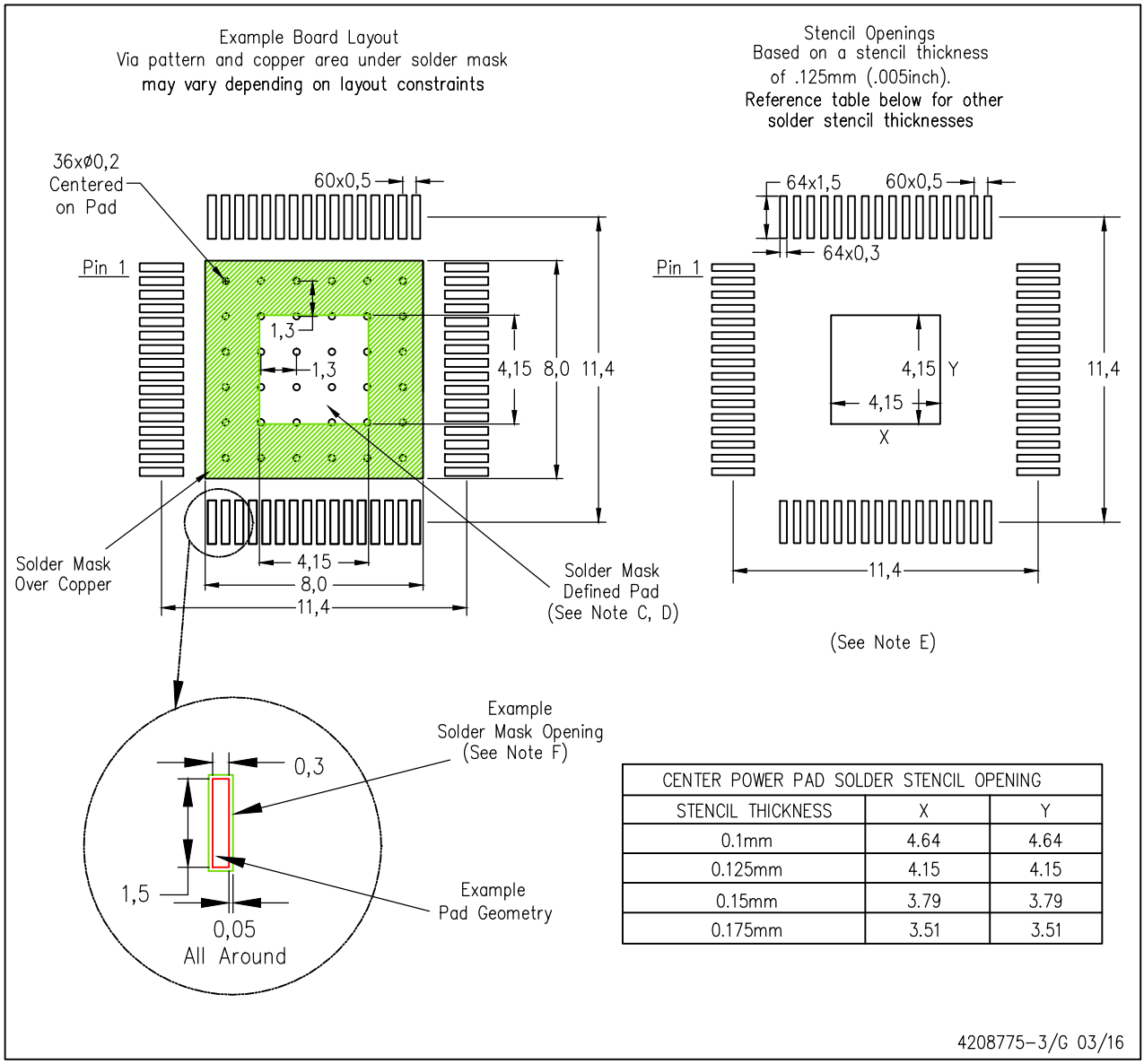
4206326–2/P 05/14

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	4.64	4.64
0.125mm	4.15	4.15
0.15mm	3.79	3.79
0.175mm	3.51	3.51

4208775–3/G 03/16

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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