MC33102

Two-State, Micropower Operational Amplifier

The MC33102 dual operational amplifier is an innovative design concept that has two separate states, a sleep mode and an awake mode. In sleep mode, the amplifier is active and waiting for an input signal. When a signal is applied causing the amplifier to source or sink 160 μA (typically) to the load, it will automatically switch to the awake mode which offers higher slew rate, gain bandwidth, and drive capability.

- Two States: “sleep mode” (Micropower) and “awake mode” (High Performance)
- Switches from Sleep Mode to Awake Mode in 4.0 μs when Output Current Exceeds the Threshold Current (R_L = 600 Ω)
- Independent Sleep Mode Function for Each Op Amp
- Standard Pinouts − No Additional Pins or Components Required
- Sleep Mode State − Can Be Used in the Low Current Idle State as a Fully Functional Micropower Amplifier
- Automatic Return to Sleep Mode when Output Current Drops Below Threshold
- No Deadband/Crossover Distortion; as Low as 1.0 Hz in the Awake Mode
- Drop−in Replacement for Many Other Dual Op Amps
- ESD Clamps on Inputs Increase Reliability without Affecting Device Operation

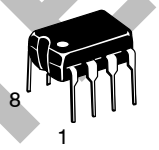
TYPICAL SLEEP MODE/AWAKE MODE PERFORMANCE

Characteristic	Sleep Mode (Typical)	Awake Mode (Typical)	Unit
Low Current Drain	45	750	μA
Low Input Offset Voltage	0.15	0.15	mV
High Output Current Capability	0.15	50	mA
Low T.C. of Input Offset Voltage	1.0	1.0	μV/°C
High Gain Bandwidth (@ 20 kHz)	0.33	4.6	MHz
High Slew Rate	0.16	1.7	V/μs
Low Noise (@ 1.0 kHz)	28	9.0	nV/√Hz

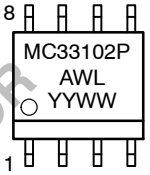
ON Semiconductor

http://onsemi.com

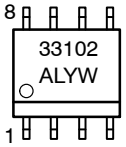
MARKING DIAGRAMS



PDIP−8
P SUFFIX
CASE 626

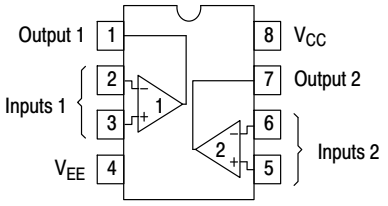


SO−8
D SUFFIX
CASE 751



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS

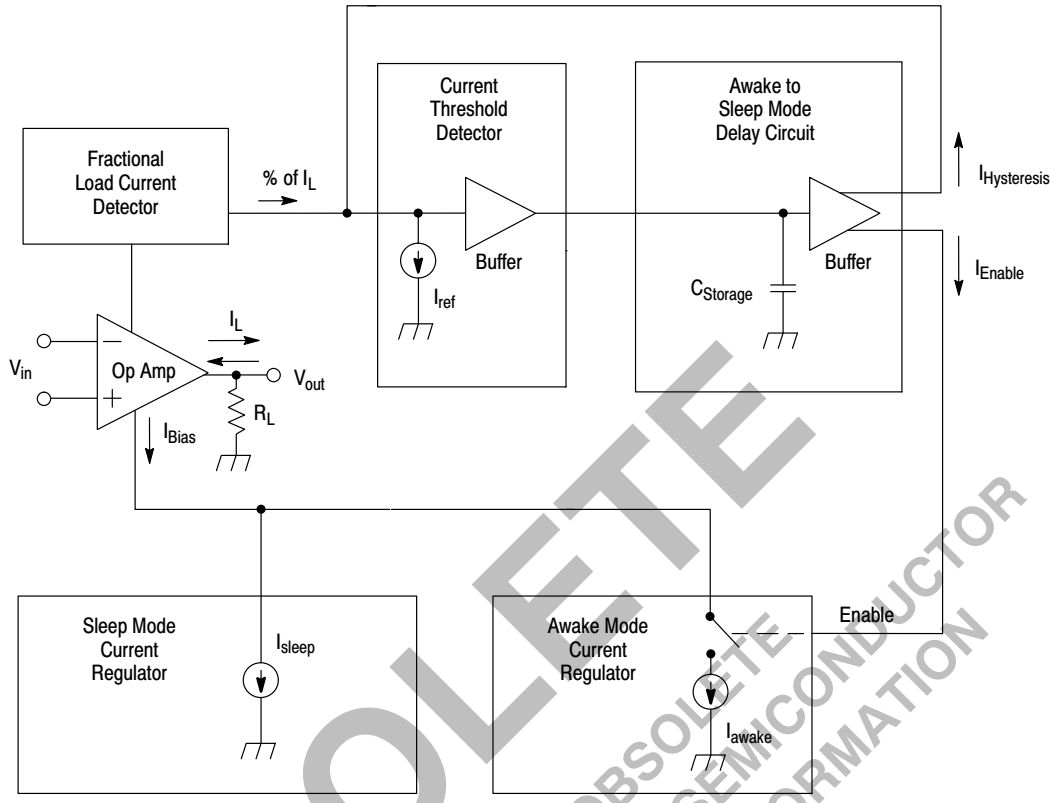


(Dual, Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC33102D	SO−8	98 Units/Rail
MC33102DR2	SO−8	2500 Tape & Reel
MC33102P	PDIP−8	50 Units/Rail

Simplified Block Diagram



MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range Input Voltage Range	V_{IDR} V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Note 2	sec
Maximum Junction Temperature Storage Temperature	T_J T_{stg}	+150 −65 to +150	°C
Maximum Power Dissipation	P_D	Note 2	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (refer to Figure 1).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	2	$\lvert V_{IO} \rvert$				mV
Sleep Mode						
T_A = +25°C			–	0.15	2.0	
T_A = −40° to +85°C			–	–	3.0	
Awake Mode						
T_A = +25°C			–	0.15	2.0	
T_A = −40° to +85°C			–	–	3.0	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\Delta V_{IO}/\Delta T$				μV/°C
T_A = −40° to +85°C (Sleep Mode and Awake Mode)			–	1.0	–	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 6	I_{IB}				nA
Sleep Mode						
T_A = +25°C			–	8.0	50	
T_A = −40° to +85°C			–	–	60	
Awake Mode						
T_A = +25°C			–	100	500	
T_A = −40° to +85°C			–	–	600	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	–	$\lvert I_{IO} \rvert$				nA
Sleep Mode						
T_A = +25°C			–	0.5	5.0	
T_A = −40° to +85°C			–	–	6.0	
Awake Mode						
T_A = +25°C			–	5.0	50	
T_A = −40° to +85°C			–	–	60	
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	5	V_{ICR}				V
Sleep Mode and Awake Mode			−13	−14.8	–	
			–	+14.2	+13	
Large Signal Voltage Gain	7	A_{VOL}				kV/V
Sleep Mode (RL = 1.0 MΩ)						
T_A = +25°C			25	200	–	
T_A = −40° to +85°C			15	–	–	
Awake Mode (V_O = ±10 V, R_L = 600 Ω)						
T_A = +25°C			50	700	–	
T_A = −40° to +85°C			25	–	–	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 10					V
Sleep Mode (V_{CC} = +15 V, V_{EE} = −15 V)						
R_L = 1.0 MΩ		V_{O+}	+13.5	+14.2	–	
R_L = 1.0 MΩ		V_{O-}	–	−14.2	−13.5	
Awake Mode (V_{CC} = +15 V, V_{EE} = −15 V)						V
R_L = 600 Ω		V_{O+}	+12.5	+13.6	–	
R_L = 600 Ω		V_{O-}	–	−13.6	−12.5	
R_L = 2.0 kΩ		V_{O+}	+13.3	+14	–	
R_L = 2.0 kΩ		V_{O-}	–	−14	−13.3	
Awake Mode (V_{CC} = +2.5 V, V_{EE} = −2.5 V)						
R_L = 600 Ω		V_{O+}	+1.1	+1.6	–	
R_L = 600 Ω		V_{O-}	–	−1.6	−1.1	
Common Mode Rejection (V_{CM} = ±13 V)	11	CMR				dB
Sleep Mode and Awake Mode			80	90	–	
Power Supply Rejection (V_{CC}/V_{EE} = +15 V/−15 V, 5.0 V/−15 V, +15 V/−5.0 V)	12	PSR				dB
Sleep Mode and Awake Mode			80	100	–	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Output Transition Current	13, 14					μA
Sleep Mode to Awake Mode (Source/Sink)		$\|I_{TH1}\|$				
(V_S = ±15 V)			200	160	–	
(V_S = ±2.5 V)			250	200	–	
Awake Mode to Sleep Mode (Source/Sink)		$\|I_{TH2}\|$				
(V_S = ±15 V)			–	142	90	
(V_S = ±2.5 V)			–	180	140	
Output Short Circuit Current (Awake Mode)	15, 16	$\|I_{SC}\|$				mA
(V_{ID} = ±1.0 V, Output to Ground)						
Source			50	110	–	
Sink			50	110	–	
Power Supply Current (per Amplifier) (A_{CL} = 1, V_O = 0V)	17	I_D				μA
Sleep Mode (V_S = ±15 V)						
T_A = +25°C			–	45	65	
T_A = −40° to +85°C			–	48	70	
Sleep Mode (V_S = ±2.5 V)						
T_A = +25°C			–	38	65	
T_A = −40° to +85°C			–	42	–	
Awake Mode (V_S = ±15 V)						
T_A = +25°C			–	750	800	
T_A = −40° to +85°C			–	800	900	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −5.0 V to +5.0 V, C_L = 50 pF, A_V = 1.0)	18	SR				V/μs
Sleep mode (R_L = 1.0 MΩ)			0.10	0.16	–	
Awake mode (R_L = 600 Ω)			1.0	1.7	–	
Gain Bandwidth Product	19	GBW				MHz
Sleep mode (f = 10 kHz)			0.25	0.33	–	
Awake mode (f = 20 kHz)			3.5	4.6	–	
Sleep mode to Awake mode Transition Time	20, 21	t_{tr1}				μs
(A_{CL} = 0.1, V_{in} = 0 V to +5.0 V)						
R_L = 600 Ω			–	4.0	–	
R_L = 10 kΩ			–	15	–	
Awake mode to Sleep mode Transition Time	22	t_{tr2}	–	1.5	–	sec
Unity Gain Frequency (Open Loop)		f_U				kHz
Sleep mode (R_L = 100 kΩ, C_L = 0 pF)			–	200	–	
Awake mode (R_L = 600 Ω, C_L = 0 pF)			–	2500	–	
Gain Margin	23, 25	A_M				dB
Sleep mode (R_L = 100 kΩ, C_L = 0 pF)			–	13	–	
Awake mode (R_L = 600 Ω, C_L = 0 pF)			–	12	–	
Phase Margin	24, 26	$\varnothing_M$				Degrees
Sleep mode (R_L = 100 kΩ, C_L = 0 pF)			–	60	–	
Awake mode (R_L = 600 Ω, C_L = 0 pF)			–	60	–	
Channel Separation (f = 100 Hz to 20 kHz)	29	CS				dB
Sleep mode and Awake mode			–	120	–	
Power Bandwidth (Awake mode)		BW_P				kHz
(V_O = 10 V_{pp}, R_L = 100 kΩ, THD ≤ 1%)			–	20	–	
Total Harmonic Distortion (V_O = 2.0 V_{pp}, A_V = 1.0)	30	THD				%
Awake mode (R_L = 600 Ω)						
f = 1.0 kHz			–	0.005	–	
f = 10 kHz			–	0.016	–	
f = 20 kHz			–	0.031	–	
DC Output Impedance (V_O = 0 V, A_V = 10, I_Q = 10 μA)	31	R_O				Ω
Sleep mode			–	1.0 k	–	
Awake mode			–	96	–	
Differential Input Resistance (V_{CM} = 0 V)		R_{in}				MΩ
Sleep mode			–	1.3	–	
Awake mode			–	0.17	–	
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}				pF
Sleep mode			–	0.4	–	
Awake mode			–	4.0	–	
Equivalent Input Noise Voltage (f = 1.0 kHz, R_S = 100 Ω)	32	e_n				nV/√Hz
Sleep mode			–	28	–	
Awake mode			–	9.0	–	
Equivalent Input Noise Current (f = 1.0 kHz)	33	i_n				pA/√Hz
Sleep mode			–	0.01	–	
Awake mode			–	0.05	–	

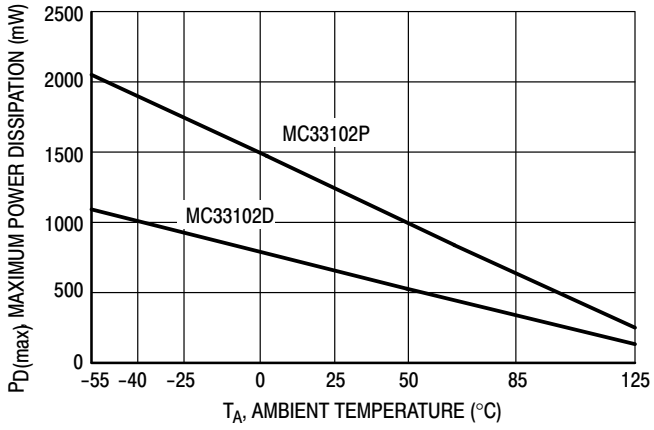


Figure 1. Maximum Power Dissipation versus Temperature

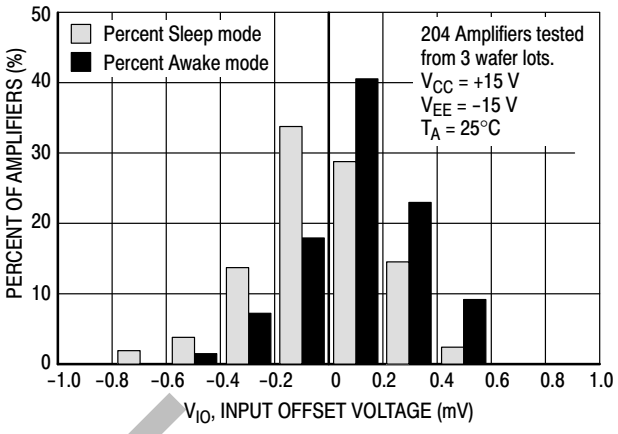


Figure 2. Distribution of Input Offset Voltage (MC33102D Package)

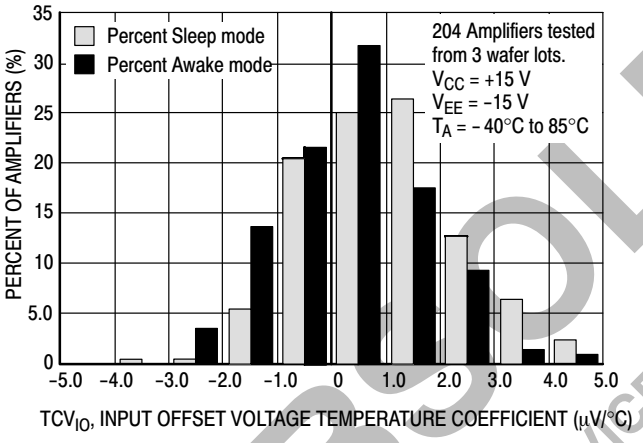


Figure 3. Input Offset Voltage Temperature Coefficient Distribution (MC33102D Package)

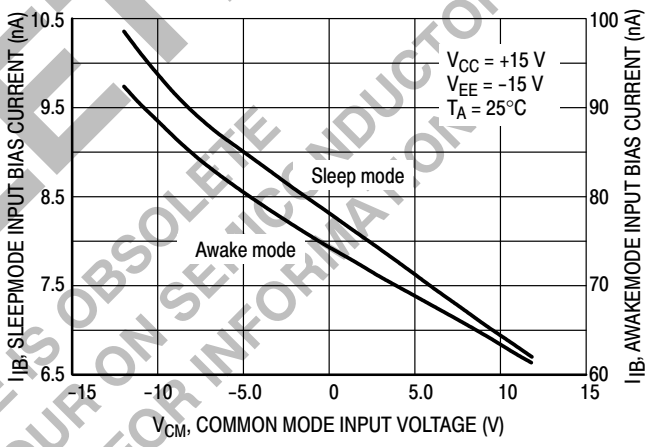


Figure 4. Input Bias Current versus Common Mode Input Voltage

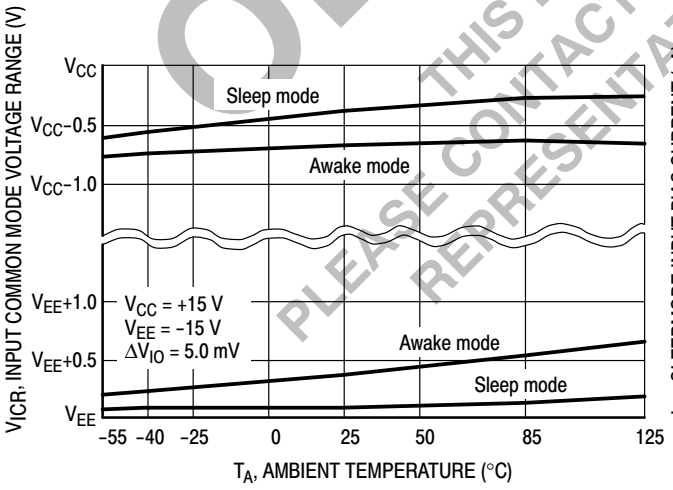


Figure 5. Input Common Mode Voltage Range versus Temperature

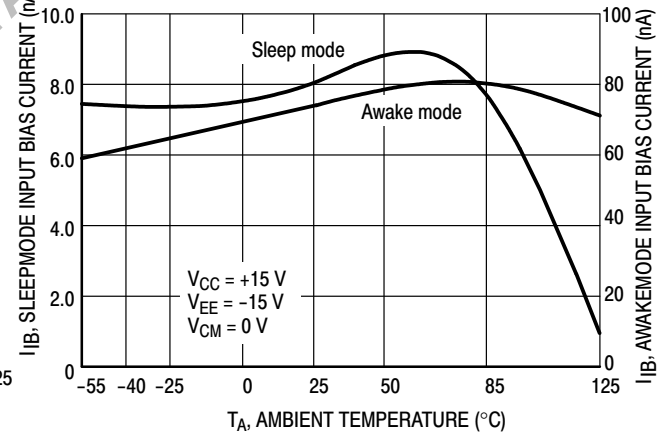


Figure 6. Input Bias Current versus Temperature

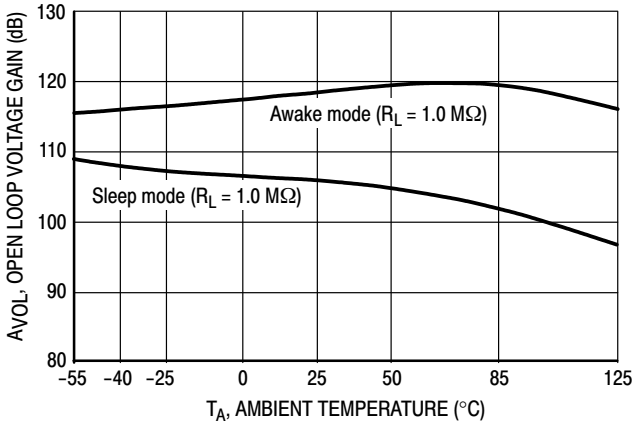


Figure 7. Open Loop Voltage Gain versus Temperature

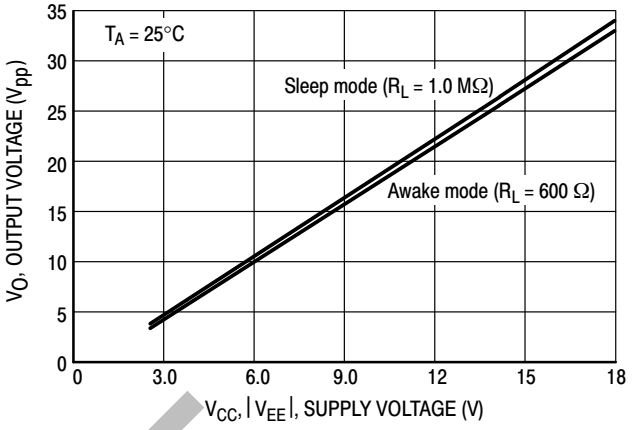


Figure 8. Output Voltage Swing versus Supply Voltage

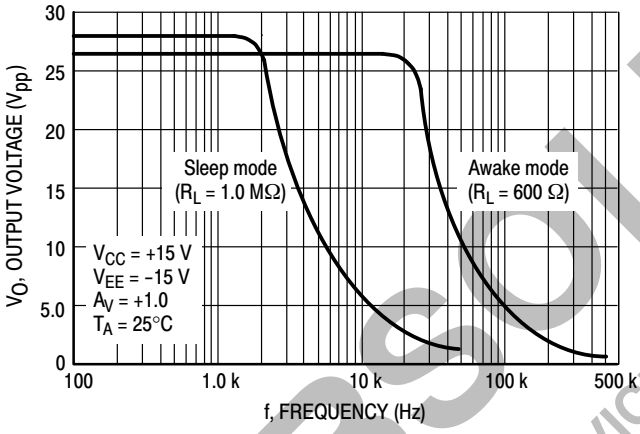


Figure 9. Output Voltage versus Frequency

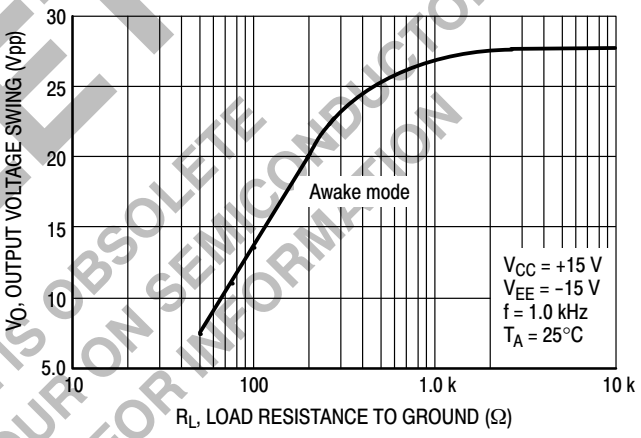


Figure 10. Maximum Peak−to−Peak Output Voltage Swing versus Load Resistance

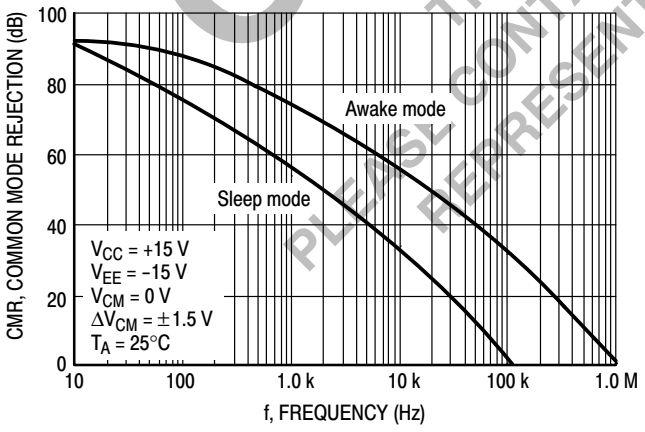


Figure 11. Common Mode Rejection versus Frequency

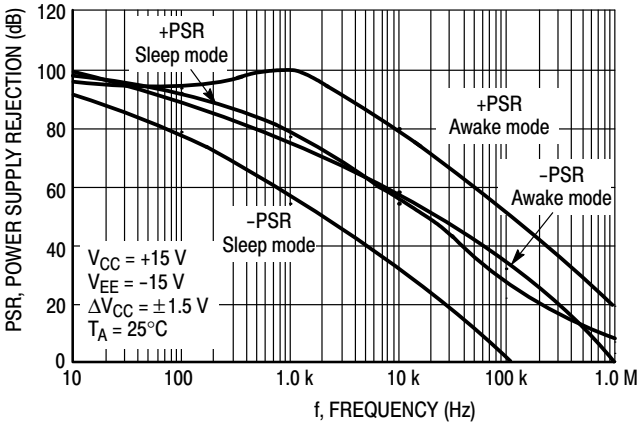


Figure 12. Power Supply Rejection versus Frequency

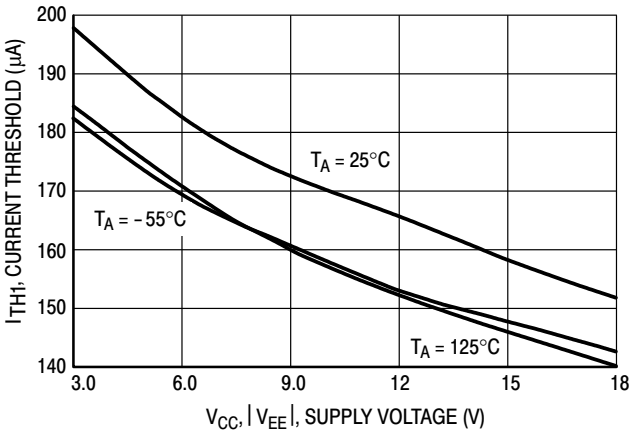


Figure 13. Sleep Mode to Awake Mode Current Threshold versus Supply Voltage

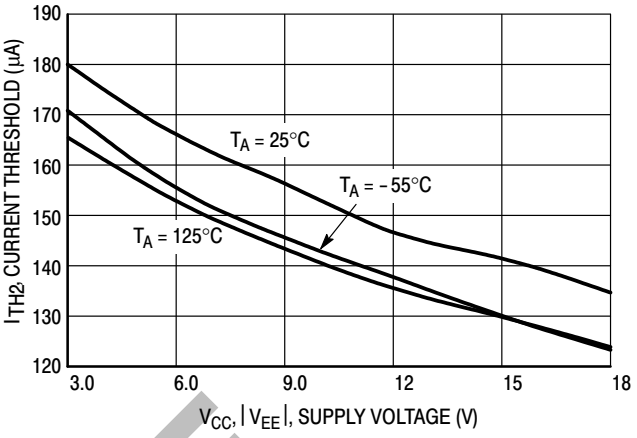


Figure 14. Awake Mode to Sleep Mode Current Threshold versus Supply Voltage

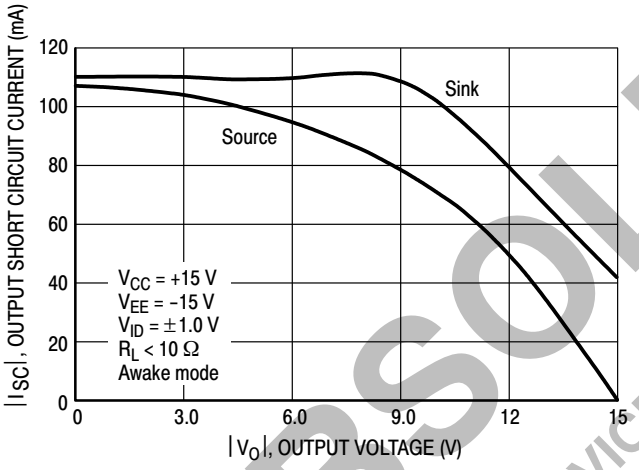


Figure 15. Output Short Circuit Current versus Output Voltage

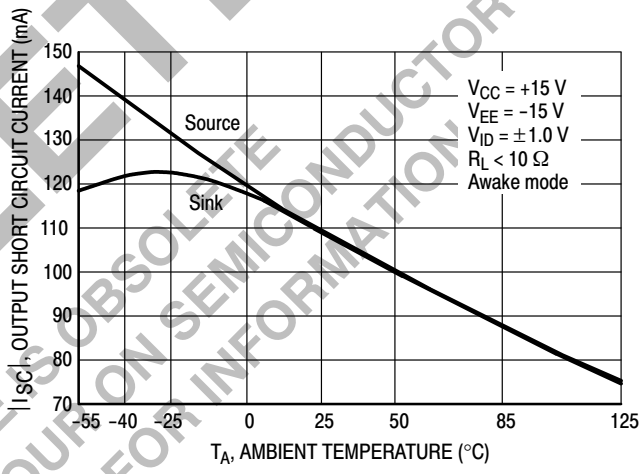


Figure 16. Output Short Circuit Current versus Temperature

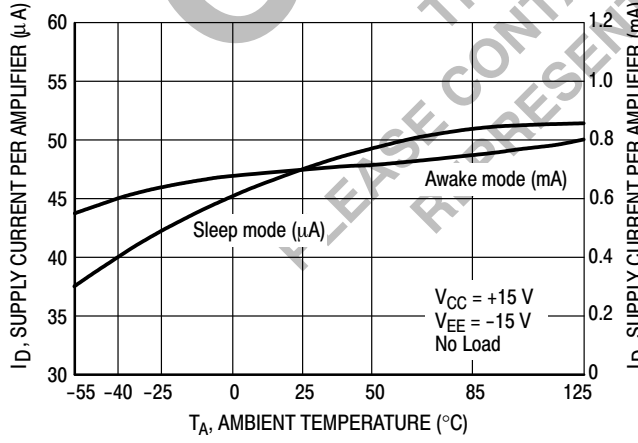


Figure 17. Power Supply Current Per Amplifier versus Temperature

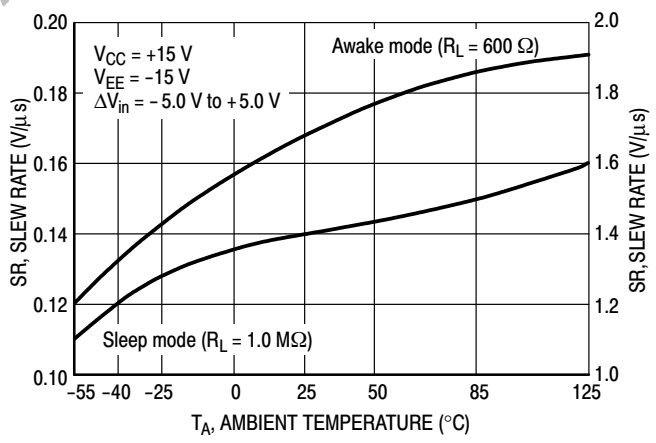


Figure 18. Slew Rate versus Temperature

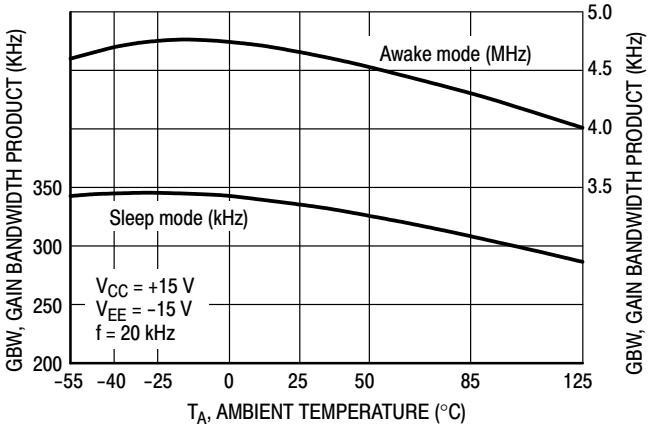


Figure 19. Gain Bandwidth Product versus Temperature

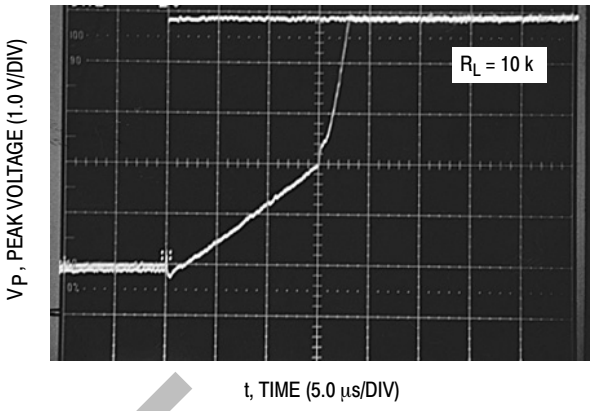


Figure 20. Sleep Mode to Awake Mode Transition Time

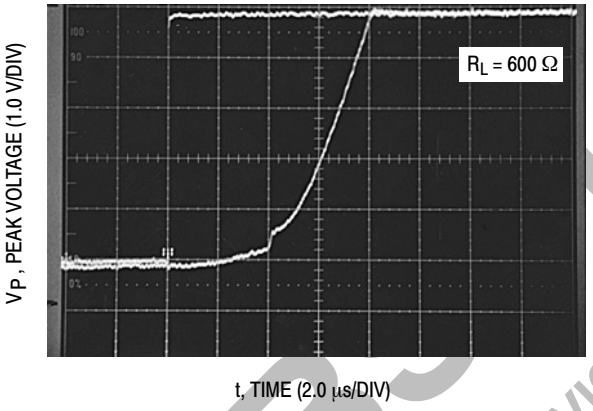


Figure 21. Sleep Mode to Awake Mode Transition Time

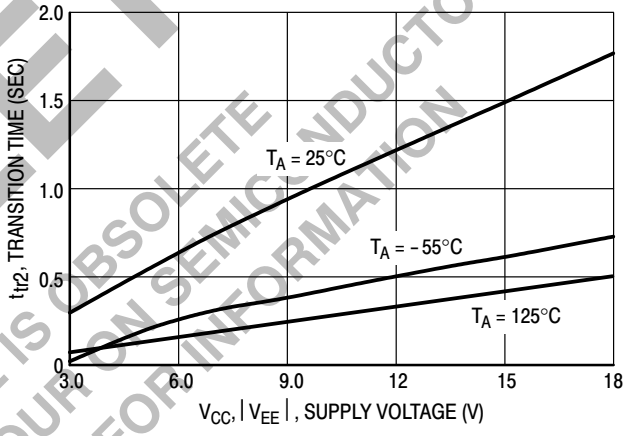


Figure 22. Awake Mode to Sleep Mode Transition Time versus Supply Voltage

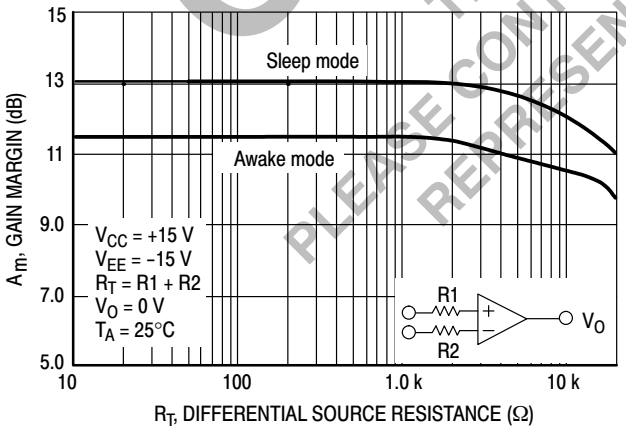


Figure 23. Gain Margin versus Differential Source Resistance

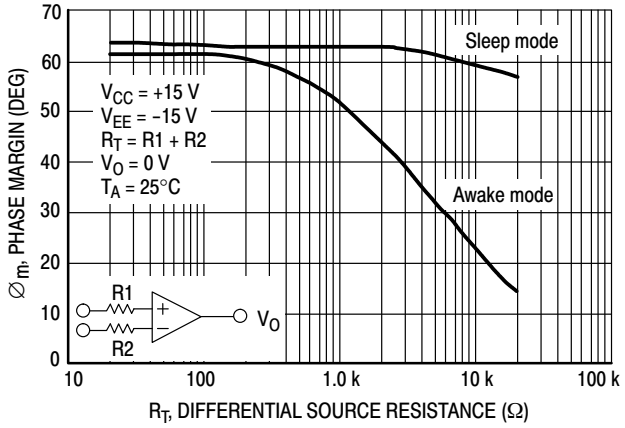


Figure 24. Phase Margin versus Differential Source Resistance

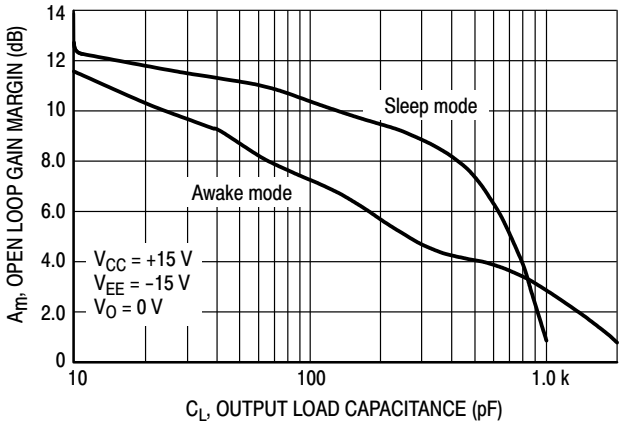


Figure 25. Open Loop Gain Margin versus Output Load Capacitance

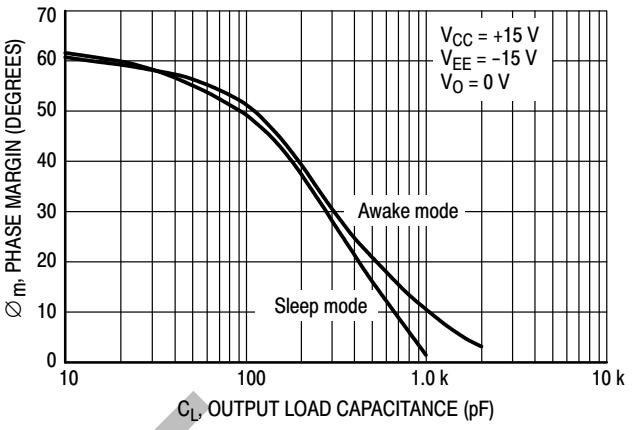


Figure 26. Phase Margin versus Output Load Capacitance

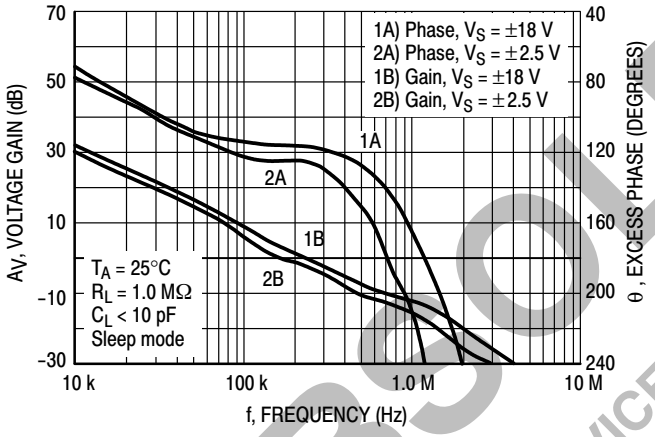


Figure 27. Sleep Mode Voltage Gain and Phase versus Frequency

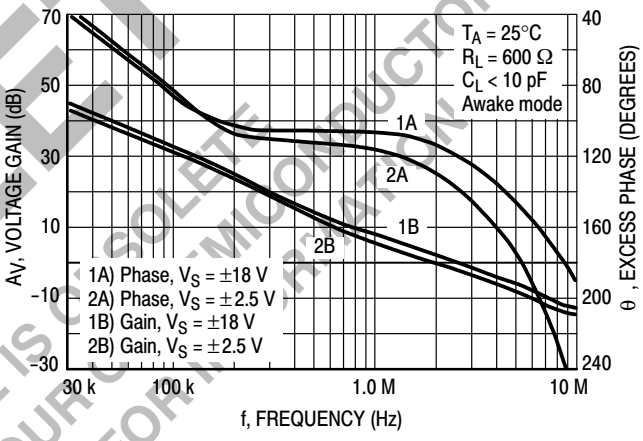


Figure 28. Awake Mode Voltage Gain and Phase versus Frequency

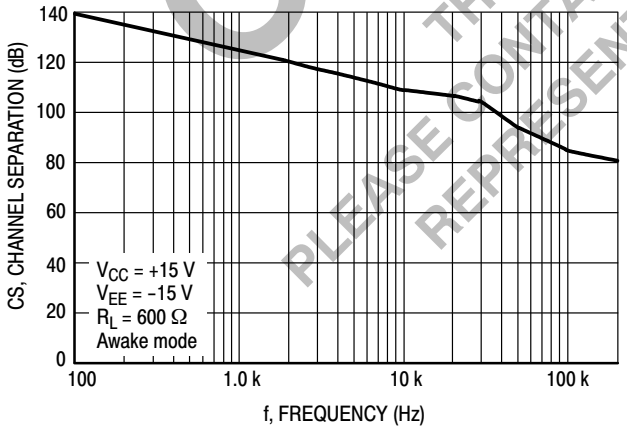


Figure 29. Channel Separation versus Frequency

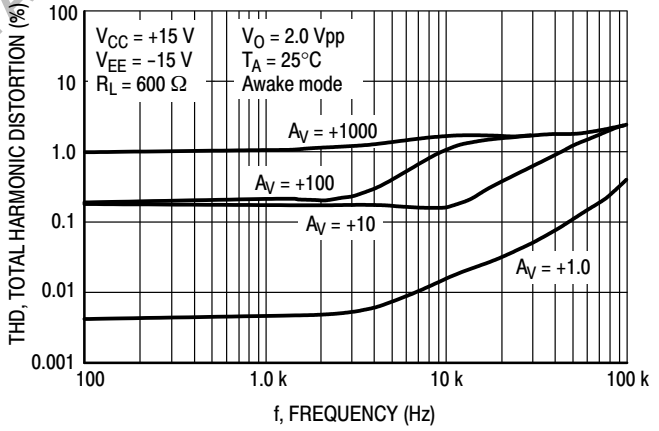


Figure 30. Total Harmonic Distortion versus Frequency

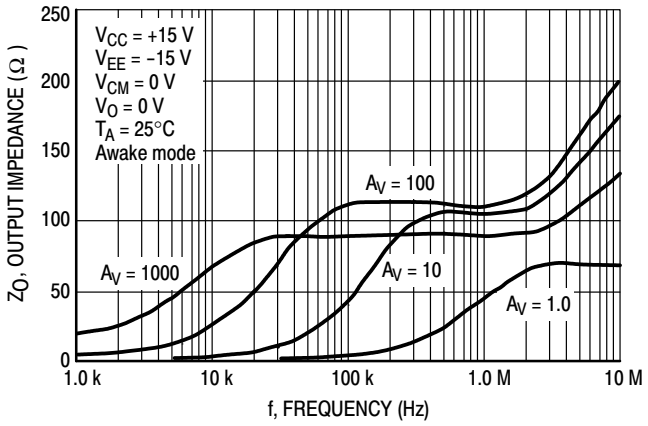


Figure 31. Awake Mode Output Impedance versus Frequency

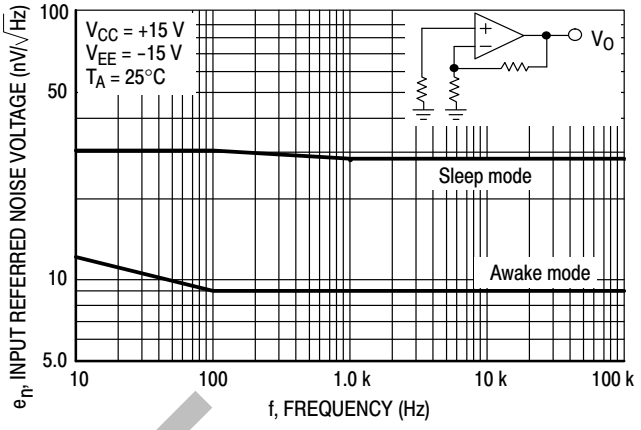


Figure 32. Input Referred Noise Voltage versus Frequency

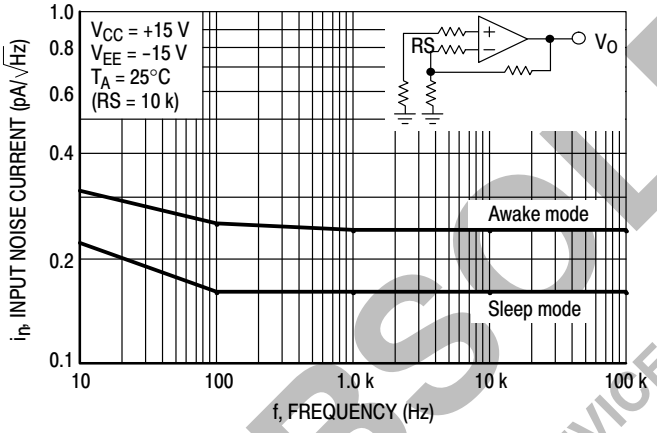


Figure 33. Current Noise versus Frequency

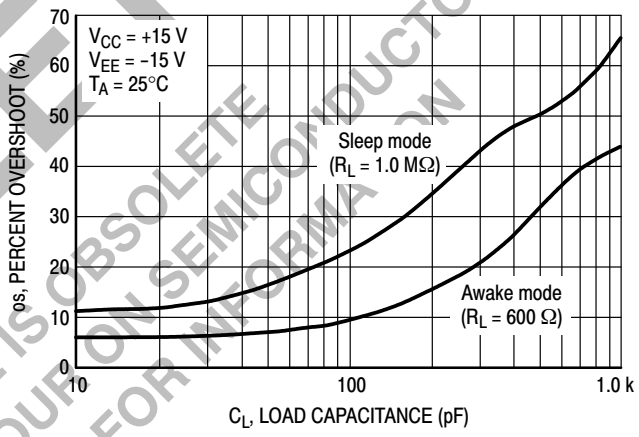


Figure 34. Percent Overshoot versus Load Capacitance

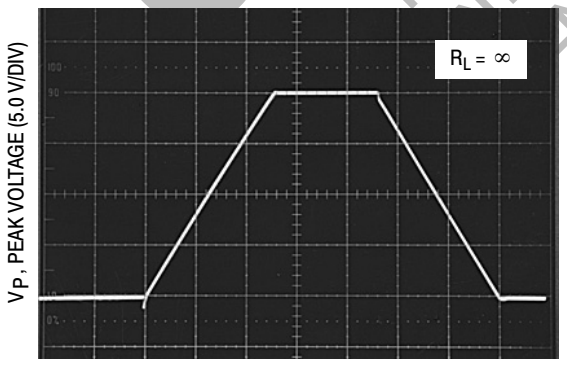


Figure 35. Sleep Mode Large Signal Transient Response

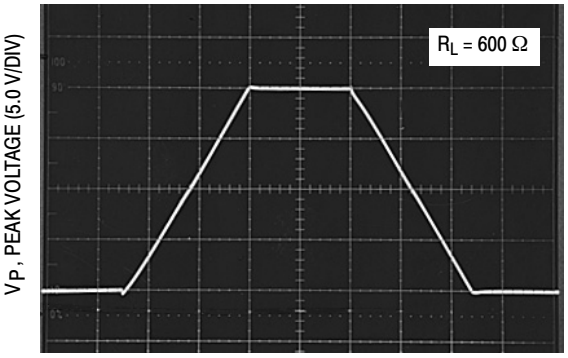


Figure 36. Awake Mode Large Signal Transient Response

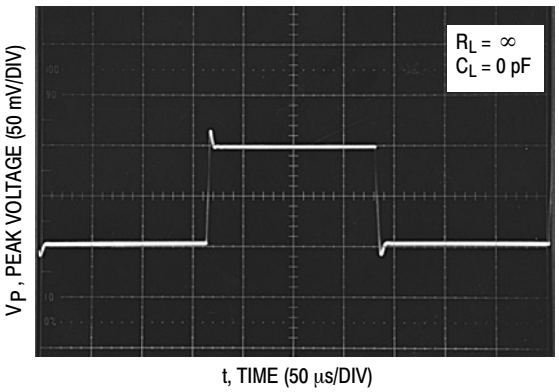


Figure 37. Sleep Mode Small Signal Transient Response

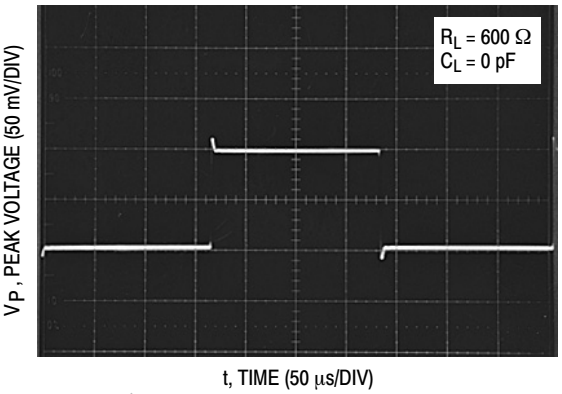


Figure 38. Awake Mode Small Signal Transient Response

CIRCUIT INFORMATION

The MC33102 was designed primarily for applications where high performance (which requires higher current drain) is required only part of the time. The two−state feature of this op amp enables it to conserve power during idle times, yet be powered up and ready for an input signal. Possible applications include laptop computers, automotive, cordless phones, baby monitors, and battery operated test equipment. Although most applications will require low power consumption, this device can be used in any application where better efficiency and higher performance is needed.

The sleep mode amplifier has two states; a sleep mode and an awake mode. In the sleep mode state, the amplifier is active and functions as a typical micropower op amp. When a signal is applied to the amplifier causing it to source or sink sufficient current (see Figure 13), the amplifier will automatically switch to the awake mode. See Figures 20 and 21 for transition times with 600 Ω and 10 kΩ loads.

The awake mode uses higher drain current to provide a high slew rate, gain bandwidth, and output current capability. In the awake mode, this amplifier can drive 27 Vpp into a 600 Ω load with $V_S = \pm 15$ V.

An internal delay circuit is used to prevent the amplifier from returning to the sleep mode at every zero crossing. This delay circuit also eliminates the crossover distortion commonly found in micropower amplifiers. This amplifier can process frequencies as low as 1.0 Hz without the amplifier returning to sleep mode, depending on the load.

The first stage PNP differential amplifier provides low noise performance in both the sleep and awake modes, and an all NPN output stage provides symmetrical source and sink AC frequency response.

APPLICATIONS INFORMATION

The MC33102 will begin to function at power supply voltages as low as $V_S = \pm 1.0$ V at room temperature. (At this voltage, the output voltage swing will be limited to a few hundred millivolts.) The input voltages must range between V_{CC} and V_{EE} supply voltages as shown in the maximum rating table. Specifically, **allowing the input to go more negative than 0.3 V below V_{EE} may cause product damage.** Also, exceeding the input common mode voltage range on either input may cause phase reversal, even if the inputs are between V_{CC} and V_{EE}.

When power is initially applied, the part may start to operate in the awake mode. This is because of the currents generated due to charging of internal capacitors. When this occurs and the sleep mode state is desired, the user will have to wait approximately 1.5 seconds before the device will switch back to the sleep mode. To prevent this from occurring, ramp the power supplies from 1.0 V to full supply. Notice that the device is more prone to switch into the awake mode when V_{EE} is adjusted than with a similar change in V_{CC}.

The amplifier is designed to switch from sleep mode to awake mode whenever the output current exceeds a preset current threshold (I_{TH}) of approximately 160 μA. As a result, the output switching threshold voltage (V_{ST}) is controlled by the output loading resistance (R_L). This loading can be a load resistor, feedback resistors, or both. Then:

$$V_{ST} = (160\ \mu A) \times R_L$$

Large valued load resistors require a large output voltage to switch, but reduce unwanted transitions to the awake mode. For instance, in cases where the amplifier is connected with a large closed loop gain (A_{CL}), the input offset voltage (V_{IO}) is multiplied by the gain at the output and could produce an output voltage exceeding V_{ST} with no input signal applied.

Small values of R_L allow rapid transition to the awake mode because most of the transition time is consumed slewing in the sleep mode until V_{ST} is reached (see Figures 20, 21). The output switching threshold voltage V_{ST} is higher for larger values of R_L, requiring the amplifier to

slew longer in the slower sleep mode state before switching to the awake mode.

The transition time (t_{tr1}) required to switch from sleep to awake mode is:

$$t_{tr1} = t_D = I_{TH}(R_L/SR_{sleepmode})$$

Where:

t_D = Amplifier delay (< 1.0 μs)

I_{TH} = Output threshold current for more transition (160 μA)

R_L = Load resistance

$Sr_{sleep\ mode}$ = Sleep mode slew rate (0.16 V/μs)

Although typically 160 μA, I_{TH} varies with supply voltage and temperature. In general, any current loading on the output which causes a current greater than I_{TH} to flow will switch the amplifier into the awake mode. This includes transition currents such as those generated by charging load capacitances. In fact, the maximum capacitance that can be driven while attempting to remain in the sleep mode is approximately 1000 pF.

$$C_{L(max)} = I_{TH}/Sr_{sleep\ mode}$$
$$= 160\ \mu A/(0.16\ V/\mu s)$$
$$= 1000\ pF$$

Any electrical noise seen at the output of the MC33102 may also cause the device to transition to the awake mode. To minimize this problem, a resistor may be added in series with the output of the device (inserted as close to the device as possible) to isolate the op amp from both parasitic and load capacitance.

The awake mode to sleep mode transition time is controlled by an internal delay circuit, which is necessary to prevent the amplifier from going to sleep during every zero crossing. This time is a function of supply voltage and temperature as shown in Figure 22.

Gain bandwidth product (GBW) in both modes is an important system design consideration when using a sleep mode amplifier. The amplifier has been designed to obtain the maximum GBW in both modes. "Smooth" AC transitions between modes with no noticeable change in the amplitude of the output voltage waveform will occur as long as the closed loop gains (A_{CL}) in both modes are substantially equal at the frequency of operation. For smooth AC transitions:

$$(A_{CLsleep\ mode})\ (BW) < GBW_{sleep\ mode}$$

Where:

$A_{CLsleep\ mode}$ = Closed loop gain in the sleep mode

BW = The required system bandwidth or operating frequency

TESTING INFORMATION

To determine if the MC33102 is in the awake mode or the sleep mode, the power supply currents (I_D+ and I_D−) must be measured. When the magnitude of **either** power supply current exceeds 400 μA, the device is in the awake mode. When the magnitudes of both supply currents are less than 400 μA, the device is in the sleep mode. Since the total supply current is typically ten times higher in the awake mode than the sleep mode, the two states are easily distinguishable.

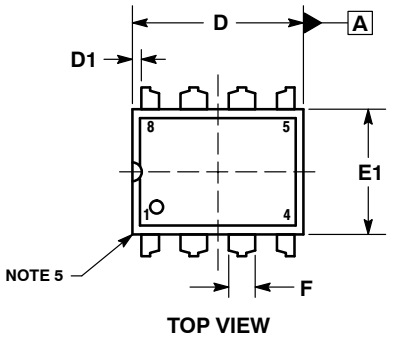
The measured value of I_D+ equals the I_D of both devices (for a dual op amp) plus the output source current of device A and the output source current of device B. Similarly, the measured value of I_D− is equal to the I_D− of both devices plus the output sink current of each device. I_{out} is the sum of the currents caused by both the feedback loop and load resistance. The total I_{out} needs to be subtracted from the measured I_D to obtain the correct I_D of the dual op amp.

An accurate way to measure the awake mode I_{out} current on automatic test equipment is to remove the I_{out} current on both Channel A and B. Then measure the I_D values before the device goes back to the sleep mode state. The transition will take typically 1.5 seconds with ±15 V power supplies.

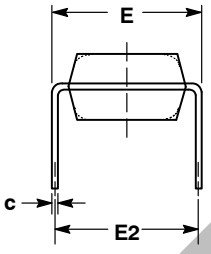
The large signal sleep mode testing in the characterization was accomplished with a 1.0 MΩ load resistor which ensured the device would remain in sleep mode despite large voltage swings.

PACKAGE DIMENSIONS

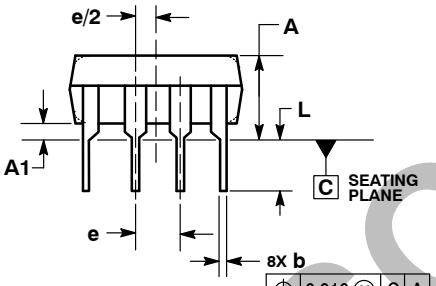
8 LEAD PDIP
CASE 626−05
ISSUE M



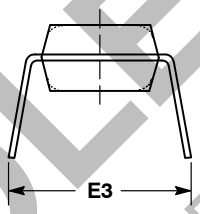
TOP VIEW



END VIEW
NOTE 3



SIDE VIEW

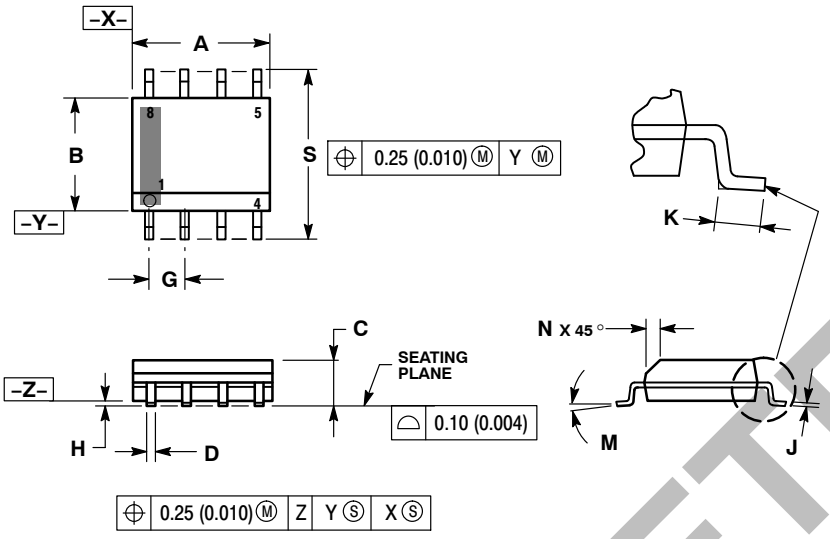


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION E IS MEASURED WITH THE LEADS RESTRAINED PARALLEL AT WIDTH E2.
4. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	----	----	0.210	----	----	5.33
A1	0.015	----	----	0.38	----	----
b	0.014	0.018	0.022	0.35	0.46	0.56
C	0.008	0.010	0.014	0.20	0.25	0.36
D	0.355	0.365	0.400	9.02	9.27	10.02
D1	0.005	----	----	0.13	----	----
E	0.300	0.310	0.325	7.62	7.87	8.26
E1	0.240	0.250	0.280	6.10	6.35	7.11
E2	0.300 BSC			7.62 BSC		
E3	----	----	0.430	----	----	10.92
e	0.100 BSC			2.54 BSC		
L	0.115	0.130	0.150	2.92	3.30	3.81

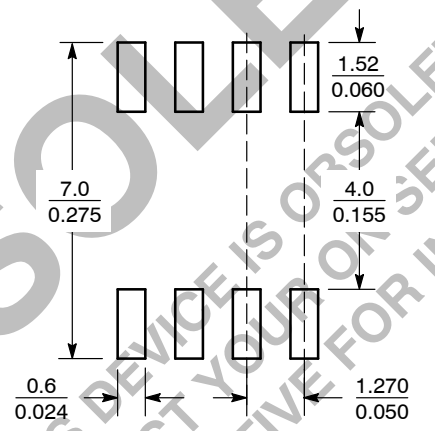
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative