46 dBm (40 W), 2.7 GHz to 3.5 GHz, GaN Power Amplifier

FEATURES

- Frequency range: 2.7 GHz to 3.5 GHz
- P_{OUT}: 46 dBm typical with P_{IN} = 21 dBm at 2.7 GHz to 3.1 GHz
- Power gain: 25 dB typical with P_{IN} = 21 dBm at 2.7 GHz to 3.1 GHz
- Small signal gain: 34.5 dB typical at 2.7 GHz to 3.1 GHz
- PAE: 56% typical with P_{IN} = 21 dBm at 2.7 GHz to 3.1 GHz
- Supply voltage: V_{DD} = 50 V at I_{DQ} = 300 mA with 10% duty cycle
- 32-lead, 5 mm × 5 mm LFCSP_CAV package

APPLICATIONS

- Weather radar
- Marine radar
- Military radar

GENERAL DESCRIPTION

The ADPA1106 is a gallium nitride (GaN), broadband power amplifier that delivers 46 dBm (40 W) with 56% typical power added efficiency (PAE) across a bandwidth of 2.7 GHz to 3.1 GHz. The ADPA1106 has a gain flatness of ±0.15 dB across the 2.7 GHz to 3.1 GHz frequency range.

The ADPA1106 is ideal for pulsed applications such as marine, weather, and military radar.

The ADPA1106 comes in a 32-lead, lead frame chip scale package, premolded cavity (LFCSP_CAV) and is specified for operation from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

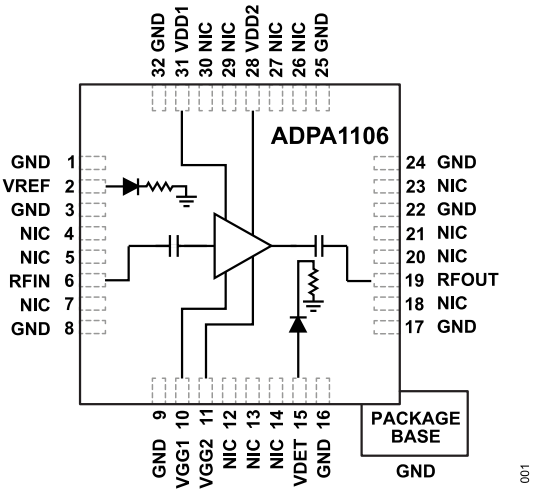

Figure 1.

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REVISION HISTORY

4/2022—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, supply voltage (V_{DD}) = 50 V, I_{DQ} = 300 mA, pulse width = 100 µs, 10% duty cycle, and frequency range = 2.7 GHz to 3.1 GHz, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	2.7		3.1	GHz	
GAIN					
Small Signal Gain (S21)	32	34.5		dB	
Gain Flatness		±0.15		dB	
RETURN LOSS					
Input (S11)		18		dB	
Output (S22)		9		dB	
POWER					
Output Power (P_{OUT})	44	46		dBm	Input power (P_{IN}) = 21 dBm
Power Gain	23	25		dB	P_{IN} = 21 dBm
PAE		56		%	P_{IN} = 21 dBm
TARGET QUIESCENT CURRENT, I_{DQ}		300		mA	Adjust the gate control voltages, V_{GG1} and V_{GG2}, to be between −4 V and 0 V to achieve an I_{DQ} = 300 mA typical value

T_A = 25°C, V_{DD} = 50 V, I_{DQ} = 300 mA, pulse width = 100 µs, 10% duty cycle, and frequency range = 3.1 GHz to 3.5 GHz, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	3.1		3.5	GHz	
GAIN					
Small Signal Gain	33.5	36		dB	
Gain Flatness		±0.55		dB	
RETURN LOSS					
S11		19		dB	
S22		9		dB	
POWER					
P_{OUT}	43.5	45.5		dBm	P_{IN} = 21 dBm
Power Gain	22.5	24.5		dB	P_{IN} = 21 dBm
PAE		55		%	P_{IN} = 21 dBm
I_{DQ}		300		mA	Adjust V_{GG1} and V_{GG2} to be between −4 V and 0 V to achieve an I_{DQ} = 300 mA typical value

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Bias Voltage	
Drain (V_{DD1} and V_{DD2})	55 V dc
Gate (V_{GG1} and V_{GG2})	−5 V to 0 V dc
RF Input Power (RFIN)	30 dBm
Maximum Drain Bias	
Pulse Width	500 µs
Duty Cycle	20%
Drain Bias Pulse Width = 100 µs at 10% Duty Cycle	
Maximum Pulsed Power Dissipation (P_{DISS}), Case Temperature (T_{CASE}) = 85°C, Derate 473 mW/°C Above 85°C	54.5 W
Nominal Pulsed Peak Channel Temperature at 85°C, P_{IN} = 21 dBm, P_{DISS} = 35 W at 3.1 GHz	158.9°C
Drain Bias Pulse Width = 200 µs at 20% Duty Cycle	
Maximum P_{DISS}, T_{CASE} = 85°C, Derate 355 mW/°C Above 85°C	40.8 W
Nominal Pulsed Peak Channel Temperature at 85°C, P_{IN} = 21 dBm, P_{DISS} = 35.3 W at 3.1 GHz	184.5°C
Maximum Channel Temperature	200°C
Storage Temperature Range	−60°C to +125°C
Operating Temperature Range	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to the PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance (°C/W) of the device. θ_{JC} was determined by measuring θ_{JC} under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CG-32-2		
Drain Bias Pulse Width = 100 µs[1]	2.11	°C/W
Drain Bias Pulse Width = 200 µs[2]	2.82	°C/W

[1] At 10% duty cycle.

[2] At 20% duty cycle.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA1106

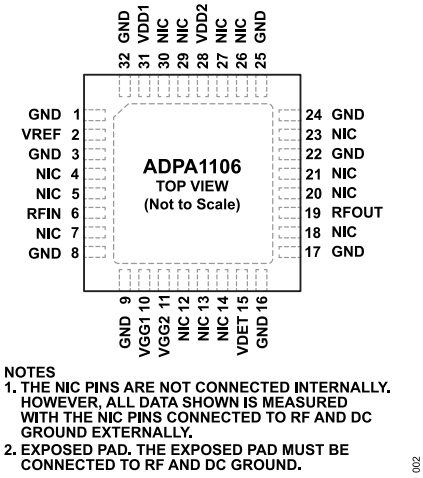
Table 5. ADPA1106, 32-Lead LFCSP_CAV

ESD Model	Withstand Threshold (V)	Class
HBM	500	1B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE NIC PINS ARE NOT CONNECTED INTERNALLY. HOWEVER, ALL DATA SHOWN IS MEASURED WITH THE NIC PINS CONNECTED TO RF AND DC GROUND EXTERNALLY.
2. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF AND DC GROUND.

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 8, 9, 16, 17, 22, 24, 25, 32	GND	Ground. The GND pins must be connected to RF and dc ground. See Figure 6 for the interface schematic.
2	VREF	Reference Diode for Temperature Compensation of VDET RF Output Power Measurements. The VREF voltage (V_{REF}) requires the application of a dc bias voltage through an external series resistor.
4, 5, 7, 12, 13, 14, 18, 20, 21, 23, 26, 27, 29, 30	NIC	Not Internally Connected. The NIC pins are not internally connected. However, all data shown is measured with the NIC pins connected to RF and dc ground externally.
6	RFIN	RF Input. The RFIN pin is ac-coupled and is matched to 50 Ω. See Figure 3 for the interface schematic.
10	VGG1	Gate Control, First Stage Gate Bias. See Figure 3 for the interface schematic.
11	VGG2	Gate Control, Second Stage Gate Bias. See Figure 4 for the interface schematic.
15	VDET	Detector Diode to Measure RF P_{OUT}. P_{OUT} detection via the VDET voltage (V_{DET}) requires the application of a dc bias voltage through an external series resistor. The VDET pin is used in combination with the VREF pin, and the difference in voltage (V_{REF} − V_{DET}) is a temperature compensated dc voltage that is proportional to the RF P_{OUT}.
19	RFOUT	RF Output. The RFOUT pin is ac-coupled and is matched to 50 Ω. See Figure 4 for the interface schematic.
28	VDD2	Amplifier Power Supply Voltage, Second Stage Drain Bias. See Figure 4 for the interface schematic.
31	VDD1	Amplifier Power Supply Voltage, First Stage Drain Bias. See Figure 3 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS

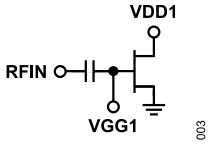


Figure 3. RFIN, VGG1, and VDD1 Interface Schematic

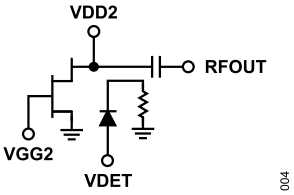


Figure 4. RFOUT, VGG2, VDD2, and VDET Interface Schematic

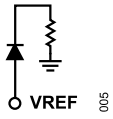


Figure 5. VREF Interface Schematic

Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

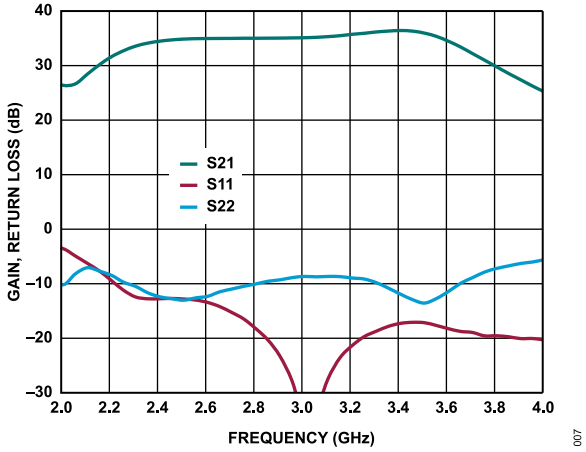


Figure 7. Small Signal Gain and Return Loss vs. Frequency

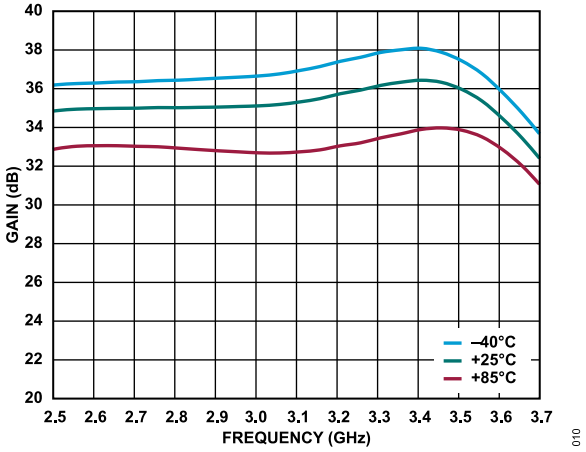


Figure 10. Small Signal Gain vs. Frequency at Various Temperatures

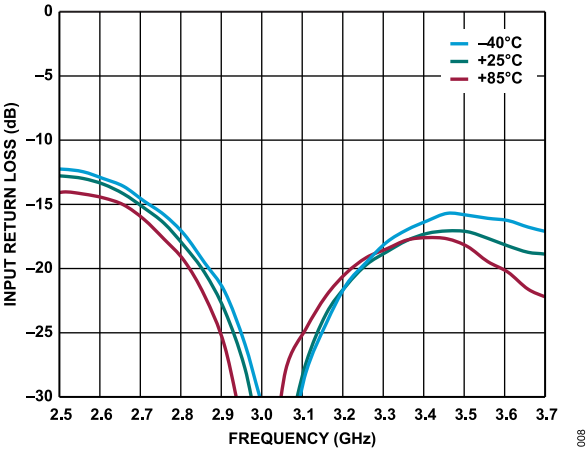


Figure 8. Input Return Loss vs. Frequency at Various Temperatures

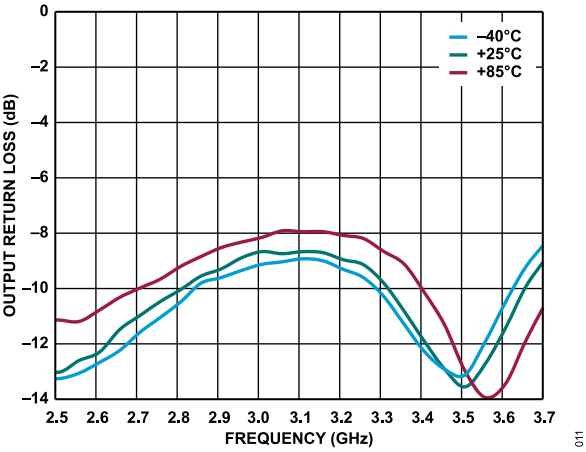


Figure 11. Output Return Loss vs. Frequency at Various Temperatures

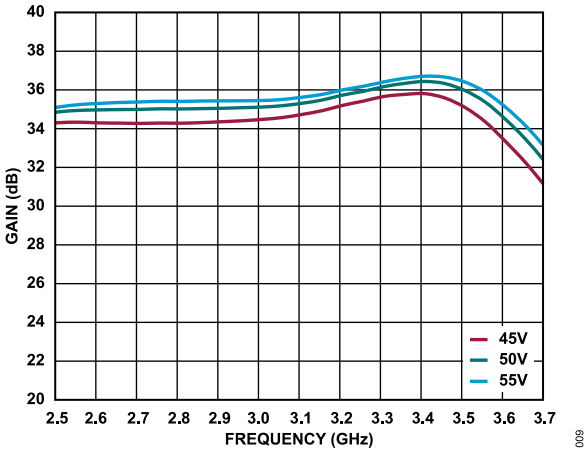


Figure 9. Small Signal Gain vs. Frequency at Various Supply Voltages, I_{DQ} = 300 mA

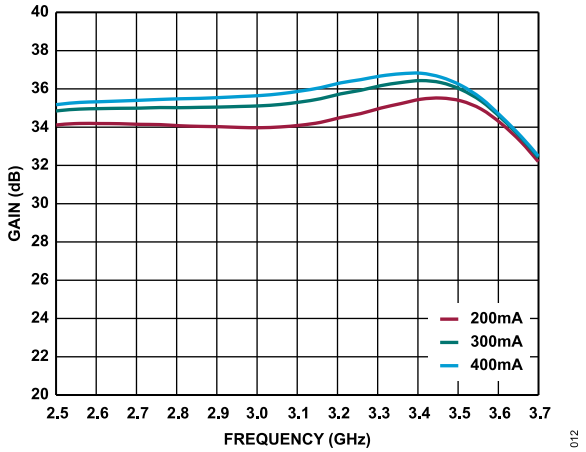


Figure 12. Small Signal Gain vs. Frequency at Various I_{DQ}, V_{DD1} and V_{DD2} = 50 V

TYPICAL PERFORMANCE CHARACTERISTICS

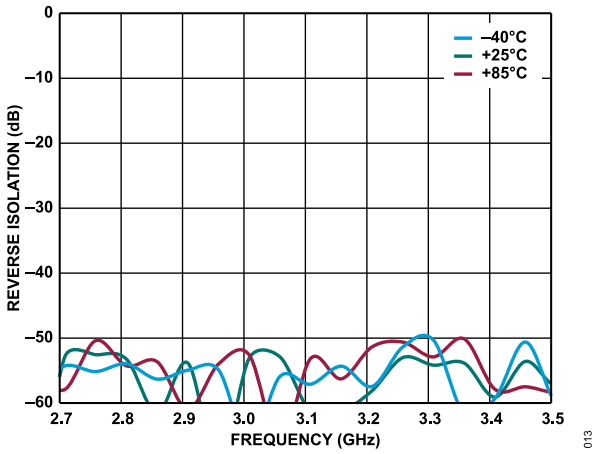


Figure 13. Reverse Isolation vs. Frequency at Various Temperatures

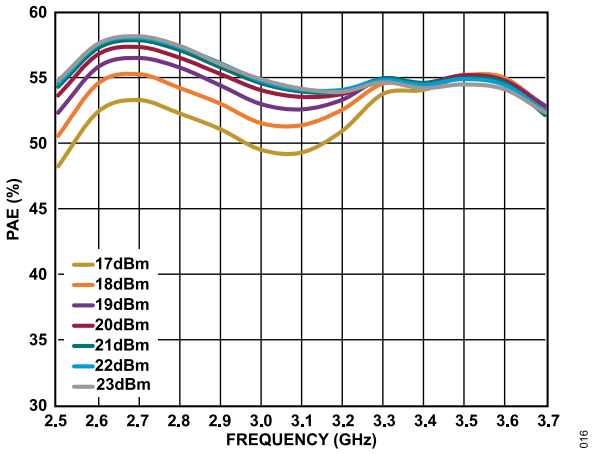


Figure 16. PAE vs. Frequency at Various P_{IN} Levels

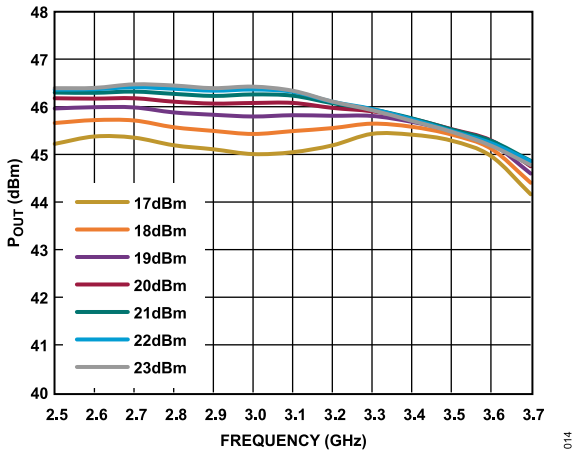


Figure 14. P_{OUT} vs. Frequency at Various P_{IN} Levels

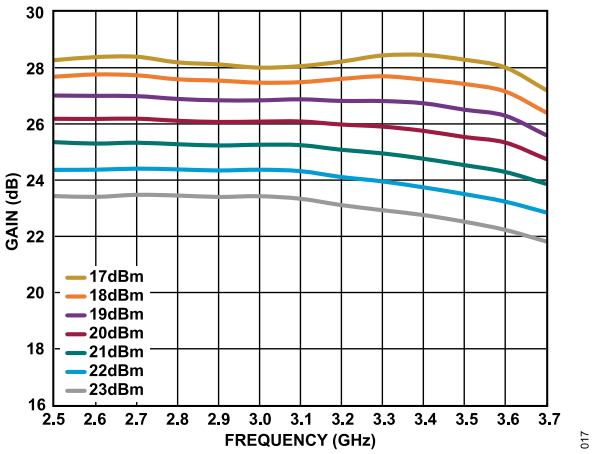


Figure 17. Gain vs. Frequency at Various P_{IN} Levels

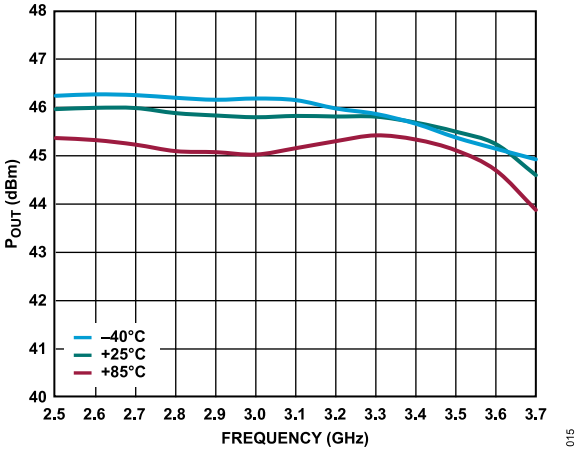


Figure 15. P_{OUT} vs. Frequency at Various Temperatures, P_{IN} = 19 dBm

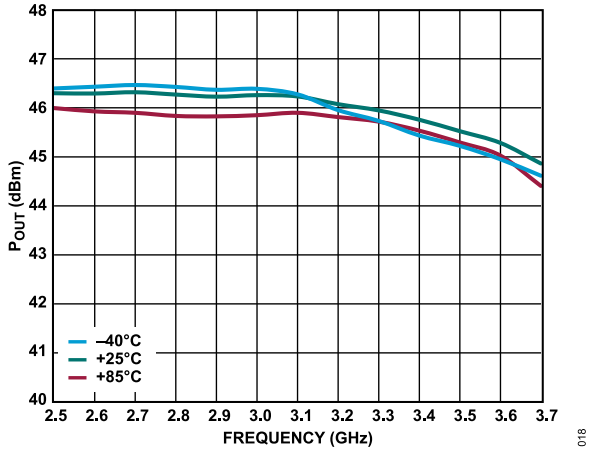


Figure 18. P_{OUT} vs. Frequency at Various Temperatures, P_{IN} = 21 dBm

TYPICAL PERFORMANCE CHARACTERISTICS

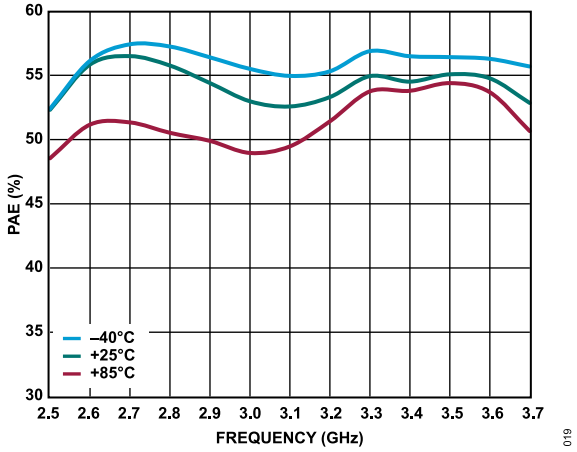


Figure 19. PAE vs. Frequency at Various Temperatures, P_{IN} = 19 dBm

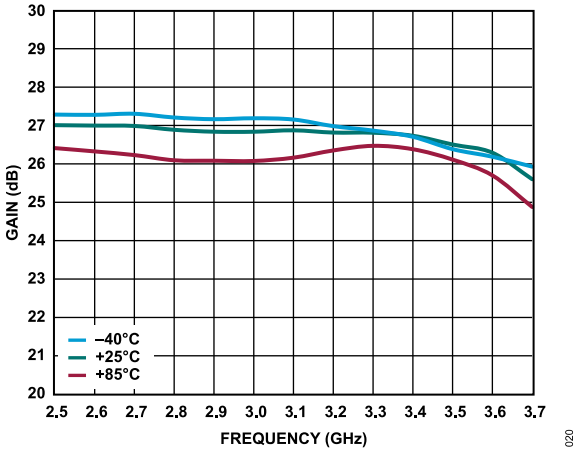


Figure 20. Gain vs. Frequency at Various Temperatures, P_{IN} = 19 dBm

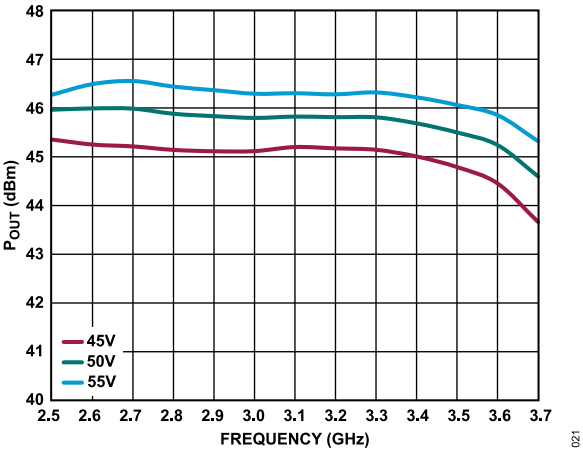


Figure 21. P_{OUT} vs. Frequency at Various Supply Voltages, P_{IN} = 19 dBm, I_{DQ} = 300 mA

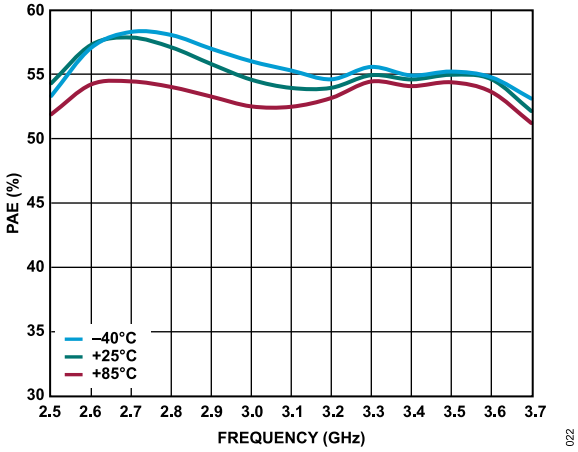


Figure 22. PAE vs. Frequency at Various Temperatures, P_{IN} = 21 dBm

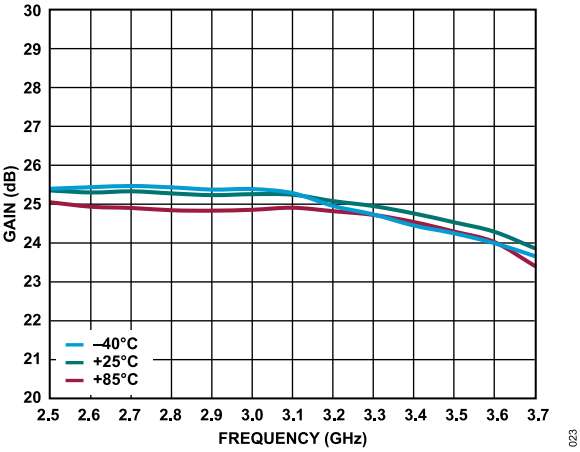


Figure 23. Gain vs. Frequency at Various Temperatures, P_{IN} = 21 dBm

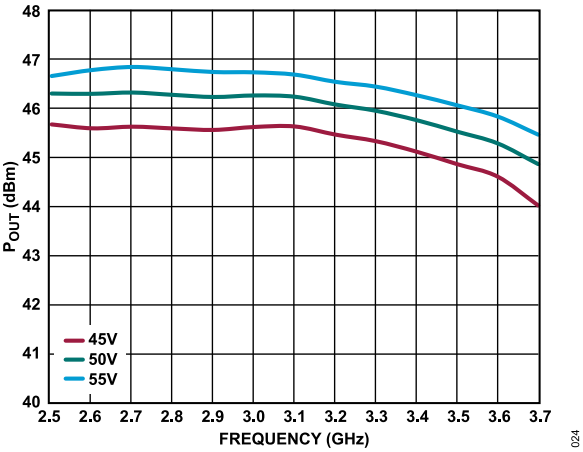


Figure 24. P_{OUT} vs. Frequency at Various Supply Voltages, P_{IN} = 21 dBm, I_{DQ} = 300 mA

TYPICAL PERFORMANCE CHARACTERISTICS

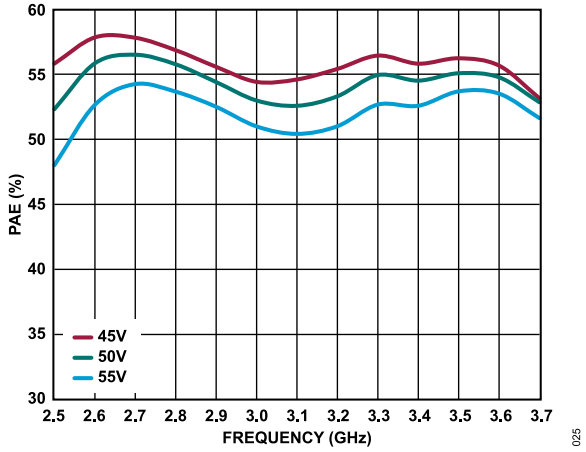


Figure 25. PAE vs. Frequency at Various Supply Voltages, P_{IN} = 19 dBm, I_{DQ} = 300 mA

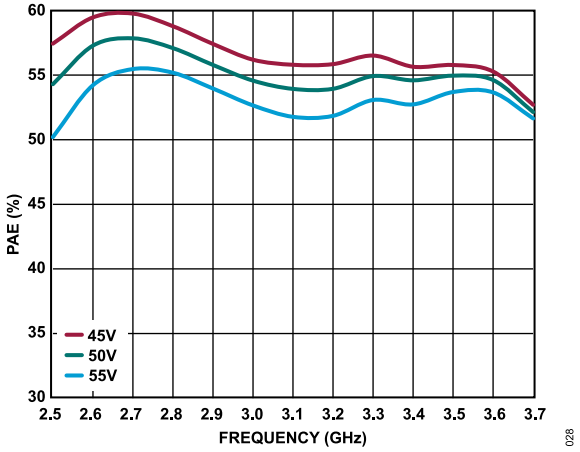


Figure 28. PAE vs. Frequency at Various Supply Voltages, P_{IN} = 21 dBm, I_{DQ} = 300 mA

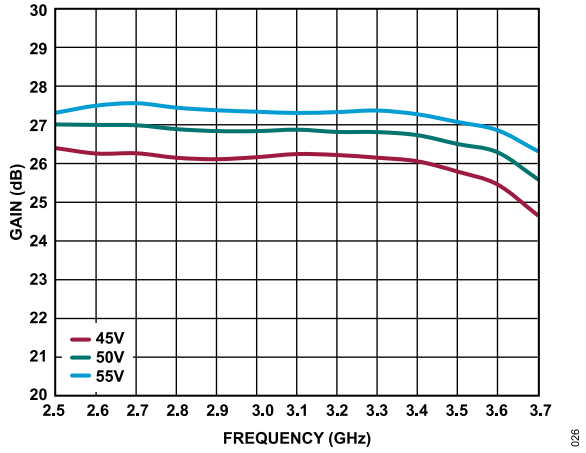


Figure 26. Gain vs. Frequency at Various Supply Voltages, P_{IN} = 19 dBm, I_{DQ} = 300 mA

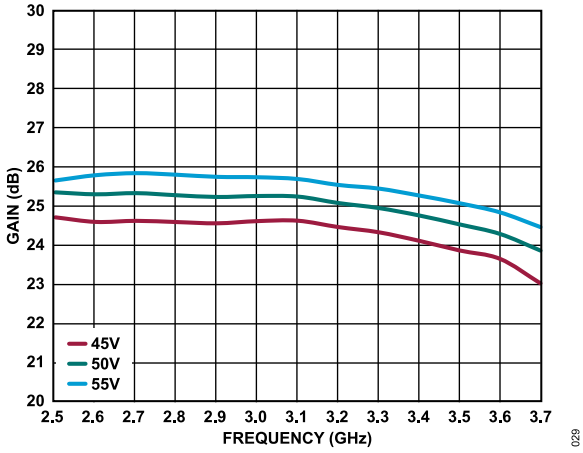


Figure 29. Gain vs. Frequency at Various Supply Voltages, P_{IN} = 21 dBm, I_{DQ} = 300 mA

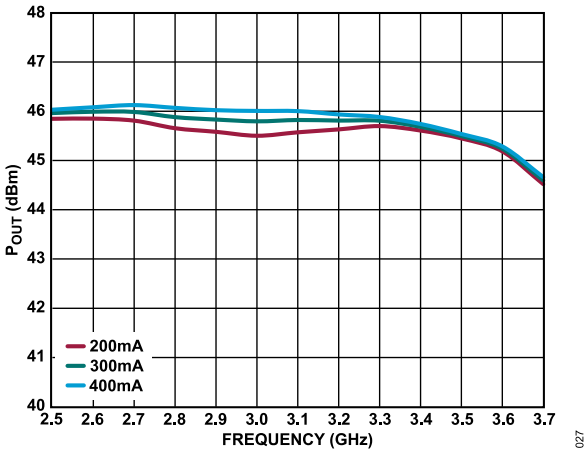


Figure 27. P_{OUT} vs. Frequency at Various I_{DQ} Supply Currents, P_{IN} = 19 dBm, V_{DD1} and V_{DD2} = 50 V

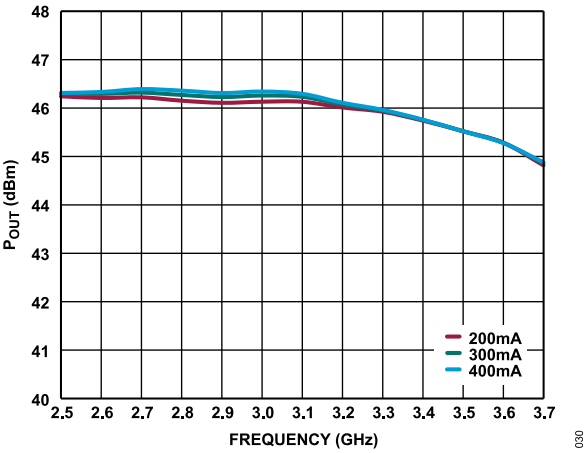


Figure 30. P_{OUT} vs. Frequency at Various I_{DQ} Supply Currents, P_{IN} = 21 dBm, V_{DD1} and V_{DD2} = 50 V

TYPICAL PERFORMANCE CHARACTERISTICS

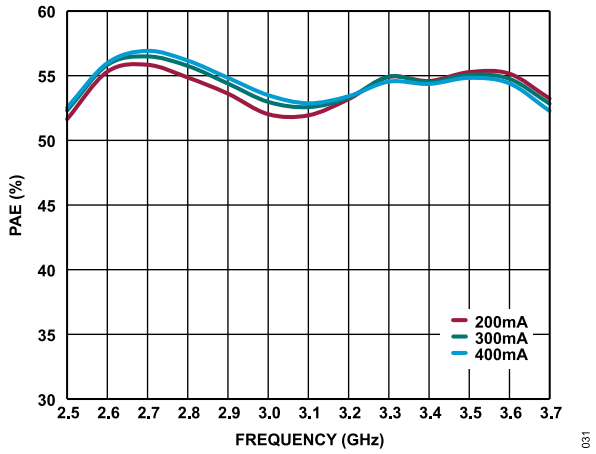


Figure 31. PAE vs. Frequency at Various I_{DQ} Supply Currents, P_{IN} = 19 dBm, V_{DD1} and V_{DD2} = 50 V

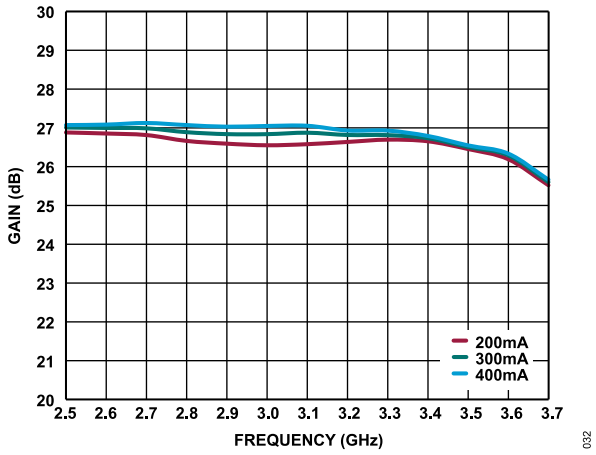


Figure 32. Gain vs. Frequency at Various I_{DQ} Supply Currents, P_{IN} = 19 dBm, V_{DD1} and V_{DD2} = 50 V

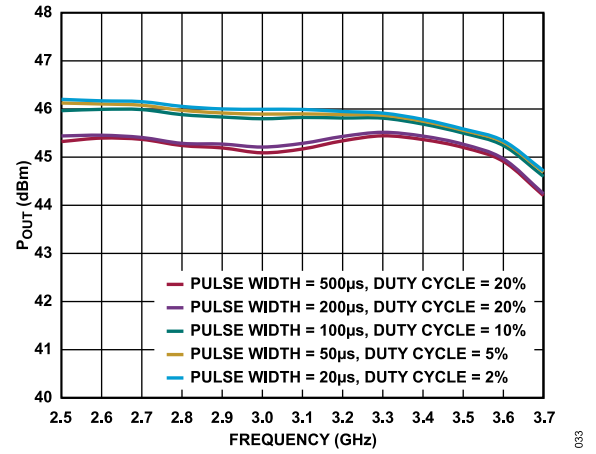


Figure 33. P_{OUT} vs. Frequency at Various Pulse Widths and Duty Cycles, P_{IN} = 21 dBm

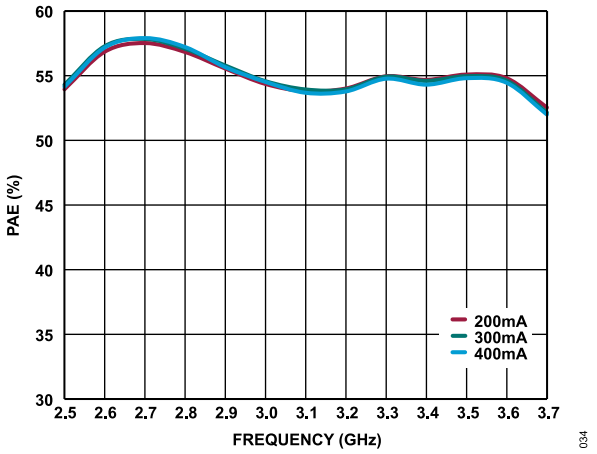


Figure 34. PAE vs. Frequency at Various I_{DQ} Supply Currents, P_{IN} = 21 dBm, V_{DD1} and V_{DD2} = 50 V

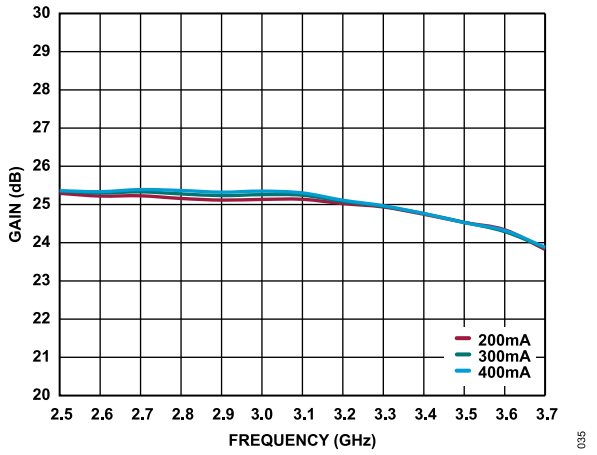


Figure 35. Gain vs. Frequency at Various I_{DQ} Currents, P_{IN} = 21 dBm, V_{DD1} and V_{DD2} = 50 V

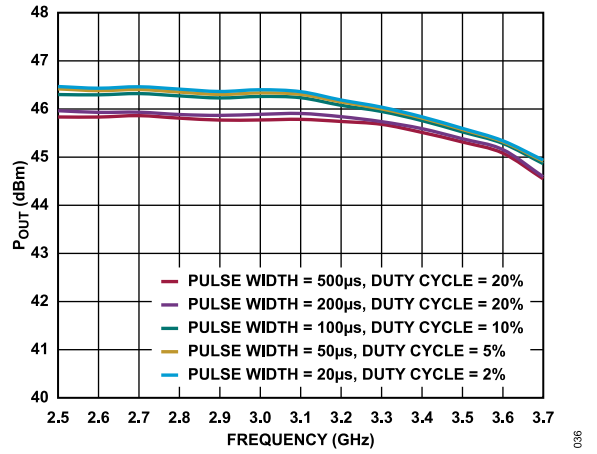


Figure 36. P_{OUT} vs. Frequency at Various Pulse Widths and Duty Cycles, P_{IN} = 21 dBm

TYPICAL PERFORMANCE CHARACTERISTICS

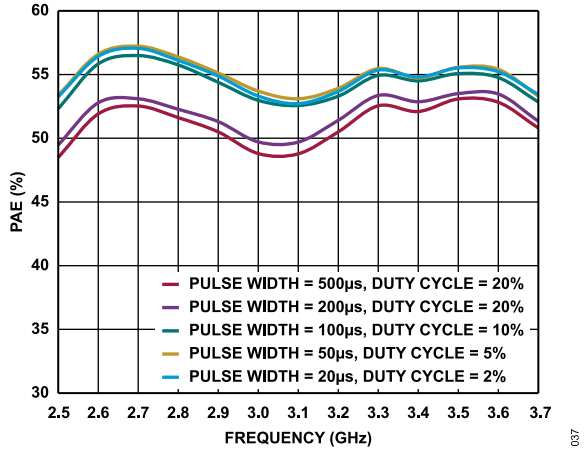


Figure 37. PAE vs. Frequency at Various Pulse Widths and Duty Cycles, P_{IN} = 19 dBm

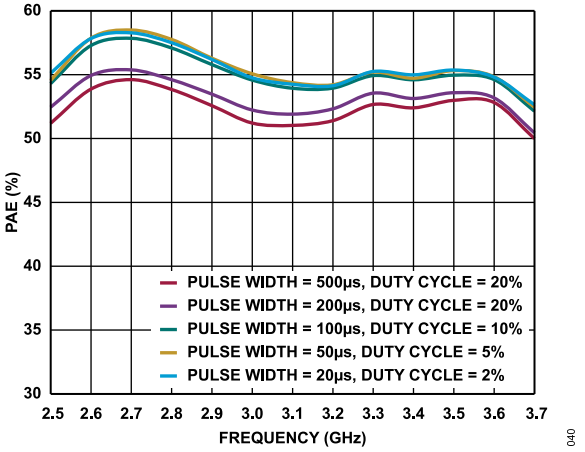


Figure 40. PAE vs. Frequency at Various Pulse Widths and Duty Cycles, P_{IN} = 21 dBm

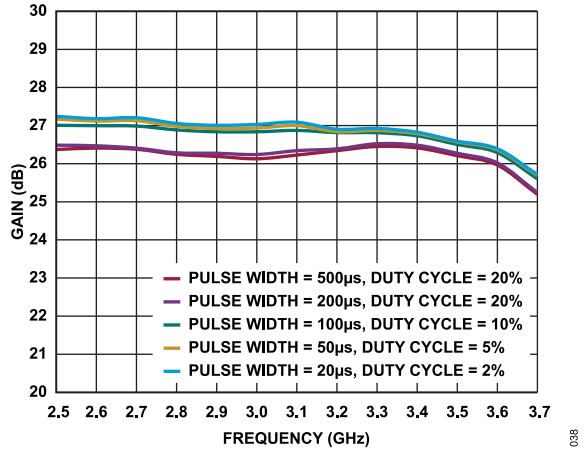


Figure 38. Gain vs. Frequency at Various Pulse Widths and Duty Cycles, P_{IN} = 19 dBm

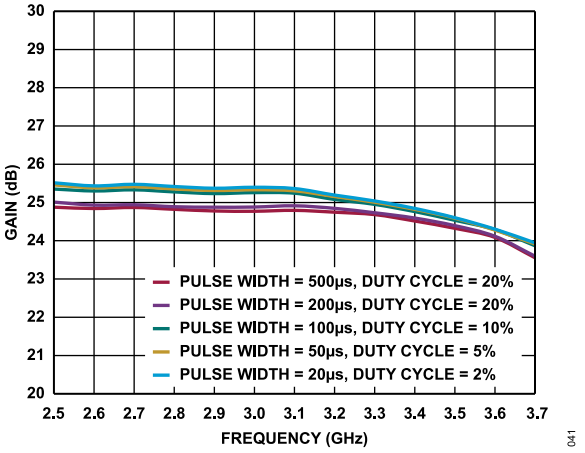


Figure 41. Gain vs. Frequency at Various Pulse Widths and Duty Cycles, P_{IN} = 21 dBm

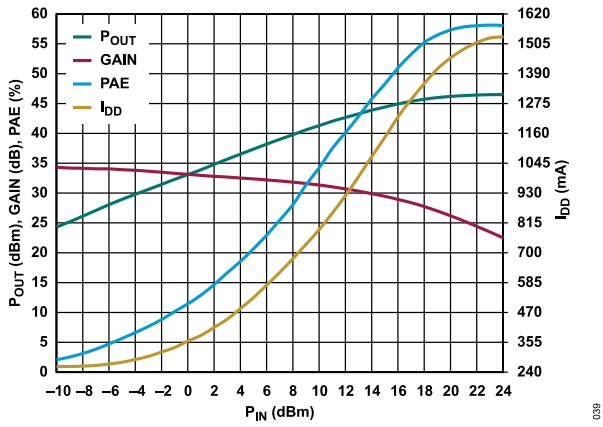


Figure 39. P_{OUT}, Gain, PAE, and Supply Current (I_{DD}) vs. P_{IN} at 2.7 GHz

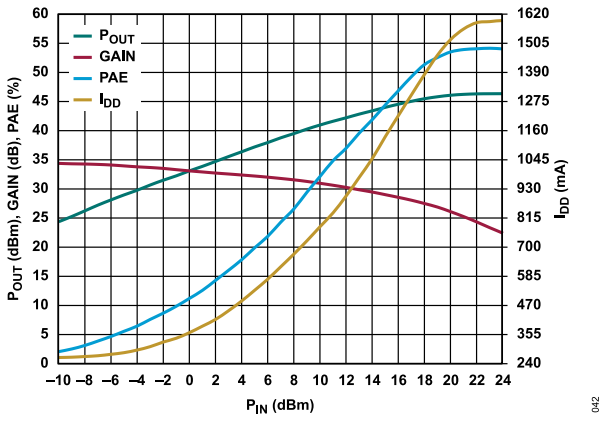


Figure 42. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 3.1 GHz

TYPICAL PERFORMANCE CHARACTERISTICS

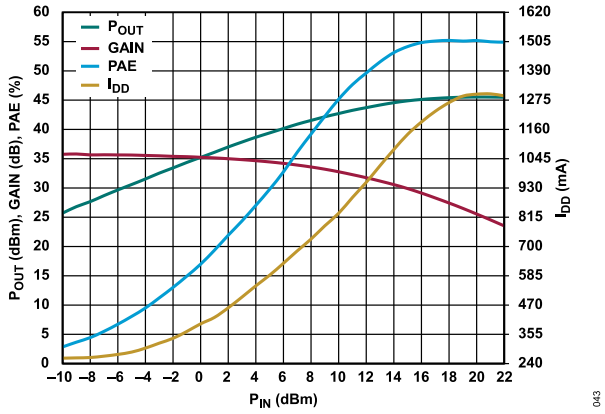


Figure 43. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 3.5 GHz

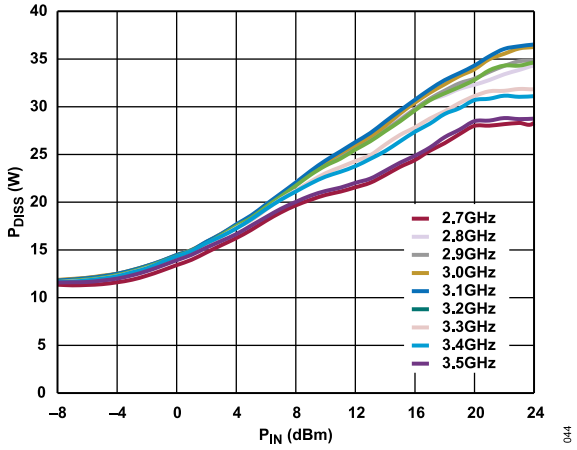


Figure 44. P_{DISS} vs. P_{IN} for Various Frequencies, Drain Bias Pulse Width = 200 µs at 20% Duty Cycle, T_{CASE} = 85°C

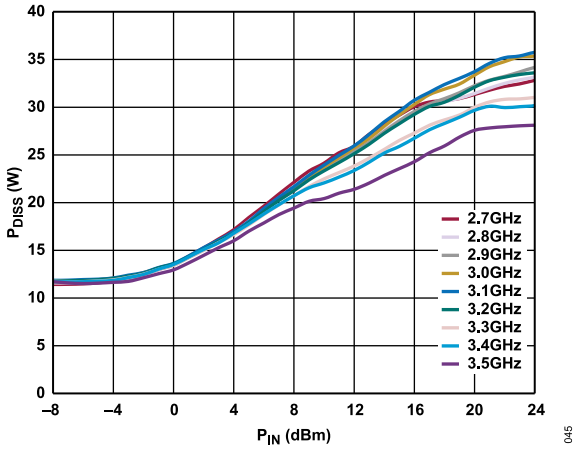


Figure 45. P_{DISS} vs. P_{IN} for Various Frequencies, Drain Bias Pulse Width = 20 µs at 2% Duty Cycle, T_{CASE} = 85°C

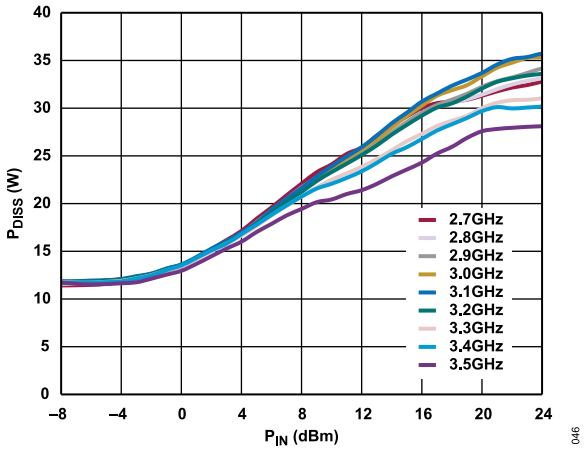


Figure 46. P_{DISS} vs. P_{IN} for Various Frequencies, Drain Bias Pulse Width = 100 µs at 10% Duty Cycle, T_{CASE} = 85°C

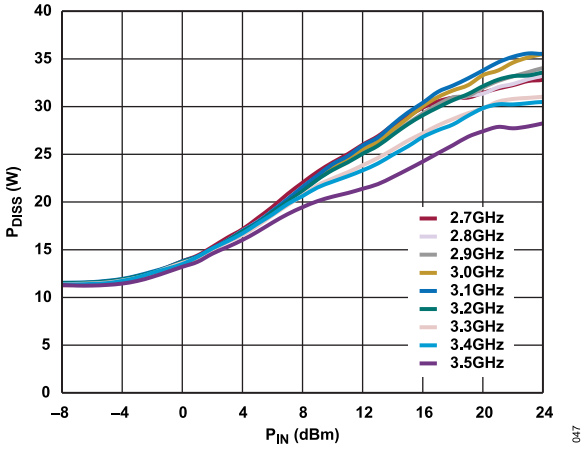


Figure 47. P_{DISS} vs. P_{IN} for Various Frequencies, Drain Bias Pulse Width = 50 µs at 5% Duty Cycle, T_{CASE} = 85°C

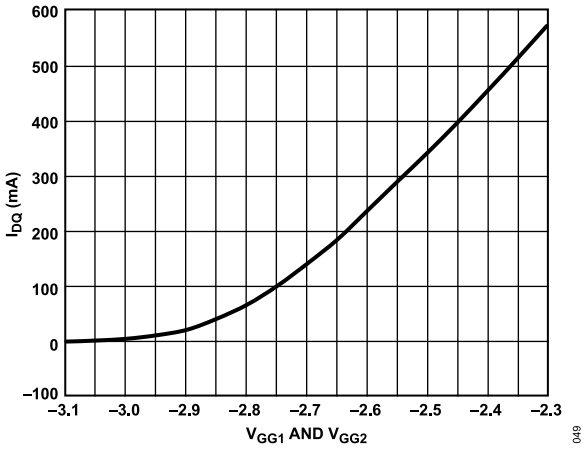


Figure 48. I_{DQ} vs. V_{GG1} and V_{GG2}, V_{DD1} and V_{DD2} = 50 V, Representative of a Typical Device

TYPICAL PERFORMANCE CHARACTERISTICS

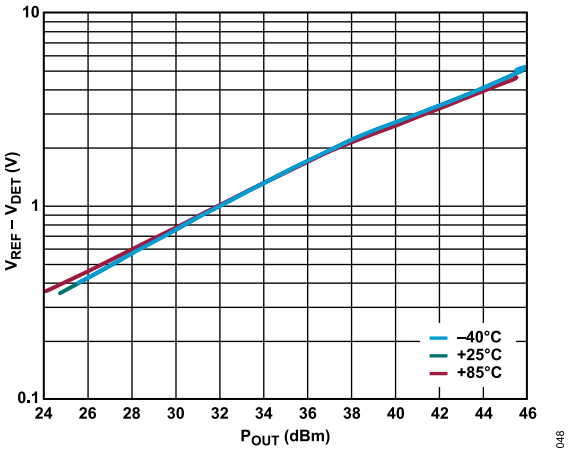


Figure 49. Detector Voltage (V_{REF} – V_{DET}) vs. P_{OUT} for Various Temperatures at 3.1 GHz

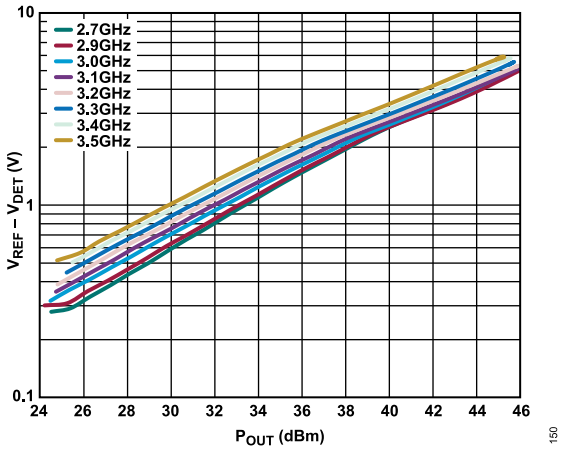


Figure 50. V_{REF} – V_{DET} vs. P_{OUT} for Various Frequencies

THEORY OF OPERATION

The ADPA1106 is a GaN power amplifier that delivers 46 dBm (40 W) of pulsed power. The device consists of two cascaded gain stages. A simplified basic block diagram is shown in Figure 51.

The recommended dc bias conditions put the device into deep Class AB operation, allowing an RF P_{IN} of 21 dBm to produce a typical pulsed P_{OUT} and PAE of 46 dBm and 56%, respectively, across the 2.7 GHz to 3.5 GHz frequency range. The bias voltage applied to the VDD1 and VDD2 pins bias the drains of the first and second gain stages, respectively (the VDD1 and VDD2 must be tied together).

The dc voltages applied to the VGG1 and VGG2 pins bias the gates of the first and second gain stages, respectively, allowing control of the drain currents for each stage (the VGG1 and VGG2 pins must be tied together).

The ADPA1106 has single-ended RFIN and RFOUT ports that are dc blocked. The impedance of these ports is nominally 50 Ω over the 2.7 GHz to 3.5 GHz operating frequency range. Consequently, the ADPA1106 can be directly inserted into a 50 Ω system without the need for external impedance matching components or ac coupling capacitors.

A portion of the RF output signal (RFOUT) is directionally coupled to a diode to detect the RF P_{OUT}. When the diode is dc biased, it rectifies the RF power and makes it available as a dc voltage at VDET. To allow temperature compensation of VDET, the reference dc voltage detected through an identical diode that is not coupled to the RF power is available on the VREF pin. The difference of V_{REF} − V_{DET} provides a temperature compensated detector voltage that is proportional to the RF P_{OUT}.

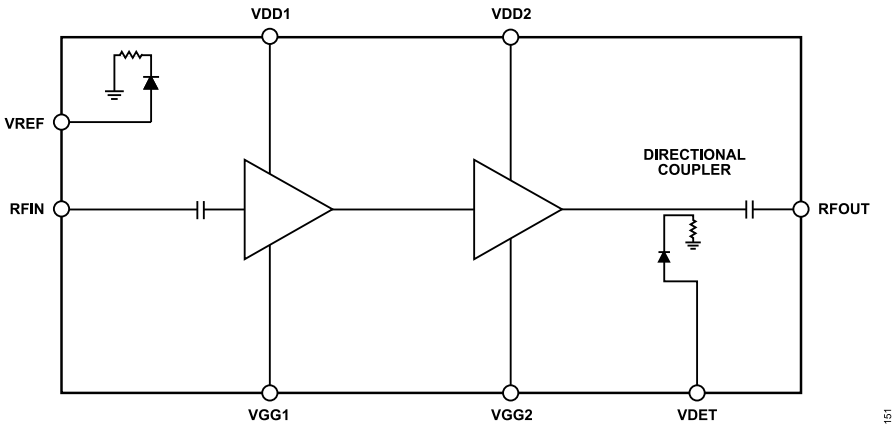


Figure 51. Basic Block Diagram

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The basic connections for operating the ADPA1106 are shown in Figure 52. Apply a power supply voltage between 45 V and 55 V (nominally 50 V) to the VDD1 and VDD2 pins (Pin 31 and Pin 28, respectively). Decouple each pin with the capacitor values shown in Figure 52. Place 3.9 Ω resistors in series with the two 390 pF power supply decoupling capacitors connected to VDD2 and VDD1. In addition, place a 3.9 Ω resistor in series with a 1000 pF capacitor connected to VDD1. Tie together the two gate voltage pins, VGG1 and VGG2, and drive these pins as shown in Figure 52. Pin 4, Pin 5, Pin 7, Pin 12, Pin 13, Pin 18, Pin 22, Pin 23, Pin 26, Pin 27, Pin 29, and Pin 30 are designated as not internally connected (NIC) pins. Although these pins are not internally connected, the NIC pins were all connected to ground during the characterization of the device.

The decoupling capacitors on the VDD1, VDD2, VGG1, and VGG2 lines represent the configuration that was used to characterize the ADPA1106. It is possible to reduce the number of capacitors on the VGG1 and VGG2 lines. General guidance is to first remove or combine the largest value capacitors that are farthest from the device. All of the capacitors and resistors connected to the VDD1 and VDD2 pins in Figure 52 must be used.

External bias is provided to the on-chip RF detection circuit via two 100 kΩ resistors that are pulled up to 5 V, which results in a current draw of approximately 100 µA. An operational amplifier configured as a differential amplifier can be used to subtract VDET from VREF to yield a temperature compensated voltage that is proportional to the RF P_{OUT} (see Figure 53).

Because the ADPA1106 cannot support continuous operation, the device must be operated in pulsed mode by pulsing either the gate voltage or the drain voltage.

Apply a voltage between 0 V and −4 V to V_{GG1} and V_{GG2} and then adjust the voltage until the desired I_{DQ} has been achieved.

In gate pulsed mode, V_{DD} is held at a fixed level (nominally +50 V) while the gate voltage is pulsed between −4 V (off) and approximately −2.3 V (on). The exact on level can be adjusted to achieve the desired I_{DQ}.

In drain pulsed mode, the V_{DD} voltage is pulsed on and off while the gate voltage is held at a fixed negative level between 0 V and −4 V. Because high currents and voltages are being switched on and off, a metal-oxide semiconductor field effect transistor (MOSFET) and a MOSFET switch driver are required in the circuit. Large capacitors are also required, which act as local reservoirs of charge and help provide the drain current required by the ADPA1106 while maintaining a steady drain voltage during the on time of the pulse.

The ADPA1106-EVALZ evaluation board package includes a plugin pulser board that contains the required circuitry to implement drain pulsed mode. See the ADPA1106-EVALZ for more information.

APPLICATIONS INFORMATION

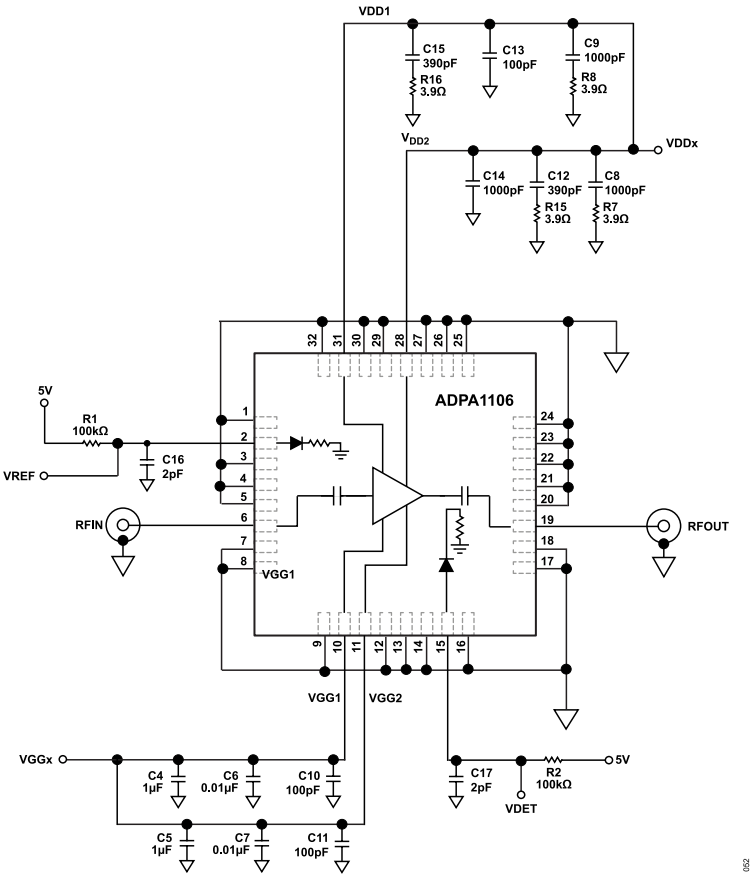


Figure 52. Basic Connections

APPLICATIONS INFORMATION

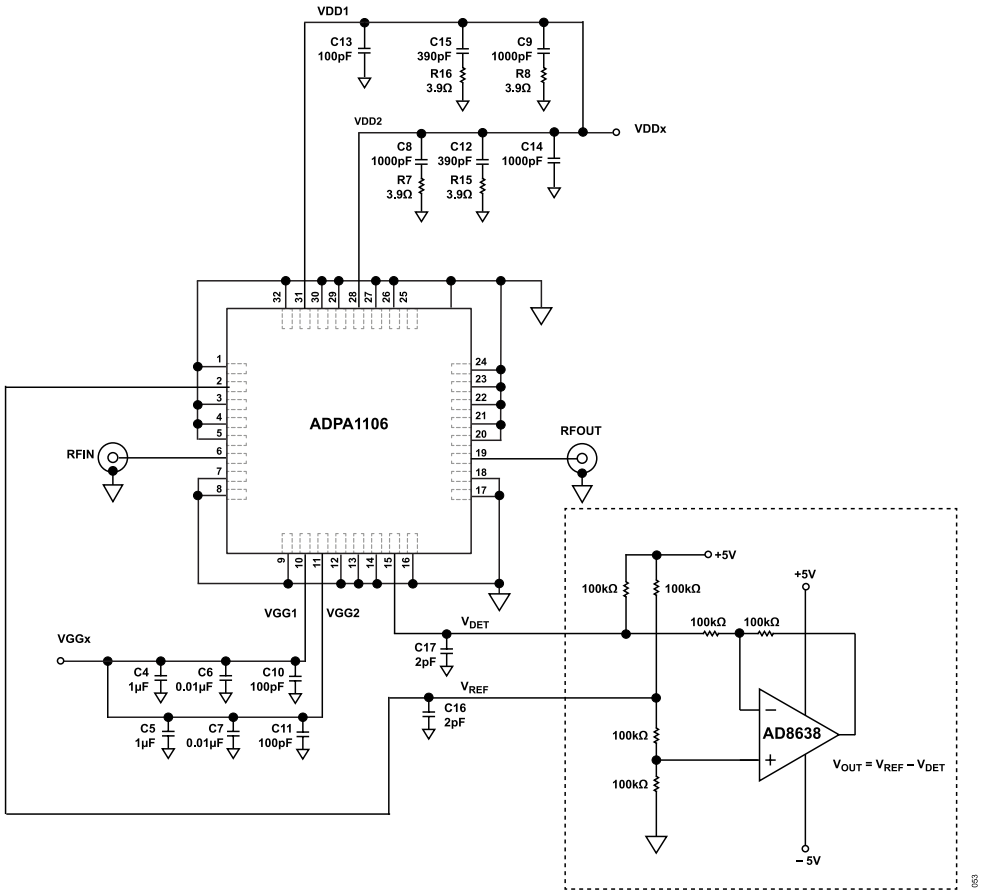


Figure 53. Recommended Detector Subtraction Circuit

THERMAL MANAGEMENT

Proper thermal management is critical to achieve the specified performance and rated operating life. Pulsed biasing is required to limit the average power dissipated and maintain a safe channel temperature. The channel (or die) temperature correlates closely with the mean time to failure.

Consider a continuous bias case (see Figure 54). When bias is applied, the channel temperature (T_{CHAN}) of the device rises through a turn on transient interval and eventually settles to a steady state value. Calculate the θ_{JC} thermal resistance of the device as the rise in T_{CHAN} above the starting T_{BASE} divided by the total device P_{DISS} with the following equation:

$$\theta_{JC} = t_{RISE}/P_{DISS}$$

where:
t_{RISE} is the peak rise in the T_{CHAN} of the device above the T_{BASE} (°C).
P_{DISS} is the power dissipation (W) of the device.

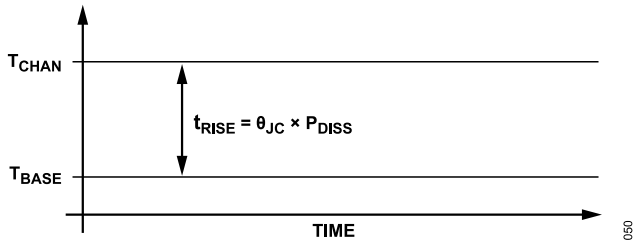


Figure 54. Continuous Bias

Next, consider a pulsed bias case at a fixed pulse width and duty cycle (see Figure 55). When bias is applied, the T_{CHAN} of the device can be described as a series of exponentially rising and decaying pulses. The peak channel temperature reached during consecutive pulses increases during the turn on transient interval, and eventually settles to a steady state condition where peak channel temperatures from pulse to pulse stabilize.

APPLICATIONS INFORMATION

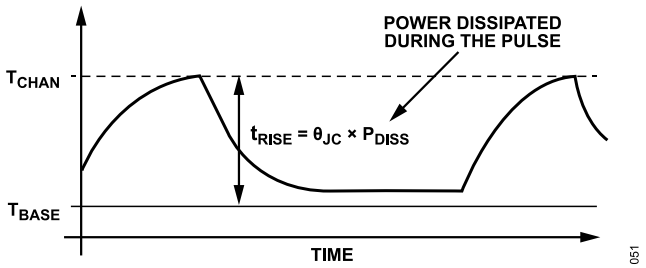


Figure 55. Pulsed Bias at Low Duty Cycle

Transient thermal measurements and analysis were performed at several different bias pulse widths and duty cycles to obtain the thermal resistance values listed in Table 7.

Table 7. Pulse Settings and Thermal Resistance Values

Pulse Settings		
Pulse Width (µs)	**Duty Cycle (%)**	**θ_{JC} (°C/W)**
100	10	2.11
200	20	2.82
300	30	3.54

The ADPA1106 amplifier is designed for a low duty-cycle pulsed application. Under continuous bias conditions, the thermal resistance increases to 6.5°C/W. Even at the nominal quiescent bias, V_{DD1} and V_{DD2} = 50 V and I_{DQ} = 0.3 A, the 15 W power dissipation results in a 97.5°C T_{CHAN} rise above T_{CASE}. If T_{CASE} is 85°C, a T_{CHAN} of 182.5°C results if the device operates continuously.

OUTLINE DIMENSIONS

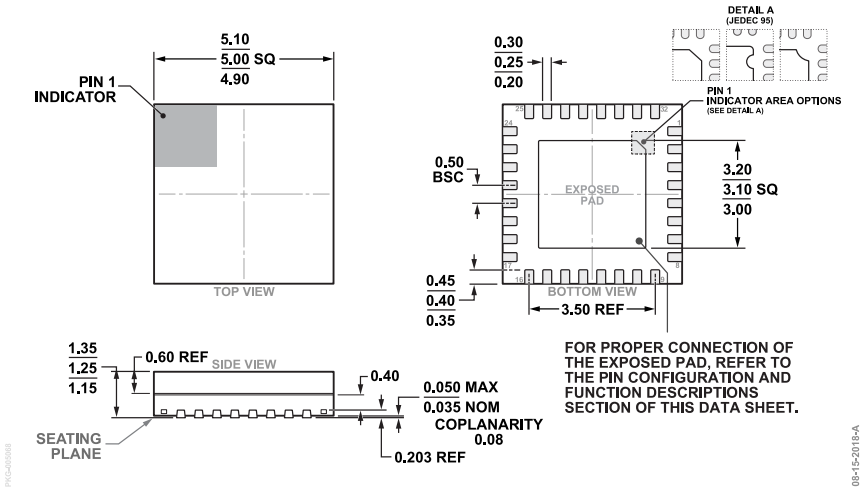


Figure 56. 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]
5 mm × 5 mm Body and 1.25 mm Package Height
(CG-32-2)
Dimensions shown in millimeters

Updated: April 14, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADPA1106ACGZN	−40°C to +85°C	32-Lead LFCSP (5 mm x 5 mm with EPAD)	Tray, 500	CG-32-2
ADPA1106ACGZN-R7	−40°C to +85°C	32-Lead LFCSP (5 mm x 5 mm with EPAD)	Reel, 500	CG-32-2

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADPA1106-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.