



STD70N02L STD70N02L-1

N-channel 25V - 0.0068Ω - 60A - DPAK - IPAK
STripFET™ III Power MOSFET

Features

| Type | V _{DSS} | R _{DS(on)} | I _D |
|-------------|------------------|---------------------|----------------|
| STD70N02L | 25V | <0.008Ω | 60A |
| STD70N02L-1 | 25V | <0.008Ω | 60A |

- R_{DS(ON)} * Qg industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

Application

- Switching applications

Description

This series of products utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

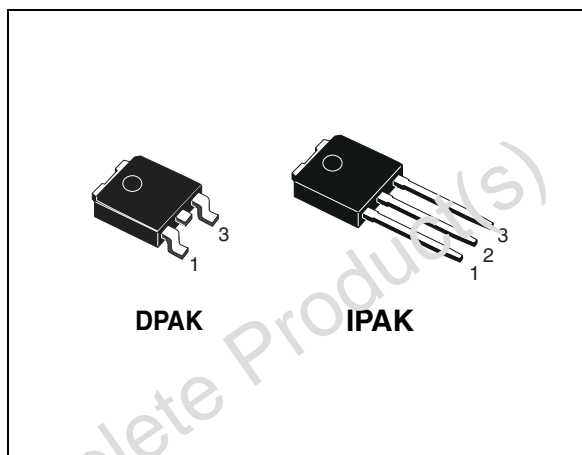


Figure 1. Internal schematic diagram

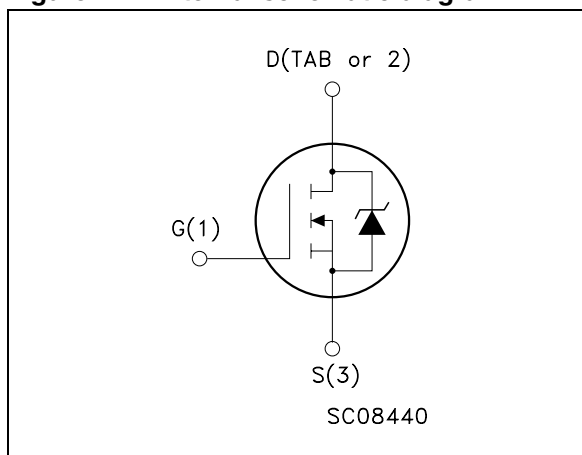


Table 1. Device summary

| Order codes | Marking | Package | Packaging |
|-------------|---------|---------|-------------|
| STD70N02L-1 | D70N02L | IPAK | Tube |
| STD70N02L | D70N02L | DPAK | Tape & reel |

Contents

| | | |
|----------|---|-----------|
| 1 | Electrical ratings | 3 |
| 2 | Electrical characteristics | 4 |
| 2.1 | Electrical characteristics (curves) | 6 |
| 3 | Test circuits | 11 |
| 4 | Package mechanical data | 12 |
| 5 | Package mechanical data | 15 |
| 6 | Revision history | 16 |

Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|------------------------------------|--|------------|-----------------------|
| $V_{\text{spike}}^{(1)}$ | Drain-source voltage rating | 30 | V |
| V_{DS} | Drain-source voltage ($V_{\text{GS}} = 0$) | 25 | V |
| V_{DGR} | Drain-gate voltage ($R_{\text{GS}} = 20\text{k}\Omega$) | 25 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| $I_{\text{D}}^{(2)}$ | Drain current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$ | 60 | A |
| I_{D} | Drain current (continuous) at $T_{\text{C}} = 100^{\circ}\text{C}$ | 42 | A |
| $I_{\text{DM}}^{(3)}$ | Drain current (pulsed) | 240 | A |
| P_{TOT} | Total dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$ | 60 | W |
| | Derating factor | 0.4 | W/ $^{\circ}\text{C}$ |
| $E_{\text{AS}}^{(4)}$ | Single pulse avalanche energy | 280 | mJ |
| T_{j} T_{stg} | Operating junction temperature Storage temperature | -55 to 175 | $^{\circ}\text{C}$ |

1. Guaranteed when external $R_{\text{g}}=4.7\Omega$ and $T_{\text{f}}<T_{\text{fmax}}$
2. Value limited by wire bonding
3. Pulse width limited by safe operating area
4. Starting $T_{\text{j}}=25^{\circ}\text{C}$, $I_{\text{d}} = 30\text{A}$, $V_{\text{DD}} = 15\text{V}$

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|-----------------------|--|-------|-----------------------------|
| $R_{\text{thj-case}}$ | Thermal resistance junction-case Max | 2.5 | $^{\circ}\text{C}/\text{W}$ |
| $R_{\text{thj-amb}}$ | Thermal resistance junction-amb Max | 100 | $^{\circ}\text{C}/\text{W}$ |
| T_{l} | Maximum lead temperature for soldering purpose | 275 | $^{\circ}\text{C}$ |

2 Electrical characteristics

(T_{case} = 25°C unless otherwise specified)

Table 4. On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|---|---|------|-----------------|----------------|----------|
| V _{(BR)DSS} | Drain-source breakdown voltage | I _D = 25mA, V _{GS} = 0 | 25 | | | V |
| I _{DSS} | Zero gate voltage drain current (V _{GS} = 0) | V _{DS} = 20V, V _{DS} = 20V, T _c = 125°C | | | 1 10 | μA μA |
| I _{GSS} | Gate body leakage current (V _{DS} = 0) | V _{GS} = ±20V | | | ±100 | nA |
| V _{GS(th)} | Gate threshold voltage | V _{DS} = V _{GS} , I _D = 250μA | 1 | 1.8 | | V |
| R _{DS(on)} | Static drain-source on resistance | V _{GS} = 10V, I _D = 30A V _{GS} = 5V, I _D = 15A | | 0.0068 0.090 | 0.008 0.014 | Ω Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--|---|--|------|-------------------|------|----------------|
| g _{fs} (1) | Forward transconductance | V _{DS} = 15V, I _D = 30A | | 27 | | S |
| C _{iss} C _{oss} C _{rss} | Input capacitance Output capacitance Reverse transfer capacitance | V _{DS} = 16V, f = 1MHz, V _{GS} = 0 | | 1400 400 55 | | pF pF pF |
| Q _g Q _{gs} C _{gd} | Total gate charge Gate-source charge Gate-drain charge | V _{DD} = 10V, I _D = 60A V _{GS} = 10V (see Figure 8) | | 24 5 3.4 | 32 | nC nC nC |
| R _G | Gate input resistance | f = 1MHz Gate DC Bias = 0 test signal level = 20mV open drain | 0.5 | 1.5 | 3 | Ω |
| Q _{OSS} (2) | Output charge | V _{DS} = 16V, V _{GS} = 0V | | 9.4 | | nC |

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%

2. Q_{OSS} = C_{oss} * D Vin, C_{oss} = C_{gd} + C_{gd}. (see [Appendix A](#))

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}=10V, I_D=30A,$ $R_G=4.7\Omega, V_{GS}=10V$ (see Figure 18) | | 10 | | ns |
| t_r | Rise time | | | 130 | | ns |
| $t_{d(off)}$ | Turn-off delay time | | | 27 | | ns |
| t_f | Fall time | | | 16 | 21.6 | ns |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|-------------------------------|--|------|------|------|------|
| I_{SD} | Source-drain current | | | | 50 | A |
| I_{SDM} | Source-drain current (pulsed) | | | | 200 | A |
| $V_{SD}^{(1)}$ | Forward on voltage | $I_{SD}=30A, V_{GS}=0$ | | | 1.3 | V |
| t_{rr} | Reverse recovery time | $I_{SD}=60A, di/dt = 100A/\mu s$ $V_{DD}=20V, T_j=150^\circ C$ (see Figure 21) | | 36 | | ns |
| Q_{rr} | Reverse recovery charge | | | 36 | | nC |
| I_{RRM} | Reverse recovery current | | | 2 | | A |

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

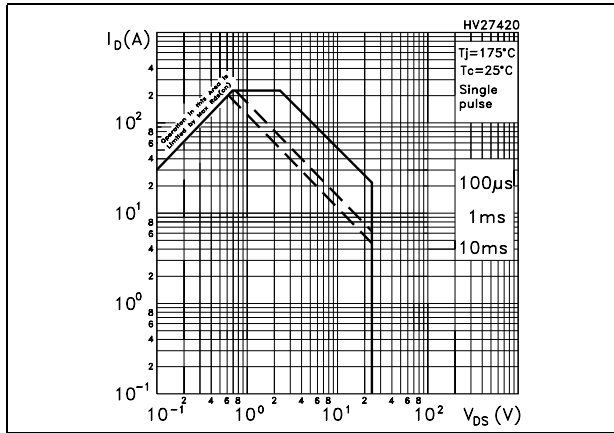


Figure 3. Thermal impedance

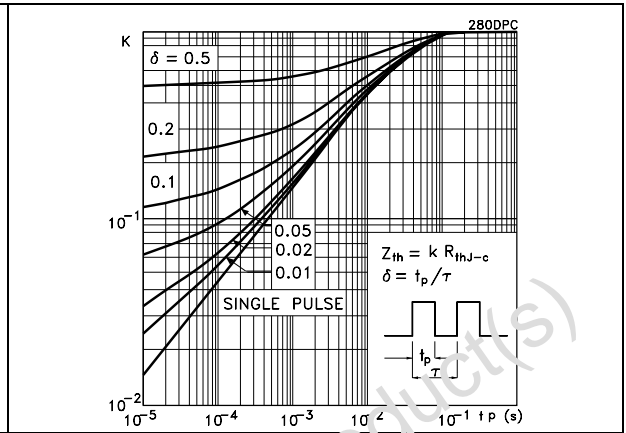


Figure 4. Output characteristics

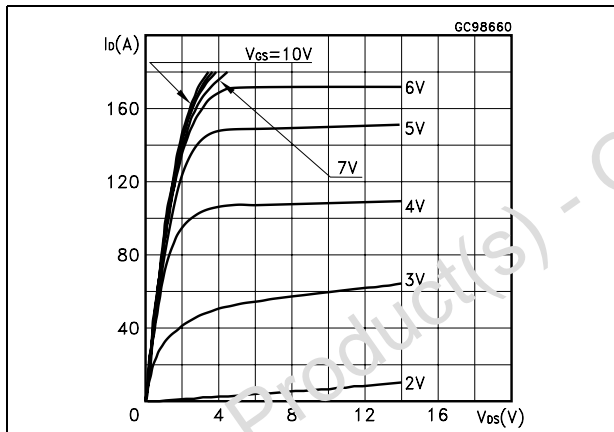


Figure 5. Transfer characteristics

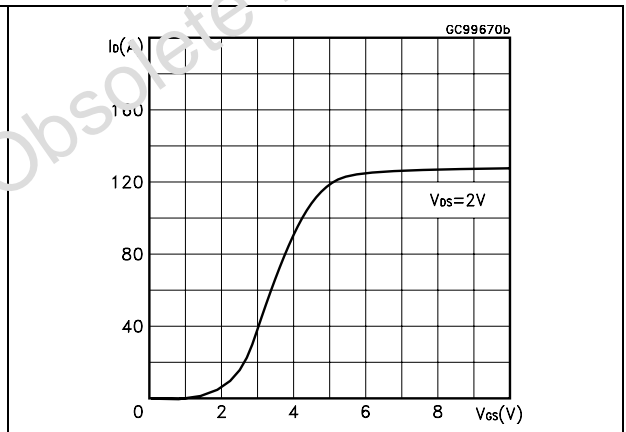


Figure 6. Transconductance

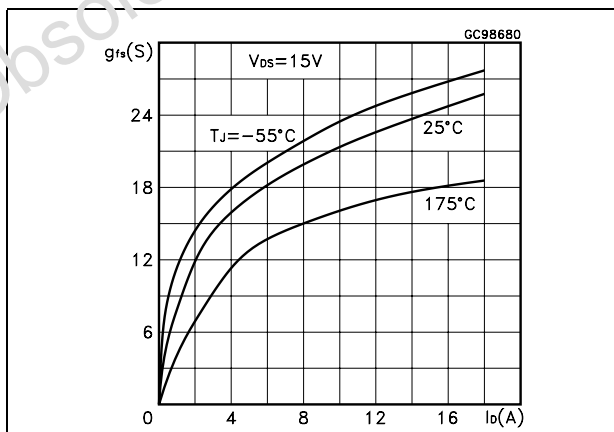


Figure 7. Static drain-source on resistance

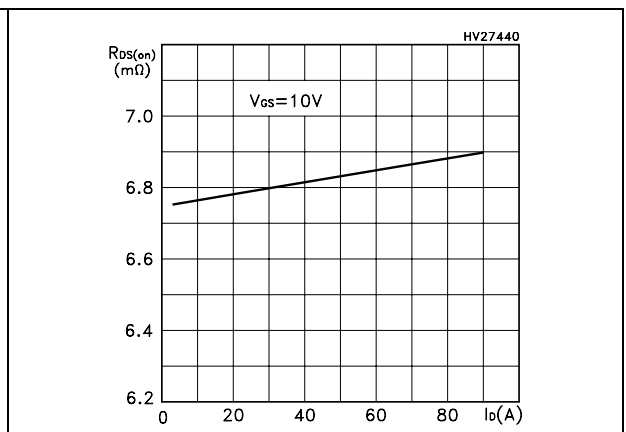


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

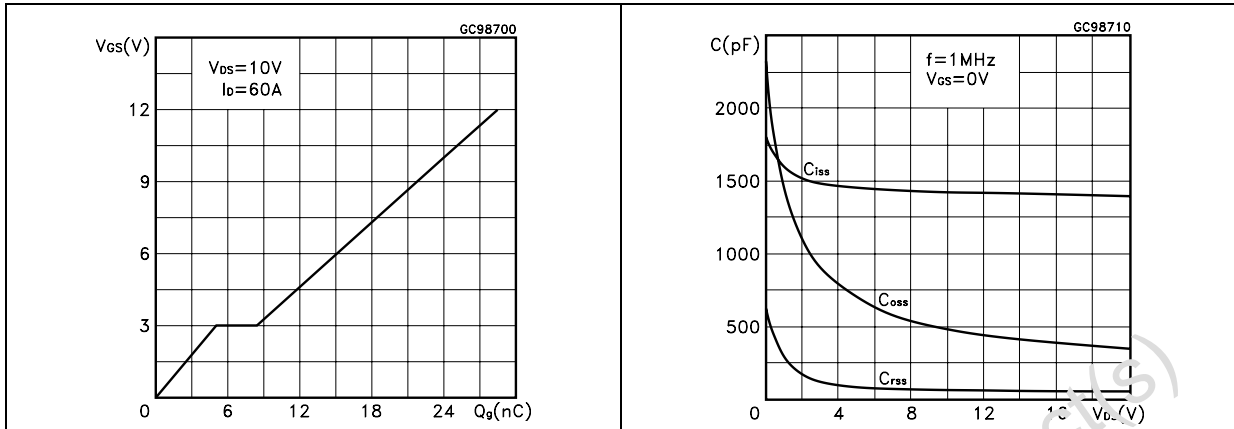


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

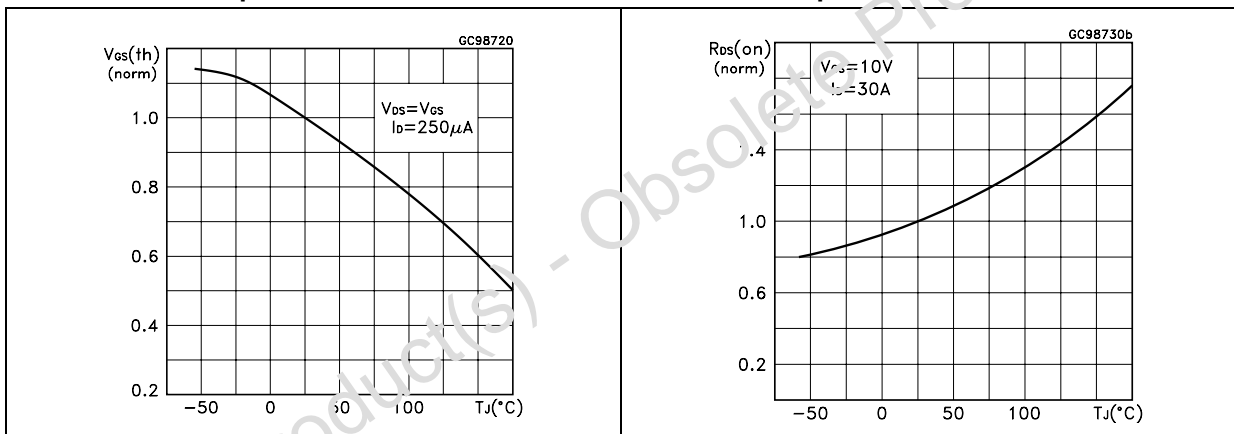


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized $B_{V_{DS}}$ vs temperature

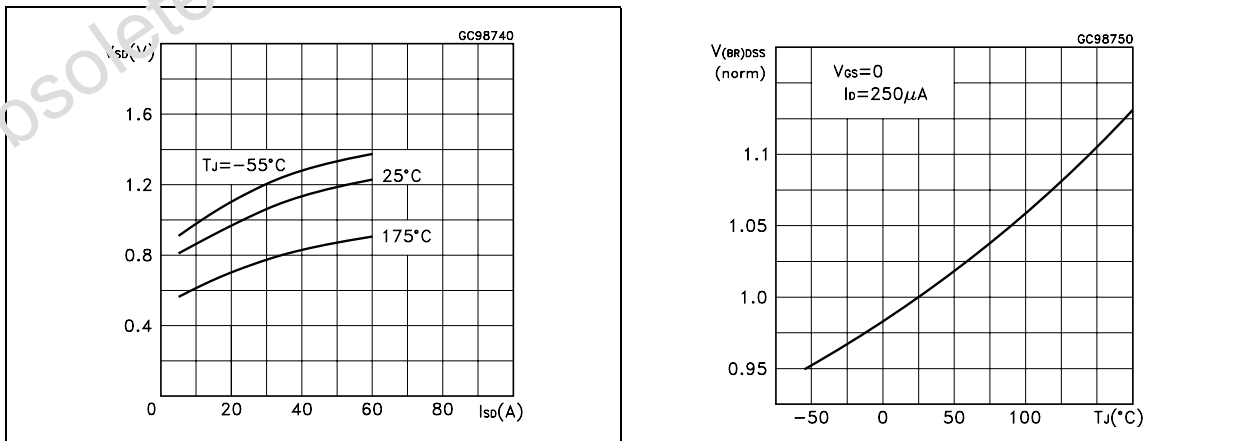
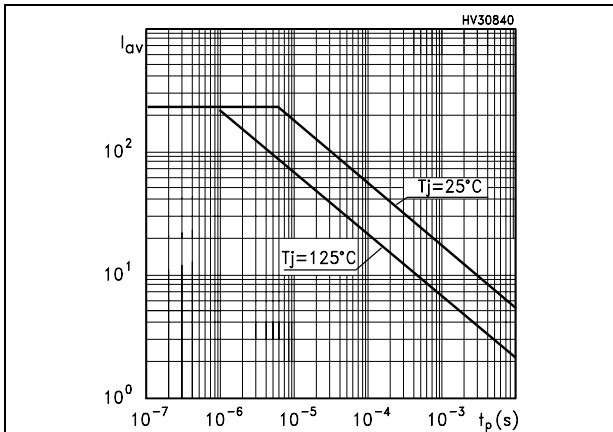


Figure 14. Allowable I_{AV} vs time in avalanche



The previous curve gives the single pulse safe operating area for unclamped inductive loads, under the following conditions:

$$P_{D(AVE)} = 0.5 \cdot (1.3 \cdot B_{VDSS} \cdot I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} \cdot t_{AV}$$

Where:

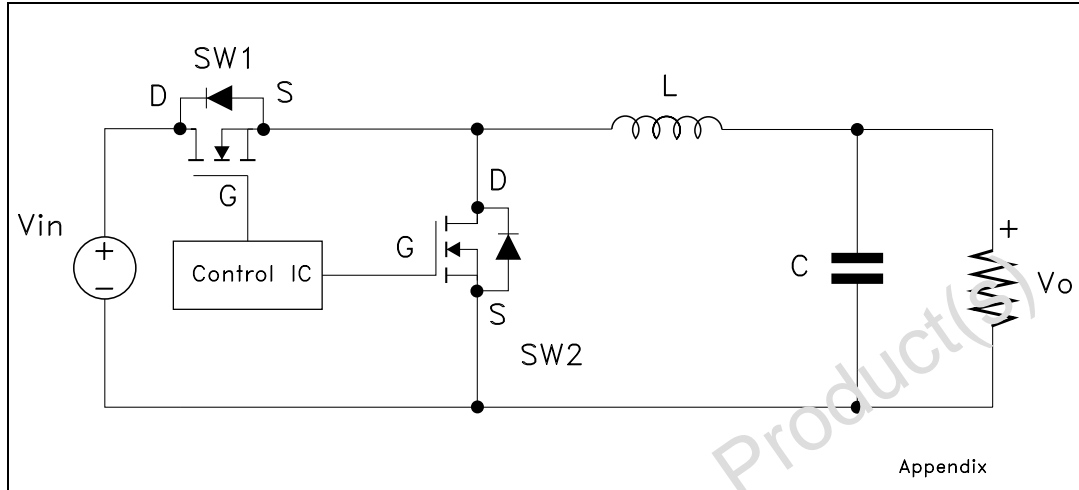
I_{AV} is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

t_{AV} is the time in avalanche

Appendix A Buck convert

Figure 15. Synchronous buck converter



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

Very low $R_{DS(on)}$ to reduce conduction losses

Small Q_{gls} to reduce the gate charge losses

Small C_{oss} to reduce losses due to output capacitance

Small Q_{rr} to reduce losses on SW1 during its turn-on

The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon.

The high side (SW1) device requires:

Small R_G and L_G to allow higher gate current peak and to limit the voltage feedback on the gate

Small Q_g to have a faster commutation and to reduce gate charge losses

Low $R_{DS(on)}$ to reduce the conduction losses

Table 8. Power losses

| | | High side switch (SW1) | Low side switch (SW2) |
|-------------------------|------------|--|---|
| P _{conduction} | | $R_{DS(on)} \cdot I_L^2 \cdot \delta$ | $R_{DS(on)} \cdot I_L^2 \cdot (1 - \delta)$ |
| P _{switching} | | $V_{in} \cdot (Q_{gsth(SW1)} + Q_{gd(SW1)}) \cdot f \cdot \frac{I_L}{I_g}$ | Zero voltage switching |
| P _{diode} | recovery | Not applicable | $^1V_{in} \cdot Q_{rr(SW2)} \cdot f$ |
| | conduction | Not applicable | $V_{f(SW2)} \cdot I_L \cdot t_{deadtime} \cdot f$ |
| P _{gate(Qg)} | | $Q_{g(SW1)} \cdot V_{gg} \cdot f$ | $Q_{gls(SV/2)} \cdot V_{gg} \cdot f$ |
| P _{Qoss} | | $\frac{V_{in} \cdot Q_{oss(SW1)} \cdot f}{2}$ | $\frac{V_{in} \cdot Q_{oss(SW2)} \cdot f}{2}$ |

Table 9. Power losses parameters

| Paramter | Meaning |
|-------------------------|--|
| d | Duty-cycle |
| Q _{gsth} | Root threshold gate charge |
| Q _{gls} | Third quadrant gate charge |
| P _{conduction} | On state losses |
| P _{switching} | On-off transition losses |
| P _{diode} | Conduction and reverse recovery diode losses |
| P _{gate} | Gate driver losses |
| P _{Qoss} | Output capacitance losses |

3 Test circuits

Figure 16. Switching times test circuit for resistive load

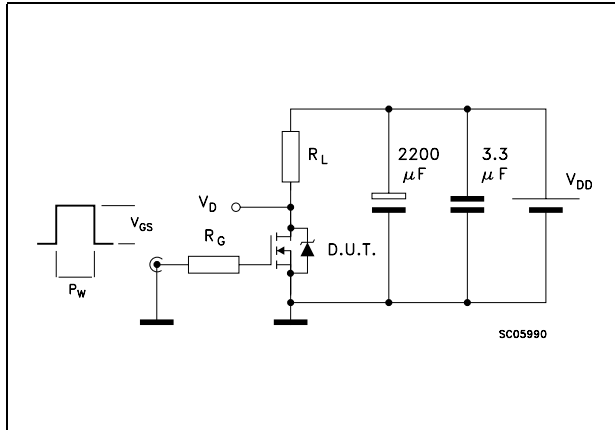


Figure 17. Gate charge test circuit

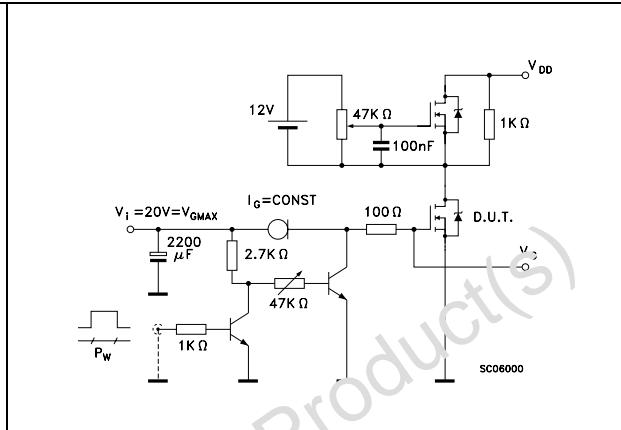


Figure 18. Test circuit for inductive load switching and diode recovery times

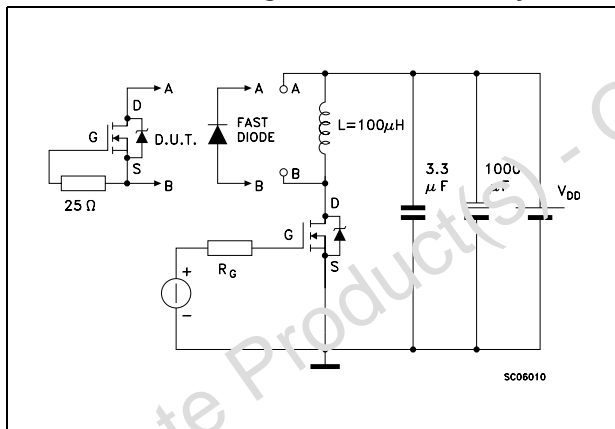


Figure 19. Unclamped inductive load test circuit

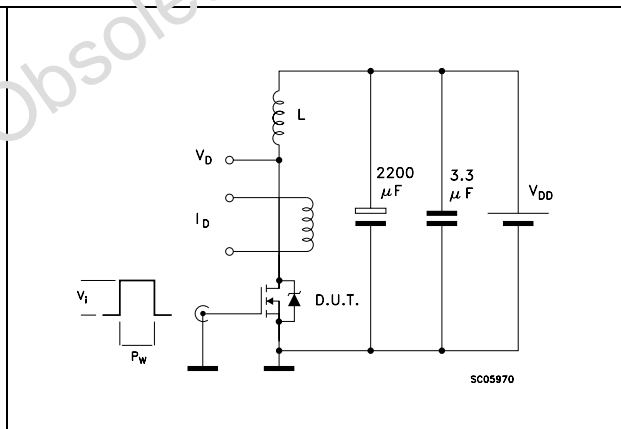


Figure 20. Unclamped inductive waveform

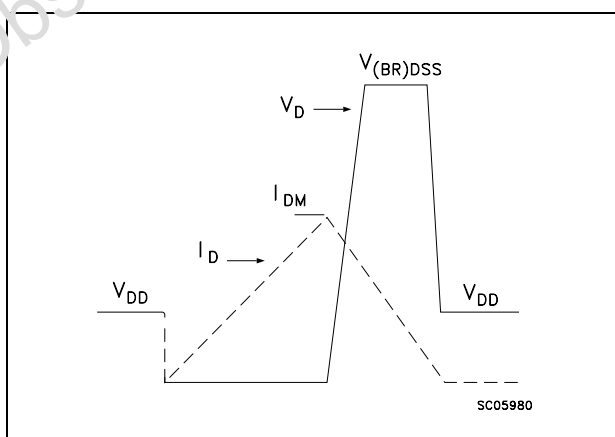
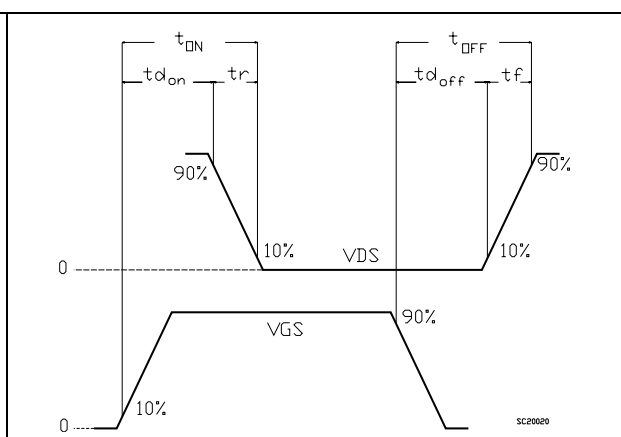


Figure 21. Switching time waveform



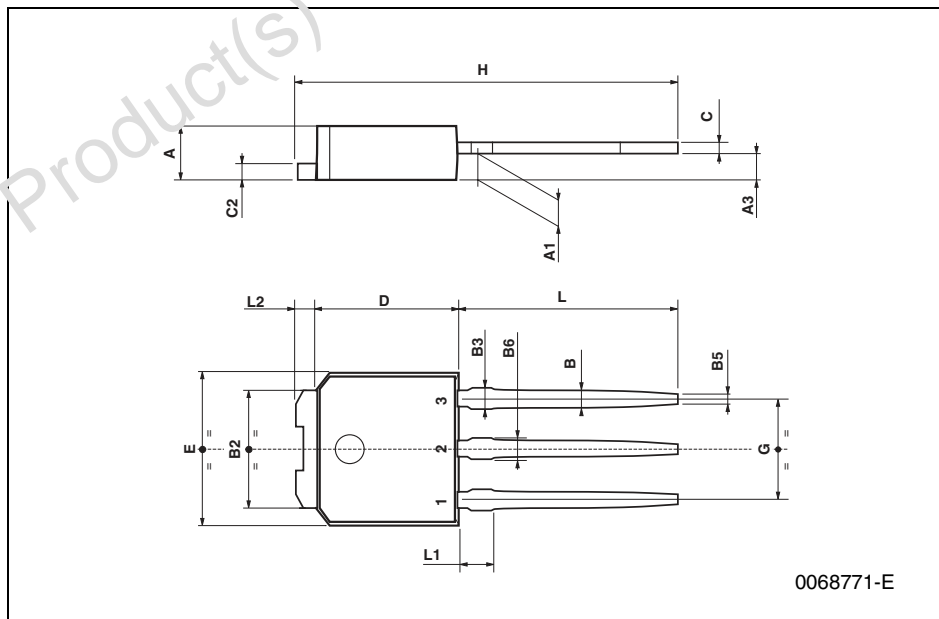
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

Obsolete Product(s) - Obsolete Product(s)

TO-251 (IPAK) MECHANICAL DATA

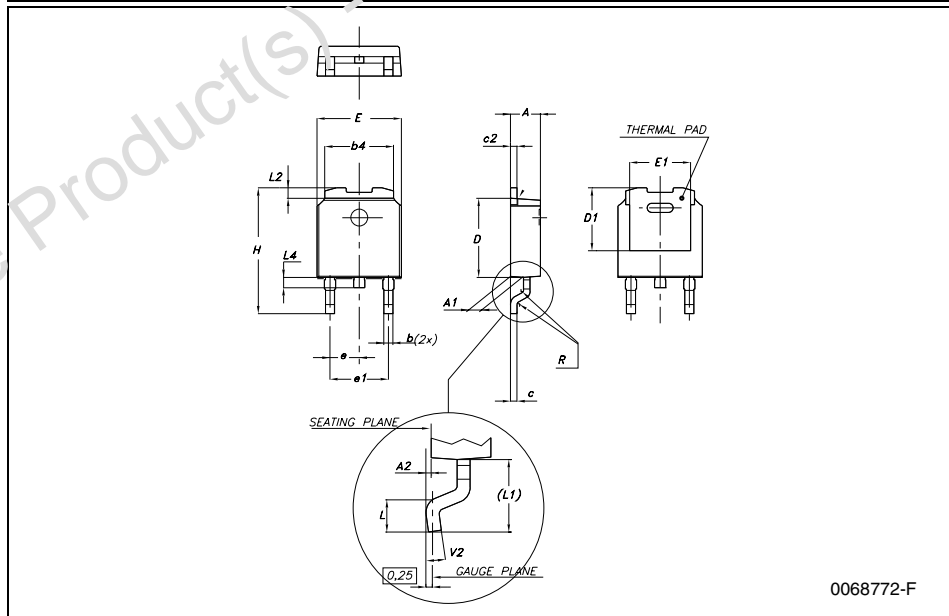
| DIM. | mm | | | inch | | |
|------|------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.2 | | 2.4 | 0.086 | | 0.094 |
| A1 | 0.9 | | 1.1 | 0.035 | | 0.043 |
| A3 | 0.7 | | 1.3 | 0.027 | | 0.051 |
| B | 0.64 | | 0.9 | 0.025 | | 0.031 |
| B2 | 5.2 | | 5.4 | 0.204 | | 0.212 |
| B3 | | | 0.85 | | | 0.033 |
| B5 | | 0.3 | | | 0.012 | |
| B6 | | | 0.95 | | | 0.037 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 0.48 | | 0.6 | 0.019 | | 0.023 |
| D | 6 | | 6.2 | 0.236 | | 0.244 |
| E | 6.4 | | 6.6 | 0.252 | | 0.260 |
| G | 4.4 | | 4.6 | 0.173 | | 0.181 |
| H | 15.9 | | 16.3 | 0.626 | | 0.641 |
| L | 9 | | 9.7 | 0.354 | | 0.370 |
| L1 | 0.8 | | 1.2 | 0.031 | | 0.047 |
| L2 | | 0.8 | 1 | | 0.031 | 0.039 |



0068771-E

DPAK MECHANICAL DATA

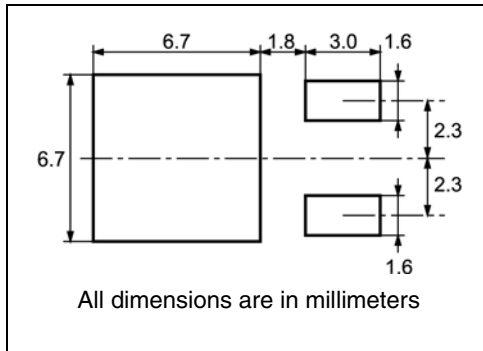
| DIM. | mm. | | | inch | | |
|------|------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 2.2 | | 2.4 | 0.086 | | 0.094 |
| A1 | 0.9 | | 1.1 | 0.035 | | 0.043 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.64 | | 0.9 | 0.025 | | 0.035 |
| b4 | 5.2 | | 5.4 | 0.204 | | 0.212 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 0.48 | | 0.6 | 0.019 | | 0.023 |
| D | 6 | | 6.2 | 0.236 | | 0.244 |
| D1 | | 5.1 | | 0.201 | | |
| E | 6.4 | | 6.6 | 0.252 | | 0.260 |
| E1 | | 4.7 | | 0.185 | | |
| e | | 2.28 | | 0.090 | | |
| e1 | 4.4 | | 4.6 | 0.173 | | 0.181 |
| H | 9.35 | | 10.1 | 0.368 | | 0.397 |
| L | 1 | | | 0.039 | | |
| (L1) | | 2.8 | | | 0.110 | |
| L2 | | 0.8 | | | 0.031 | |
| L4 | 0.6 | | 1 | 0.023 | | 0.039 |
| R | | 0.2 | | | 0.008 | |
| V2 | 0° | | 8° | 0° | | 8° |



0068772-F

5 Package mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot for tape start 2.0 mm min. width

T

C

N

G measured at hub

| DIM. | mm | | inch | |
|------|------|------|-------|--------|
| | MIN. | MAX. | MIN. | MAX. |
| A | | 330 | | 12.992 |
| B | 1.5 | | 0.059 | |
| C | 12.8 | 13.2 | 0.504 | 0.520 |
| D | 20.2 | | 0.795 | |
| G | 16.4 | 18.4 | 0.645 | 0.724 |
| N | 50 | | 1.968 | |
| T | | 22.4 | | 0.881 |

| BASE QTY | BULK QTY |
|----------|----------|
| 2500 | 2500 |

TAPE MECHANICAL DATA

| DIM. | mm | | inch | |
|----------------|------|------|-------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A ₁ | 6.8 | 7 | 0.267 | 0.275 |
| B ₀ | 10.4 | 10.6 | 0.409 | 0.417 |
| B ₁ | | 12.1 | | 0.476 |
| D | 1.5 | 1.6 | 0.059 | 0.063 |
| D ₁ | 1.5 | | 0.059 | |
| E | 1.65 | 1.85 | 0.065 | 0.073 |
| F | 7.4 | 7.6 | 0.291 | 0.299 |
| K ₀ | 2.55 | 2.75 | 0.100 | 0.108 |
| P ₀ | 3.9 | 4.1 | 0.153 | 0.161 |
| P ₁ | 7.9 | 8.1 | 0.311 | 0.319 |
| P ₂ | 1.9 | 2.1 | 0.075 | 0.082 |
| R | 40 | | 1.574 | |
| W | 15.7 | 16.3 | 0.618 | 0.641 |

10 pitches cumulative tolerance on tape +/- 0.2 mm

For machine ref. only including draft and radii concentric around B₀

TRL

FEED DIRECTION

Bending radius

6 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 29-Aug-2005 | 1 | First release |
| 02-Dec-2005 | 2 | Modified Appendix A |
| 07-Apr-2006 | 3 | New template |
| 03-May-2006 | 4 | New value in Table 4 , new curve (see Figure 14) |
| 25-Oct-2007 | 5 | Updated BV_{dss} value |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED REPRESENTATIVE OF ST, ST PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS, WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com