KEY FEATURES

- **SMPTE 259M and SMPTE 344M compliant**
- **dual coaxial cable driving outputs**
- **50Ω differential PECL input**
- **single 3.3V power supply operation**
- **space-saving 8-lead SOIC**
- **operating temperature range: 0°C to 70°C**
- **pin compatible with GS1528 HD-LINX™ II multirate SDI dual slew-rate cable driver**
- **Pb-free and Green**

APPLICATIONS

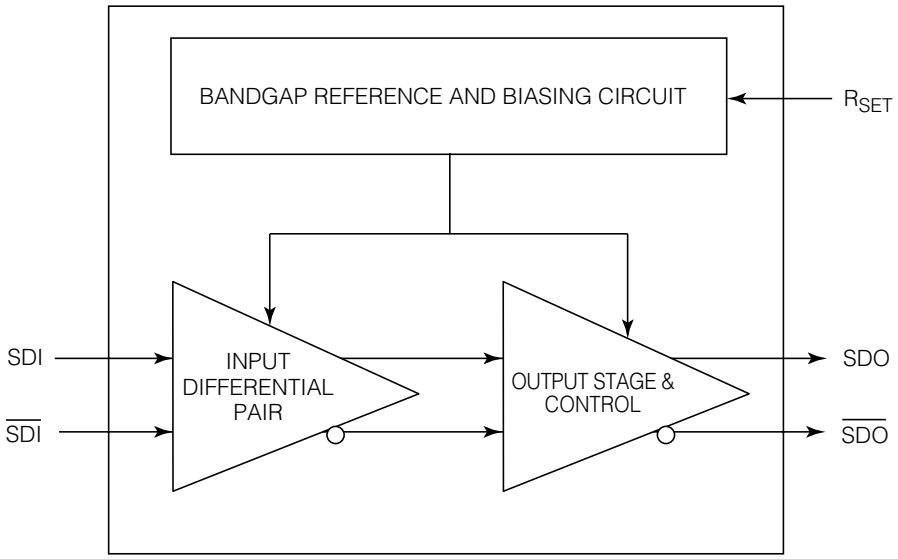
- SMPTE 259M Coaxial Cable Serial Digital Interfaces

DESCRIPTION

The GS9068 is a second generation high-speed bipolar integrated circuit designed to drive one or two 75Ω co-axial cables at data rates up to 540Mb/s.

The GS9068 accepts a LVPECL level differential input, which may be AC coupled. External biasing resistors at the inputs are not required.

Power consumption is typically 160mW using a +3.3V DC power supply.



GS9068 FUNCTIONAL BLOCK DIAGRAM

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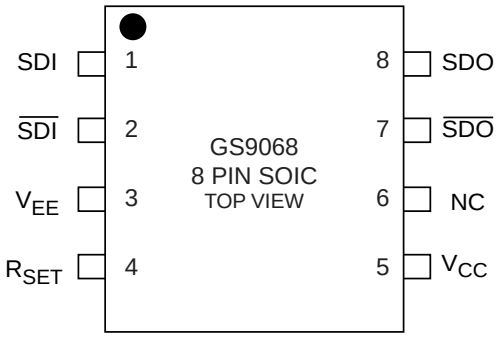
1. PIN OUT

1.1 PIN ASSIGNMENT



1.2 PIN DESCRIPTIONS

PIN NUMBER	NAME	TYPE	DESCRIPTION
1,2	SDI, $\overline{SDI}$	Input	Serial digital differential input.
3	V_{EE}	Input Power	Most negative power supply connection - connect to GND.
4	R_{SET}	Input	External output amplitude control resistor.
5	V_{CC}	Input Power	Most positive power supply connection - connect to +3.3V.
6	NC	-	No Connect.
7,8	SDO, $\overline{SDO}$	Output	Serial digital differential output.

2. ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise indicated

PARAMETER	VALUE
Supply Voltage	-0.5V to 3.6 V_{DC}
Input ESD Voltage	500V
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Power Dissipation	300mW
Lead Temperature (soldering, 10 sec)	260°C

CAUTION

The GS9068 is sensitive to electrostatic discharge. Use extreme caution, observing all ESD-prevention practices, during handling and assembly. The SDI inputs of the GS9068 must be protected from electrostatic discharge and electrical overstress during the handling and operation of circuit assemblies containing the device.

2.2 DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{EE} =0V, T_A = 0°C to 70°C, 270Mb/s unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYPICAL	MAX	UNITS	TEST LEVEL
Supply Voltage	V_{CC}		3.1	3.3	3.5	V	3
Power Consumption	P_D		-	160	-	mW	5
Supply Current	I_s		-	48	-	mA	1
Output Voltage	V_{OC}	Common mode	-	V_{CC} - $\Delta V_{SDO(SE)}$	-	mV	6
Input Voltage	V_{IC}	Common mode	1.6 + $\Delta V_{SDI(DIFF)}/2$	-	V_{CC} - $\Delta V_{SDI(DIFF)}/2$	mV	1

2.3 AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{EE} =0V, T_A = 0°C to 70°C, 270Mb/s unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYPCAL	MAX	UNITS	TEST LEVEL
Serial input data rate	DR_{SDI}		-	-	540	Mb/s	1
Input Voltage Swing	$\Delta V_{SDI(DIFF)}$	Differential	300	-	2000	mV_{p-p}	1
Output Voltage Swing	$\Delta V_{SDO(SE)}$	Single Ended into 75Ω external load R_{SET} = 750Ω	750	800	850	mV_{p-p}	1
Additive jitter			-	-	30	ps	1
Rise/Fall time	t_r, t_f	20% - 80%	400	-	800	ps	1
Mismatch in rise/fall time	Δt_r, Δt_f		-	-	30	ps	1
Duty cycle distortion			-	-	100	ps	1
Overshoot			-	-	8	%	1
Output Return Loss	ORL		15	-	-	dB	7

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.
10. Wafer Probe

3. DETAILED DESCRIPTION

3.1 SERIAL DIGITAL INPUT

SDI/$\overline{SDI}$ are high impedance differential inputs. Several conditions must be observed when interfacing to these inputs:

1. The differential input signal amplitude must be between 300 and 2000mVpp.
2. For DC coupling to the device, the common mode voltage must be between $1.6+\Delta V_{SDI(DIFF)}$ and $VCC-\Delta V_{SDI(DIFF)}$.
3. For input trace lengths longer than approximately 1cm, the inputs should be terminated as shown in the Typical Application Circuit.

The GS9068 inputs are self-biased, allowing for simple AC coupling to the device. For serial digital video, a minimum capacitor value of 4.7µF should be used to allow coupling of pathological test signals. A tantalum capacitor is recommended.

3.2 SERIAL DIGITAL OUTPUT

The GS9068 outputs are current mode and will drive 800mV into a 75Ω load. These outputs are protected from accidental static damage with internal static protection diodes.

The SMPTE 259M standard requires that the output of a cable driver have a source impedance of 75Ω and a return loss of at least 15dB between 5MHz and 540MHz. In order for an SDI output circuit using the GS9068 to meet this specification, the output circuit shown in the Typical Application Circuit is recommended.

The value of L_{COMP} will vary depending on the PCB layout, with a typical value of 5.6nH. A 4.7µF capacitor is used for AC coupling the output of the GS9068. This value is chosen to ensure that pathological signals can be coupled without a significant DC component occurring.

See Section 4, Application Reference Design, for more details.

When measuring return loss at the GS9068 output, it is necessary to take the measurement for both a logic high and a logic low output condition. This is because the output protection diodes act as a varactor (voltage controlled capacitor) as shown in Figure 1. Consequently, the output capacitance of the GS9068 is dependent on the logic state of the output.

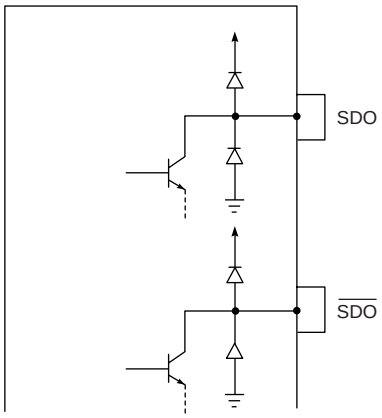


Fig. 1 Static Protection Diodes

3.3 OUTPUT RETURN LOSS MEASUREMENT

To perform a practical return loss measurement, it is necessary to force the GS9068 output to a DC high or low condition. The actual return loss will be based on the outputs being static at V_{CC} or V_{CC}-1.6V. Under normal operating conditions the outputs of the GS9068 swing between V_{CC}-0.4V and V_{CC}-1.2V, so the measured value of return loss will not represent the actual operating return loss.

A simple method of calculating the values of actual operating return loss is to interpolate the two return loss measurements. In this way, the values of return loss are estimated at V_{CC}-0.4V and V_{CC}-1.2V based on the measurements at V_{CC} and V_{CC}-1.6V.

The two values of return loss (high and low) will typically differ by several decibels. If the measured return loss is R_H for logic high and R_L for logic low, then the two values can be interpolated as follows:

$$R_{IH} = R_H - (R_H - R_L)/4, \text{ and}$$

$$R_{IL} = R_L + (R_H - R_L)/4,$$

where R_{IH} is the interpolated logic high value and R_{IL} is the interpolated logic low value.

For example, if R_H = -18dB and R_L = -14dB, then the interpolated values are R_{IH} = -17dB and R_{IL} = -15dB.

3.4 OUTPUT AMPLITUDE ADJUSTMENT

The output amplitude of the GS9068 can be adjusted by changing the value of the R_{SET} resistor as shown in Figure 2 and Table 1 below. For an 800mV$_{p-p}$ output with a nominal ±7% tolerance, a value of 750Ω is required. A ±1% SMT resistor should be used.

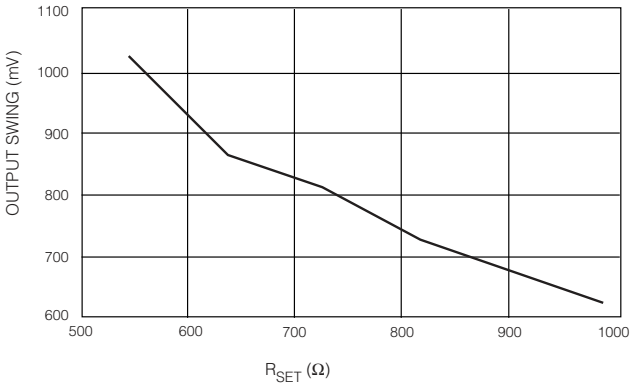


Fig. 2 Output Amplitude Adjustment

The R_{SET} resistor is part of the high speed output circuit of the GS9068. The resistor should be placed as close as possible to the R_{SET} pin. In addition, the PCB capacitance should be minimized at this node by removing the PCB groundplane beneath the R_{SET} resistor and the R_{SET} pin.

Table 1: R_{SET} vs V_{OD}

R_{SET} (Ω)	OUTPUT SWING
995	608mV
824	734mV
750	800mV
600	884mV
573	1040mV

NOTE: For reliable operation of the GS9068 over the full temperature range, do not use an R_{SET} value below 573Ω.

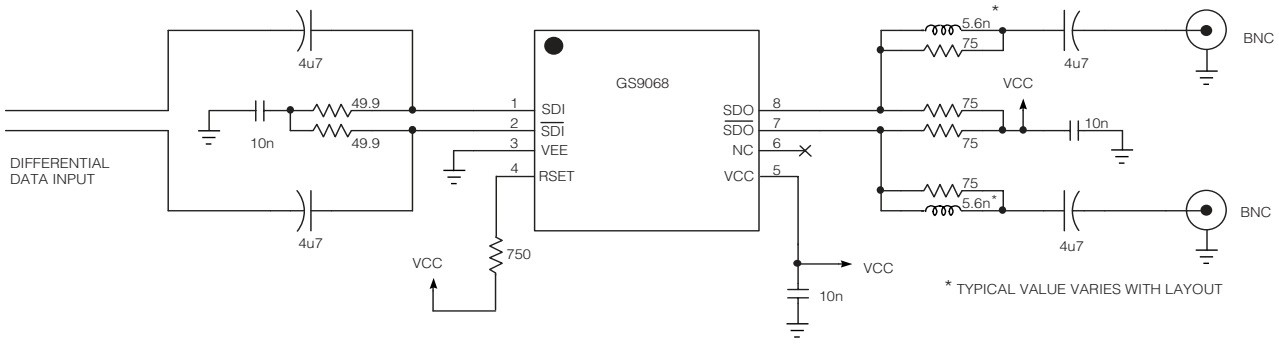
4. APPLICATION REFERENCE DESIGN

4.1 PCB LAYOUT

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- The PCB groundplane is removed under the GS9068 output components to minimize parasitic capacitance.
- The PCB ground plane is removed under the GS9068 R_{SET} pin and resistor to minimize parasitic capacitance.
- Input and output BNC connectors are surface mounted in-line to eliminate a transmission line stub caused by a BNC mounting via high speed traces which are curved to minimize impedance variations due to change of PCB trace width.

4.2 TYPICAL APPLICATION CIRCUIT



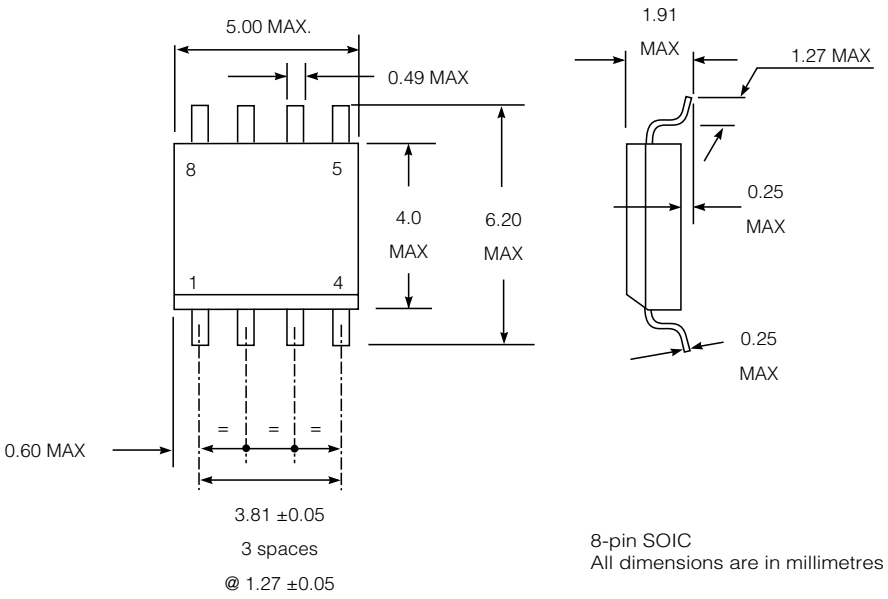
NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.

5. REFERENCES

Compliant with SMPTE 259M and SMPTE 344M.

6. PACKAGE & ORDERING INFORMATION

6.1 PACKAGE DIMENSIONS



8-pin SOIC
All dimensions are in millimetres

6.2 ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	Pb-FREE AND GREEN
GS9068-CKA	8 pin SOIC	0°C to 70°C	No
GS9068-CTA	8 pin SOIC Tape	0°C to 70°C	No
GS9068-CKAE3	8 pin SOIC	0°C to 70°C	Yes
GS9068-CTAE3	8 pin SOIC Tape	0°C to 70°C	Yes

7. REVISION HISTORY

VERSION	ECR	DATE	CHANGES AND/OR MODIFICATIONS
A	120608	July 2002	New Document
B	125775	July 2002	Added detailed block descriptions and initial applications information.
0	127024	December 2002	Document upgraded to Preliminary Data Sheet and AC/DC Characteristics edited to match current design specification limits.
1	128544	March 2003	Document upgraded to Data Sheet.
2	133977	June 2004	Added lead-free and green information.

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES

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