

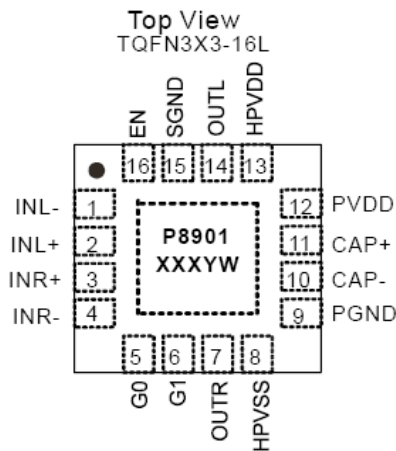
## Description

The PAM8901 stereo headphone driver is designed for portable equipment where board space is at a premium. The PAM8901 uses a unique, patent pending architecture to produce a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors, saving cost, board space, and component height.

The PAM8901 delivers up to 25mW per channel into a 16Ω load and has low 0.03% THD+N. A high power-supply rejection ratio (80dB at 1kHz) allows this device to operate from noisy digital supplies without an additional linear regulator.

The PAM8901 operates from a single supply from 2.5V to 5.5V, has short-circuit and over temperature protection. Shutdown mode reduces supply current to less than 1μA.

## Pin Assignments



## Features

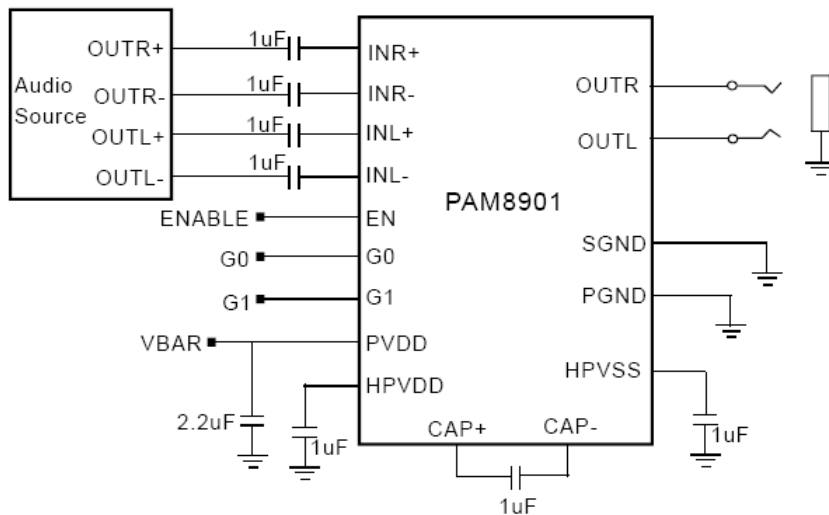
- Patent Pending 3 phase power line shift
- charge pump Eliminates Need for DC-Blocking Capacitors
- TrueCapFree Architecture, Output Biased at 0V (System Ground)
- Excellent Low Frequency Fidelity
- 80dB PSRR at 1kHz
- Less than 1uA Shutdown current
- Support both Fully differential and Single-Ended Inputs
- Short Circuit and Over Temperature Protection
- Selectable Gain settings:-6dB,0dB,3dB and 6dB
- Available in Space Saving Packages: TQFN3x3-16L

## Applications

- Smart Phones/Cellular Phones
- Notebook Computers
- Portable DVD Player
- Personal Digital Assistants (PDAs)
- Electronic Dictionaries
- Digital Still Cameras
- Portable Gaming

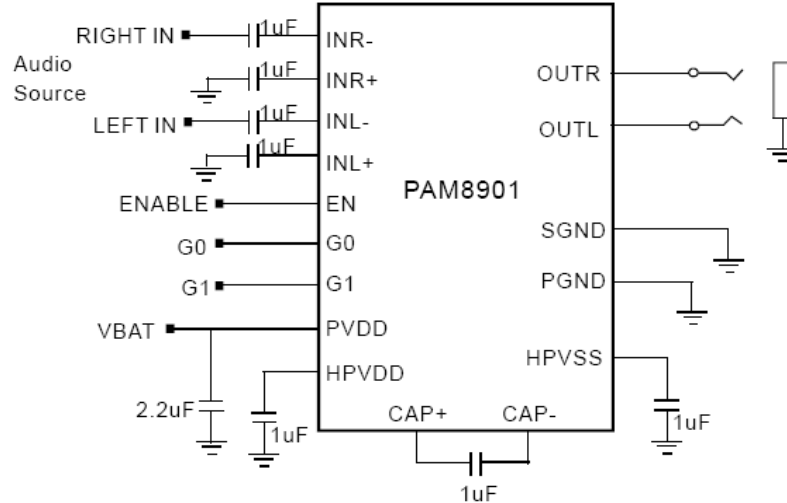
## Typical Applications Circuit

Typical Application Configuration with Differential Input Signals



**Typical Applications Circuit (cont.)**

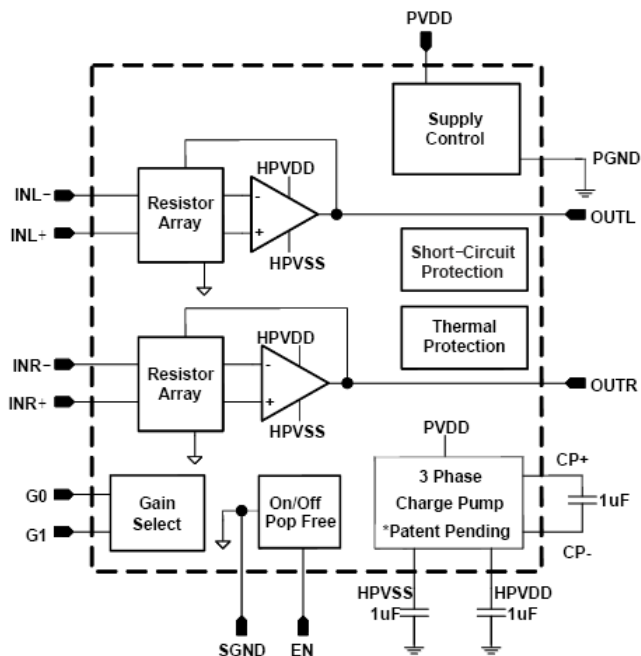
**Typical Application Configuration with Single-Ended Input Signal**



**Pin Descriptions**

| Pin Number | T-QFN3x3-16L Pin Name | I/O/P | Function  |
|------------|-----------------------|-------|---|
| 1          | INL-                  | I     | Inverting left input for differential signals.  |
| 2          | INL+                  | I     | Non-inverting left input for differential signals.  |
| 3          | INR+                  | I     | Inverting right input for differential signals.   |
| 4          | INR-                  | I     | Non-inverting right input for differential signals.   |
| 5          | G0                    | I     | Gain select bit 0   |
| 6          | G1                    | I     | Gain select bit 1   |
| 7          | OUTR                  | O     | Right headphone amplifier output. Connect to right terminal of headphone jack.                    |
| 8          | HPVSS                 | P     | Charge pump output and negative power supply for output amplifiers; connect 1µF capacitor to GND  |
| 9          | PGND                  | P     | Power Ground  |
| 10         | CAP-                  | O     | Charge pump negative flying cap.  |
| 11         | CAP+                  | O     | Charge pump positive flying cap.  |
| 12         | PVDD                  | P     | Power V <sub>DD</sub> .   |
| 13         | HPVDD                 | O     | Positive power supply for headphone amplifiers. Charge pump positive half V <sub>DD</sub> output. |
| 14         | OUTL                  | O     | Left headphone amplifier output. Connect to left terminal of headphone jack.                      |
| 15         | SGND                  | I     | Amplifier reference voltage.  |
| 16         | EN                    | I     | Amplifier enabled. Connect to logic low to shutdown; connect to logic high to activate            |

## Functional Block Diagram



### Absolute Maximum Ratings (@T<sub>A</sub> = +25°C, unless otherwise specified.)

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

| Parameter                              | Rating   | Unit |
|--|--|------|
| Supply Voltage (PV <sub>DD</sub> )     | 6.0  | V    |
| Input Voltage (INR+, INR-, INL+, INL-) | HPV <sub>SS</sub> -0.3 to HPV <sub>DD</sub> +0.3 | V    |
| Control Interface Voltage (G0, G1, EN) | -0.3 to PV <sub>DD</sub> +0.3                    | V    |
| Storage Temperature                    | -65 to +150                                      | °C   |
| Maximum Junction Temperature           | 150  |      |
| Soldering Temperature                  | 250, 10sec                                       |      |

### Recommended Operating Conditions (@T<sub>A</sub> = +25°C, unless otherwise specified.)

| Parameter                  | Rating      | Unit |
|----------------------------|-------------|------|
| Supply Voltage Range       | 2.5 to 5.5  | V    |
| Ambient Temperature Range  | -40 to +85  | °C   |
| Junction Temperature Range | -40 to +125 |      |

### Thermal Information

| Parameter                                | Symbol          | Package    | Max | Unit |
|--|-----------------|------------|-----|------|
| Thermal Resistance (Junction to Ambient) | θ <sub>JA</sub> | TQFN3x3-16 | 35  | °C/W |
| Thermal Resistance (Junction to Case)    | θ <sub>JC</sub> | TQFN3x3-16 | 14  | °C/W |

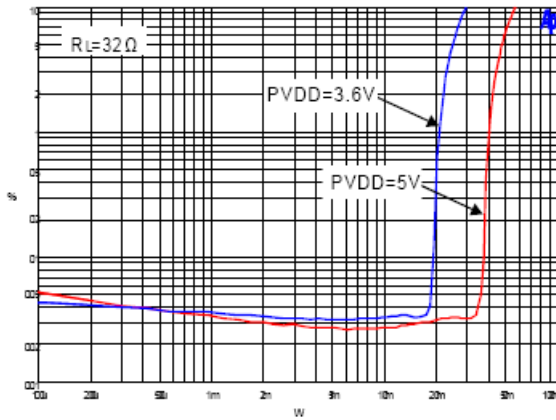
**Electrical Characteristics** (@ $T_A = +25^\circ\text{C}$ , PVDD = 3.6V, RL = 16 $\Omega$  unless otherwise specified.)

| Parameter                            | Symbol           | Test Conditions                                  | Min | Typ  | Max | Units                      |
|--------------------------------------|------------------|--|-----|------|-----|----------------------------|
| Supply Voltage                       | PVDD             |  | 2.5 |      | 5.5 | V                          |
| Quiescent Current                    | I <sub>Q</sub>   | EN = PVDD, No Load                               |     | 4    |     | mA                         |
| Output Power per Channel             | P <sub>O</sub>   | THD = 1%, f = 1kHz, R <sub>L</sub> = 16 $\Omega$ |     | 35   |     |                            |
|                                      |                  | THD = 1%, f = 1kHz, R <sub>L</sub> = 32 $\Omega$ |     | 25   |     | mW                         |
| Shutdown Current                     | I <sub>SD</sub>  | EN = 0V, PVDD = 2.5V to 5.5V                     |     | 0.1  | 1   | $\mu\text{A}$              |
| EN High Level Input Voltage          | VIH              |  | 1.4 |      |     | V                          |
| EN Low Level Input Voltage           | VIL              |  |     |      | 0.6 | V                          |
| G0, G1 High Level Input Voltage      | VGH              |  | 1.4 |      |     | V                          |
| G0, G1 Low Level Input Voltage       | VGL              |  |     |      | 0.6 | V                          |
| Output Offset Voltage                | V <sub>OS</sub>  |  |     | 1    | 5   | mV                         |
| Closed-Loop Voltage Gain             | AV               | G0 = 0V, G1 = 0V                                 |     | -6   |     | dB                         |
|                                      |                  | G0 = PVDD, G1 = 0V                               |     | 0    |     | dB                         |
|                                      |                  | G0 = 0V, G1 = PVDD                               |     | 3    |     | dB                         |
|                                      |                  | G0 = PVDD, G1 = PVDD                             |     | 6    |     | dB                         |
| Power Supply Rejection Ratio         | PSRR             | Input A C-GND, f + 1KHz, VPP = 200mV             |     | 75   |     | dB                         |
| Total Harmonic Distortion Plus Noise | THD+N            | P <sub>O</sub> = 20mW, f = 1kHz                  |     | 0.03 |     | %                          |
| Signal to Noise Ratio                | SNR              | P <sub>O</sub> = 20mW, into 16 $\Omega$          |     | 100  |     | dB                         |
| Noise Output Voltage                 | EN               | A-Weighted                                       |     | 10   |     | $\mu\text{V}_{\text{RMS}}$ |
| Crosstalk                            | CS               | PO = 15mW, f = 1kHz                              |     | 80   |     | dB                         |
| Chargepump Switching Frequency       | f <sub>OSC</sub> |  | 1.2 | 1.5  | 1.8 | MHz                        |
| Start-Up Time                        | t <sub>ON</sub>  | EN from low to high                              |     | 0.4  |     | Ms                         |
| Thermal Shutdown                     | OTP              | Threshold  |     | 150  |     | $^\circ\text{C}$           |
| Thermal Shutdown Hysteresis          | OTPH             | Hysteresis                                       |     | 20   |     | $^\circ\text{C}$           |

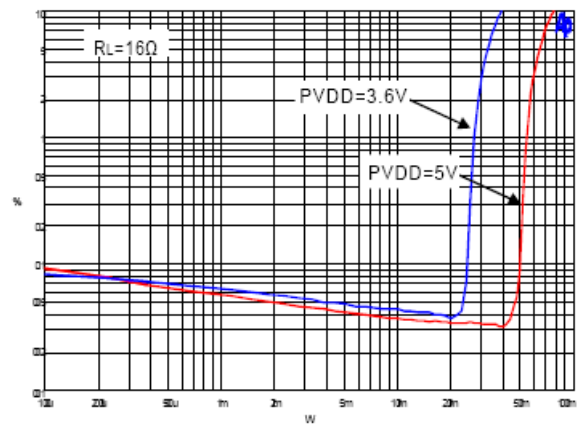
NOT RECOMMENDED FOR NEW DESIGN

**Typical Performance Characteristics** (@ $T_A = +25^\circ\text{C}$ , PVDD=3.6V,  $f = 1\text{kHz}$ , Gain = 6dB, unless otherwise specified.)

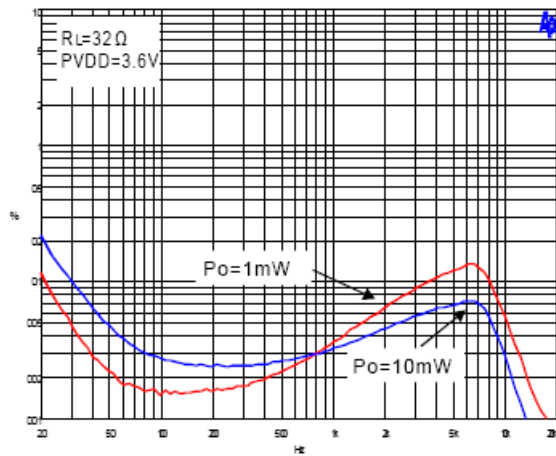
1. THD+N vs Output Power



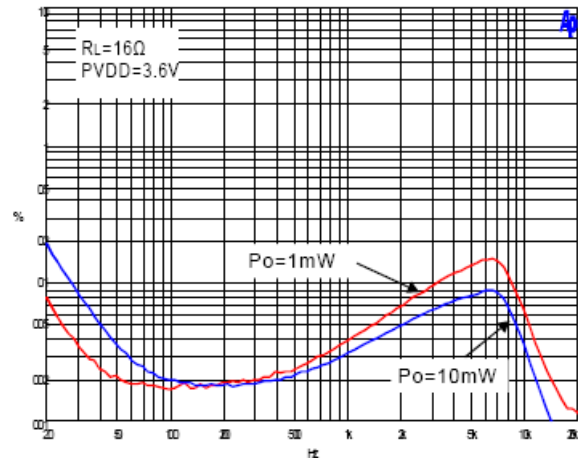
2. THD+N vs Output Power



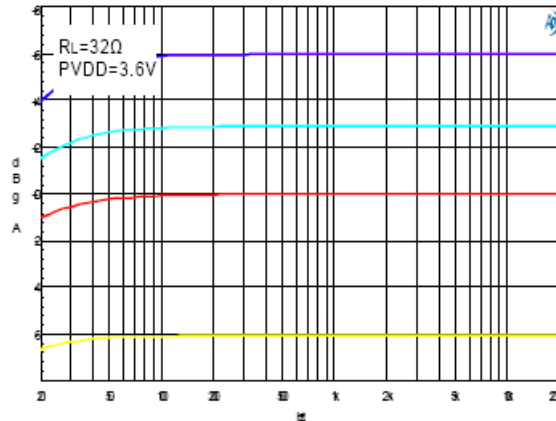
3. THD+N vs Frequency



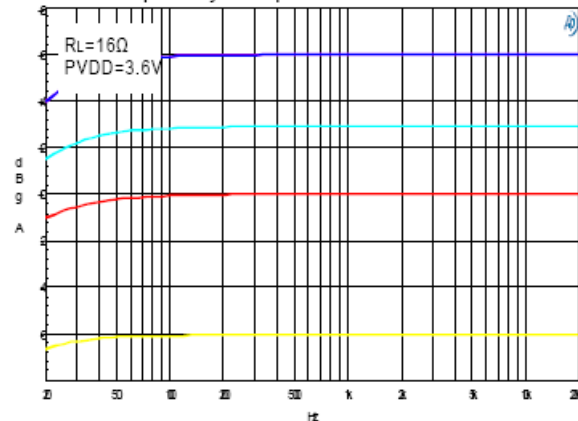
4. THD+N vs Frequency



5. Frequency Response

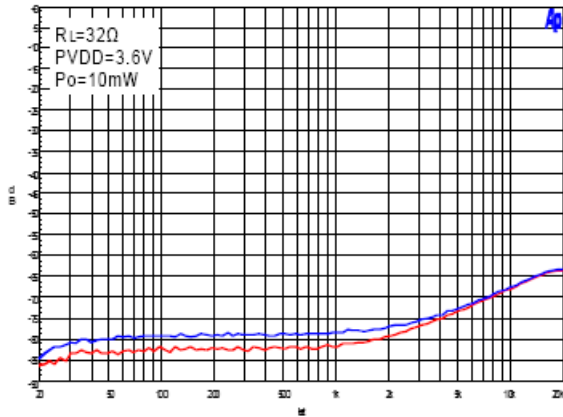


6. Frequency Response

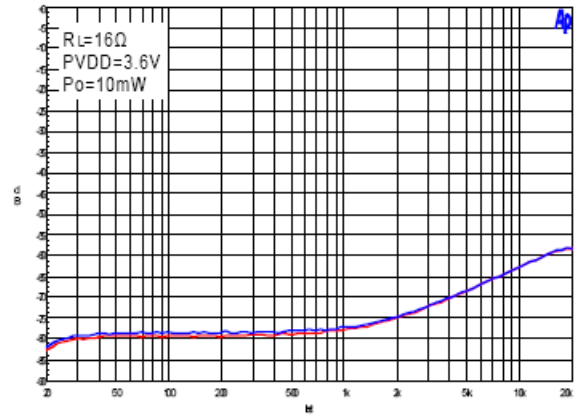


**Typical Performance Characteristics** (cont.) (@ $T_A=+25^{\circ}\text{C}$ ,  $\text{PVDD}=3.6\text{V}$ ,  $f=1\text{kHz}$ ,  $\text{Gain}=6\text{dB}$ , unless otherwise specified.)

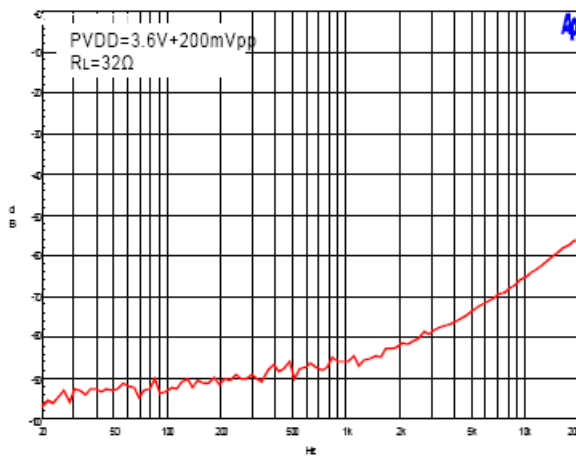
7. Crosstalk



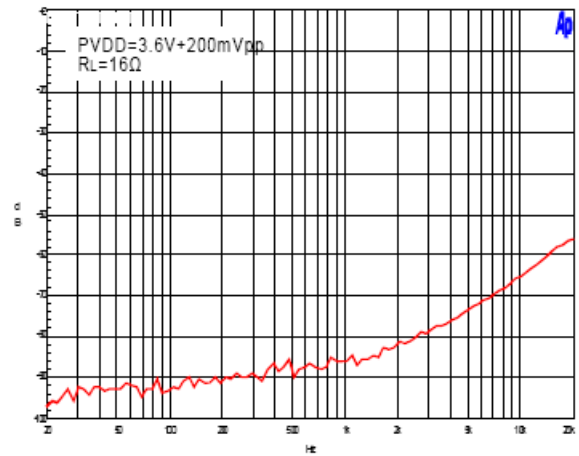
8. Crosstalk



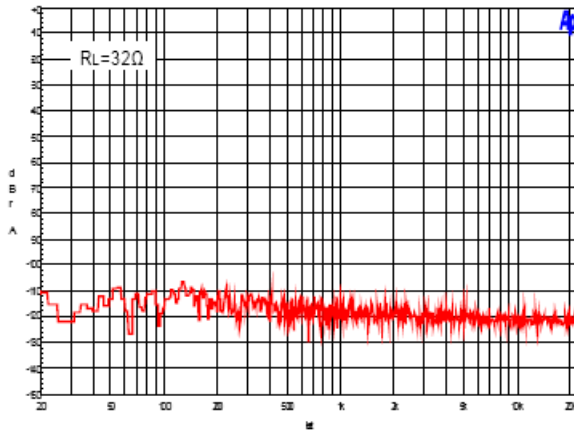
9. PSRR



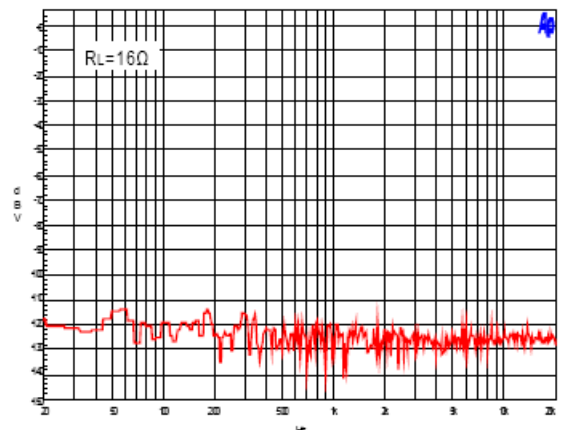
10. PSRR



11. FFT Noise

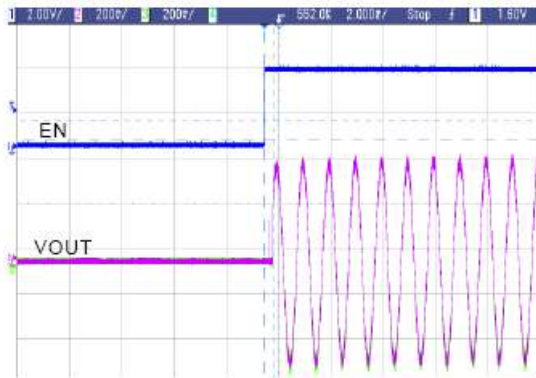


12. FFT Noise



**Typical Performance Characteristics** (cont.) (@ $T_A = +25^\circ\text{C}$ ,  $C_{IN}=10\mu\text{F}$ ,  $C_O=10\mu\text{F}$ ,  $L=4.7\mu\text{H}$ , unless otherwise specified.)

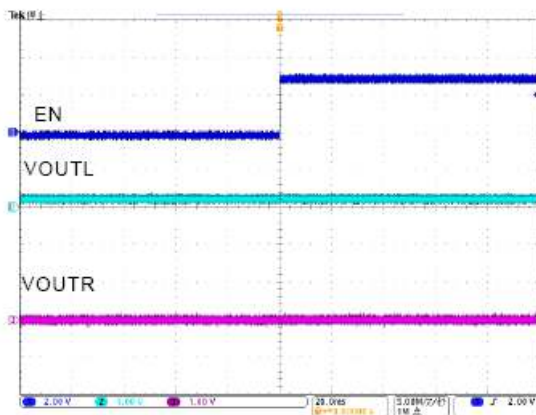
13. Start up with signal



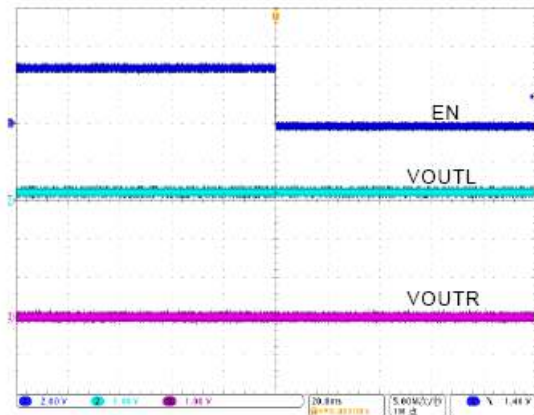
14. Shutdown with signal



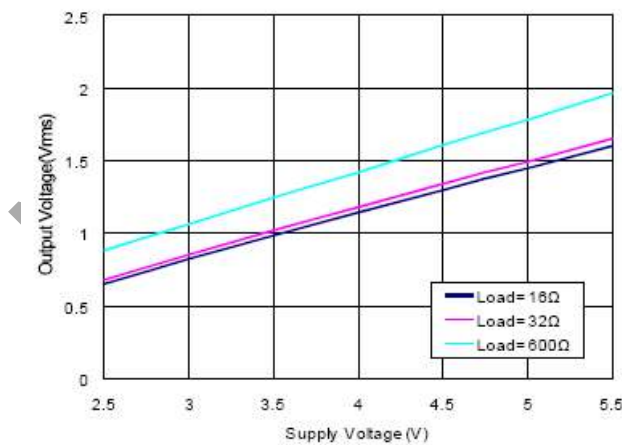
15. Start up without signal



16. Shutdown without signal



17. Output Voltage vs Supply Voltage



## Application Information

The basic PAM8901 application circuit is shown in page 1 and page 2.

### Gain Control

The PAM8901 has four gain settings which are controlled with pins G0 and G1. The following table gives an overview of the gain function.

| G0 Voltage | G1 Voltage | Amplifier Gain |
|------------|------------|----------------|
| ≤0.6V      | ≤0.6V      | -6dB           |
| ≥1.4V      | ≤0.6V      | 0dB            |
| ≤0.6V      | ≥1.4V      | 3dB            |
| ≥1.4V      | ≥1.4V      | 6dB            |

### Input Coupling Capacitors

Input coupling capacitors block any DC bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize PAM8901 turn-on pop to an inaudible level. The input capacitors are in series with PAM8901 internal input resistors, creating a high-pass filter. The following Equation calculates the highpass filter corner frequency.

$$f_c = \frac{1}{2\pi R_{IN} C_{IN}}$$

The input impedance,  $R_{IN}$ , is dependent on device gain. Larger input capacitors decrease the corner frequency. See the following table for input impedance values.

| G0 Voltage | G1 Voltage | $R_{IN}$ |
|------------|------------|----------|
| ≤0.6V      | ≤0.6V      | 26.4kΩ   |
| ≥1.4V      | ≤0.6V      | 19.8kΩ   |
| ≤0.6V      | ≥1.4V      | 16.5kΩ   |
| ≥1.4V      | ≥1.4V      | 13.2kΩ   |

For a given high-pass cutoff frequency, the minimum input coupling capacitor is found as:

$$C_{IN} = \frac{1}{2\pi f_c R_{IN}}$$

Example: Design for a 20Hz corner frequency with a PAM8901 gain of +6dB. The input impedance table gives  $R_{IN}$  as 13.2kΩ. The  $C_{IN}$  Equation shows the input coupling capacitors must be at least 0.6μF to achieve a 20Hz highpass corner frequency. Choose a 0.68μF standard value capacitor for each PAM8901 input (X5R material or better is required for best performance).

### Charge Pump Flying Capacitor, HPVDD Capacitor and HPVSS Capacitor

The PAM8901 uses a built-in charge pump to generate a positive and negative voltage supply for the headphone amplifiers. The charge pump flying capacitor connects between CAP+ and CAP-. It transfers charge to generate the positive and negative supply voltage. The HPVDD capacitor or HPVSS capacitor must be at least equal in or larger than value to the flying capacitor to allow maximum charge transfer. Use low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance) to maximize charge pump efficiency. Typical values are 1μF for the HPVDD, HPVSS and flying capacitors.

### Power Supply Decoupling Capacitors

The PAM8901 TrueCapFree headphone amplifier requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use good low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance). Place a 2.2μF capacitor within 5mm of the PVDD pin. Reducing the distance between the decoupling capacitor and PVDD minimizes parasitic inductance and resistance, improving PAM8901 supply rejection performance. Use 0402 or smaller size capacitors if possible.

### Power Supply Sequencing

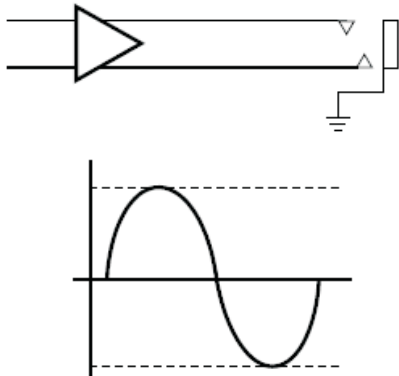
Use input coupling capacitors to ensure inaudible turn-on pop. Activate the PAM8901 after all audio sources have been activated and their output voltages have settled. On power down, deactivate the PAM8901 before deactivating the audio input source. The EN pin controls device shutdown: Set to 0.6V or lower to deactivate the PAM8901; set to 1.4V or higher to activate.



## Application Information (cont.)

### TrueCapFree Headphone Amplifiers

The TrueCapFree amplifier architecture operates from a single supply voltage and uses two internal charge pumps to generate a positive supply and a rail for the headphone amplifier. The output voltages are centered around 0V and are capable of positive and negative voltage swings as shown in the following drawing.



TrueCapFree amplifiers require no output DC-blocking capacitors. The headphone connector shield pin connects to ground and will interface with headphones and non-headphone accessories. The PAM8901 is a TrueCapFree amplifier.

### LAYOUT RECOMMENDATIONS

#### Exposed Pad on PAM8901JR

Solder the exposed metal pad on the PAM8901 TQFN package to the landing pad on the PCB. Connect the landing pad to ground or leave it electrically unconnected (floating). Do not connect the landing pad to PVDD or to any other power supply voltage. If the pad is grounded, it must be connected to the same ground as the PGND pin 9. Soldering the thermal pad is required for mechanical reliability and enhances thermal conductivity of the package.

#### GND Connections

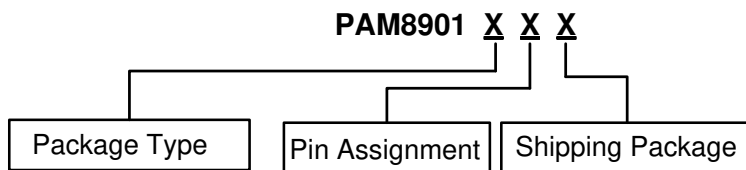
The SGND pin is an input reference and must be connected to the headphone ground connector pin. This ensures no turn-on pop and minimizes output offset voltage. Do not connect more than  $\pm 0.3V$  to SGND.

PGND is a power ground. Connect supply decoupling capacitors for PVDD, HPVDD, and HPVSS to PGND.

#### Power Supply Connections

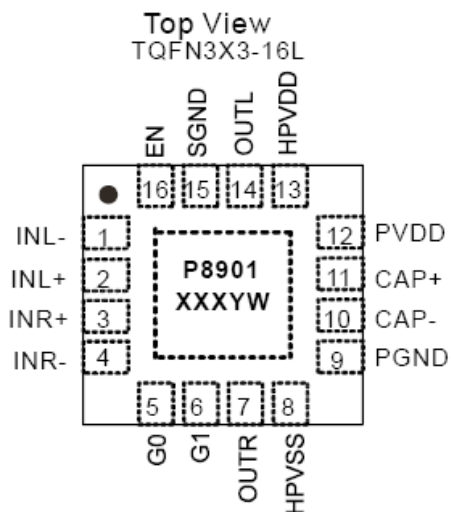
Connect the supply voltage to the PVDD pin and decouple it with an X5R or better capacitor. Place both PVDD capacitor within 5mm of PVDD pin on the PAM8901. Ensure that the ground connection of PVDD capacitor has a minimum length return path to the device. Failure to properly decouple the PAM8901 may degrade audio or EMC performance.

**Ordering Information**



| Part Number | Package Type | Standard Package        |
|-------------|--------------|-------------------------|
| PAM8901JER  | TQFN3x3-16L  | 3000 Units/ Tape & Reel |

**Marking Information**

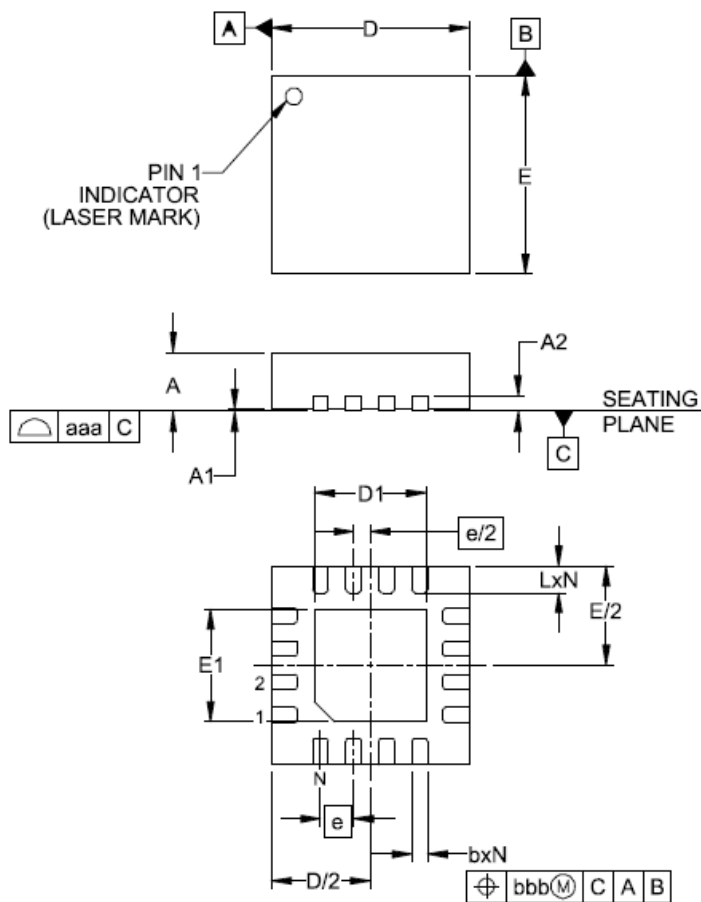


X: Internal Code  
Y: Year  
W: Week

NOT FOR M/L

**Package Outline Dimensions** (All dimensions in mm.)

TQFN3x3mm-16



| DIMENSIONS (Millimeters) |         |      |      |
|--------------------------|---------|------|------|
|                          | MIN     | TYP  | MAX  |
| A                        | 0.40    | 0.50 | 0.60 |
| A1                       | 0.00    | 0.02 | 0.05 |
| A2                       | 0.20    |      |      |
| b                        | 0.18    | 0.25 | 0.30 |
| D                        | 2.90    | 3.00 | 3.10 |
| D1                       | 1.55    | 1.70 | 1.80 |
| E                        | 2.90    | 3.00 | 3.10 |
| E1                       | 1.55    | 1.70 | 1.80 |
| e                        | 0.50BSC |      |      |
| L                        | 0.30    | 0.40 | 0.50 |
| N                        | 16      |      |      |
| aaa                      | 0.08    |      |      |
| bbb                      | 0.10    |      |      |

- Notes:
1. Controlling dimensions are in millimeters (angles in degrees).
  2. Coplanarity applies to the exposed pad as well as the terminals.
  3. DAP is 1.90 x 1.90mm.

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