TPS40021EVM−001 High-Efficiency Synchronous Buck Converter with PWM Controller Evaluation Module (HPA009)

Sophie Chen *System Power*

Contents

1 Introduction

The TPS4002x family of devices are low-input voltage synchronous, voltage-mode buck controllers. Built upon the TPS40000 products, the TPS4002x family provides enhanced operation and design flexibility through user programmability. The uses of the predictive gate drive and charge pump/boost circuits combine to provide a highly efficient, smaller and less expensive converter. It can be widely used in networking equipment, servers, base stations, DSP power, and telecommunication applications. The datasheet describes the functionalities of the controller in more detail. This User's Guide describes the TPS40021EVM−001 evaluation module (HPA009), a step-down application from 3.3 V to 1.5 V with the TPS400021 PWM controller.

A schematic of the evaluation module is shown in Figure 1. A recommended parts list is provided in Table 1. The layout of the PCB board is shown in Figure 9.

The specification of this evaluation module is as follows:

- Input voltage: $2.5\ V \le V_{IN} \le 5.0\ V$
- Nominal voltage: 3.3 V
- Output voltage V_{OUT}: 1.5 V
- Output current I_{OUT}: 20 A
- Switching frequency: 300 kHz

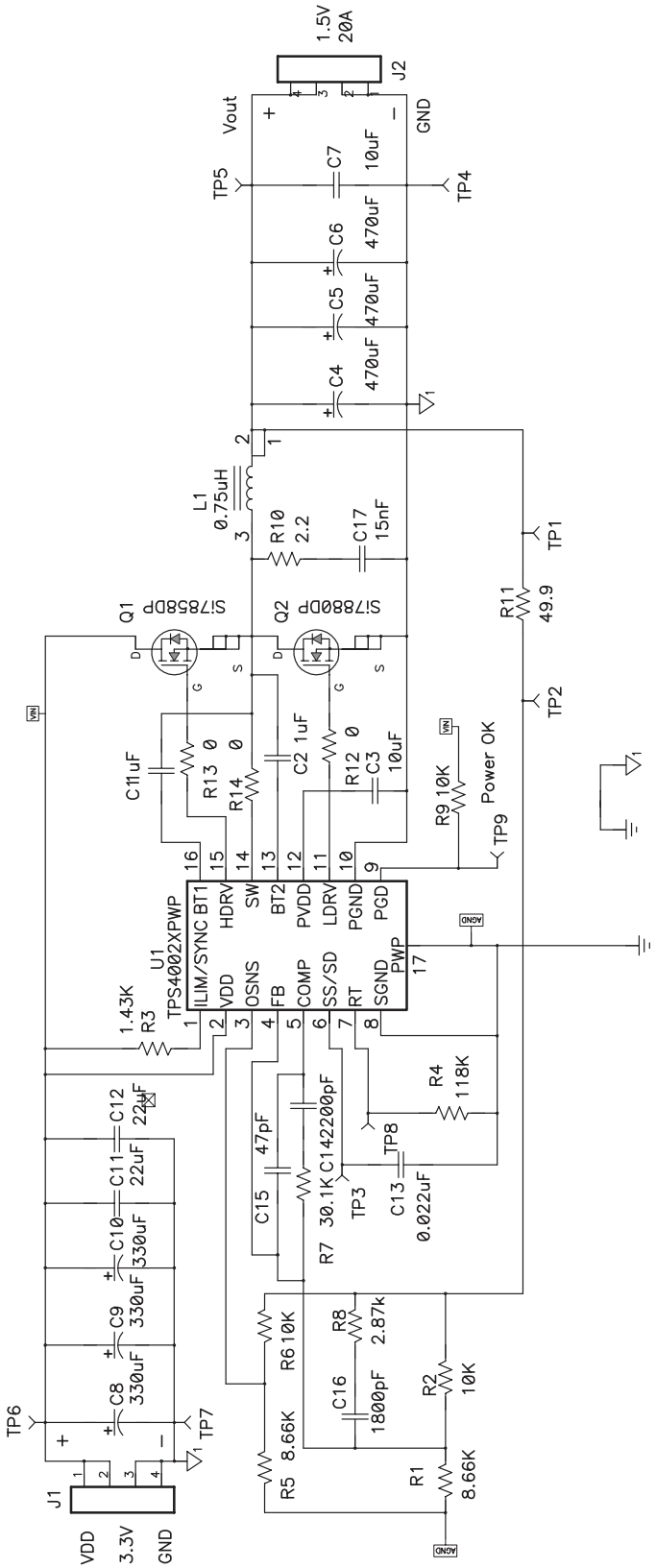

Figure 1. HPA009 Schematic

2 Design Procedure

2.1 Frequency Setting

Choosing the switching frequency demands a trade-off. The higher the frequency, the smaller the inductance and capacitance needed, so the smaller the size, but then the switching losses are higher, and efficiency is poorer. For this evaluation module, 300 kHz is chosen for reasonable efficiency and size.

A resistor R4, which is connected from pin 7 to ground, programs the oscillator frequency. The approximate operating frequency is calculated in equation (1).

$$\text{R4 (k}\Omega) = = \frac{35.4}{f_{OSC}\,(\text{MHz})} \approx 118\ \text{k}\Omega \tag{1}$$

Therefore, a 118-kΩ resistor is chosen for 300 kHz operation.

2.2 Inductance Value

The inductance value can be calculated by equation (2).

$$L_{(min)} = \frac{V_{OUT}}{f \times I_{RIPPLE}} \times \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) \tag{2}$$

where I_{RIPPLE} is the ripple current flowing through the inductor, which affects the output voltage ripple and core losses.

Based on 20% ripple current and 300 kHz, the inductance value is calculated to 0.76 µH and a 0.75-µH inductor (part number is CDEP149−0R7) is chosen. The ESR of this inductor is 1.1 mΩ and the loss is 440 mW, which is approximately 1.5% of output power.

2.3 Input and Output Capacitors

The output capacitance and its ESR needed are calculated in equations (3) and (4).

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} \tag{3}$$

$$ESR_{OUT} = \frac{V_{RIPPLE}}{I_{RIPPLE}} \tag{4}$$

With 1% output voltage ripple, the needed capacitance is at least 114 µF and its ESR should be less than 3.7 mΩ. Three 2.5-V, 470-µF, POSCAP capacitors from Sanyo are used. The ESR is 10 mΩ each.

The required input capacitance is calculated in equation (5). The calculated value is approximately 348 µF. Three 6.3-V, 330-µF POSCAP capacitors with 10 mΩ ESR are used to handle 10 A of RMS input current. Additionally, two ceramic capacitors are used to reduce the switching ripple current.

$$C_{IN(min)} = I_{OUT(max)} \times D_{(max)} \times \frac{T_S}{V_{RIPPLE}} \tag{5}$$

2.4 Compensation Design

Voltage-mode control is used in this evaluation module, using R2, R7, R8, C14, C15, and C16 to form a Type-III compensation network. The L-C frequency of the power stage is approximately 4.9-kHz and the ESR-zero is around 34 kHz. The overall crossover frequency, f_{0db}, is chosen at 43-kHz for reasonable transient response and stability. Two zeros f_{Z1} and f_{Z2} from the compensator are set at 2.4 kHz and 4 kHz. The two poles, f_{P1} and f_{P2} are set at 34 kHz and 115 kHz. The frequency of poles and zeros are defined by the following equations:

$$f_{Z1} = \frac{1}{2\pi \times R7 \times C14} \tag{6}$$

$$f_{Z2} = \frac{1}{2\pi \times R2 \times C11} \quad \text{(assuming R2} \gg \text{R8)} \tag{7}$$

$$f_{P1} = \frac{1}{2\pi \times R8 \times C11} \tag{8}$$

$$f_{P2} = \frac{1}{2\pi \times R7 \times C12} \quad \text{(assuming C14} \gg \text{C12)} \tag{9}$$

The transfer function for the compensator is calculated in equation (10).

$$A(s) = \frac{(1 + s \times C14 \times R7) \times [1 + s \times C11 \times (R2 + R3)]}{s \times R2 \times C14 \times \left[\left(1 + \frac{C12}{C14}\right) + s \times R7 \times C12\right] \times (1 + s \times R8 \times C11)} \tag{10}$$

Figure 3 shows the close loop gain and phase. The overall crossover frequency is approximately 30 kHz. The phase margin is 57°.

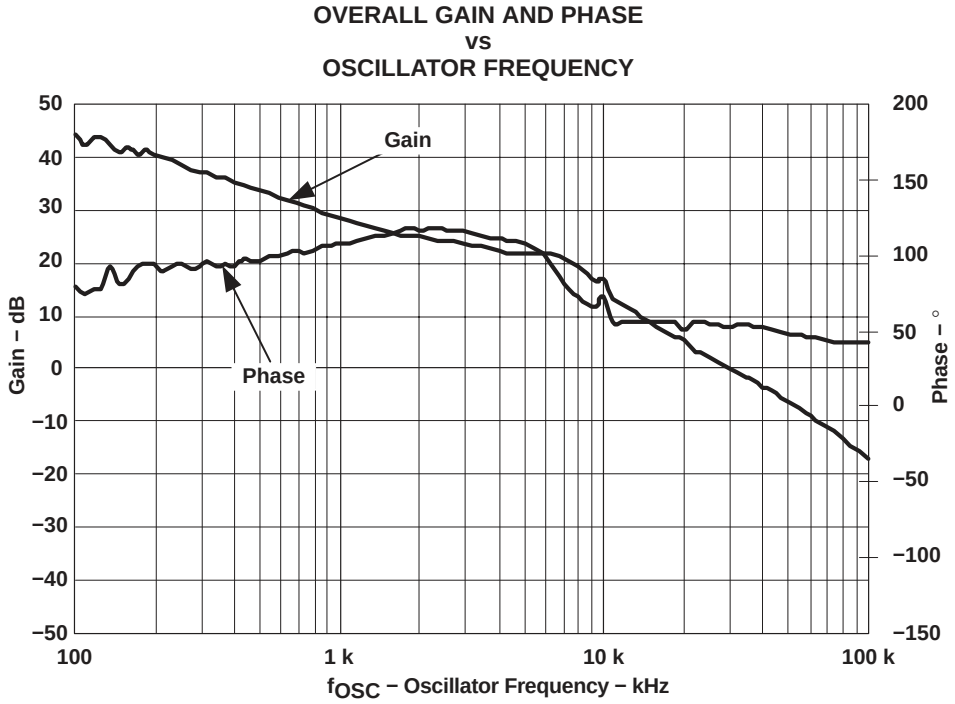

Figure 2.

2.5 MOSFETs and Diode

For a 1.5-V output voltage, the lower the $R_{DS(on)}$ of the MOSFET, the higher the efficiency. Due to the high current and high conduction loss, the MOSFET should have very low conduction resistance ($R_{DS(on)}$) and thermal resistance. Si7858DP is chosen for its low $R_{DS(on)}$ (between 3 mΩ and 4 mΩ) and Power-Pak package.

2.6 Current Limiting

Resistor R3 sets the over current limit threshold. The $R_{DS(on)}$ of the upper MOSFET is used as a current sensor. The current limit is initialized at 40% above the maximum output current, $I_{OUT(max)}$, which is 28 A. Then R3 can be calculated in equation (11) and yields a value of 1.43 kΩ.

$$I_{LIM} = \left(20 \times \frac{V_{REF}}{R4}\right) = \left(20 \times \frac{0.7\ V}{118\ k\Omega}\right) = 118.6\ (\mu A) \tag{11}$$

$$R3 = \frac{K \times R_{DS(on)} \times I_{OUT}}{I_{LIM}\ (\mu A)} = \frac{1.5 \times 4\ (m\Omega) \times 28\ A}{I_{LIM}\ (\mu A)} = 1.43\ (k\Omega) \tag{12}$$

where

- $R_{DS(on)}$ is the on-resistance of Q1 (4 mΩ)
- Temperature coefficient, K=1.5
- V_{REF}=0.7 V
- R4=118 kΩ

2.7 Voltage Sense Regulator

R1 and R2 operate as the output voltage divider. The internal reference voltage (V_{REF}) is 0.7 V. The relationship between the output voltage and divider is described in equation (8). Using a 10-kΩ resistor for R2 and 1.5-V output regulation, R1 is calculated as 8.66 kΩ.

$$\frac{V_{REF}}{R1} = \frac{V_{OUT}}{R1 + R2} \rightarrow \frac{0.7\ V}{R1} = \frac{1.5\ V}{R1 + 10\ k\Omega} \rightarrow R1 = 8.66\ k\Omega \tag{13}$$

2.8 Transient Comparator

The output voltage transient comparators provide a quick response, first strike, approach to output voltage transients. The output voltage is sensed through a resistor divider at the OSNS pin, using R5 and R6 shown in Figure 2. If an overvoltage condition is detected, the HDRV gate drive is shut off and the LDRV gate drive is turned on until the output is returned to regulation. Similarly, if an output undervoltage condition is sensed, the HDRV gate drive goes to 95% duty cycle to pump the output back up quickly. The voltage divider should keep same ratio as the output voltage sensor for the PWM comparator. Resistor R5=8.66 kΩ and R6=10 kΩ in this evaluation module.

3 Test Results

3.1 Efficiency Curves

The tested efficiency at different loads and input voltages are shown in Figure 3. The maximum efficiency is as high as 92.4% at 1.5-V output. The efficiency is around 87.7% when the load current (I_{LOAD}) is 20 A.

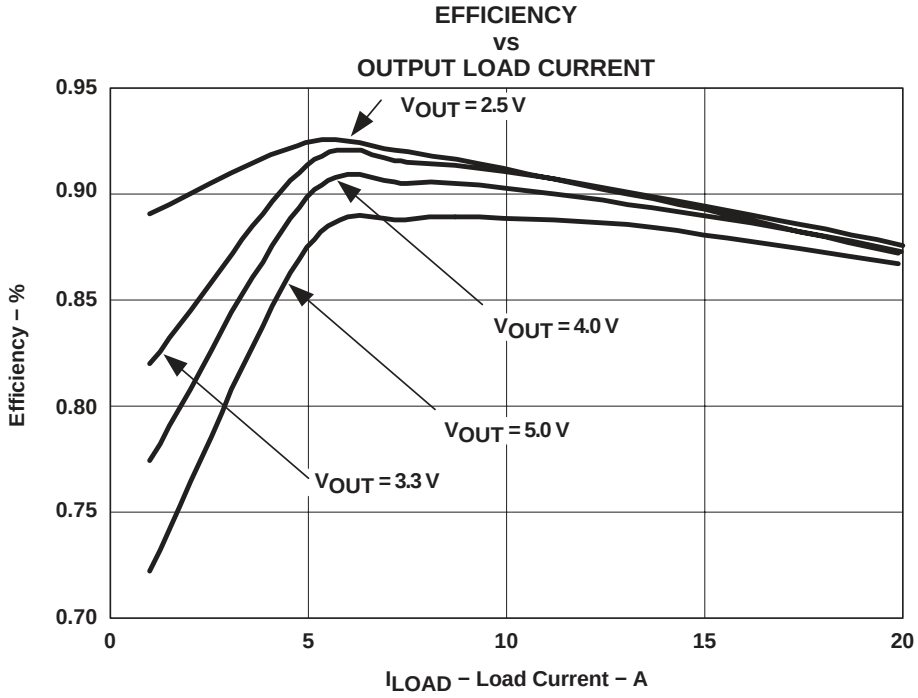

Figure 3.

3.2 Typical Operation Waveform

Typical operating waveforms are shown in Figure 4.

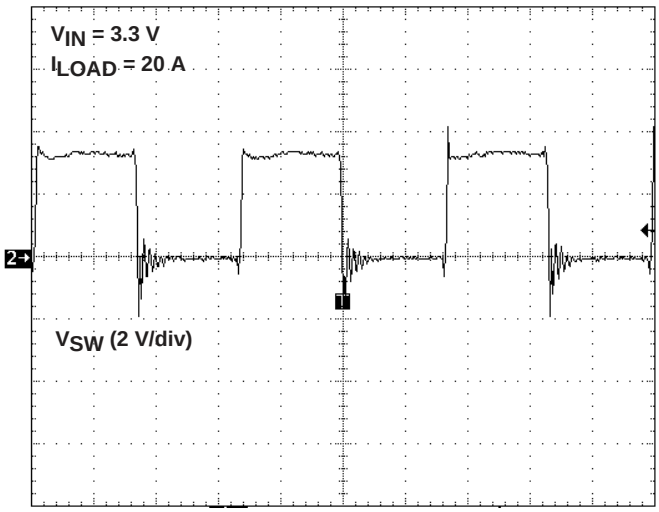

Figure 4. Switch Node Waveform

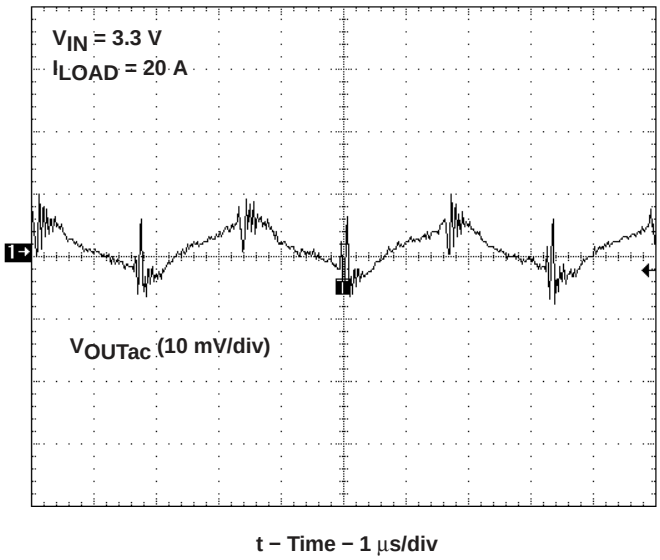

Figure 5. Output Ripple

3.3 Transient Response and Output Ripple Voltage

The output ripple is about 15 mV_{P-P} at 20-A output which is shown in Figure 5. When the load changes from 0 A to 13 A, the overshoot voltage is approximately 80 mV, and the undershoot is is approximately 60 mV as shown in Figure 6. When the transient comparator is triggered, the powergood (PG) signal goes low.

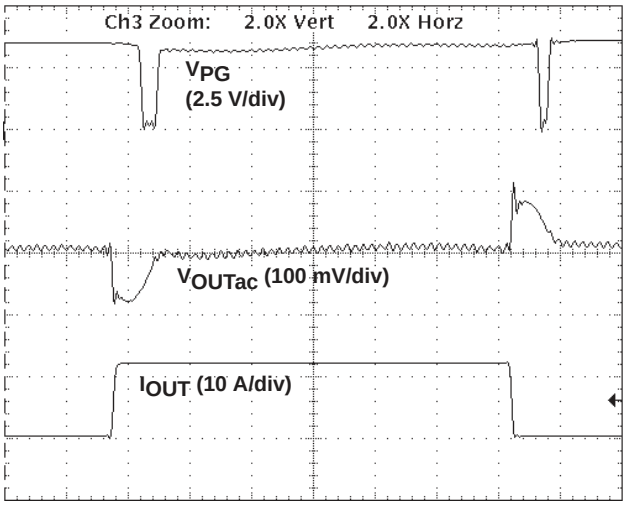

Figure 6. Transient Response

Figures 7 and 8 show the transient waveform with and without the transient comparator. Using the transient comparator yields a settling time of 10-µs faster than without.

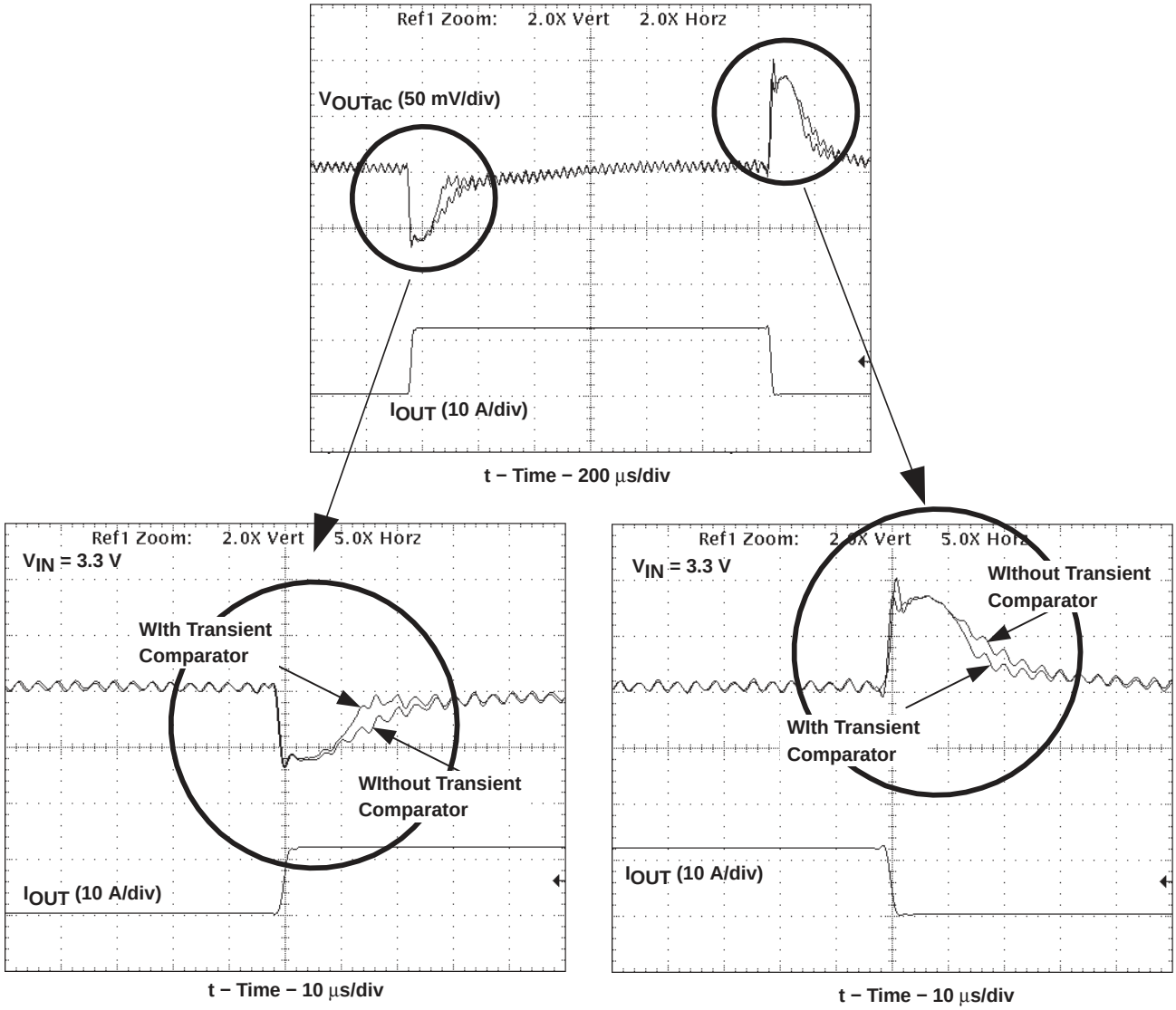

Figure 7. Transient Response Undershoot

Figure 8. Transient Response Overshoot

4 PCB Layout

Figures 7 through 11, shows the parts placement and the PCB layout of the evaluation board. All the components are on the top side of the board. The bottom side of the board is the ground plane. The PWB is made large to dissipate the losses.

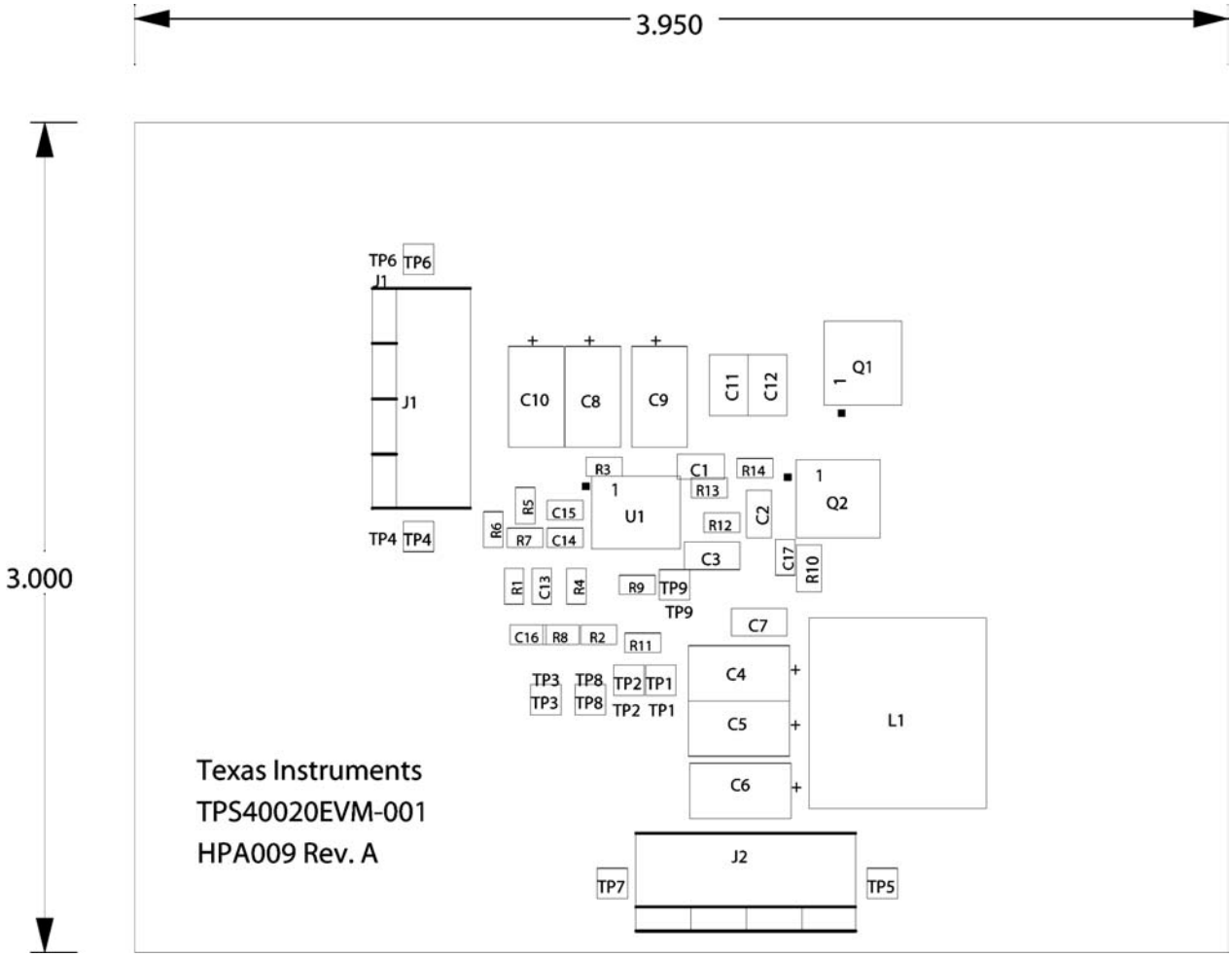

Figure 9. Parts Placement

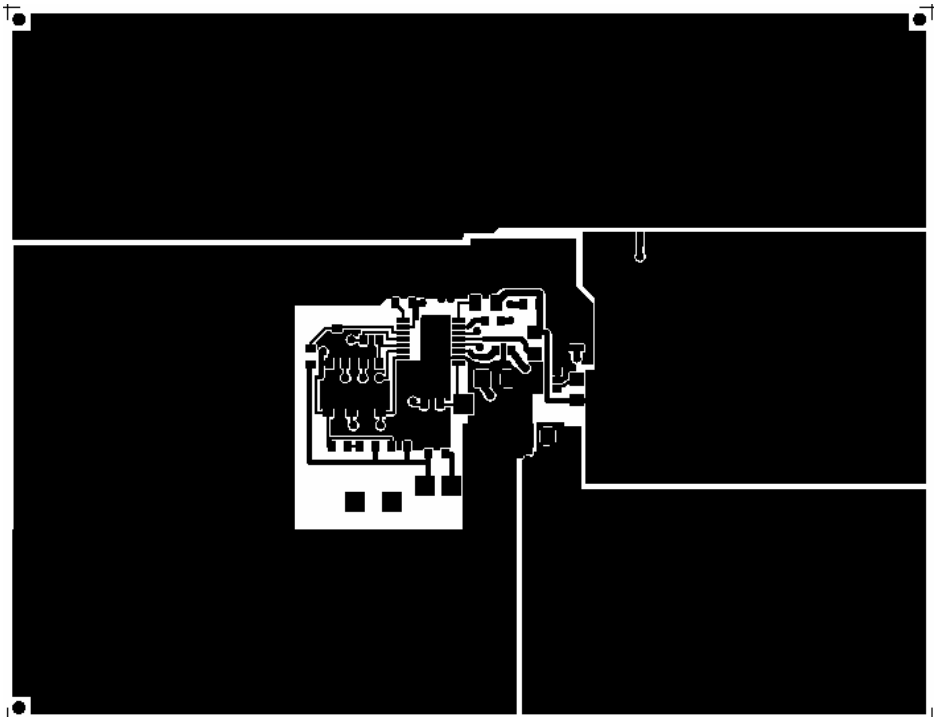

Figure 10. Top Layer

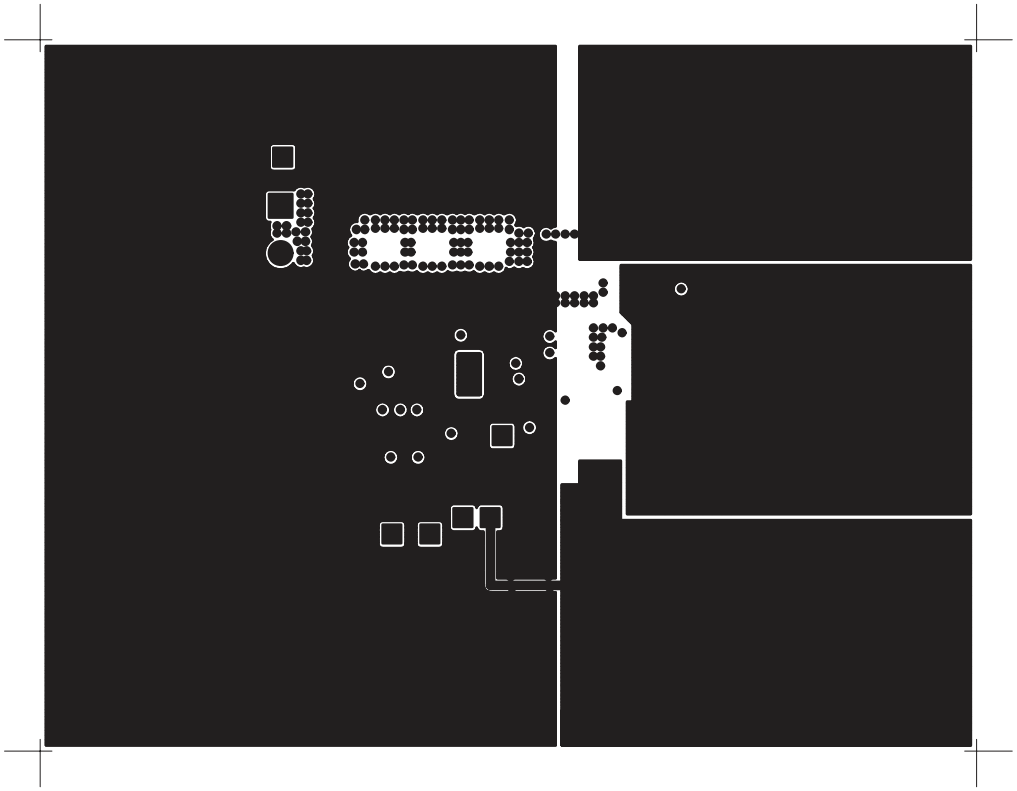

Figure 11. Layer 2

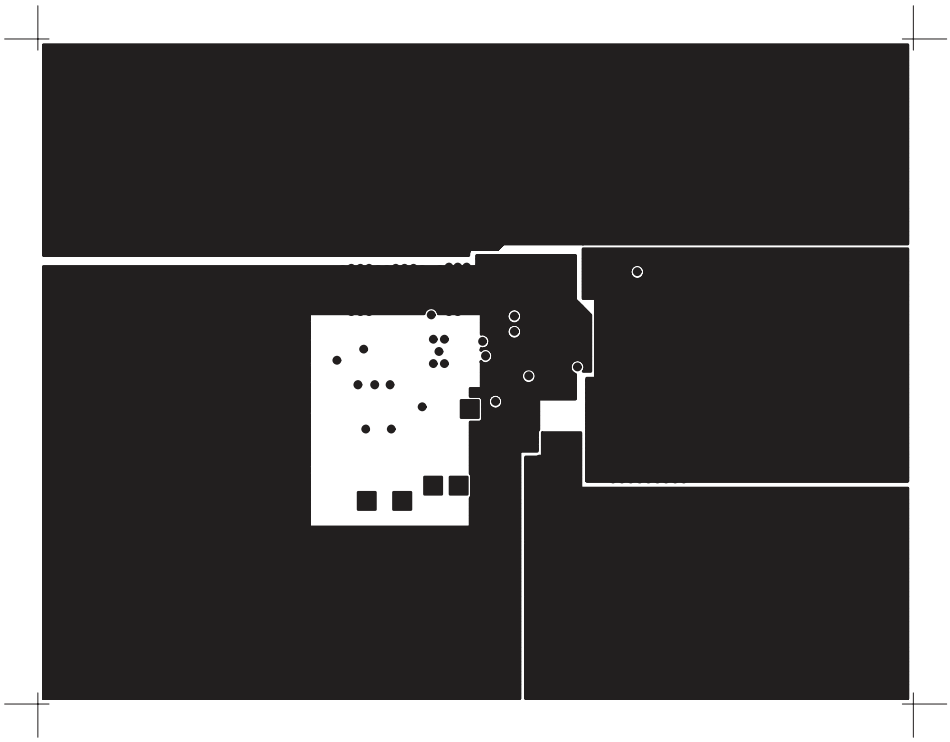

Figure 12. Layer 3

Figure 13. Bottom Layer

5 List of Materials

Table 1 lists the parts values of the evaluation board. These values can be modified to meet the application requirements.

Table 1. HPA009 List of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	SIZE	MFR	PART NUMBER
C1, C2	2	Capacitor, ceramic, 1 μF, 10 V, X7R,10%	805	Taiyo Yuden	LMK212BJ105KD
C11, C12	2	Capacitor, ceramic, 22 μF, 6.3−V, 20%	1210	Taiyo Yuden	JMK325BJ226MM
C13	1	Capacitor, ceramic, 0.022 μF, X7R 25−V, 5%	603	Vishay	VJ0603Y223JXXAT
C14	1	Capacitor, ceramic, 2200 pF, X7R, 25−V, 5%	603	Vishay	VJ0603Y222JXXAT
C15	1	Capacitor, ceramic, 47 pF, 50−V, 2%	603	Vishay	VJ0603A470GXAAT
C16	1	Capacitor, ceramic, 1800 pF, X7R, 25−V, 5%	603	Vishay	VJ0603Y822JXXAT
C3, C7	2	Capacitor, ceramic, 10 μF, 6.3 V, 20%	1206	Taiyo Yuden	JMK316BJ106ML
C4, C5, C6	3	Capacitor, POSCAP, 470 μF, 2.5 V, 10 mΩ, 20%	7343 (D)	Sanyo	2R5TPD470M
C8, C9, C10	3	Capacitor, POSCAP, 330-μF, 6.3−V,10 mΩ, 20%	7343 (D)	Sanyo	6TPD330M
C17	1	Capacitor, ceramic, 15 nF, X7R, 25 V, 5%	603	Vishay	VJ0603153KXXAT
J1, J2	2	Terminal block, 4-pin, 15 A, 5.1 mm	0.80 × 0.35	OST	ED2227
L1	1	Inductor, SMT, 0.75 μH, 24 A, 1.1 mΩ	0.598 × 0.638	Sumida	CDEP149−0R7
Q1	1	MOSFET, N-channel, 12 V, 29 A, 3 mΩ	PowerPak-SO8	Siliconix	Si7858DP
Q2	1	MOSFET, N-channel, 30 V, 29 A, 3 mΩ		Siliconix	Si7880DP
R1, R5	2	Resistor, chip, 8.66 kΩ, 1/16 W, 1%	603	Std	Standard
R2, R6	2	Resistor, chip, 10 kΩ, 1/16 W, 1%	603	Std	Standard
R3	1	Resistor, chip, 1.43 kΩ, 1/16 W, 1%	603	Std	Standard
R4	1	Resistor, chip, 118 kΩ, 1/16 W, 1%	603	Std	Standard
R7	1	Resistor, chip, 30.1 kΩ, , 1/16 W, 1%	603	Std	Standard
R8	1	Resistor, chip, 2.87 kΩ, 1/16 W, 1%	603	Std	Standard
R9	1	Resistor, chip, 10 kΩ, 1/16 W, 1%	603	Std	Standard
R10	1	Resistor, chip, 2.2 Ω, 1/16 W, 1%	805	Std	Standard
R11	1	Resistor, chip, 49.9 Ω, 1/16 W, 1%	603	Std	Standard
R12	1	Resistor, chip, 4.7 Ω, 1/16 W, 1%	603	Std	Standard
U1(1)	1	Enhanced, low input voltage−mode, synchronous buck controller	HTSSOP−16	TI	TPS40021PWP

(1) May not be substituted.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265