

# MOSFET

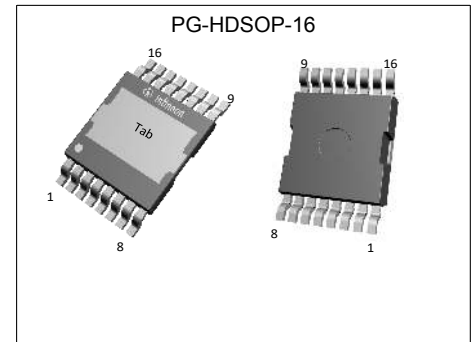
## OptiMOS™ 5 Power-Transistor, 150 V

### Features

- N-channel, normal level
- Very low on-resistance  $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

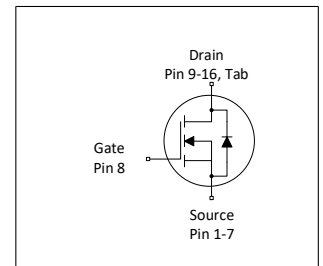
### Product validation

Fully qualified according to JEDEC for Industrial Applications



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	150	V
$R_{DS(on),max}$	4.4	$m\Omega$
$I_D$	174	A
$Q_{oss}$	200	nC
$Q_G$	71	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
IPTC044N15NM5	PG-HDSOP-16	044N15N5	-

## Table of Contents

Description .....	1
Maximum ratings .....	3
Thermal characteristics .....	3
Electrical characteristics .....	4
Electrical characteristics diagrams .....	6
Package Outlines .....	10
Revision History .....	13
Trademarks .....	13
Disclaimer .....	13

## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	174 123 115 19.4	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=8\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=40\text{ °C/W}^2)$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	696	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	321	mJ	$I_D=100\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	300 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=40\text{ °C/W}^2)$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.5	°C/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>2)</sup>	$R_{thJA}$	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimum footprint	$R_{thJA}$	-	-	62	°C/W	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3.0	3.8	4.6	V	$V_{DS}=V_{GS}$ , $I_D=235\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1.0 100	$\mu\text{A}$	$V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	3.7 4.0	4.4 5.0	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ $V_{GS}=8\text{ V}$ , $I_D=25\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	0.9	1.3	$\Omega$	-
Transconductance	$g_{fs}$	-	110	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$ , $I_D=50\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	5400	7000	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	1300	1950	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	30	53	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	17	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	5.0	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	25	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	6.5	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	29	-	nC	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	20	-	nC	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	14	21	nC	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	23	-	nC	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	71	89	nC	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=75\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	200	266	nC	$V_{DS}=75\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	174	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	696	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.82	1.0	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	45	91	ns	$V_R=75\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	49	98	nC	$V_R=75\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test.

### 4 Electrical characteristics diagrams

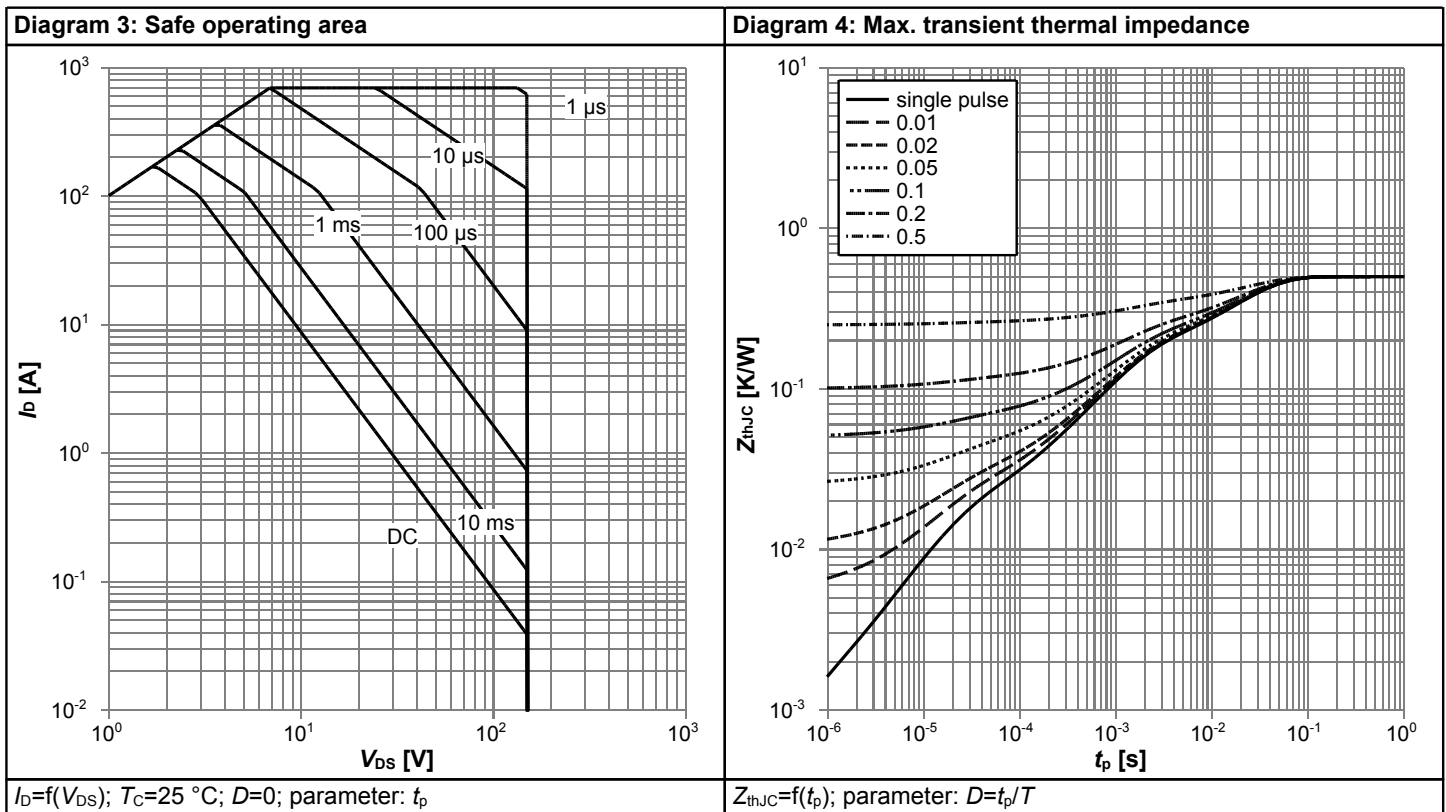
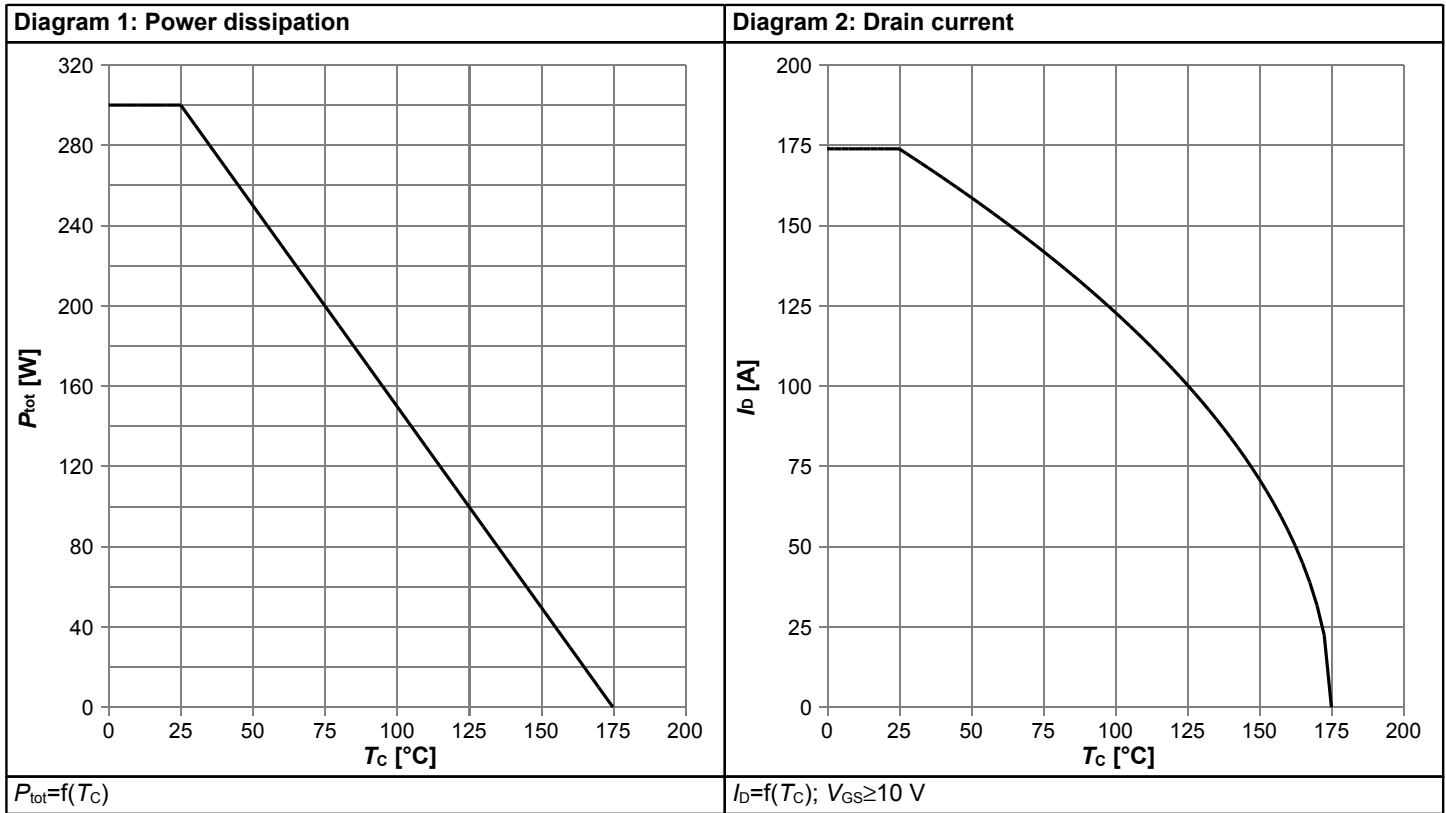
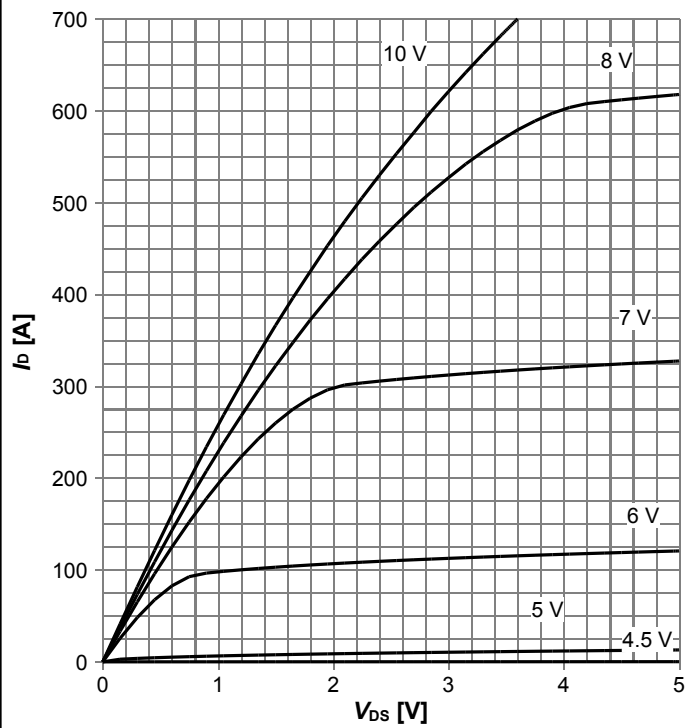
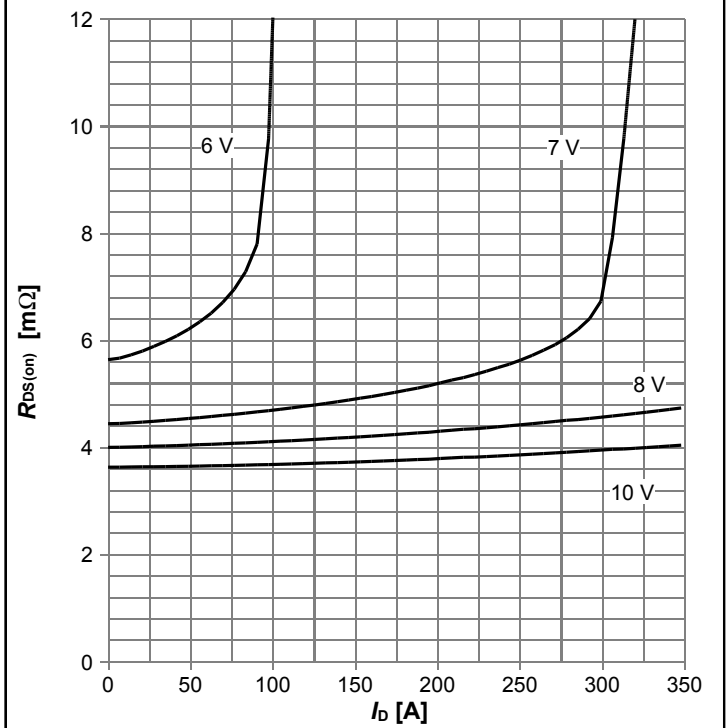


Diagram 5: Typ. output characteristics



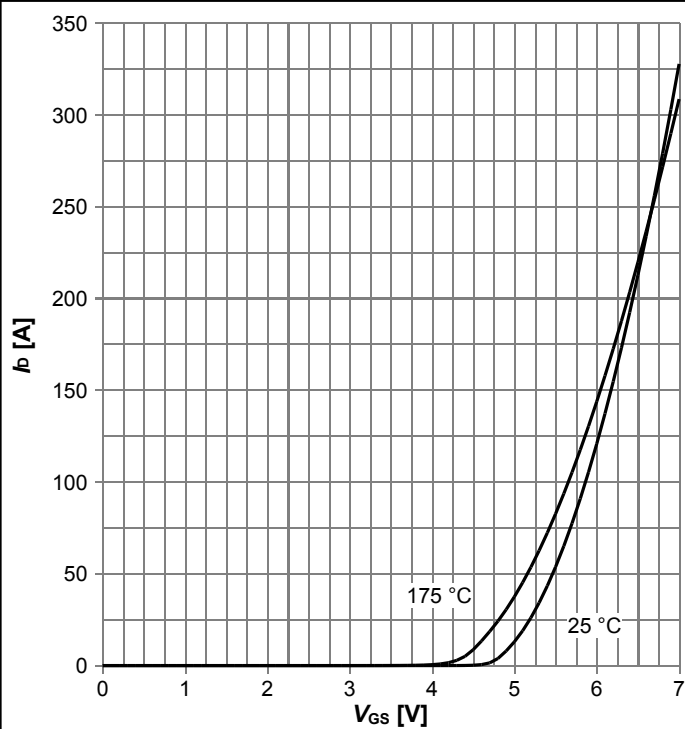
$I_D = f(V_{DS})$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



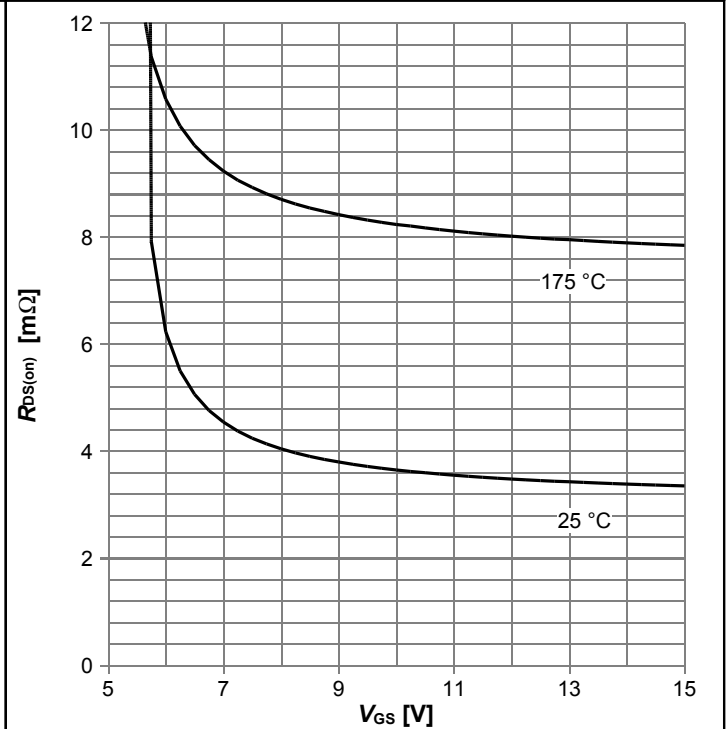
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



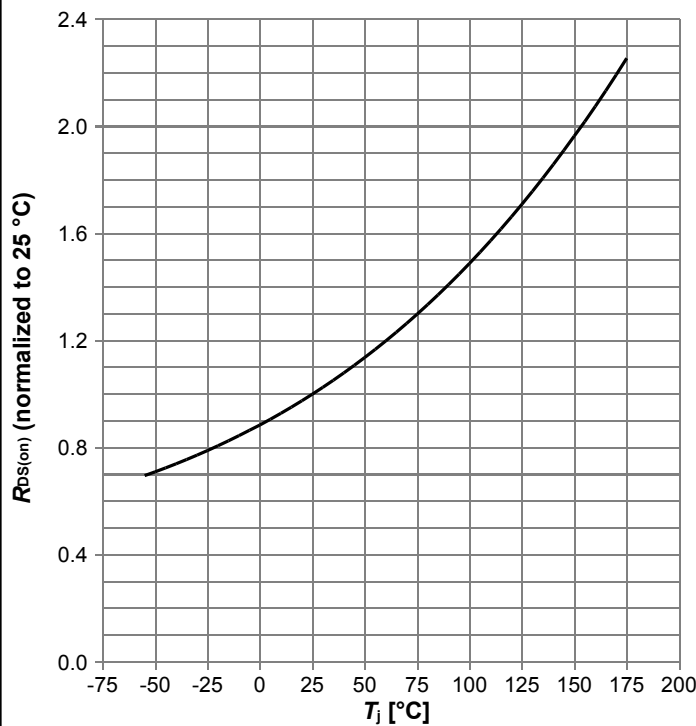
$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

Diagram 8: Typ. drain-source on resistance



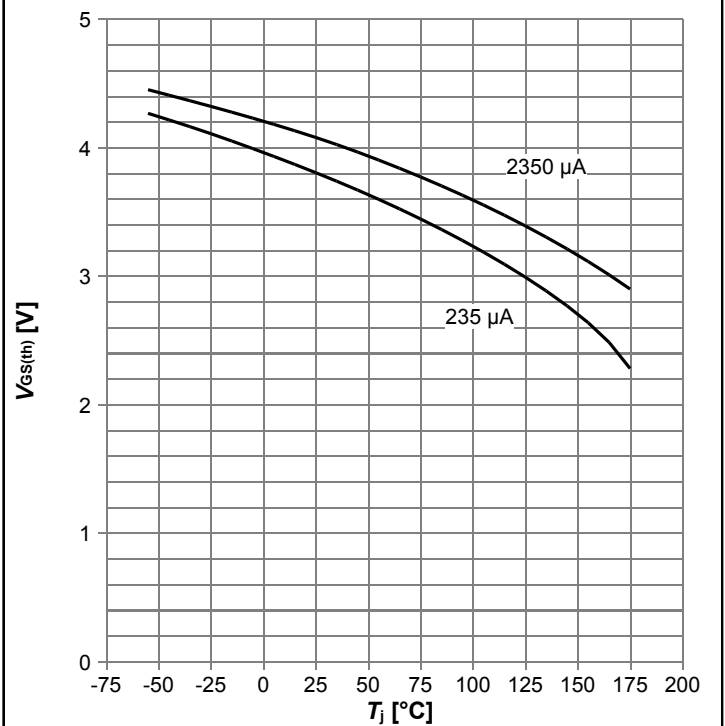
$R_{DS(on)} = f(V_{GS})$ ,  $I_D = 50\text{ A}$ ; parameter:  $T_j$

Diagram 9: Normalized drain-source on resistance



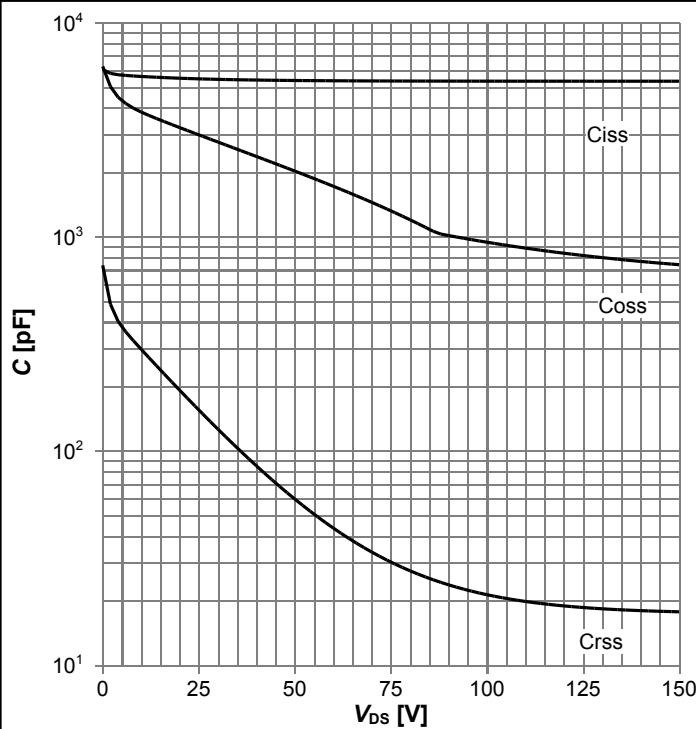
$R_{DS(on)}=f(T_j)$ ,  $I_D=50$  A,  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



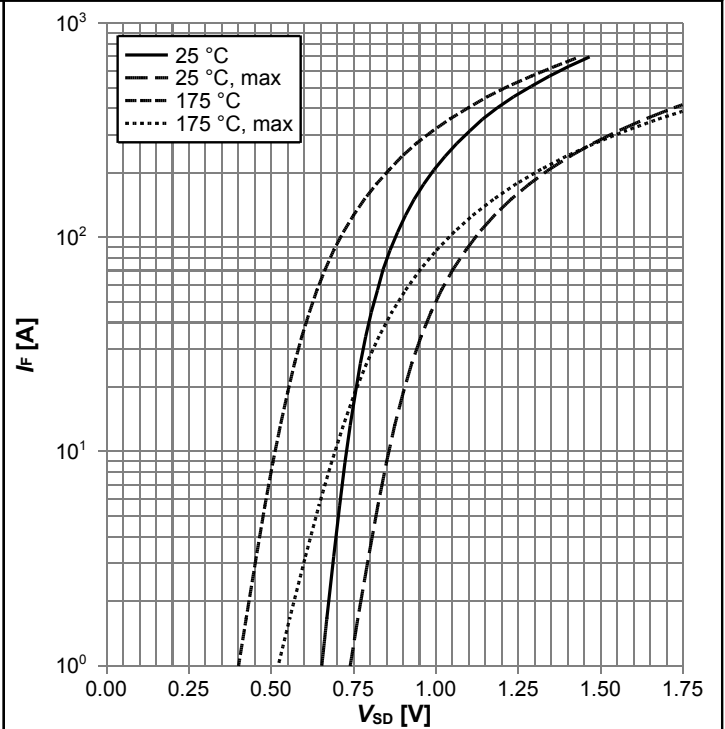
$V_{GS(th)}=f(T_j)$ ,  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

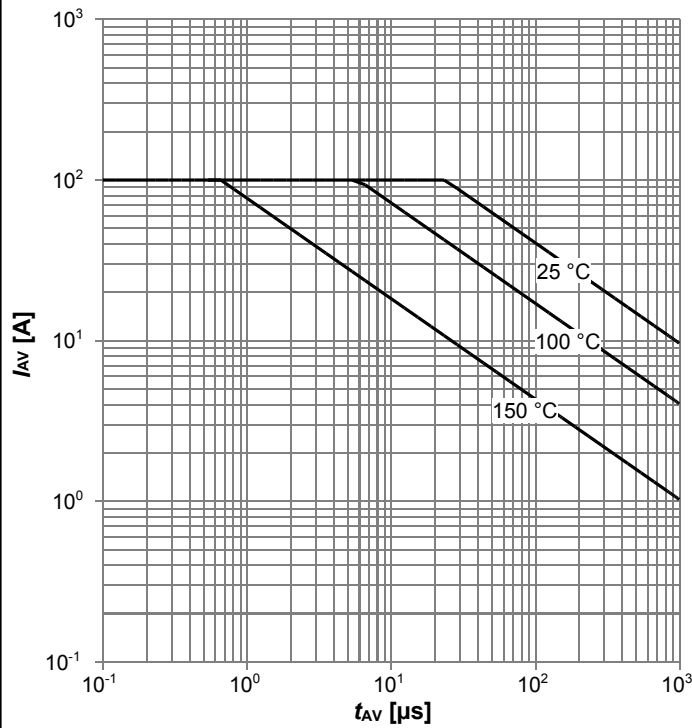
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

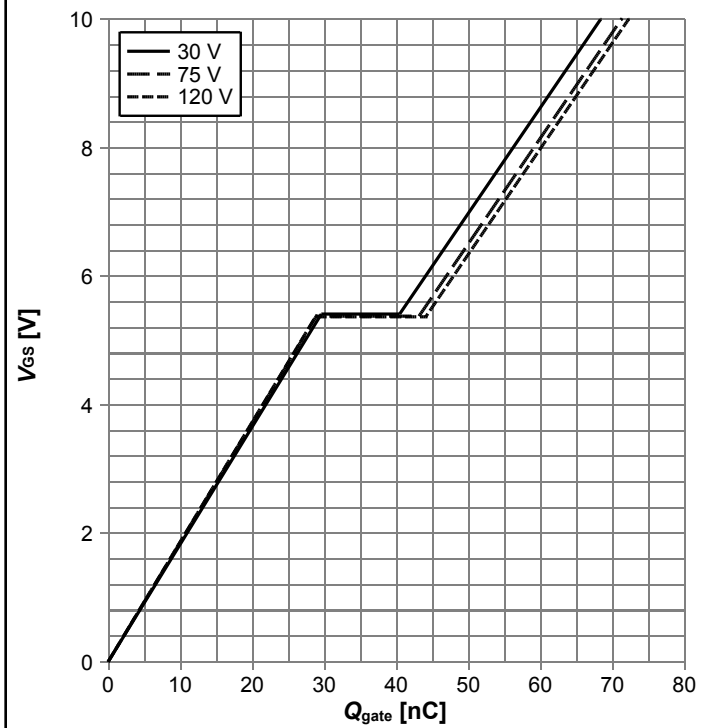


Diagram 13: Avalanche characteristics



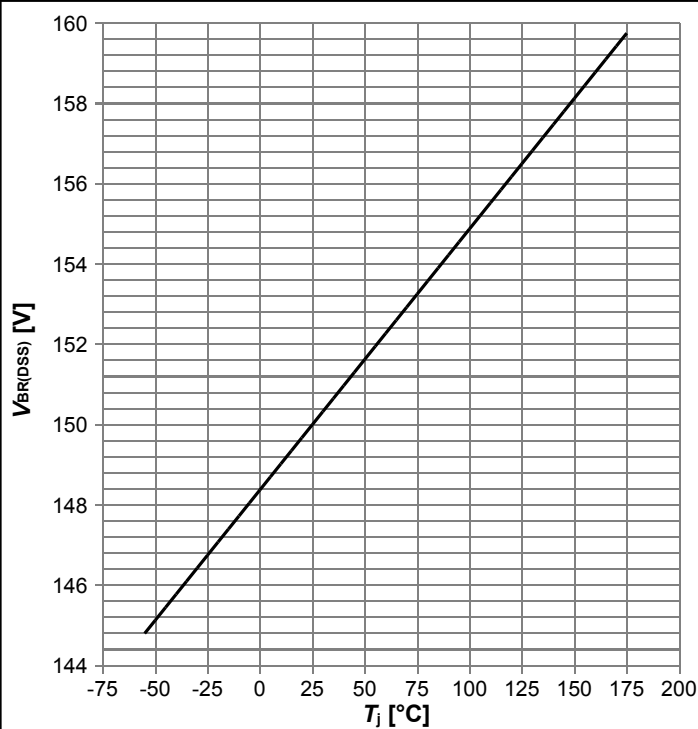
$I_{AS}=f(t_{AV})$ ;  $R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

Diagram 14: Typ. gate charge



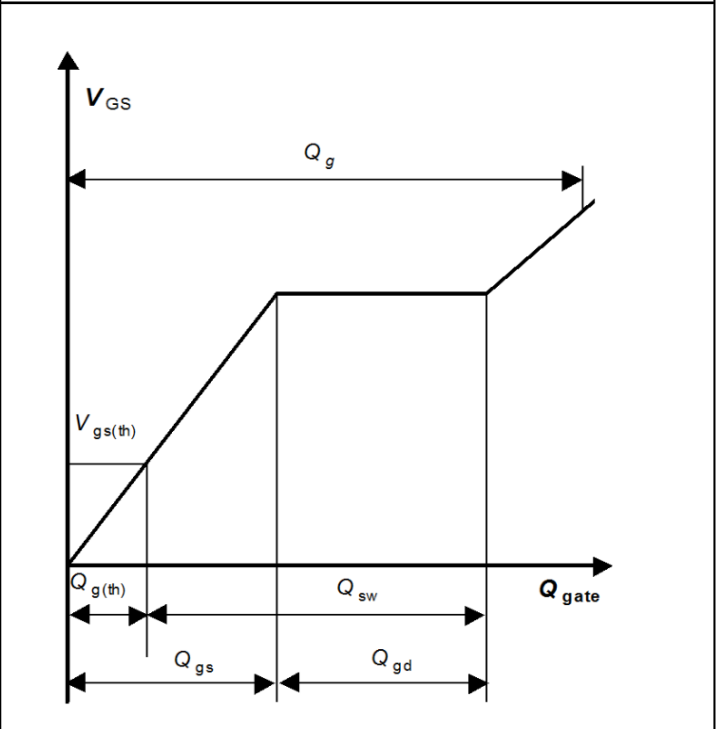
$V_{GS}=f(Q_{gate})$ ,  $I_D=50$  A pulsed,  $T_j=25$  °C; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage

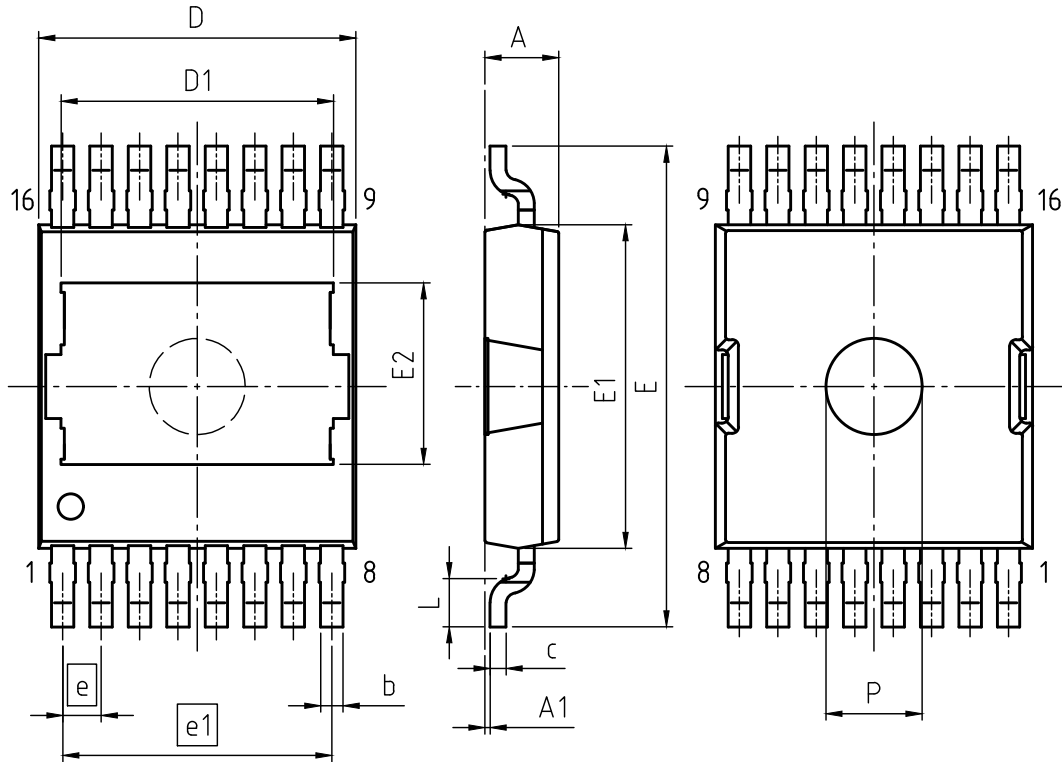


$V_{BR(DSS)}=f(T_j)$ ;  $I_D=1$  mA

Diagram Gate charge waveforms



## 5 Package Outlines



PACKAGE - GROUP NUMBER: <b>PG-HDSOP-16-U01</b>		
REVISION: 01	DATE: 18.12.2020	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.25	2.35
A1	0.01	0.16
b	0.60	0.80
c	0.40	0.60
D	9.70	10.10
D1	8.20	8.40
E	14.80	15.20
E1	10.00	10.30
E2	5.57	5.77
e	1.20	
e1	8.40	
L	1.40	1.60
P	2.90	3.10

Figure 1 Outline PG-HDSOP-16, dimensions in mm

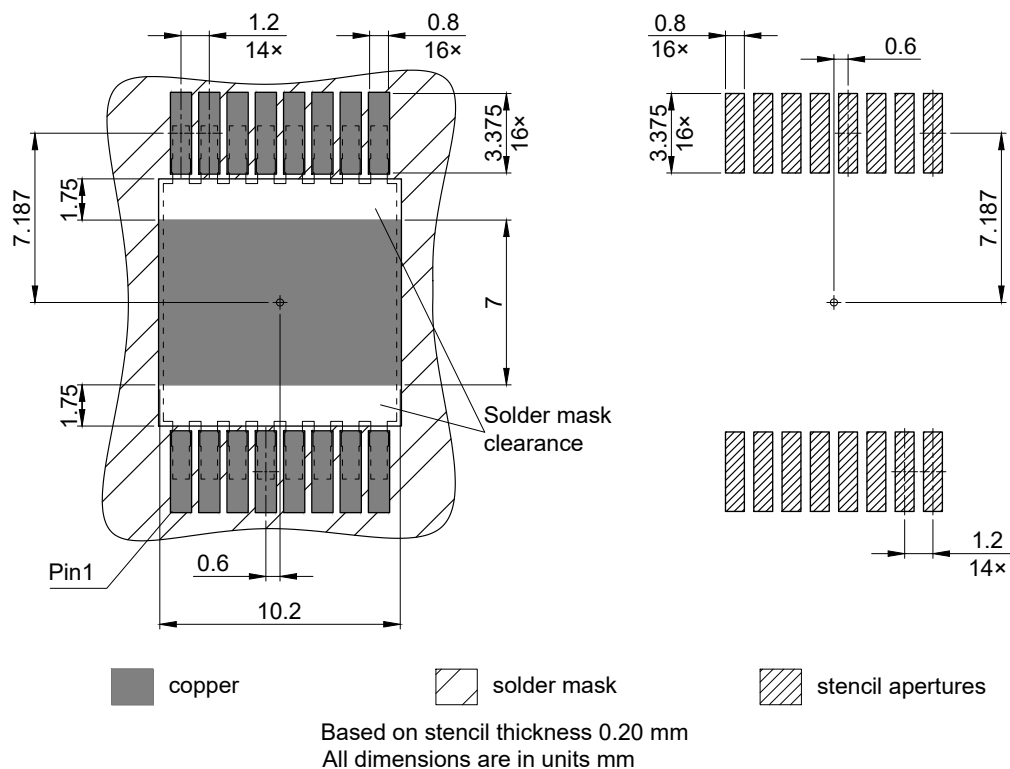
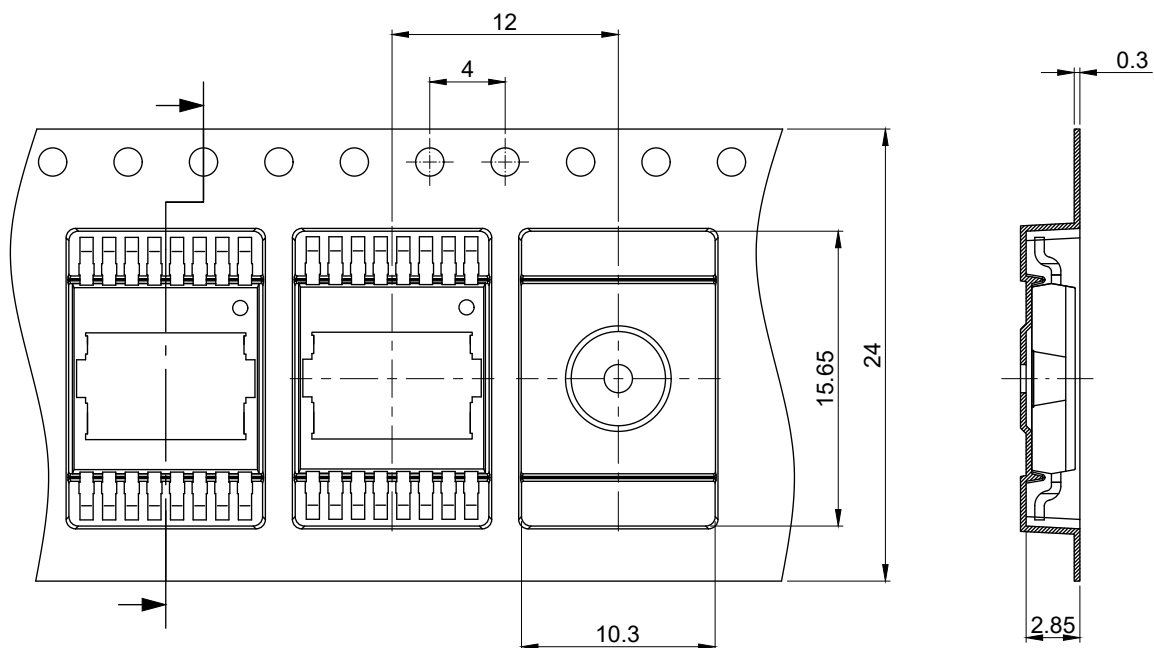



Figure 2 Outline Footprint (PG-HDSOP-16), dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [  ]

**Figure 3 Outline Tape (PG-HDSOP-16), dimensions in mm**

## Revision History

IPTC044N15NM5

**Revision: 2023-03-13, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-05-05	Release of final version
2.1	2023-03-13	Update Coss max

### Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

### We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

[erratum@infineon.com](mailto:erratum@infineon.com)

### Published by

**Infineon Technologies AG**

**81726 München, Germany**

**© 2023 Infineon Technologies AG**

**All Rights Reserved.**

### Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffungsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

### Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.