iPOWIR™ TECHNOLOGY

Synchronous Buck Dual Channel Power Block

Integrated Power Semiconductors, Drivers, & Passives

Features

- 60A Multiphase building block
- No derating up to T_{PCB} = 95ºC
- Integrated 6V LDO
- Operation up to 1 MHz
- Bi-directional current flow
- Under Voltage Lockout
- Optimized for low power loss
- LGA interface
- 11mm x 7.65mm outline

Applications

- Multi-phase Architectures
- Low Duty-Ratio, High Current
- Microprocessor Power Supplies
- High Frequency Low Profile DC-DC Converters

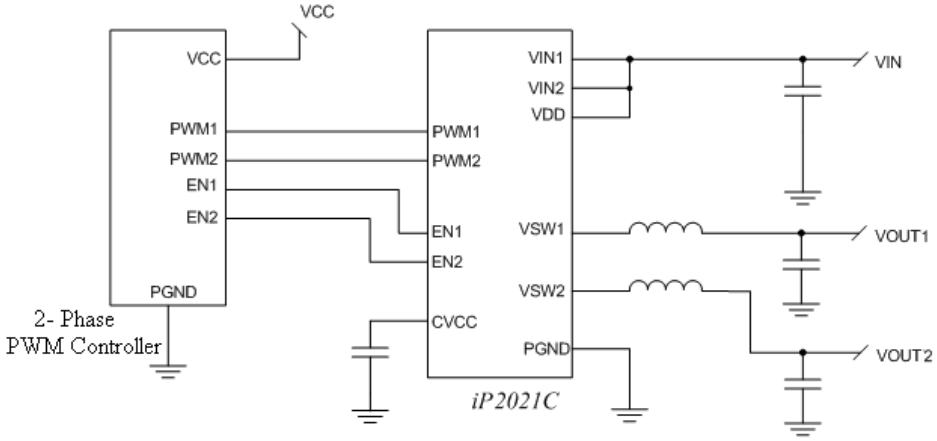
Package Description	Interface Connection	Standard Quantity
iP2021CPbF	LGA	10
iP2021CTRPbF	LGA	2000

Description

The iP2021C is a fully optimized solution for high current synchronous buck dual-phase or dual output applications. Board space and design time are greatly reduced because most of the components required for both power stages are integrated into a single 11mm x 7.7mm power block. The only additional components required for a complete converter are a PWM controller, the output inductors, and the input and output capacitors.

iPOWIR technology offers designers an innovative board space saving solution for applications requiring high power densities. iPOWIR technology solutions are also optimized internally for layout, heat transfer and component selection.

Typical Application (Dual Output)



Absolute Maximum Ratings

V_{IN1}, V_{IN2} to PGND ..... -0.3V to 16V
V_{DD} to PGND ..... -0.3V to 16V
PWM1, PWM2 to PGND ..... -0.3V to 7.5V (Note 1)
EN1, EN2 to PGND ..... -0.3V to 7.5V (Note 1)
Storage Temperature ..... -60ºC to 150ºC
Operating Block Temperature (T_{BLK}) ..... -40ºC to 135ºC (Note 2)
ESD Rating ..... JEDEC, JESD22-A114 (HBM[4KV], Class 3A)
..... JEDEC, JESD22-A115 (MM[400V], Class C)
MSL Rating 3
Reflow Temperature ..... 260ºC Peak

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied.

Recommended Operation Conditions

PARAMETER	Min	Typ	Max	Units	Conditions
Input Voltage (V_{DD}, V_{IN1},V_{IN2})	8	-	14	V	
Output Current (I_{OUT})	-	-	30	A	Current per channel
Output Voltage (V_{OUT})	-	-	5	V	
Switching Frequency (F_{SW})	300	-	1000	kHz	
Minimum VSW On Time	50	-	-	ns	
Block Temperature (T_{BLK})	-10	-	125	ºC	

Electrical Specifications

These specifications apply for T_{BLK} = 0ºC to 125ºC, V_{DD} = V_{IN1} = V_{IN2} = 8V to 14V unless otherwise specified.

PARAMETER	Min	Typ	Max	Units	Conditions
P_{Loss}					
Power Block Losses	-	11.2 (Note 3)	-	W	V_{DD} = V_{IN1} = V_{IN2} = 12V, V_{OUT} = 1.3V, I_{OUT} = 60A (outputs combined), F_{SW} = 1MHz, L = 325nH, T_{BLK} = 25ºC
V_{IN} (V_{IN1}, V_{IN2}, V_{DD})					
Quiescent Current	-	4	8	mA	V_{DD} = V_{IN1} = V_{IN2} = 12V, EN1 = EN2 = 0V

PARAMETER	Min	Typ	Max	Units	Conditions
CV_{CC}					
Output Voltage	-	6	-	V	V_{DD} = 8V – 14.5V
Output Capacitor	1	-	-	µF	
CV_{CC} Power On Reset					
CV_{CC} Rising		4.15	4.5	V	-40ºC to 125ºC
CV_{CC} Falling	3.6	3.95		V	
CV_{CC} Threshold		200		mV	
ENABLE INPUT (EN1, EN2)					
Logic Level Low Threshold	-	-	0.8	V	-40ºC to 125ºC
Logic Level High Threshold	2.0	-	-	V	
Threshold Hysteresis	-	100	-	mV	
Weak Pull Down Resistance	-	100k	-	Ω	
Rising Propagation Delay	-	40	-	ns	
Falling Propagation Delay	-	75	-	ns	
PWM INPUT (PWM1, PWM2)					
Logic Level Low Threshold	-	-	0.8	V	-40ºC to 125ºC
Logic Level High Threshold	2.0	-	-	V	
Threshold Hysteresis	-	100	-	mV	
Weak Pull Down Resistance	-	100k	-	Ω	
Rising Propagation Delay (t_{PDH})	-	60	-	ns	See Figure 8 for timing diagram
Falling Propagation Delay (t_{PDL})	-	30	-	ns	

Notes:

1. Must not exceed 7.5V
2. Highest die temperature inside the package
3. Guaranteed by design, but not tested in production

Power Loss Curve

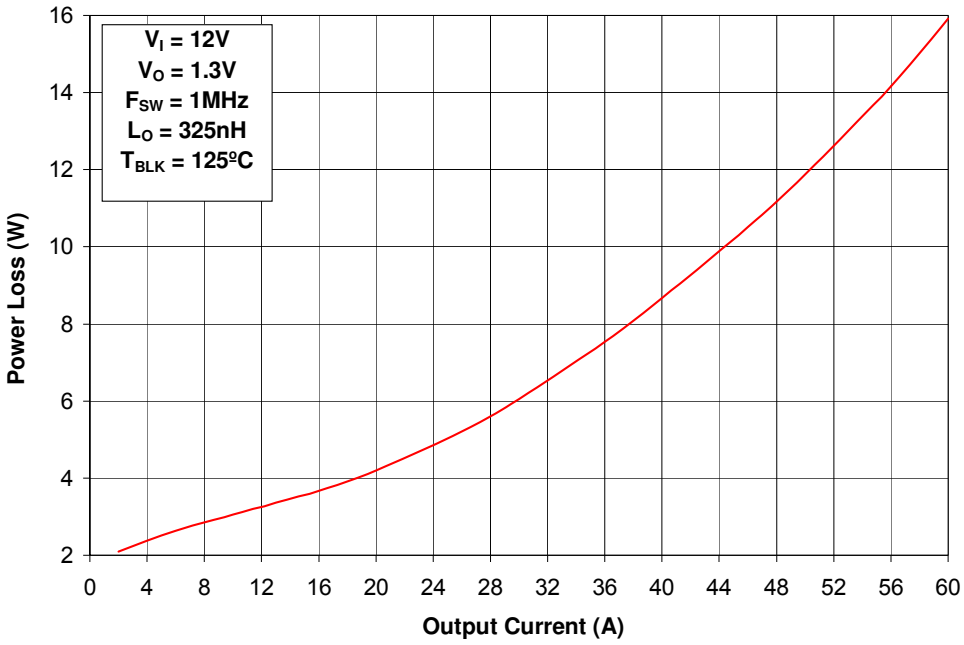


Figure 1 Power Loss Curve

SOA Curve

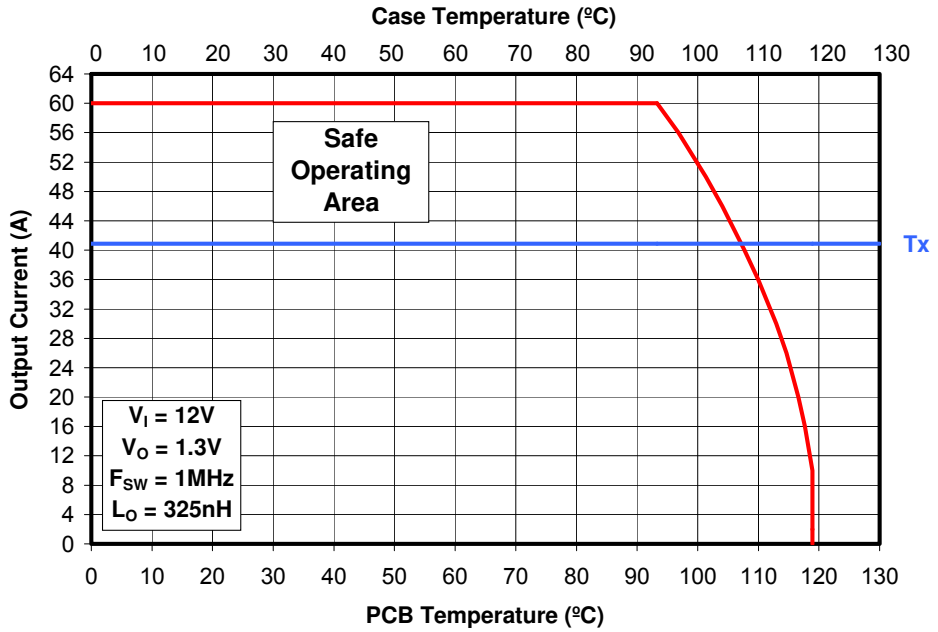


Figure 2 Safe Operating Area Curve

Typical Performance Curves

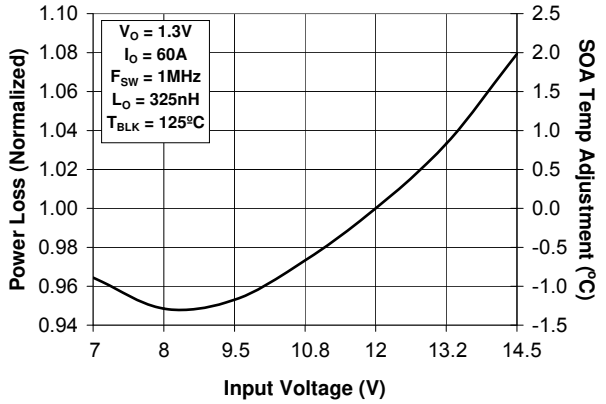


Figure 3 Normalized Power Loss vs. Input Voltage

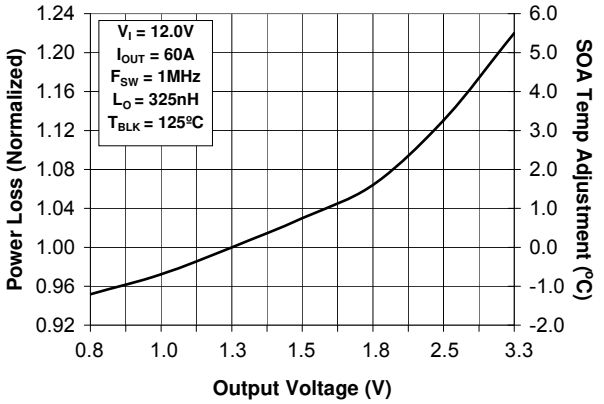


Figure 4 Normalized Power Loss vs. Output Voltage

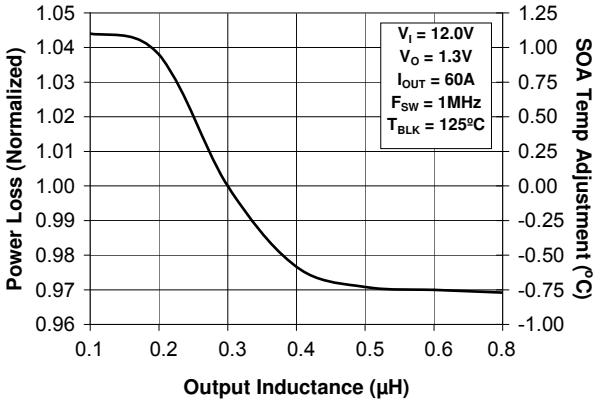


Figure 5 Normalized Power Loss vs. Inductance

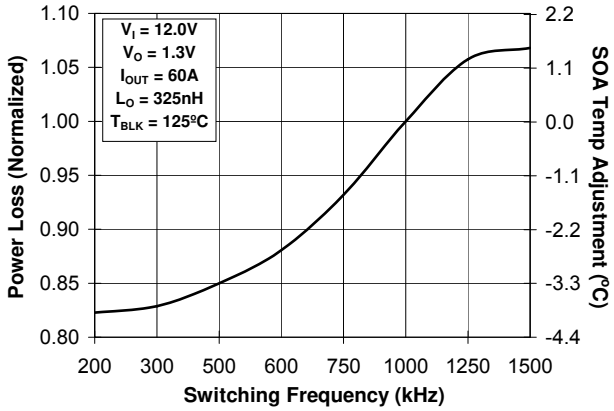


Figure 6 Normalized Power Loss vs. Switching Frequency

Power Loss Measurement Setup

$P_{IN} = V_{IN} \times (I_{IN1} + I_{IN2})$

$P_{OUT} = V_{OUT1} \times I_{OUT1} + V_{OUT2} \times I_{OUT2}$

$P_{LOSS} = P_{IN} - P_{OUT}$

Note: All currents and voltages are average values

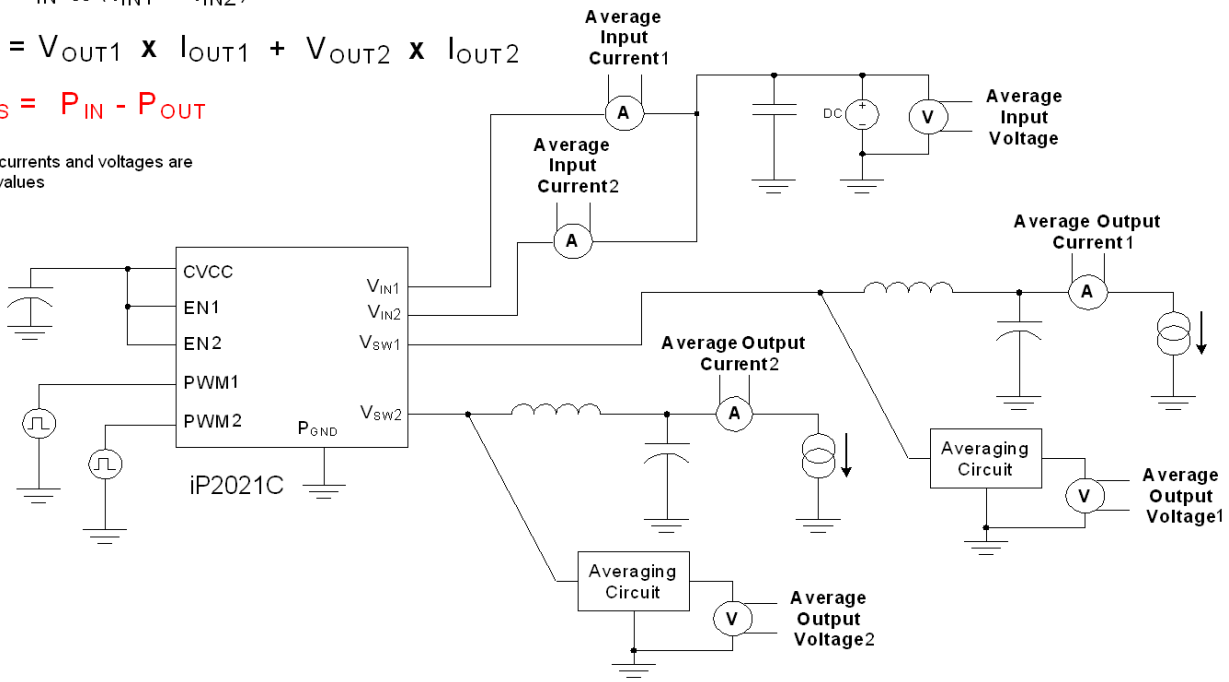


Figure 7 Power Loss Test Circuit

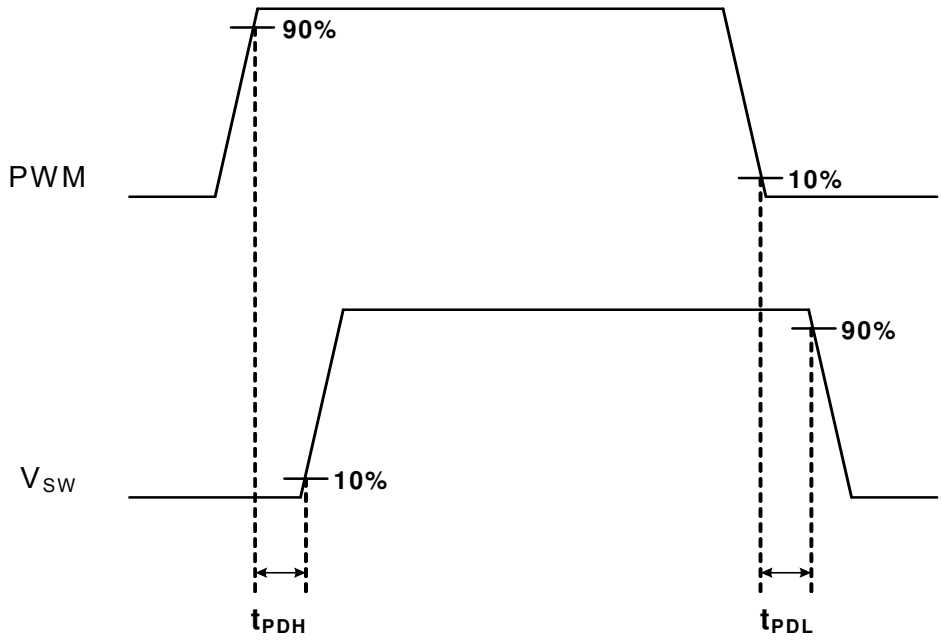


Figure 8 Timing Diagram

Applying the Safe Operating Area (SOA) Curve

The SOA graph incorporates power loss and thermal resistance information in a way that allows one to solve for maximum current capability in a simplified graphical manner. It incorporates the ability to solve thermal problems where heat is drawn out through the printed circuit board and the top of the case. Please refer to International Rectifier Application Note AN1047 for further details on using this SOA curve in your thermal environment.

Procedure

1. Calculate (based on estimated Power Loss) or measure the Case temperature on the device and the board temperature near the device (1mm from the edge).
2. Draw a line from Case Temperature axis to the PCB Temperature axis.
3. Draw a vertical line from the T_X axis intercept to the SOA curve.
4. Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the SOA continuous current.

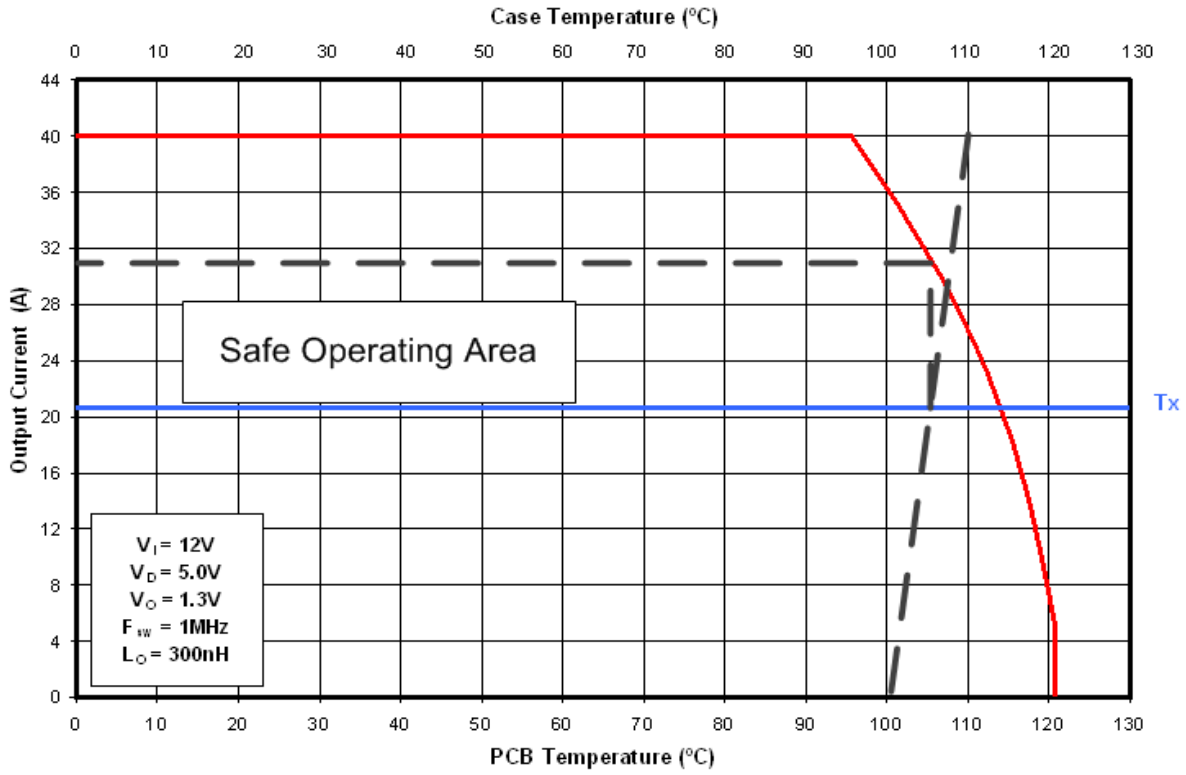


Figure 9 SOA Example, Continuous current ≈ 31A for T_{PCB} = 100ºC & T_{CASE} = 110ºC

Calculating Power Loss and SOA for Different Operating Conditions

To calculate Power Loss for a given set of operating conditions, the following procedure should be followed:

Power Loss Procedure

1. Determine the maximum current and obtain the typical power loss from Figure 1
2. Use the normalized curves to obtain power loss values that match the operating conditions in the application
3. The typical power loss under the application conditions is then the product of the power loss from Figure 1 and the normalized values.

To calculate the Safe Operating Area (SOA) for a given set of operating conditions, the following procedure should be followed:

SOA Procedure

1. Determine the maximum PCB and CASE temperature at the maximum operating current for each iP2021C
2. Use the normalized curves to obtain SOA temperature adjustments that match the operating conditions in the application
3. Then, add the sum of the SOA temperature adjustments to the T_X axis intercept in Figure 2

Design Example

Operating Conditions:

Output Current = 50A Input Voltage = 10V Output Voltage = 1.3V

Switching Freq = 750 kHz Inductor = 0.2µH

Calculating Typical Power Loss:

(Figure 1) Typical power loss = 12W

(Figure 3) Normalized power loss for input voltage ≈ 0.96

(Figure 5) Normalized power loss for output inductor ≈ 1.035

(Figure 6) Normalized power loss for switch frequency ≈ 0.93

Calculated Typical Power Loss ≈ 12W x 0.96 x 1.0 x 1.035 x 0.93 ≈ 11.1W

Calculating SOA Temperature:

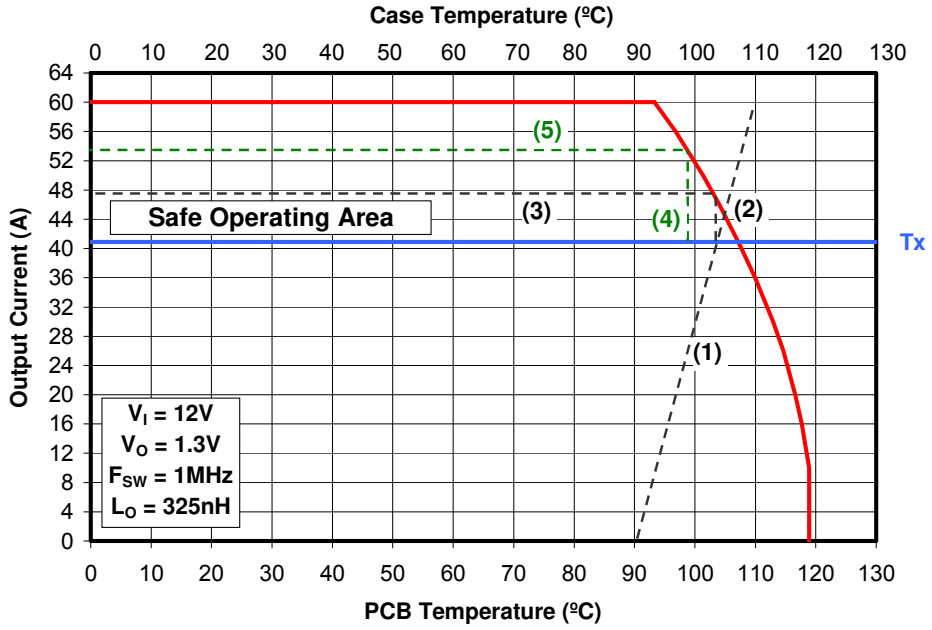
(Figure 3) SOA temperature adjustment for input voltage ≈ -1.0ºC

(Figure 5) SOA temperature adjustment for output inductor ≈ 0.95ºC

(Figure 6) SOA temperature adjustment for switch frequency ≈ -1.5ºC

T_X axis intercept adjustment ≈ -1.0ºC + 0.95ºC – 1.5ºC ≈ -1.55ºC

Assuming T_{PCB} = 90ºC & T_{CASE} = 110ºC, the following example shows how the SOA current is adjusted for T_X decrease of 4.5ºC.



1. Draw a line from Case Temperature axis to the PCB Temperature axis.
2. Draw a vertical line from the T_X axis intercept to the SOA curve.
3. Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the SOA continuous current.
4. Draw a new vertical line from the T_X axis by adding or subtracting the SOA adjustment temperature from the original T_X intercept point.
5. Draw a horizontal line from the intersection of the new vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the new SOA continuous current.

The SOA adjustment indicates the part is still allowed to run at a continuous current of 53.5A.

Internal Block Diagram

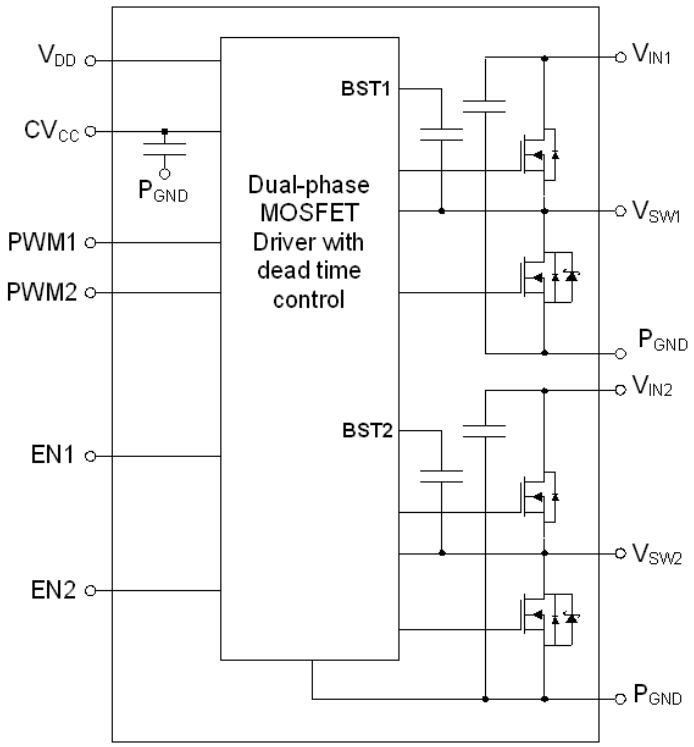


Figure 10 Internal Block Diagram

Pin Description

Pin Number	Pin Name	Description
1, 9	V_{IN1},V_{IN2}	Input Voltage Pin. Connect input capacitors close to this pin.
2, 8	V_{SW1}, V_{SW2}	Voltage Switching Node – pin connection to the output inductor
3, 7	PGND	Power Ground
4	CV_{CC}	Output of internal regulator. Connect 1uF external bypass capacitor.
5, 6	PWM1, PWM2	Input signal to MOSFET drivers. When PWM is HIGH, the control FET is on and sync FET is off. When PWM is LOW, the sync FET is on and the control FET is off.
10, 11	EN2, EN1	When set to logic level high, internal circuitry of the device is enabled. When set to logic level low, the control and synchronous FETs are turned off.
12	V_{DD}	Supply voltage for internal circuitry

Recommended PCB Layout

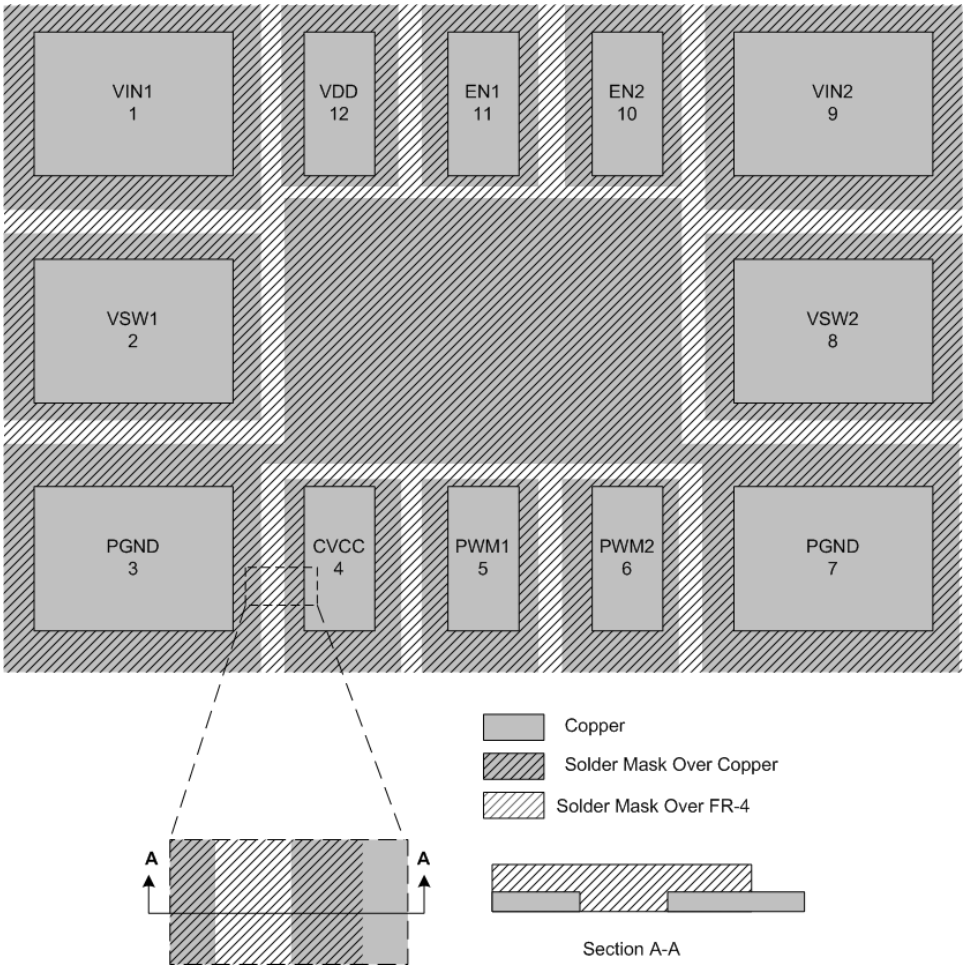
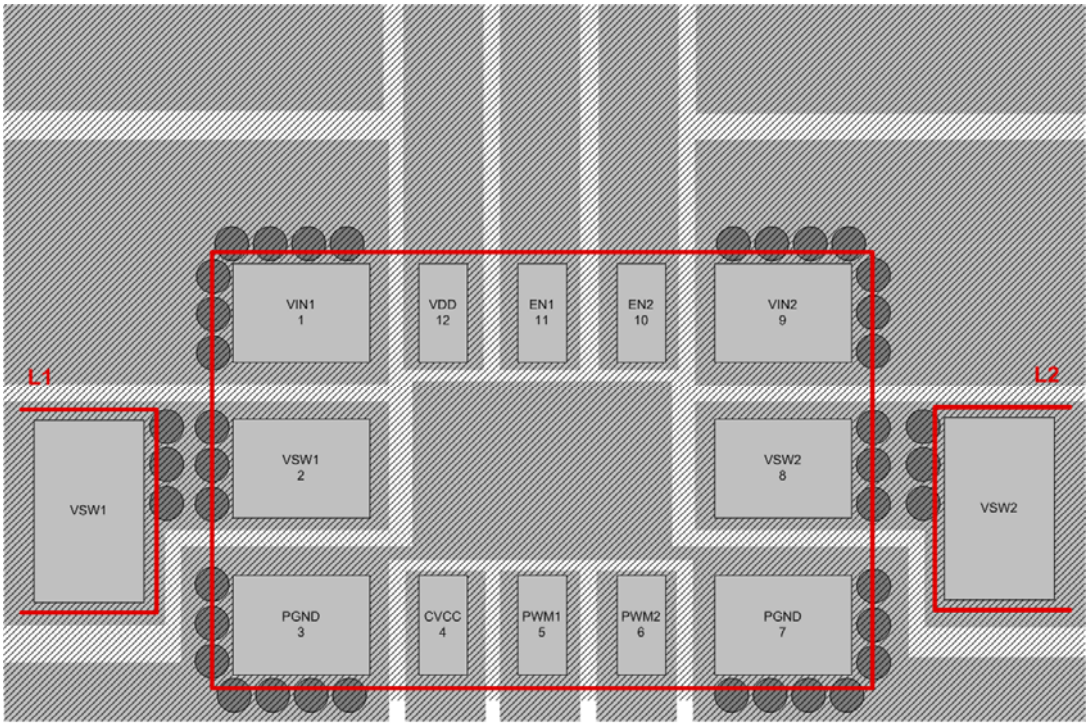


Figure 11 Top Copper and Solder-mask Layer of PCB Layout

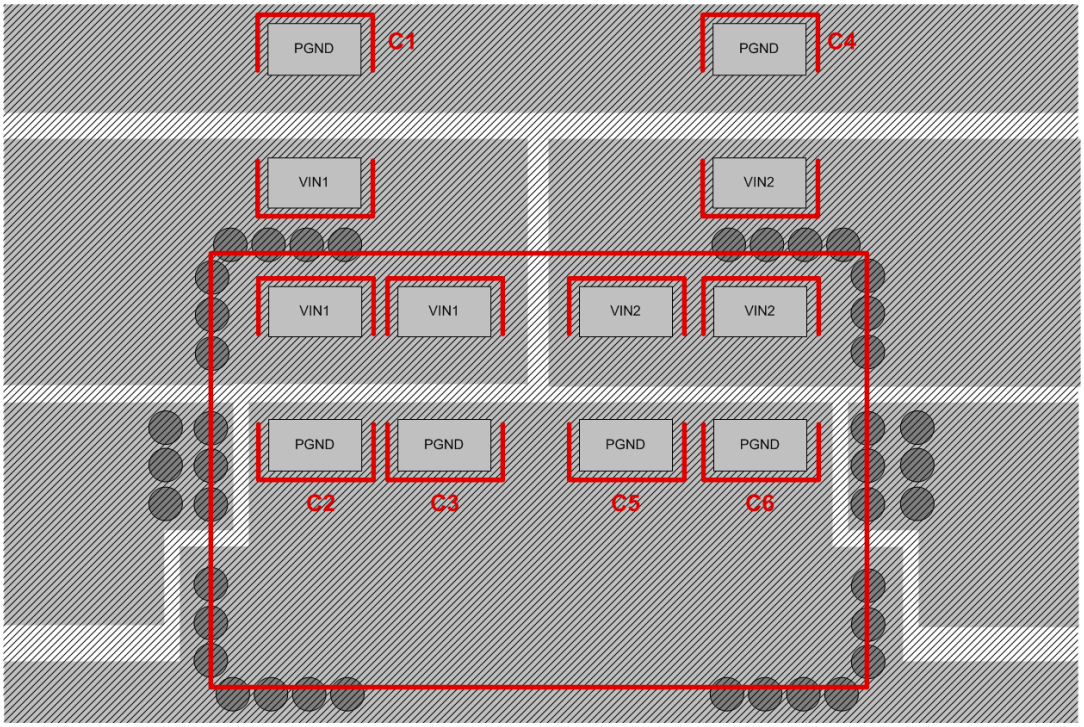
PCB Layout Guidelines

The following guidelines are recommended to reduce the parasitic values and optimize overall performance:

- All pads on the iP2021C footprint design need to be Solder-mask defined (see Figure 11). Also refer to International Rectifier application notes AN1028 and AN1029 for further footprint design guidance.
- Place as many vias around the Power pads (V_{IN1}, V_{IN2}, V_{SW1}, V_{SW2} and PGND) for both electrical and optimal thermal performance (see Figure 12).
- A minimum of three 10µF, X5R, 16V ceramic capacitors per phase of iP2021C are needed for 28A operation at 1MHz. This will result in the lowest loss due to input capacitor ESR.
- Placement of the ceramic input capacitors is critical to optimize switching performance. Place all six ceramic capacitors (C1-C6) right underneath the iP2021C footprint (see Figure 12 Bottom Component Layer).
- Dedicate at least two layer for PGND only
- Duplicate the Power Nodes on multiple layers (refer to AN1029).



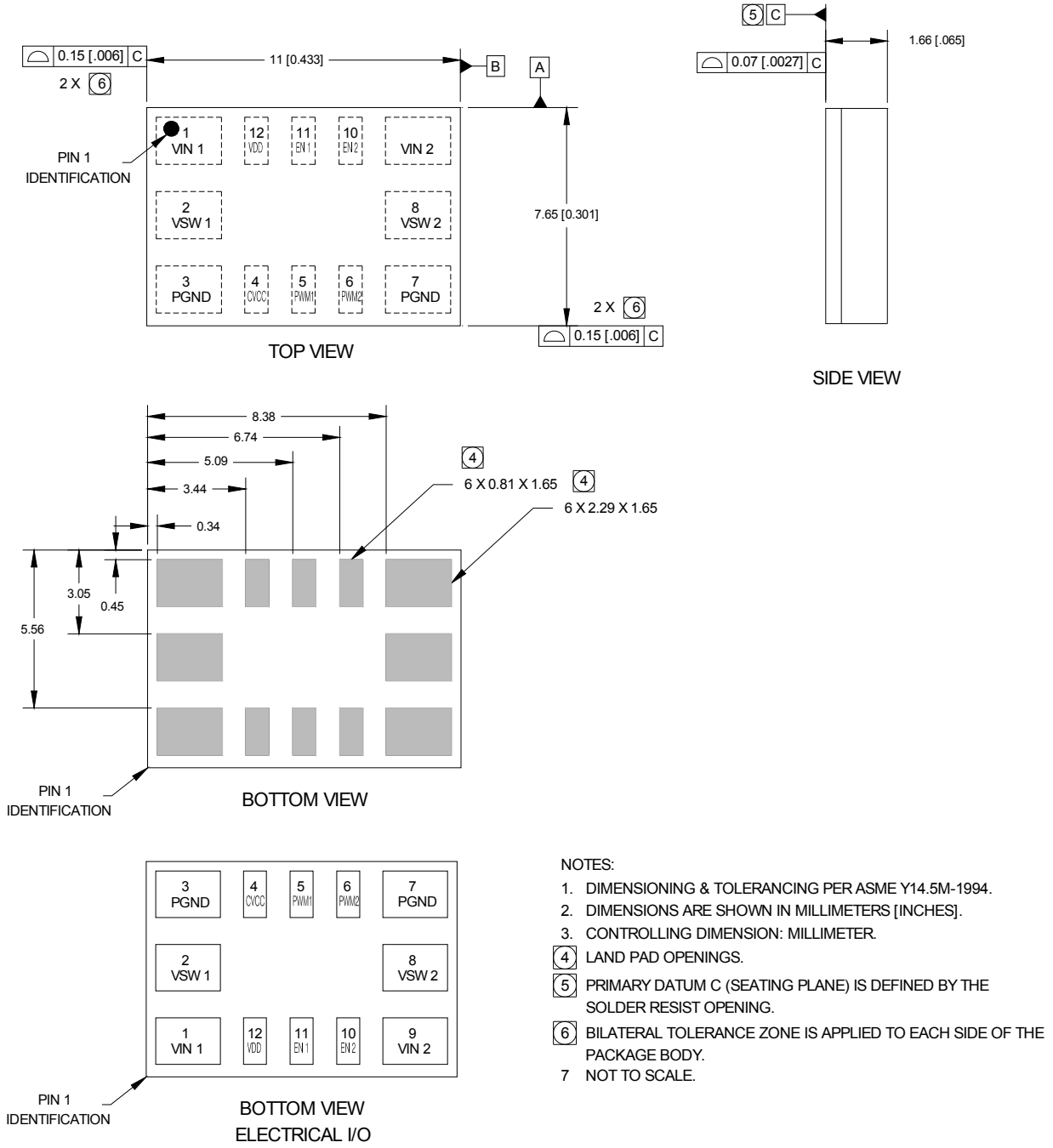
Top Component Layer



Bottom Component Layer

Figure 12 Top & Bottom Component and Via Placement (Topside, Transparent view down)

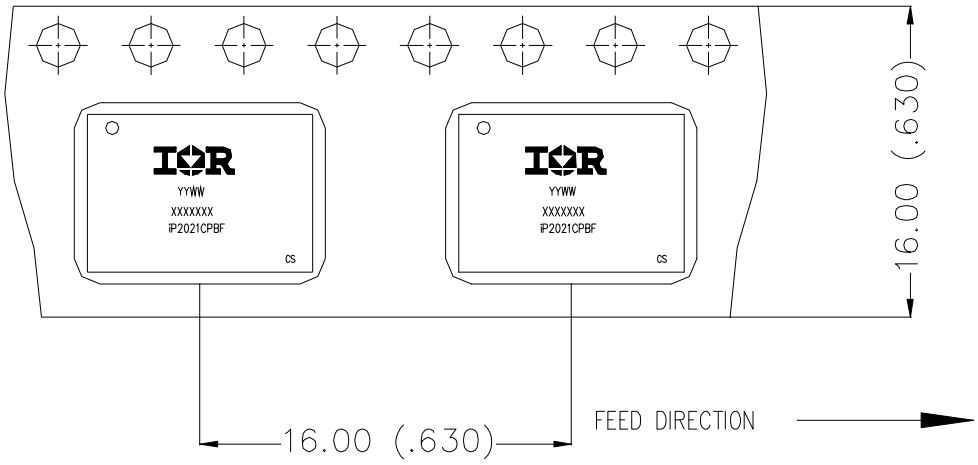
Mechanical Outline Drawing



NOTES:

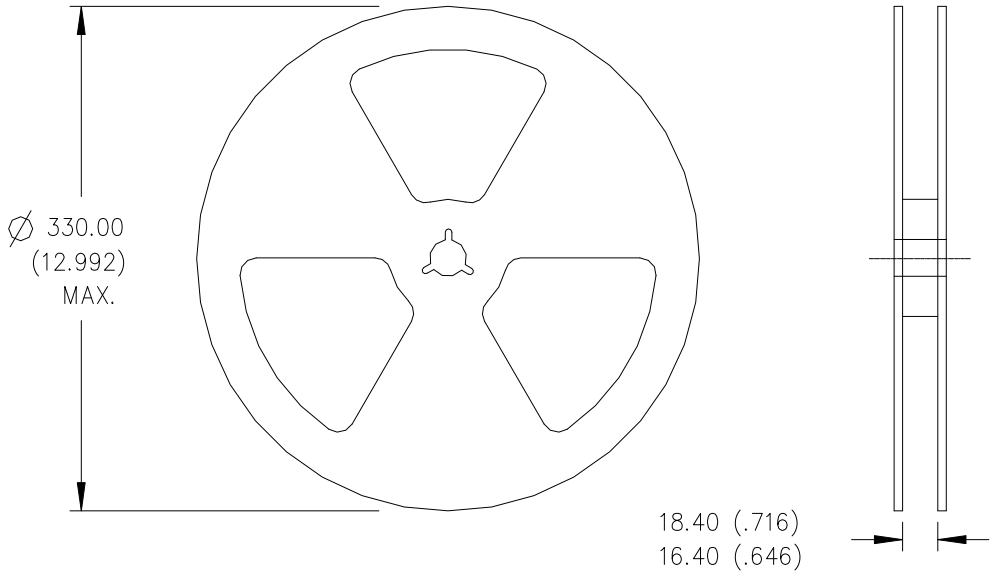
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: MILLIMETER.
4. LAND PAD OPENINGS.
5. PRIMARY DATUM C (SEATING PLANE) IS DEFINED BY THE SOLDER RESIST OPENING.
6. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
7. NOT TO SCALE.

Figure 13 Mechanical Outline Drawing



NOTE:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Figure 14 Tape and Reel Information

Recommended Solder Paste Stencil Design

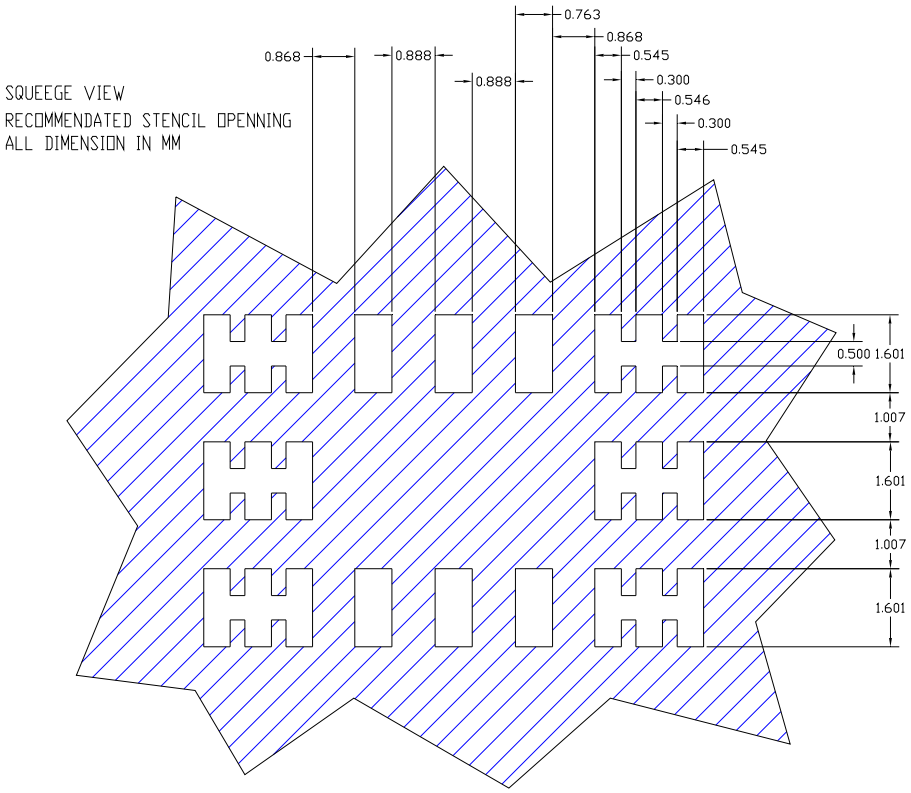


Figure 15 Solder Paste Stencil Design

The recommended reflow peak temperature is 260°C. The total furnace time is approximately 5 minutes with approximately 10 seconds at peak temperature.

Part Marking

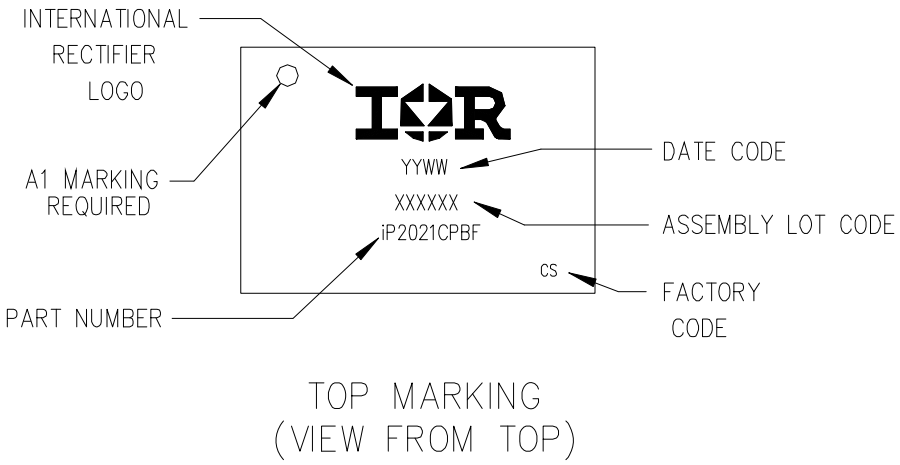


Figure 16 Part Marking