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**PRELIMINARY**

**CYW20713**

# Single-Chip Bluetooth Transceiver and Baseband Processor

The Cypress CYW20713 is a monolithic, single-chip, Bluetooth 4.0 compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver. Manufactured using the industry's most advanced 65 nm CMOS low-power process, the CYW20713 employs the highest level of integration, eliminating all critical external components, and thereby minimizing the device's footprint and costs associated with the implementation of Bluetooth solutions.

The CYW20713 brings the latest mobile connectivity technology to automotive radio and industrial Bluetooth applications. Offering automotive Grade 3 (-40°C to +85°C) temperature performance, the CYW20713 is tested to AECQ100 environmental stress guidelines and manufactured in ISO9001 and TS16949 certified facilities.

## Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

**Table 1. Mapping Table for Part Number between Broadcom and Cypress**

| Broadcom Part Number | Cypress Part Number |
|----------------------|---------------------|
| BCM20713             | CYW20713            |
| BCM20713A1KUBG       | CYW20713A1KUBG      |
| BCM20713A1KUFBXG     | CYW20713A1KUFBXG    |

## Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Cypress documents, go to:  
<http://www.cypress.com/glossary>

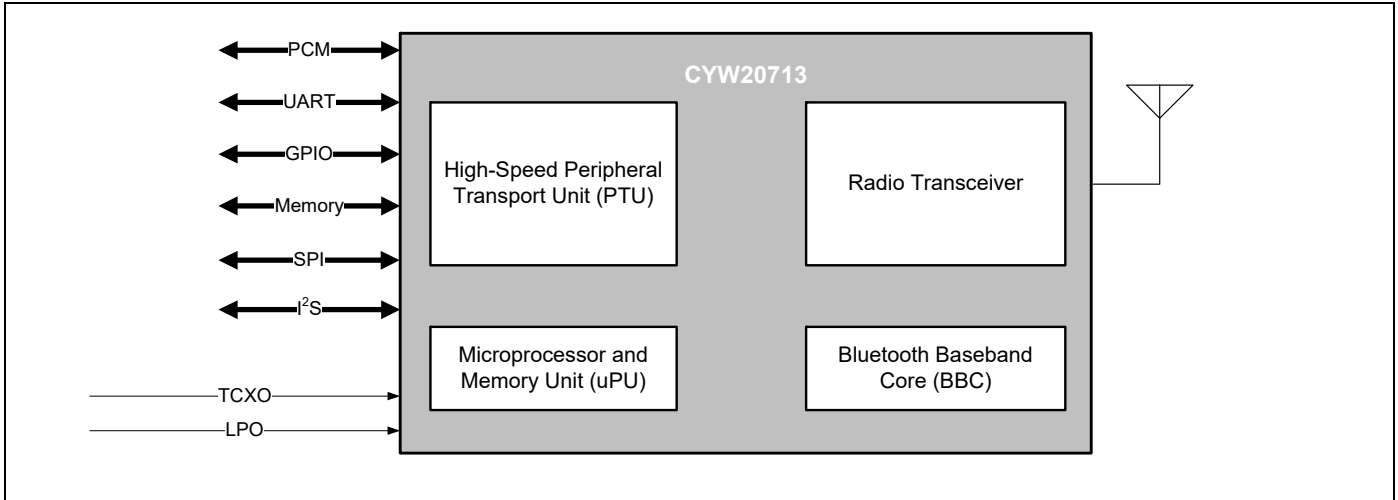
## Features

- Bluetooth 4.0 + EDR compliant.
- Class 1 capable with built-in PA.
- Programmable output power control meets Class 1, Class 2, or Class 3 requirements.
- Use supply voltages up to 5.5V. Supports Cypress SmartAudio®, wide-band speech, SBC codec, and packet loss concealment.
- Fractional-N synthesizer supports frequency references from 12 MHz to 52 MHz.
- Automatic frequency detection for standard crystal and TCXO values when an external 32.768 kHz reference clock is provided.
- Ultra-low power consumption.
- Supports serial flash interfaces.
- Available in 42-bump WLBGA and 50-ball FPBGA packages.
- ARM7TDMI-S-based microprocessor with integrated ROM and RAM.
- Supports patch RAM download without external memory.
- Qualified for Bluetooth Core Specification 5.0 with all Bluetooth 4.0 optional features
  - QDID: [119366](#)
  - Declaration ID: [D040196](#)

## Applications

- Automotive handsfree radios
- Automotive data communication
- Industrial appliances

Figure 1. System Block Diagram



### IoT Resources

Cypress provides a wealth of data at <http://www.cypress.com/internet-things-iot> to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (<http://community.cypress.com/>).

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## 1. Overview

The Cypress CYW20713 complies with the Bluetooth Core Specification, version 4.0 and is designed for use with a standard host controller interface (HCI) UART. The combination of the Bluetooth baseband core (BBC), a Peripheral Transport Unit (PTU), and an ARM-based microprocessor with on-chip ROM provides a complete lower layer Bluetooth protocol stack, including the link controller (LC), link manager (LM), and HCI.

### 1.1 Major Features

Major features of the CYW20713 include:

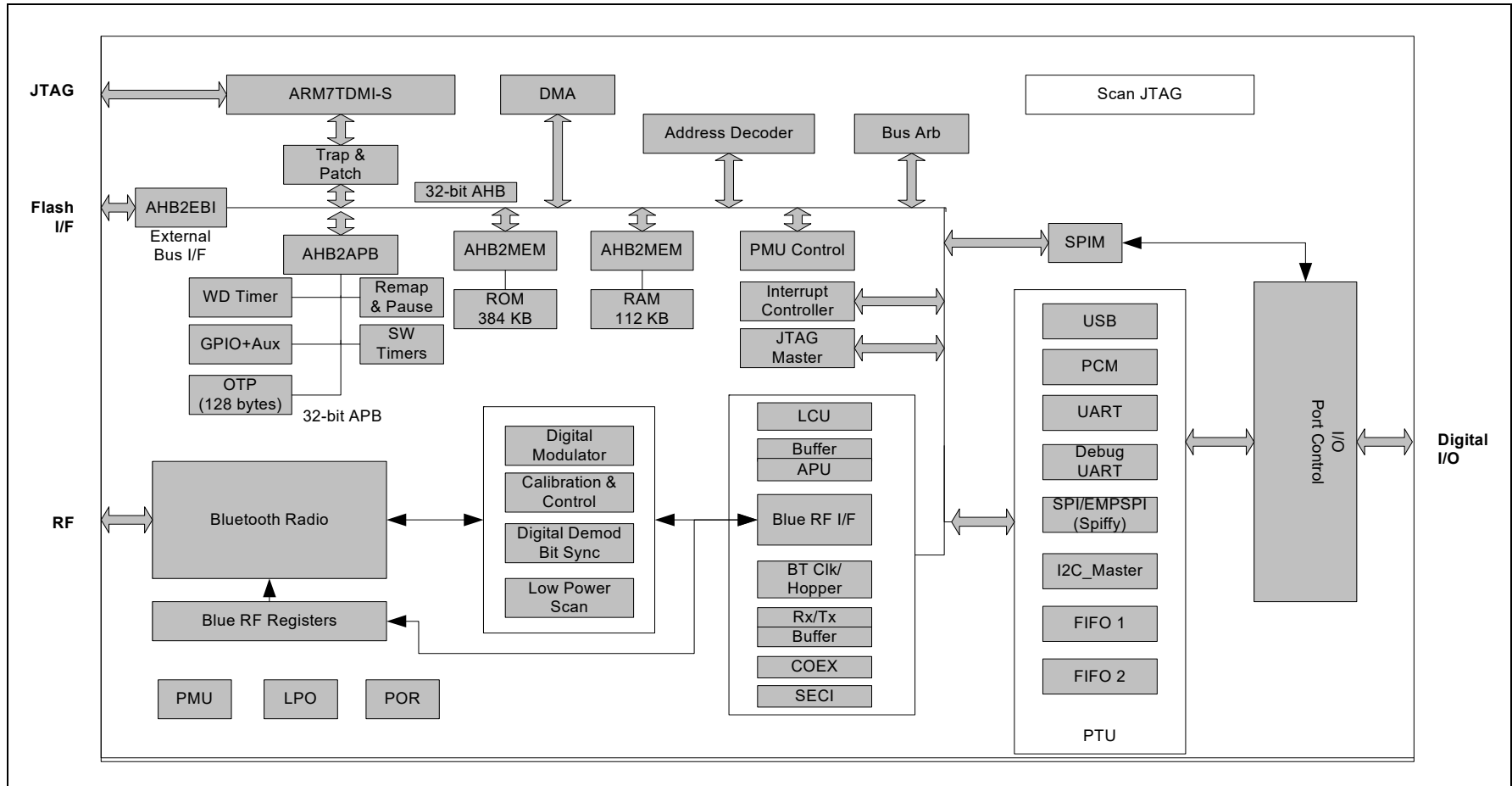
- Support for Bluetooth 4.0 + EDR, including the following options:
  - Whitelist size of 25
  - Enhanced Power Control
  - HCI Read Encryption Key Size command
- Full support for Bluetooth 2.1 + EDR additional features:
  - Secure simple pairing (SSP)
  - Encryption pause resume (EPR)
  - Enhance inquiry response (EIR)
  - Link supervision time out (LSTO)
  - Sniff subrating (SSR)
  - Erroneous data (ED)
  - Packet boundary flag (PBF)
- Built-in low drop-out (LDO) regulators (2)
  - 1.63 to 5.5V input voltage range
  - 1.8 to 3.3V intermediate programmable output voltage
- Integrated RF section
  - Single-ended, 50 ohm RF interface
  - Built-in TX/RX switch functionality
  - TX Class 1 output power capability
  - -88 dBm RX sensitivity basic rate
- Supports maximum Bluetooth data rates over HCI UART and SPI interfaces
- Multipoint operation, with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO links, with Scatternet support
- Scatternet operation, with up to four active piconets (with background scan and support for ScatterMode)
- High-speed HCI UART transport support
  - H4 five-wire UART (four signal wires, one ground wire)
  - H5 three-wire UART (two signal wires, one ground wire)
  - Maximum UART baud rates of 4 Mbps
  - Low-power out-of-band BT\_WAKE and HOST\_WAKE signaling
  - VSC from host transport to UART
  - Proprietary compressing scheme (allows more than two simultaneous A2DP packets and up to five devices at a time)
- Channel quality-driven data rate (CQDDR) and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes:
  - Bluetooth standard hold and sniff
  - Deep sleep modes and regulator shutdown

- Supports wideband speech (WBS) over PCM and packet loss concealment (PLC) for better audio quality
- 2-, 3-, and 4-wire coexistence
- Power amplifier (PA) shutdown for externally controlled coexistence, such as WIMAX
- Built-in LPO clock or operation using an external LPO clock
- TCXO input and auto-detection of all standard handset clock frequencies (supports low-power crystal, which can be used during Power Saving mode with better timing accuracy)
- OR gate for combining a host clock request with a Bluetooth clock request (operates even when the Bluetooth core logic is powered off)
- Larger patch RAM space to support future enhancements
- Serial flash Interface with native support for devices from several manufacturers
- One-time programmable (OTP) memory

1.2 Block Diagram

Figure 2 on page 6 shows the interconnect of the major CYW20713 physical blocks and associated external interfaces.

Figure 2. Functional Block Diagram



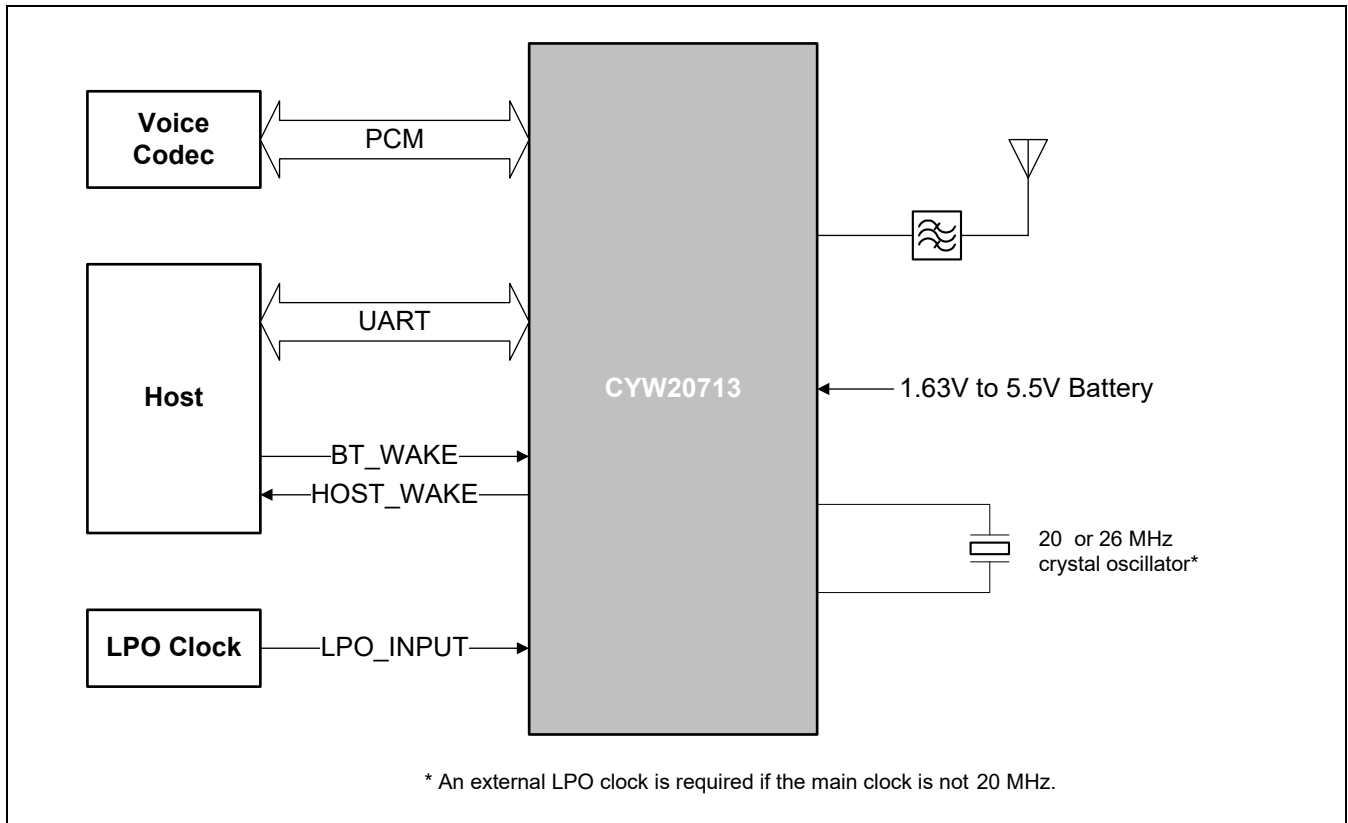
### 1.3 Usage Model

The CYW20713 is designed to provide a direct interface to industrial systems, as shown in Figure 3. The device has flexible PCM and UART interfaces, enabling it to transparently connect to existing circuits.

The device incorporates a number of unique features to accommodate integration into industrial systems.

- The PCM interface provides multiple modes of operation to support both master and slave, as well as hybrid interfacing to one or more external codec devices.
- The UART interface supports hardware flow control with tight integration to power control sideband signaling to support the lowest power operation.
- Few external components are required for integration.

**Figure 3. Usage Model**





## 2. Integrated Radio Transceiver

The CYW20713 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The CYW20713 is fully compliant with the Bluetooth Radio Specification and enhanced data rate specification and meets or exceeds the requirements to provide the highest communication link quality of service.

### 2.1 Transmitter Path

The CYW20713 features a fully integrated zero IF transmitter. The baseband transmitted data is digitally modulated in the modem block and up-converted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q up-conversion, a high-output power amplifier (PA), and RF filtering.

The CYW20713 also incorporates modulation schemes to support enhanced data rates.

- $\pi/4$ -DQPSK for 2 Mbps
- 8-DPSK for 3 Mbps

#### 2.1.1 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK,  $\pi/4$ -DQPSK, and 8-DPSK signals. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

#### 2.1.2 Power Amplifier

The CYW20713 has an integrated PA that can be configured for Class 2 operation, transmitting up to +4 dBm. The PA can also be configured for Class 1 operation, transmitting up to +10 dBm at the chip in gFSK mode, when a minimum supply voltage of 2.5V is applied to VDDTF.

Because of the linear nature of the PA, combined with integrated filtering, minimal external filtering is required to meet Bluetooth and regulatory harmonic and spurious requirements.

Using a highly linearized, temperature compensated design, the PA can transmit +10 dBm for basic rate and +8 dBm for enhanced data rates (2 to 3 Mbps). A flexible supply voltage range allows the PA to operate from 1.2V to 3.3V. A minimum supply voltage of 2.5V is required at VDDTF to achieve +10 dBm of transmit power.

## 2.2 Receiver Path

The receiver path uses a low IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the device to be used in most applications without off-chip filtering. For integrated handset operation where the Bluetooth function is integrated close to the cellular transmitter, minimal external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

#### 2.2.1 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer uses the low IF received signal to perform an optimal frequency tracking and bit synchronization algorithm.

#### 2.2.2 Receiver Signal Strength Indicator

The CYW20713 radio provides a Receiver Signal Strength Indicator (RSSI) signal to the baseband so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

## 2.3 Local Oscillator Generation

Local Oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The device uses fully-integrated PLL loop filters.

## 2.4 Calibration

The radio transceiver features an automated calibration scheme that is fully self-contained in the radio. User interaction is not required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all major blocks in the radio, including gain and phase characteristics of filters, matching between key components, and key gain blocks. Calibration, which takes process and temperature variations into account, occurs transparently during the settling time of the hops, adjusting for temperature variations as the device cools and heats during normal operation.

### 2.5 Internal LDO Regulator

Two internal Low Drop-Out (LDO) voltage regulators eliminate the need for external voltage regulators and therefore reduce the BOM. The first LDO is a preregulator (HV LDO). The second LDO (Main LDO) supplies the main power to the CYW20713 (see [Figure 2 on page 6](#)).

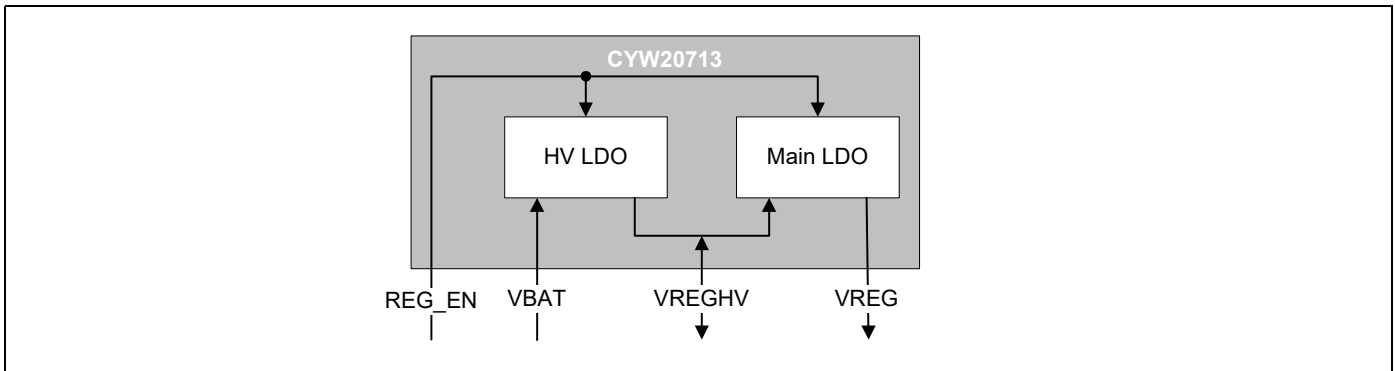
The HV LDO has an input voltage range of 2.3V to 5.5V. The input VBAT is ideal for batteries. The VREGHV output is programmable from 1.8V to 3.3V, in 100 mV steps. The dropout voltage is 200 mV. The HV LDO can supply up to 95 mA, which leaves spare power for external circuitry such as an RF power amp for higher transmit power. If the HV LDO is not used, to turn off the HV LDO and minimize current consumption, connect the VBAT input to the VREGHV output. Firmware can then disable the HV LDO, saving the quiescent current.

The HV LDO default output voltage is 2.9V, allowing this regulator to be used to power external NV memory devices, as well as the VDDO rail. The firmware can then adjust this output to as low as 1.8V, if desired, to power VDDTF.

The main LDO has a 1.22V output (VREG) and is used to supply main power to the CYW20713. The input of this LDO (VREGHV) has an input voltage range of from 1.63V to 3.63V. The output of the HV LDO is internally connected to the input to the main LDO. Power can be applied to VREGHV when the HV LDO is not used. The main LDO supplies power to the entire device for Class 2 operation. The main LDO can drive up to 60 mA, which leaves spare power for external circuitry. The main LDO is bypassed by not connecting anything to its output (VREG) and driving 1.12V–1.32V directly to VDDC and VDDRF.

REG\_EN provides a control signal for the host to control power to the CYW20713. When power is enabled, the CYW20713 will require complete initialization.

**Figure 4. LDO Functional Block Diagram**



### 3. Bluetooth Baseband Core

The Bluetooth baseband core (BBC) implements the time critical functions required for high-performance Bluetooth operation. The BBC manages buffering, segmentation, and data routing for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types and HCI command types.

#### 3.1 Transmit and Receive Functions

The following transmit and receive functions are implemented in the BBC hardware to increase the reliability and security of the TX/RX data before sending the data over the air:

In the transmitter:

- Data framing
- Forward error correction (FEC) generation
- Header error control (HEC) generation
- Cyclic redundancy check (CRC) generation
- Key generation
- Data encryption
- Data whitening

In the receiver:

- Symbol timing recovery
- Data deframing
- FEC
- HEC
- CRC
- Data decryption
- Data dewhitening

#### 3.2 Bluetooth 4.0 + EDR Features

The CYW20713 supports Bluetooth 4.0 + EDR, including the following options:

- Whitelist size of 25
- Enhanced Power Control
- HCI Read Encryption Key Size command

The CYW20713 provides full support for Bluetooth 2.1 + EDR additional features:

- Secure simple pairing (SSP)
- Encryption pause resume (EPR)
- Enhance inquiry response (EIR)
- Link supervision time out (LSTO)
- Sniff subrating (SSR)
- Erroneous data (ED)
- Packet boundary flag (PBF)

#### 3.3 Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number, based on the link controller state, Bluetooth clock, and device address.

### 3.4 Link Control Layer

The link control layer is part of the Bluetooth link control functions implemented in dedicated logic in the link control unit (LCU). This layer consists of the Command Controller that takes commands from the software and other controllers that are activated or configured by the Command Controller to perform the link control tasks.

There are two major states—standby and connection. Each task establishes a different state in the Bluetooth link controller. In addition, there are eight substates—page, page scan, inquiry, inquiry scan, park, sniff subrate, and hold.

### 3.5 Test Mode Support

The CYW20713 fully supports Bluetooth Test Mode, including the transmitter tests, normal and delayed Loopback tests, and the reduced hopping sequence.

In addition to the standard Bluetooth Test mode, the device supports enhanced testing features to simplify RF debugging and qualification and type approval testing.

These test features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Directs receiver output to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant bit stream transmission
  - Unmodulated, 8-bit fixed pattern, PRBS-9, or PRBS-15
  - Enables modulated signal measurements with standard RF test equipment
- Packetized connectionless transmitter test
  - Hopping or fixed frequency
  - Multiple packet types supported
  - Multiple data patterns supported
- Packetized connectionless receiver test
  - Fixed frequency
  - Multiple packet types supported
  - Multiple data patterns supported

### 3.6 Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked through power management registers or packet handling in the baseband core. This section contains descriptions of the PMU features.

#### 3.6.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions, accordingly.

#### 3.6.2 Host Controller Power Management

The host can place the device in a sleep state, in which all nonessential blocks are powered off and all nonessential clocks are disabled. Power to the digital core is maintained so that the state of the registers and RAM is not lost. In addition, the LPO clock is applied to the internal sleep controller so that the chip can wake automatically at a specified time or based on signaling from the host. The goal is to limit the current consumption to a minimum, while maintaining the ability to wake up and resume a connection with minimal latency.

If a scan or sniff session is enabled while the device is in Sleep mode, the device automatically will wake up for the scan/sniff event, then go back to sleep when the event is done. In this case, the device uses its internal LPO-based timers to trigger the periodic wake up. While in Sleep mode, the transports are idle. However, the host can signal the device to wake up at any time. If signaled to wake up while a scan or sniff session is in progress, the session continues but the device will not sleep between scan/sniff events. Once Sleep mode is enabled, the wake signaling mechanism can also be thought of as a sleep signaling mechanism, since removing the wake status will often cause the device to sleep.

In addition to a Bluetooth device wake signaling mechanism, there is a host wake signaling mechanism. This feature provides a way for the Bluetooth device to wake up a host that is in a reduced power state.

There are two mechanisms for the device and the host to signal wake status to each other:

|  |   |
|--|---|
| Bluetooth WAKE (BT_WAKE) and Host WAKE (and HOST_WAKE) signaling | The BT_WAKE pin (GPIO_0) allows the host to wake the BT device, and HOST_WAKE (GPIO_1) is an output that allows the BT device to wake the host.   |
| In-band UART signaling   | The CTS and RTS signals of the UART interface are used for BT wake (CTS) and Host wake (RTS) functions in addition to their normal function on the UART interface. Note that this applies for both H4 and H5 protocols. |

When running in SPI mode, the CYW20713 has a mode where it enters Sleep mode when there is no activity on the SPI interface for a specified (programmable) amount of time. Idle mode is detected when the SPI\_CSN is left deasserted. Whether to sleep on an idle interface and the amount of time to wait before entering Sleep mode can be programmed by the host. Once the CYW20713 enters sleep, the host can wake it by asserting SPI\_CSN. If the host decides to sleep, the CYW20713 will wake up the host by asserting SPI\_INT when it has data for it.

**Note:** Successful operation of the power management handshaking signals requires coordinated support between the device firmware and the host software

**Table 2. Power Control Pin Summary**

| Pin                | Direction               | Description  |
|--------------------|-------------------------|--|
| BT_WAKE (GPIO_0)   | Host output<br>BT input | Bluetooth device wake-up: Signal from the host to the Bluetooth device that the host requires attention.<br><ul style="list-style-type: none"> <li>■ Asserted = Bluetooth device must wake up or remain awake.</li> <li>■ Deasserted = Bluetooth device may sleep when sleep criteria are met.</li> </ul> The polarity of this signal is software configurable and can be asserted high or low. By default, BT_WAKE is active-low (if BT-WAKE is low it requires the device to wake up or remain awake). |
| HOST_WAKE (GPIO_1) | BT output<br>Host input | Host wake-up. Signal from the Bluetooth device to the host indicating that Bluetooth device requires attention.<br><ul style="list-style-type: none"> <li>■ Asserted = Host device must wake up or remain awake.</li> <li>■ Deasserted = Host device may sleep when sleep criteria are met.</li> </ul> The polarity of this signal is software configurable and can be asserted high or low.   |
| CLK_REQ (GPIO_5)   | BT output               | Clock request<br><ul style="list-style-type: none"> <li>■ Asserted = External clock reference required</li> <li>■ Deasserted = External clock reference may be powered down</li> </ul> The polarity of CLK_REQ is software configurable and can be set to active high (TM0 = 1) or active low (TM0 = 0).   |
| REG_EN             | BT input                | Enables the internal preregulator and main regulator outputs. REG_EN is active-high.<br><ul style="list-style-type: none"> <li>■ 1 = Enabled</li> <li>■ 0 = Disabled</li> </ul>  |

**3.6.3 Bluetooth Baseband Core Power Management**

The device provides the following low-power operations for the Bluetooth Baseband Core (BBC):

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth specified low-power connection modes—Sniff, Hold, and Park. While in these low-power connection modes, the device runs on the Low Power Oscillator and wakes up after a predefined time period.

### Backdrive Protection

The CYW20713 provides a backdrive protection feature that allows the device to be turned off while the host and other devices in the system remain operational. When the device is not needed in the system, VDD\_RF and VDDC are shut down and VDDO remains powered. This allows the device to be effectively off, while keeping the I/O pins powered so that they do not draw extra current from other devices connected to the I/O.

#### Notes:

VDD\_RF collectively refers to the VDDTF, VDDIF, VDDLNA, VDDPX, and VDDRF RF power supplies.  
Never apply voltage to I/O pins if VDDO is not applied.

During the low power shutdown state and as long as VDDO remains applied to the device, all outputs are tristated and all digital and analog clocks are disabled. Input voltages must remain within the limits defined for normal operation. This is done to either prevent current draw and back loading on digital signals in the system. It also enables the device to be fully integrated in an embedded device and take full advantage of the lowest power savings modes. If VDDC is powered up externally (not connected to VREG), VDDC requires 750K ohms to ground during low-power shutdown. If VDDC is powered up by VREG, VDDC does not require 750K ohms to ground because the internal main LDO has about 750 K ohms to ground when turned off.

Several signals, including the frequency reference input (XTAL\_IN) and external LPO input (LPO\_IN), are designed to be high-impedance inputs that will not load down the driving signal, even if VDDO power is not applied to the chip. The other signals with back drive prevention are RST\_N, COEX\_OUT0, COEX\_OUT1, COEX\_IN, PCM\_SYNC, PCM\_CLK, PCM\_OUT, PCM\_IN, UART\_RTS\_N, UART\_CTS\_N, UART\_RXD, UART\_TXD, GPIO\_0, GPIO\_1, GPIO\_2, GPIO\_4, GPIO\_7, CFG\_SEL, and OTP\_DIS.

All other IO signals must remain at VSS until VDDO is applied. Failing to do this can result in unreliable startup behavior.

When powered on, using REG\_EN is the same as applying power to the CYW20713. The device does not have information about its state before being powered-down.

### 3.7 Adaptive Frequency Hopping

The CYW20713 supports host channel classification and dynamic channel classification Adaptive Frequency Hopping (AFH) schemes, as defined in the Bluetooth specification.

Host channel classification enables the host to set a predefined hopping map for the device to follow.

If dynamic channel classification is enabled, the device gathers link quality statistics on a channel-by-channel basis to facilitate channel assessment and channel map selection. To provide a more accurate frequency hop map, link quality is determined using both RF and baseband signal processing.

### 3.8 Collaborative Coexistence

The CYW20713 provides extensions and collaborative coexistence to the standard Bluetooth AFH for direct communication with WLAN devices. Collaborative coexistence enables WLAN and Bluetooth to operate simultaneously in a single device. The device supports industry-standard coexistence signaling, including 802.15.2, and supports Cypress and third-party WLAN solutions.

Using a multi-tiered prioritization approach, relative priorities between data types and applications can be set. This approach maximizes the performance-WLAN data throughput vs. voice quality vs. link performance.

A PA shutdown pin is available to allow full external control of the RF output for other types of coexistence, such as WIMAX.

### 3.9 Serial Enhanced Coexistence Interface

The Serial Enhanced Coexistence Interface (Serial ECI or SECI) is a proprietary Cypress interface between Cypress WLAN devices and Bluetooth devices. It is an optional replacement to the legacy 3- or 4-wire coexistence feature, which is also available.

The following key features are associated with the interface:

- Enhanced coexistence data can be exchanged over SECI\_IN and SECI\_OUT.
- It supports generic UART communication between WLAN and Bluetooth devices.
- To conserve power, it is disabled when inactive.
- It supports automatic resynchronization upon waking from sleep mode.
- It supports a baud rate of up to 4 Mbps.

#### 3.9.1 SECI Advantages

The advantages of the SECI over the legacy 3-wire coexistence interface are:

- Only two wires are required: SECI\_IN and SECI\_OUT.
- Up to 48-bits of coexistence data can be exchanged.

Previous Cypress stand-alone Bluetooth devices such as the CYW2070 supported only a 3-wire or 4-wire coexistence interface. Previous Cypress WLAN and Bluetooth combination devices such as the CYW4325, CYW4329, and CYW4330 support an internal parallel enhanced coexistence interface for more efficient WLAN and Bluetooth information exchange. The SECI allows enhanced coexistence information to be passed to a companion Cypress WLAN chip through a serial interface using fewer I/O than the 3-wire coexistence scheme.

The 48-bits of the SECI significantly enhance WLAN and Bluetooth coexistence by sharing such information as frequencies used and radio usage times. The exact contents of the SECI are Cypress confidential.

#### 3.9.2 SECI I/O

The CYW20713 does not have dedicated SECI\_IN or SECI\_OUT pins, but the two pin functions can be mapped to the following digital I/O: the UART, GPIO, SPIM (or BSC), PCM, and COEX pins. Pin function mapping is controlled by the config file that is either stored in NVRAM or downloaded directly into on-chip RAM from the host.

## 4. Microprocessor Unit

The CYW20713 microprocessor unit runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is based on the ARM7TDMIS 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The microprocessor also includes 384 KB of ROM memory for program storage and boot ROM, 112 KB of RAM for data scratch-pad, and patch RAM code.

The internal boot ROM provides flexibility during power-on reset to enable the same device to be used in various configurations, including automatic host transport selection from SPI or UART, with or without external NVRAM. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. These patches can be downloaded from the host to the device through the SPI or UART transports, or using external NVRAM. The device can also support the integration of user applications and profiles using an external serial flash memory.

### 4.1 NVRAM Configuration Data and Storage

#### 4.1.1 Serial Interface

The CYW20713 includes an SPI master controller that can be used to access serial flash memory. The SPI master contains an AHB slave interface, transmit and receive FIFOs, and the SPI core PHY logic. Data is transferred to and from the module by the system CPU. DMA operation is not supported.

The CYW20713 supports serial flash vendors Atmel, MXIC, and Numonyx. The most commonly used parts from two of these vendors are:

- AT25BCM512B, manufactured by Atmel
- MX25V512ZUI-20G, manufactured by MXIC

### 4.2 EEPROM

The CYW20713 includes a Broadcom Serial Control (BSC) master interface. The BSC interface supports low-speed and fast mode devices and is compatible with I<sup>2</sup>C slave devices. Multiple I<sup>2</sup>C master devices and flexible wait state insertion by the master interface or slave devices are not supported. The CYW20713 provides 400 kHz, full speed clock support.

The BSC interface is programmed by the CPU to generate the following BSC transfer types on the bus:

- Read-only
- Write-only
- Combined read/write
- Combined write-read

NVRAM may contain configuration information about the customer application, including the following:

- Fractional-N information
- BD\_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data

### 4.3 External Reset

The CYW20713 has an integrated power-on reset circuit which completely resets all circuits to a known power on state. This action can also be driven by an external reset signal, which can be used to externally control the device, forcing it into a power-on reset state. The RST\_N signal input is an active-low signal for all versions of the CYW20713. The CYW20713 requires an external pull-up resistor on the RST\_N input. Alternatively, the RST\_N input can be connected to REG\_EN or driven directly by a host GPIO.



#### 4.4 One-Time Programmable Memory

The CYW20713 includes a One-Time Programmable (OTP) memory, allowing manufacturing customization and avoiding the need for an on-board NVRAM. If customization is not required, then the OTP does not need to be programmed. Whether the OTP is programmed or not, it is disabled after the boot process completes to save power.

The OTP size is 128 bytes.

The OTP is designed to store a minimal amount of information. Aside from OTP data, most user configuration information will be downloaded into RAM after the CYW20713 boots up and is ready for host transport communication. The OTP contents are limited to:

- Parameters required prior to downloading user configuration to RAM.
- Parameters unique to a customer design.

##### 4.4.1 Contents

The following are typical parameters programmed into the OTP memory:

- BD\_ADDR
- Software license key
- Output power calibration
- Frequency trimming
- Initial status LED drive configuration

The OTP contents also include a static error correction table to improve yield during the programming process as well as forward error correction codes to eliminate any long-term reliability problems. The OTP contents associated with error correction are not visible by customers.

##### 4.4.2 Programming

OTP memory programming takes place through a combination of Cypress software integrated with the manufacturing test software and code embedded in CYW20713 firmware.

Programming the OTP requires a 3.3V supply. The OTP programming supply comes from the VDDO pin. The OTP power supply can be as low as 1.8V in order to read the OTP contents. OTP\_DIS is brought out to a pin on the WLBGA package but not on the FPBGA package, and is internally pulled low. If the OTP\_DIS pin is left floating or externally pulled low, then the OTP will be enabled. If the OTP\_DIS pins is externally pulled high, then the OTP will be disabled.

## 5. Peripheral Transport Unit

This section discusses the PCM, UART, and SPI peripheral interfaces. The CYW20713 has a 1040 byte transmit and receive FIFO, which is large enough to hold the entire payload of the largest EDR BT packet (3-DH5).

### 5.1 PCM Interface

The CYW20713 PCM interface can connect to linear PCM codec devices in master or slave mode. In master mode, the device generates the PCM\_BCLK and PCM\_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface as inputs to the device.

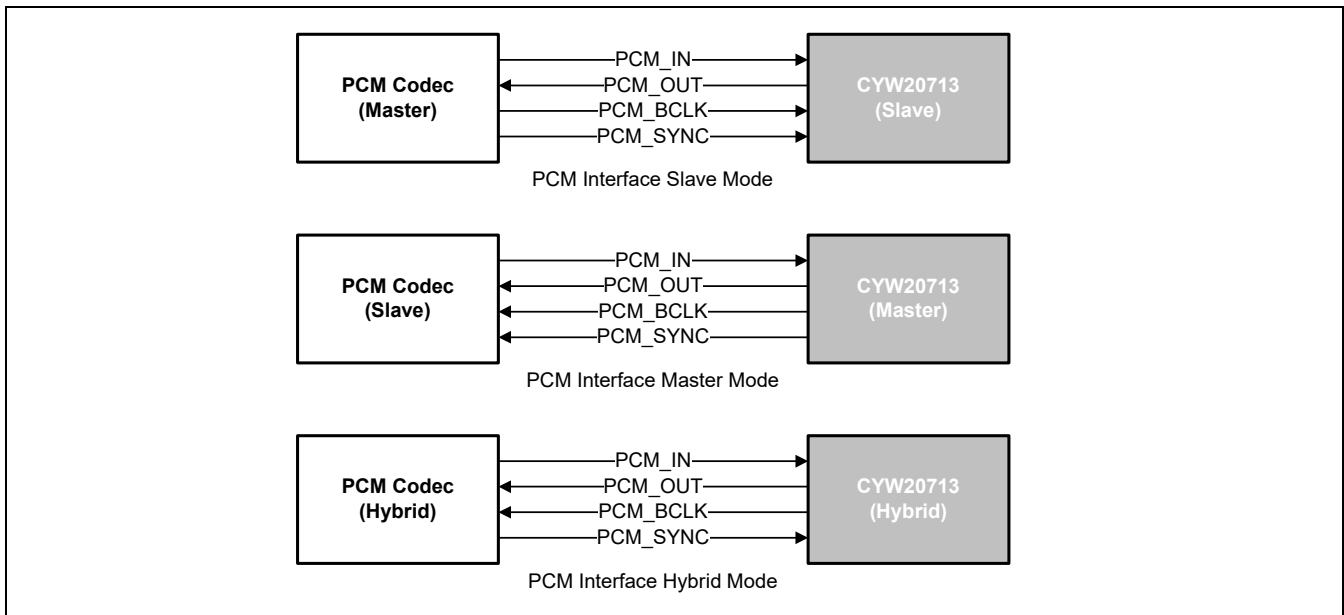
The device supports up to three SCO or eSCO channels through the PCM interface and each channel can be independently mapped to any available slot in a frame.

The host can adjust the PCM interface configuration using vendor-specific HCI commands or it can be setup in the configuration file.

#### 5.1.1 System Diagram

Figure 5 shows options for connecting the device to a PCM codec device as a master or a slave.

**Figure 5. PCM Interface with Linear PCM Codec**



**5.1.2 Slot Mapping**

The device supports up to three simultaneous, full-duplex SCO or eSCO channels. These channels are time-multiplexed onto the PCM interface using a time slotting scheme based on the audio sampling rate, as described in [Table 3](#).

**Table 3. PCM Interface Time Slotting Scheme**

| Audio Sample Rate | Time Slotting Scheme  |                |      |     |   |     |   |      |   |      |   |      |    |
|-------------------|---|----------------|------|-----|---|-----|---|------|---|------|---|------|----|
| 8 kHz             | The number of slots depends on the selected interface rate, as follows:<br><table border="1"> <thead> <tr> <th>Interface rate</th> <th>Slot</th> </tr> </thead> <tbody> <tr> <td>128</td> <td>1</td> </tr> <tr> <td>256</td> <td>2</td> </tr> <tr> <td>512</td> <td>4</td> </tr> <tr> <td>1024</td> <td>8</td> </tr> <tr> <td>2048</td> <td>16</td> </tr> </tbody> </table> | Interface rate | Slot | 128 | 1 | 256 | 2 | 512  | 4 | 1024 | 8 | 2048 | 16 |
| Interface rate    | Slot  |                |      |     |   |     |   |      |   |      |   |      |    |
| 128               | 1   |                |      |     |   |     |   |      |   |      |   |      |    |
| 256               | 2   |                |      |     |   |     |   |      |   |      |   |      |    |
| 512               | 4   |                |      |     |   |     |   |      |   |      |   |      |    |
| 1024              | 8   |                |      |     |   |     |   |      |   |      |   |      |    |
| 2048              | 16  |                |      |     |   |     |   |      |   |      |   |      |    |
| 16 kHz            | The number of slots depends on the selected interface rate, as follows:<br><table border="1"> <thead> <tr> <th>Interface rate</th> <th>Slot</th> </tr> </thead> <tbody> <tr> <td>256</td> <td>1</td> </tr> <tr> <td>512</td> <td>2</td> </tr> <tr> <td>1024</td> <td>4</td> </tr> <tr> <td>2048</td> <td>8</td> </tr> </tbody> </table>                                     | Interface rate | Slot | 256 | 1 | 512 | 2 | 1024 | 4 | 2048 | 8 |      |    |
| Interface rate    | Slot  |                |      |     |   |     |   |      |   |      |   |      |    |
| 256               | 1   |                |      |     |   |     |   |      |   |      |   |      |    |
| 512               | 2   |                |      |     |   |     |   |      |   |      |   |      |    |
| 1024              | 4   |                |      |     |   |     |   |      |   |      |   |      |    |
| 2048              | 8   |                |      |     |   |     |   |      |   |      |   |      |    |

Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

**5.1.3 Wideband Speech**

The CYW20713 provides support for wideband speech (WBS) in two ways:

- **Transparent mode:** The host encodes WBS packets and the encoded packets are transferred over the PCM bus for SCO or eSCO voice connections. In Transparent mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 kbps bit rate.
- **On-chip SmartAudio® technology:** The CYW20713 can perform Subband-Codec (SBC) encoding and decoding of linear 16 bits at 16 kHz (256 kbps rate) transferred over the PCM bus.

**5.1.4 Frame Synchronization**

The device supports both short and long frame synchronization types in both master and slave configurations. In short frame synchronization mode, the frame synchronization signal is an active-high pulse at the 8 kHz audio frame rate (which is a single bit period in width) and synchronized to the rising edge of the bit clock. The PCM slave expects PCM\_SYNC to be high on the falling edge of the bit clock and the first bit of the first slot to start at the next rising edge of the clock. In the long frame synchronization mode, the frame synchronization signal is an active-high pulse at the 8 kHz audio frame rate. However, the duration is 3-bit periods and the pulse starts coincident with the first bit of the first slot.

**5.1.5 Data Formatting**

The device can be configured to generate and accept several different data formats. The device uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits is configurable to support various data formats on the PCM interface. The remaining three bits are ignored on the input, and may be filled with zeros, ones, a sign bit, or a programmed value on the output. The default format is 13-bit two's complement data, left justified, and clocked most significant bit first.

**5.2 HCI Transport Detection Configuration**

The CYW20713 supports the following interface types for the HCI transport from the host:

- UART (H4 and H5)
- SPI

Only one host interface can be active at a time. The firmware performs a transport detect function at boot-time to determine which host is the active transport. It can auto-detect the UART interface, but the SPI interface must be selected by strapping the SCL pin to 0. The complete algorithm is summarized as follows:

1. Determine if SCL is pulled low. If it is, select SPI as HCI host transport.
2. Determine if any local NVRAM contains a valid configuration file. If it does and a transport configuration entry is present, select the active transport according to entry, and then exit the transport detection routine.
3. Look for CTS\_N = 0 on the UART interface. If it is present, select UART.
4. Repeat [Step 3](#) until transport is determined.

**5.3 UART Interface**

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate can be selected via a vendor-specific UART HCI command. The interface supports Bluetooth UART HCI (H4) specifications. The default baud rate for H4 is 115.2 Kbaud.

The following baud rates are supported:

|         |           |           |
|---------|-----------|-----------|
| ■ 9600  | ■ 115200  | ■ 2000000 |
| ■ 14400 | ■ 230400  | ■ 3000000 |
| ■ 19200 | ■ 460800  | ■ 3250000 |
| ■ 28800 | ■ 921600  | ■ 3692000 |
| ■ 38400 | ■ 1444444 | ■ 4000000 |
| ■ 57600 | ■ 1500000 |           |

Normally, the UART baud rate is set by a configuration record downloaded after reset or by automatic baud rate detection. The host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is provided through a vendor-specific command.

The CYW20713 UART operates with the host UART correctly, provided the combined baud rate error of the two devices is within ±2%.

*5.3.1 HCI 3-Wire Transport (UART H5)*

The CYW20713 supports H5 UART transport for serial UART communications. H5 reduces the number of signal lines required by eliminating CTS and RTS, when compared to H4. In addition, in-band sleep signaling is supported over the same interface so that the 4-wire UART and the 2-wire sleep signaling interface can be reduced to a 2-wire UART interface, saving four I/Os on the host.

H5 requires the use of an external LPO. CTS must be pulled low.

**5.4 SPI**

The CYW20713 supports a slave SPI HCI transport with an input clock range of up to 16 MHz. Higher clock rates may be possible. The physical interface between the SPI master and the CYW20713 consists of the four SPI signals (SPI\_CSB, SPI\_CLK, SPI\_SI, and SPI\_SO) and one interrupt signal (SPI\_INT). The CYW20713 can be configured to accept active-low or active-high polarity on the SPI\_CSB chip select signal. It can also be configured to drive an active-low or active-high SPI\_INT interrupt signal. Bit ordering on the SPI\_SI and SPI\_SO data lines can be configured as either little-endian or big-endian. Additionally, proprietary sleep mode, half-duplex handshaking is implemented between the SPI master and the CYW20713.

SPI\_INT is required to negotiate the start of a transaction. The SPI interface does not require flow control in the middle of a payload. The FIFO is large enough to handle the largest packet size. Only the SPI master can stop the flow of bytes on the data lines, since it controls SPI\_CSB and SPI\_CLK. Flow control should be implemented in higher layer protocols.

## 6. Frequency References

The CYW20713 uses two different frequency references for normal and low-power operational modes. An external crystal or frequency reference driven by a Temperature Compensated Crystal Oscillator (TCXO) signal is used to generate the radio frequencies and normal operation clocking. Either an external 32.768 kHz or fully integrated internal Low-Power Oscillator (LPO) is used for low-power mode timing.

### 6.1 Crystal Interface and Clock Generation

The CYW20713 uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing, enabling it to operate from any of a multitude of frequency sources. The source can be external, such as a TCXO, or a crystal interfaced directly to the device.

The default frequency reference setting is for a 20 MHz crystal or TCXO. The signal characteristics for the crystal interface are listed in [Table 4 on page 20](#).

**Table 4. Crystal Interface Signal Characteristics**

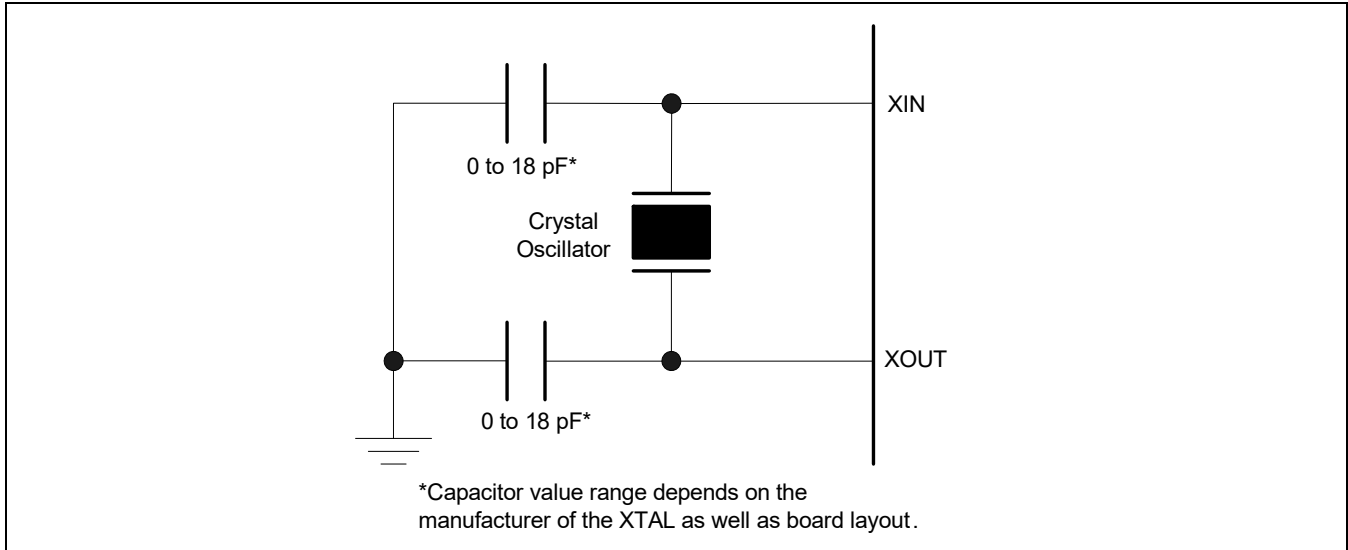
| Parameter   | Crystal   | External Frequency Reference  | Units             |
|---|---|---|-------------------|
| Acceptable frequencies  | 12–52 MHz in 2 ppm <sup>a</sup> steps   | 12–52 MHz in 2 ppm <sup>a</sup> steps   | –                 |
| Crystal load capacitance  | 12 (typical)  | N/A   | pF                |
| ESR   | 60 (max)  | –   | Ω                 |
| Power dissipation   | 200 (max)   | –   | μW                |
| Input signal amplitude  | N/A   | 400 to 2000<br>2000 to 3300 (requires a 10 pF DC blocking capacitor to attenuate the signal)    | mV <sub>p-p</sub> |
| Signal type   | N/A   | Square-wave or sine-wave  | –                 |
| Input impedance   | N/A   | ≥ 1<br>≤ 2  | MΩ<br>pF          |
| Phase noise   | N/A   | –   | –                 |
| @ 1 kHz   | N/A   | < –120 <sup>b</sup>   | dBc/Hz            |
| @ 10 kHz  | N/A   | < –131 <sup>b</sup>   | dBc/Hz            |
| @ 100 kHz   | N/A   | < –136 <sup>b</sup>   | dBc/Hz            |
| @ 1 MHz   | N/A   | < –136 <sup>b</sup>   | dBc/Hz            |
| Auto-detection frequencies when using external LPO <sup>c</sup> | 12, 13, 14.4, 15.36, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 33.6, 37.4, and 38.4 | 12, 13, 14.4, 15.36, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 33.6, 37.4, and 38.4 | MHz               |
| Tolerance without frequency trimming <sup>d</sup>               | ±20   | ±20   | ppm               |
| Initial frequency tolerance trimming range                      | ±50   | ±50   | ppm               |

- a. The frequency step size is approximately 80 Hz resolution.
- b. With a 26 MHz reference clock. For a 13 MHz clock, subtract 6 dB. For a 52 MHz clock, add 6 dB.
- c. Auto-detection of the frequency requires the crystal or external frequency reference to have less than ±50 ppm of variation and also requires an external LPO frequency which has less than ±250 ppm of variation at the time of detection.
- d. AT-Cut crystal or TXCO recommended.

### 6.2 Crystal Oscillator

The CYW20713 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator, including all external components, is shown in [Figure 6](#).

**Figure 6. Recommended Oscillator Configuration**

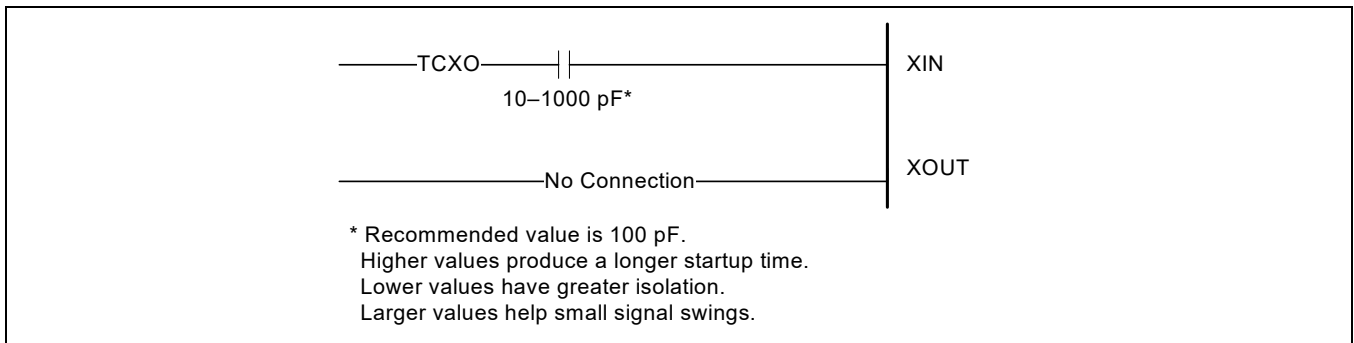


### 6.3 External Frequency Reference

An external frequency reference generated by a TCXO signal that may be directly connected to the crystal input pin on the CYW20713, as shown in [Figure 7](#). The external frequency reference input is designed to not change loading on the TCXO when the CYW20713 is powered up or powered down.

When using the CYW20713 with the TXCO OR gate option, GPIO 6 must be driven active high or active low. Excessive leakage current results if GPIO6 is allowed to float.

**Figure 7. Recommended TCXO Connection**



#### 6.3.1 TCXO Clock Request Support

If the application utilizes an external TCXO as a clock reference, the CYW20713 provides a clock request output to allow the system to power off the TCXO when not in use. Optionally, some packages support a TCXO OR function that allows a clock request in the system to be combined with the CYW20713 clock request output, without requiring an extra component on the board.

**Clock Request Output**

The CLK\_REQ signal on the GPIO\_5 lead is asserted whenever the CYW20713 is in the Awake state. It is deasserted when in Sleep state. When the CYW20713 is sleeping, it uses an LPO clock (external or internal) as the timing reference.

The TM0 lead controls the polarity of the CLK\_REQ output on GPIO\_5 as follows:

- TM0 = 0      CLK\_REQ is active low
- TM0 = 1      CLK\_REQ is active high

If the clock request feature is not desired, GPIO\_5 can be configured for other functions.

**TCXO OR Option**

The CYW20713 has an optional feature that allows the application to perform a logical OR function on a system TCXO clock request signal and the CYW20713 clock request to form one clock request output to the TCXO device. This logical OR function is embedded in the pad ring so that it is available at any time, as long as the pad ring is receiving a VDDO supply. The function works even if the CYW20713's digital core is sleeping or completely powered off.

To use this feature, the TCXO\_MODE lead must be tied high. In this mode, the GPIO\_6 lead functions as the external clock request input. Without TCXO\_MODE asserted, GPIO\_5 functions as the clock request output (based only on the internal clock requirements of the CYW20713) and the state of GPIO\_6 is ignored.

As mentioned earlier, the TM0 lead controls the polarity of the CLK\_REQ output on GPIO\_5. However, it assumes that GPIO\_6 input polarity is already consistent with the desired polarity on GPIO\_5/CLK\_REQ. Therefore, when TM0 is 1 for an active high output, the function is a simple OR between the external GPIO\_6 and the internal clock request state. However, when TM0 is 0 for an active low output, the logic inverts the internal clock request signal and performs an AND between it and the GPIO\_6 input. Even though it is using an OR gate, it still provides a logical AND on the two clock request states.

Since the logic assumes that it is also active low (similar to GPIO\_5 output), it does not invert the GPIO\_6 input first. [Table 5 on page 22](#) shows the truth table.

**Table 5. Truth Table**

| GPIO_6<br>CLK_REQ_IN | Internal Clock Request State<br>(0 = sleep) | TM0<br>(0 = active low output) | GPIO_5<br>CLK_REQ |
|----------------------|---|--------------------------------|-------------------|
| 0                    | 0   | 0                              | 0                 |
| 0                    | 1   | 0                              | 0                 |
| 1                    | 0   | 0                              | 1                 |
| 1                    | 1   | 0                              | 0                 |
| 0                    | 0   | 1                              | 0                 |
| 0                    | 1   | 1                              | 1                 |
| 1                    | 0   | 1                              | 1                 |
| 1                    | 1   | 1                              | 1                 |

**Package Options and TCXO Mode**

Only a few package options bring out TM0 to balls, allowing the application to configure them. In most packages, these pins are already configured.

Table 6 lists available package options.

**Table 6. Package Options**

| Part Number      | Package Description | TM0             |
|------------------|---------------------|-----------------|
| CYW20713A1KUFBXG | 50-ball FPBGA       | Brought to ball |
| CYW20713A1KUBG   | 42-bump WLPGA       | 1               |

**6.4 Frequency Selection**

Any frequency within the range specified for the crystal and TCXO reference can be used. These frequencies include standard handset reference frequencies (12, 13, 14.4, 15.36, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 33.6, 37.4, and 38.4 MHz) and any frequency between these reference frequencies, as desired by the system designer. Since bit timing is derived from the reference frequency, the CYW20713 must have the reference frequency set correctly in order for the UART and PCM interfaces to function properly.

The CYW20713 reference frequency can be set in one of three ways.

- Use the default 20 MHz frequency
- Designate the reference frequency in external NVRAM
- Auto-detect the standard handset reference frequencies using an external LPO clock

The CYW20713 is set to a default frequency of 20 MHz at the factory. For a typical design using a crystal, it is recommended that the default frequency be used, since this simplifies the design by removing the need for either external NVRAM or external LPO clock.

If the application requires a frequency other than the default, the value can be stored in an external NVRAM. Programming the reference frequency in NVRAM provides the maximum flexibility in the selection of the reference frequency, since any frequency within the specified range for crystal and external frequency reference can be used. During power-on reset (POR), the device downloads the parameter settings stored in NVRAM, which can be programmed to include the reference frequency and frequency trim values. Typically, this is how a PC Bluetooth application is configured.

For applications such as handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the CYW20713 automatically detects the reference frequency and programs itself to the correct reference frequency. In order for auto-frequency detection to work properly, the CYW20713 must have a valid and stable 32.768 kHz external LPO clock present during POR. This eliminates the need for NVRAM in applications where the external LPO clock is available and an external NVRAM is typically not used.

**6.5 Frequency Trimming**

The CYW20713 uses a fractional-N synthesizer to digitally fine-tune the frequency reference input to within  $\pm 2$  ppm tuning accuracy. This trimming function can be applied to either the crystal or an external frequency source such as a TCXO. Unlike the typical crystal-trimming methods used, the CYW20713 changes the frequency using a fully digital implementation and is much more stable and unaffected by crystal characteristics or temperature. Input impedance and loading characteristics remain unchanged on the TCXO or crystal during the trimming process and are unaffected by process and temperature variations.

The option to use or not use frequency trimming is based on the system designer’s cost trade-off between bill-of-materials (BOM) cost of the crystal and the added manufacturing cost associated with frequency trimming. The frequency trimming value can either be stored in the host and written to the CYW20713 as a vendor-specific HCI command or stored in NVRAM and subsequently recalled during POR.

Frequency trimming is not a substitute for the poor use of tuning capacitors at an crystal oscillator (XTAL). Occasionally, trimming can help alleviate hardware changes.



## 6.6 LPO Clock Interface

The LPO clock is the second frequency reference that the CYW20713 uses to provide low-power mode timing for park, hold, and sniff. The LPO clock can be provided to the device externally, from a 32.768 kHz source or the CYW20713 can operate using the internal LPO clock.

The LPO can be internally driven from the main clock. However, sleep current will be impacted.

The accuracy of the internal LPO limits the maximum park, hold, and sniff intervals.

**Table 7. External LPO Signal Requirements**

| Parameter   | External LPO Clock       | Units    |
|---|--------------------------|----------|
| Nominal input frequency                                 | 32.768                   | kHz      |
| Frequency accuracy                                      | ±250                     | ppm      |
| Input signal amplitude                                  | 200 to 3600              | mVp-p    |
| Signal type   | Square-wave or sine-wave | –        |
| Input impedance (when power is applied or power is off) | >100<br><5               | kΩ<br>pF |

## 7. Pin Information

### 7.1 Pin Descriptions

Table 8. CYW20713 Signal Descriptions

| Signal                    | FPBGA 50-Ball | WLBGA 42-Bump | I/O | Power Do-<br>main | Description   |
|---------------------------|---------------|---------------|-----|-------------------|---|
| <b>Radio</b>              |               |               |     |                   |   |
| RES                       | G4            | D6            | O   | VDD_RF            | External calibration resistor, 15 kΩ @ 1%   |
| RFP                       | D1            | C7            | I/O | VDD_RF            | RF I/O antenna port   |
| XIN                       | G2            | F5            | I   | VDD_RF            | Crystal or reference input  |
| XOUT                      | G3            | E5            | O   | VDD_RF            | Crystal oscillator output   |
| <b>Analog</b>             |               |               |     |                   |   |
| LPO_IN                    | A4            | B4            | I   | VDDRF             | External LPO input  |
| <b>Voltage Regulators</b> |               |               |     |                   |   |
| REG_EN                    | B2            | B5            | I   | VDDO              | HV LDO and main enable  |
| VBAT                      | A3            | A5            | I   | N/A               | HV LDO input  |
| VREGHV                    | A2            | A6            | I/O | N/A               | HV LDO output: main LDO input   |
| VREG                      | A1            | A7            | O   | N/A               | Main LDO output   |
| <b>Straps</b>             |               |               |     |                   |   |
| RST_N                     | B4            | C5            | I   | VDDO              | Active-low reset input  |
| TM0                       | C4            | –             | I   | VDDO              | Clock request polarity select   |
| TM1                       | –             | –             | I   | VDDO              | Internally connected to ground  |
| TM2                       | F3            | C6            | I   | VDDO              | Reserved: connect to ground.  |
| <b>Digital I/O</b>        |               |               |     |                   |   |
| GPIO_0                    | B5            | C3            | I/O | VDDO              | GPIO/BT_WAKE  |
| GPIO_1                    | B3            | B3            | I/O | VDDO              | GPIO/HOST_WAKE  |
| GPIO_2                    | –             | –             | I/O | VDDO              | GPIO  |
| GPIO_3                    | –             | –             | I/O | VDDO              | GPIO/LINK_IND<br><b>Note:</b> Can be configured for active high or low as well as open drain.   |
| GPIO_4                    | –             | –             | I/O | VDDO              | GPIO  |
| GPIO_5                    | E6            | F4            | I/O | VDDO              | GPIO/CLK_REQ<br>TCXO-OR Function Out available on some packages. See <a href="#">Section 10.: "Ordering Information," on page 50.</a> |
| GPIO_6                    | E3            | D5            | I/O | VDDO              | GPIO<br>TCXO-OR Function In available on some packages. See <a href="#">Section 10.: "Ordering Information," on page 50.</a>          |
| GPIO_7                    | B7            | –             | I/O | VDDO              | DETATCH/CARD_DETECT   |
| UART_RXD                  | D8            | D2            | I/O | VDDO              | UART receive data   |
| UART_TXD                  | C8            | C2            | I/O | VDDO              | UART transmit data  |
| UART_RTS_N                | D7            | F2            | I/O | VDDO              | UART request to send output   |
| UART_CTS_N                | E8            | E3            | I/O | VDDO              | UART clear to send input  |

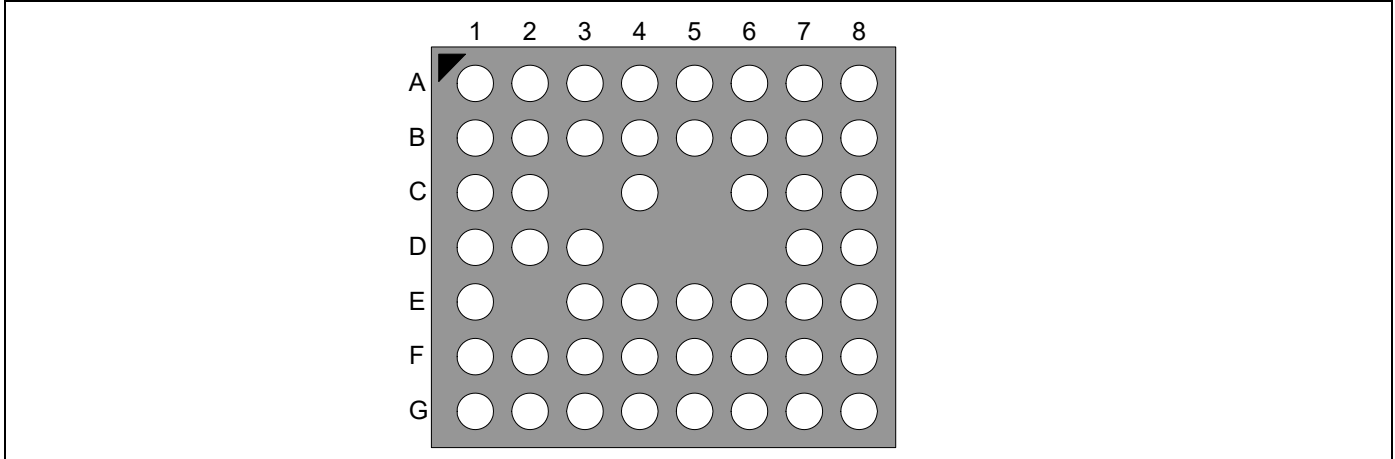
**Table 8. CYW20713 Signal Descriptions (Cont.)**

| Signal          | FPBGA 50-Ball | WLBGA 42-Bump | I/O | Power Do-main | Description   |
|-----------------|---------------|---------------|-----|---------------|---|
| SCL             | F7            | E1            | I/O | VDDO          | I <sup>2</sup> C clock                                |
| SDA             | E7            | D1            | I/O | VDDO          | I <sup>2</sup> C data                                 |
| SPIM_CLK        | A8            | C1            | I/O | VDDO          | Serial flash SPI clock                                |
| SPIM_CS_N       | C7            | E2            | I/O | VDDO          | Serial flash active-low chip select                   |
| PCM_IN          | F6            | D4            | I/O | VDDO          | PCM/I2S data input                                    |
| PCM_OUT         | G6            | E4            | I/O | VDDO          | PCM/I2S data output                                   |
| PCM_CLK         | F4            | C4            | I/O | VDDO          | PCM/I2S clock   |
| PCM_SYNC        | F5            | A4            | I/O | VDDO          | PCM sync/I2S word select                              |
| COEX_IN         | B6            | –             | I/O | VDDO          | Coexistence input                                     |
| COEX_OUT0       | E4            | –             | I/O | VDDO          | Coexistence output                                    |
| COEX_OUT1       | E5            | –             | I/O | VDDO          | Coexistence output                                    |
| OTP_DIS         | –             | A2            | I/O | VDDO          | OTP disable pin. By default, leave this pin floating. |
| <b>Supplies</b> |               |               |     |               |   |
| VDDIF           | B1            | –             | I   | N/A           | Radio IF PLL supply                                   |
| VDDTF           | C1            | B7            | I   | N/A           | Radio PA supply                                       |
| VDDLNA          | E1            | –             | I   | N/A           | Radio LNA supply                                      |
| VDDRF           | F1            | E7            | I   | N/A           | Radio supply  |
| VDDPX           | G1            | F7            | I   | N/A           | Radio RF PLL supply                                   |
| VDDC            | A5            | A3            | I   | N/A           | Core logic supply                                     |
| VDDC            | B8            | F1            | I   | N/A           | Core logic supply                                     |
| VDDC            | F8            | –             | I   | N/A           | Core logic supply                                     |
| VDDO            | G5            | D3            | I   | N/A           | Digital I/O supply voltage                            |
| VDDO            | A6            | –             | I   | N/A           | Digital I/O supply voltage                            |
| VDDO            | G8            | –             | I   | N/A           | Digital I/O supply voltage                            |
| NC              | –             | B1            | I   | N/A           | No connect  |
| VSS             | C2            | D7            | –   | N/A           | Ground  |
| VSS             | D2            | B6            | –   | N/A           | Ground  |
| VSS             | F2            | E6            | –   | N/A           | Ground  |
| VSS             | D3            | F6            | –   | N/A           | Ground  |
| VSS             | C6            | F3            | –   | N/A           | Ground  |
| VSS             | A7            | A1            | –   | N/A           | Ground  |
| VSS             | G7            | –             | –   | N/A           | Ground  |
| VSS             | –             | B2            | –   | N/A           | Ground  |

**7.2 Ball Maps**

Figure 8 shows the top view of the 50-ball 4.5 x 4 x 0.6 mm (FPBGA).

**Figure 8. 50-Ball 4.5 x 4 x 0.6 mm (FPBGA) Array**

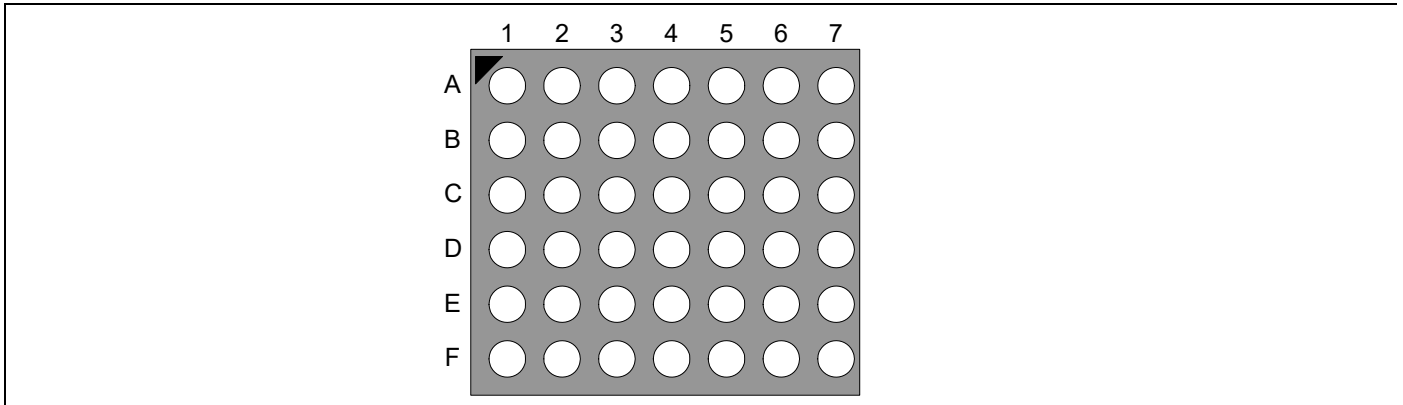


**Table 9. Ball Map for the 50-Ball CYW20713A1KUFBXG**

|          | 1      | 2      | 3      | 4         | 5         | 6       | 7          | 8          |
|----------|--------|--------|--------|-----------|-----------|---------|------------|------------|
| <b>A</b> | VREG   | VREGHV | VBAT   | LPO_IN    | VDDC      | VDDO    | VSS        | SPIM_CLK   |
| <b>B</b> | VDDIF  | REG_EN | GPIO_1 | RST_N     | GPIO_0    | COEX_IN | GPIO_7     | VDDC       |
| <b>C</b> | VDDTF  | VSS    | –      | TM0       | –         | VSS     | SPIM_CS_N  | UART_TXD   |
| <b>D</b> | RFP    | VSS    | VSS    | –         | –         | –       | UART_RTS_N | UART_RXD   |
| <b>E</b> | VDDLNA | –      | GPIO6  | COEX_OUT0 | COEX_OUT1 | GPIO_5  | SDA        | UART_CTS_N |
| <b>F</b> | VDDRF  | VSS    | TM2    | PCM_CLK   | PCM_SYNC  | PCM_IN  | SCL        | VDDC       |
| <b>G</b> | VDDPX  | XIN    | XOUT   | RES       | VDDO      | PCM_OUT | VSS        | VDDO       |

Figure 9 shows the top view of the 42-bump, 2.97 x 2.46 x 0.5 mm array.

**Figure 9. 42-Bump 2.97 x 2.46 x 0.5 mm Array (Top View)**



**Table 10. Ball Map for the 42-Bump CYW20713A1KUBG**

|          | <b>1</b> | <b>2</b>   | <b>3</b>   | <b>4</b> | <b>5</b> | <b>6</b> | <b>7</b> |
|----------|----------|------------|------------|----------|----------|----------|----------|
| <b>A</b> | VSS      | OTP_DIS    | VDDC       | PCM_SYNC | VBAT     | VREGHV   | VREG     |
| <b>B</b> | N/C      | VSS        | GPIO_1     | LPO_IN   | REG_EN   | VSS      | VDDTF    |
| <b>C</b> | SPIM_CLK | UART_TXD   | GPIO_0     | PCM_CLK  | RST_N    | TM2      | RFP      |
| <b>D</b> | SDA      | UART_RXD   | VDDO       | PCM_IN   | GPIO_6   | RES      | VSS      |
| <b>E</b> | SCL      | SPIM_CS_N  | UART_CTS_N | PCM_OUT  | XOUT     | VSS      | VDDRF    |
| <b>F</b> | VDDC     | UART_RTS_N | VSS        | GPIO_5   | XIN      | VSS      | VDDPX    |

## 8. Electrical Characteristics

Note: All voltages listed in Table 11 are referenced to  $V_{DD}$

Table 11. Absolute Maximum Ratings

| Rating                                  | Signal/Parameter    | Value      | Unit |
|---|---------------------|------------|------|
| DC supply voltage for RF                | VDD_RF <sup>a</sup> | 1.32       | V    |
| DC supply voltage for core              | VDDC                | 1.32       | V    |
| DC supply voltage for I/O               | VDDO <sup>b</sup>   | 3.6        | V    |
| DC supply voltage for PA                | VDDTF               | 3.3        | V    |
| Maximum voltage on input or output pins | VIMAX               | VDDO + 0.3 | V    |
| Minimum voltage on input or output pins | VIMIN               | VSS – 0.3  | V    |
| Storage temperature                     | TSTG                | –40 to 125 | °C   |

- a. VDD\_RF collectively refers to the VDDIF, VDDLNA, VDDPX, and VDDRF RF power supplies.  
 b. If VDDO is not applied, voltage should never be applied to any digital I/O pins (I/O pins should never be driven or pulled high). The list of digital I/O pins includes the following (these pins are listed in Section 7.: "Pin Information," on page 25 with VDDO shown as their power domain):  
 GPIO[3], GPIO[5], GPIO[6]  
 SCL, SDA  
 N\_MODE  
 SPIM\_CS\_N, SPIM\_CLK

Table 12. Power Supply

| Parameter                                     | Symbol              | Minimum | Typical | Maximum | Unit   |
|---|---------------------|---------|---------|---------|--------|
| DC supply voltage for RF                      | VDD_RF <sup>a</sup> | 1.159   | 1.22    | 1.281   | V      |
| DC supply noise for RF, from 100 kHz to 1 MHz | VDD_RF <sup>b</sup> | –       | –       | 150     | μV rms |
| DC supply voltage for core                    | VDDC                | 1.159   | 1.22    | 1.281   | V      |
| DC supply voltage for I/O                     | VDDO                | 1.7     | –       | 3.6     | V      |
| DC supply                                     | VDDTF <sup>c</sup>  | 1.12    | –       | 3.3     | V      |

- a. VDD\_RF collectively refers to the VDDIF, VDDLNA, VDDPX, VDDLNA, VDDRF RF power supplies.  
 b. Overall performance defined using integrated regulation.  
 c. VDDTF for Class 2 must be connected to VREG (main LDO output). VDDTF for Class 1 must be connected to VREGHV (HV LDO output) or an external voltage source. Refer to the Cypress compatibility guide for configuration details. VDDTF requires a capacitor to ground. The value of the capacitor must be tuned to ensure optimal RF RX sensitivity. The typical capacitor value is 10 pF for both packages. The value may depend on board layout.

Table 13. High-Voltage Regulator (HV LDO) Electrical Specifications

| Parameter                               | Minimum | Typical | Maximum | Unit |
|---|---------|---------|---------|------|
| Input voltage                           | 2.3     | –       | 5.5     | V    |
| Output voltage                          | 1.8     | –       | 3.3     | V    |
| Max current load                        | –       | –       | 95      | mA   |
| Load capacitance                        | 1       | –       | 10      | μF   |
| Load capacitor ESR                      | 0.01    | –       | 2       | Ω    |
| PSRR                                    | 20      | –       | 40      | dB   |
| Turn-on time ( $C_{load} = 2.2 \mu F$ ) | –       | –       | 200     | μs   |
| Dropout voltage                         | –       | –       | 200     | mV   |

**Table 14. Main Regulator (Main LDO) Electrical Specifications**

| Parameter        | Minimum | Typical | Maximum | Unit |
|------------------|---------|---------|---------|------|
| Input voltage    | 1.63    | –       | 3.63    | V    |
| Output voltage   | 1.159   | 1.22    | 1.281   | V    |
| Load current     | –       | –       | 60      | mA   |
| Load capacitance | 1       | –       | 2.2     | μF   |
| ESR              | 0.1     | –       | 0.5     | Ω    |
| Turn-on time     | –       | –       | 300     | μs   |
| PSRR             | 15      | –       | –       | dB   |
| Dropout voltage  | –       | –       | 200     | mV   |

**Note:** By default, the drive strength settings specified in [Table 15](#) are for 3.3V. To achieve the required drive strength for a VDDIO of 2.5V or 1.8V, contact a Cypress technical support representative (see [IoT Resources](#) for contact information).

**Table 15. Digital I/O Characteristics**

| Characteristics   | Symbol          | Minimum     | Typical | Maximum | Unit |
|---|-----------------|-------------|---------|---------|------|
| Input low voltage (VDDO = 3.3V)                           | V <sub>IL</sub> | –           | –       | 0.8     | V    |
| Input high voltage (VDDO = 3.3V)                          | V <sub>IH</sub> | 2.0         | –       | –       | V    |
| Input low voltage (VDDO = 1.8V)                           | V <sub>IL</sub> | –           | –       | 0.6     | V    |
| Input high voltage (VDDO = 1.8V)                          | V <sub>IH</sub> | 1.1         | –       | –       | V    |
| Output low voltage  | V <sub>OL</sub> | –           | –       | 0.4     | V    |
| Output high voltage                                       | V <sub>OH</sub> | VDDO – 0.4V | –       | –       | V    |
| Input low current   | I <sub>IL</sub> | –           | –       | 1.0     | μA   |
| Input high current  | I <sub>IH</sub> | –           | –       | 1.0     | μA   |
| Output low current (VDDO = 3.3V, V <sub>OL</sub> = 0.4V)  | I <sub>OL</sub> | –           | –       | 3.0     | mA   |
| Output high current (VDDO = 3.3V, V <sub>OH</sub> = 2.9V) | I <sub>OH</sub> | –           | –       | 3.0     | mA   |
| Output low current (VDDO = 1.8V, V <sub>OL</sub> = 0.4V)  | I <sub>OL</sub> | –           | –       | 3.0     | mA   |
| Output high current (VDDO = 1.8V, V <sub>OH</sub> = 1.4V) | I <sub>OH</sub> | –           | –       | 3.0     | mA   |
| Input capacitance   | C <sub>IN</sub> | –           | –       | 0.4     | pF   |

**8.1 Electrostatic Discharge Specifications**

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

**Table 16. ESD Specifications**

| Types                | Symbol       | Conditions  | ESD Rating                   | Units |
|----------------------|--------------|---|------------------------------|-------|
| Human body model     | ESD_HAND_HBM | Human body model contact discharge per AEC-Q100-002     | 3.5                          | kV    |
| Machine model        | ESD_HAND_MM  | Machine model contact discharge per AEC-Q100-003        | 150                          | V     |
| Charged device model | ESD_HAND_CDM | Charged device model contact discharge per AEC-Q100-011 | 500<br>(750V on corner pins) | V     |

**Table 17. Pad I/O Characteristics<sup>a</sup>**

| I/O Pad Characteristics |                   |           |
|-------------------------|-------------------|-----------|
| Pad Name                | Pull-Up/Pull-Down | Fail-Safe |
| COEX_OUT0               | Y                 | Y         |
| COEX_OUT1               | Y                 | Y         |
| COEX_IN                 | Y                 | Y         |
| PCM_CLK                 | Y                 | Y         |
| PCM_OUT                 | Y                 | Y         |
| PCM_IN                  | Y                 | Y         |
| PCM_SYNC                | Y                 | Y         |
| UART_RTS_N              | Y                 | Y         |
| UART_CTS_N              | Y                 | Y         |
| UART_RXD                | Y                 | Y         |
| UART_TXD                | Y                 | Y         |
| GPIO_0                  | Y                 | Y         |
| GPIO_1                  | Y                 | Y         |
| GPIO_2                  | Y                 | Y         |
| GPIO_4                  | Y                 | Y         |
| GPIO_7                  | Y                 | Y         |
| RST_N                   | N/A               | Y         |
| OTP_DIS                 | Y                 | N         |

a. All digital I/O internal pull-up or pull-down values are around 60 kΩ.



**Table 18. Current Consumption—Class 1(10 dBm)**

| Operational Mode                              | Conditions   | Typical | Units |
|---|--|---------|-------|
| Receive (1 Mbps)                              | Current level during receive of a basic rate packet  | 31      | mA    |
| Transmit (1 Mbps)                             | Current level during transmit of a basic rate packet, GFSK output power = 10 dBm   | 65      | mA    |
| Receive (EDR)                                 | Current level during receive of a 2 or 3 Mbps rate packet  | 32      | mA    |
| Transmit (EDR)                                | Current level during transmit of a 2 or 3 Mbps rate packet, GFSK output power = 10 dBm   | 59      | mA    |
| DM1/DH1                                       | Average current during basic rate max throughput connection which includes only this packet type.  | 45      | mA    |
| DM3/DH3                                       | Average current during basic rate max throughput connection which includes only this packet type.  | 46      | mA    |
| DM5/DH5                                       | Average current during max basic rate throughput connection which includes only this packet type.  | 48      | mA    |
| HV1   | Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.   | 38      | mA    |
| HV2   | Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.   | 23      | mA    |
| HV3   | Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.   | 17      | mA    |
| HCI only active                               | Average current when waiting for HCI command UART or SPI transports.   | 4.8     | mA    |
| Sleep   | UART transport active, external LPO clock available.   | 55      | μA    |
| Sleep, HV Reg Bypass                          | UART transport active, external LPO clock available, HV LDO disabled and in bypass mode.   | 45      | μA    |
| Inquiry Scan (1.28 sec)                       | Periodic scan rate is 1.28 sec.  | 350     | μA    |
| Page Scan (R1)                                | Periodic scan rate is R1 (1.28 sec).   | 350     | μA    |
| Inquiry Scan + Page Scan (R1)                 | Both inquiry and page scans are interlaced together at 1.28 sec periodic scan rate.  | 630     | μA    |
| Sniff master (500 ms)                         | Attempt and timeout parameters set to 4. Quality connection which rarely requires more than minimum packet exchange.   | 175     | μA    |
| Sniff slave (500 ms)                          | Attempt and timeout parameters set to 4. Quality connection which rarely requires more than minimum packet exchange. Sniff master follows optimal sniff protocol of CYW20713 master. | 160     | μA    |
| Sniff (500 ms) + Inquiry/Page Scan (R1)       | Same conditions as Sniff master and Page Scan (R1). Scan maybe either Inquiry Scan or Page Scan at 1.28 sec periodic scan rate.  | 455     | μA    |
| Sniff (500ms) + Inquiry Scan + Page Scan (R1) | Same conditions as Sniff master and Inquiry Scan + Page Scan.  | 760     | μA    |

**Table 19. Current Consumption—Class 2 (2 dBm)**

| Operational Mode                               | Conditions   | Typical | Unit |
|--|--|---------|------|
| Receive (1 Mbps)                               | Current level during receive of a basic rate packet  | 31      | mA   |
| Transmit (1 Mbps)                              | Current level during transmit of a basic rate packet, GFSK output power = 2 dBm  | 44      | mA   |
| Receive (EDR)                                  | Current level during receive of a 2 or 3 Mbps rate packet  | 32      | mA   |
| Transmit (EDR)                                 | Current level during transmit of a 2 or 3 Mbps rate packet, GFSK output power = 2 dBm  | 41      | mA   |
| DM1/DH1  | Average current during basic rate max throughput connection, which includes only this packet type.   | 35      | mA   |
| DM3/DH3  | Average current during basic rate max throughput connection, which includes only this packet type.   | 36      | mA   |
| DM5/DH5  | Average current during max basic rate throughput connection, which includes only this packet type.   | 37      | mA   |
| HV1  | Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.   | 28      | mA   |
| HV2  | Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.   | 17      | mA   |
| HV3  | Average current during SCO voice connection consisting of only this packet type. ACL channel is in 500 ms sniff.   | 13      | mA   |
| HCI only active                                | Average current when waiting for HCI command UART or SPI transports.   | 4.8     | mA   |
| Sleep  | UART transport active, external LPO clock available.   | 55      | μA   |
| Sleep, HV Reg Bypass                           | UART transport active, external LPO clock available, HV LDO disabled and in bypass mode.   | 45      | μA   |
| Inquiry Scan (1.28 sec)                        | Periodic scan rate is 1.28 sec.  | 350     | μA   |
| Page Scan (R1)                                 | Periodic scan rate is R1 (1.28 sec).   | 350     | μA   |
| Inquiry Scan + Page Scan (R1)                  | Both inquiry and page scans are interlaced together at 1.28 sec periodic scan rate.  | 630     | μA   |
| Sniff master (500 ms)                          | Attempt and timeout parameters set to 4. Quality connection which rarely requires more than minimum packet exchange.   | 145     | μA   |
| Sniff slave (500 ms)                           | Attempt and timeout parameters set to 4. Quality connection which rarely requires more than minimum packet exchange. Sniff master follows optimal sniff protocol of CYW20713 master. | 135     | μA   |
| Sniff (500 ms) + Inquiry/Page Scan (R1)        | Same conditions as Sniff master and Page Scan (R1). Scan can be either Inquiry Scan or Page Scan at 1.28 sec periodic scan rate.   | 425     | μA   |
| Sniff (500 ms) + Inquiry Scan + Page Scan (R1) | Same conditions as Sniff master and Inquiry Scan + Page Scan.  | 730     | μA   |

**Table 20. Operating Conditions**

| Parameter         | Conditions | Minimum | Typical | Maximum | Unit |
|-------------------|------------|---------|---------|---------|------|
| Temperature       | Industrial | -40.0   | -       | 85      | °C   |
| Power supply      | RF, Core   | 1.14    | 1.22    | 1.32    | V    |
| PA supply (VDDTF) | -          | 1.14    | 2.9     | 3.3     | V    |

**8.2 RF Specifications**

**Table 21. Receiver RF Specifications<sup>a, b</sup>**

| Parameter  | Conditions                               | Minimum | Typical <sup>c</sup> | Maximum | Unit |
|--|--|---------|----------------------|---------|------|
| <b>General</b>   |  |         |                      |         |      |
| Frequency range  | –  | 2402    | –                    | 2480    | MHz  |
| RX sensitivity <sup>d</sup>                              | GFSK, 0.1% BER, 1 Mbps, FPBGA package    | –       | –89 <sup>e</sup>     | –85     | dBm  |
|  | GFSK, 0.1% BER, 1 Mbps, WLBGA package    | –       | –88 <sup>e</sup>     | –84     | dBm  |
|  | p/4-DQPSK, 0.01% BER, 2 Mbps             | –       | –91 <sup>e</sup>     | –85     | dBm  |
|  | 8-DPSK, 0.01% BER, 3 Mbps FPBGA package  | –       | –86 <sup>e</sup>     | –81     | dBm  |
|  | 8-DPSK, 0.01% BER, 3 Mbps, WLBGA package | –       | –85 <sup>e</sup>     | –80     | dBm  |
| Maximum input  | GFSK, 1 Mbps                             | –       | –                    | –20     | dBm  |
| Maximum input  | p/4-DQPSK, 8-DPSK, 2/3 Mbps              | –       | –                    | –20     | dBm  |
| <b>Interference Performance</b>                          |  |         |                      |         |      |
| C/I cochannel  | GFSK, 0.1% BER                           | –       | –                    | 11      | dB   |
| C/I 1 MHz adjacent channel                               | GFSK, 0.1% BER                           | –       | –                    | 0       | dB   |
| C/I 2 MHz adjacent channel                               | GFSK, 0.1% BER                           | –       | –                    | –30.0   | dB   |
| C/I ≥ 3 MHz adjacent channel                             | GFSK, 0.1% BER                           | –       | –                    | –40.0   | dB   |
| C/I image channel  | GFSK, 0.1% BER                           | –       | –                    | –9.0    | dB   |
| C/I 1 MHz adjacent to image channel                      | GFSK, 0.1% BER                           | –       | –                    | –20.0   | dB   |
| C/I cochannel  | p/4-DQPSK, 0.1% BER                      | –       | –                    | 13      | dB   |
| C/I 1 MHz adjacent channel                               | p/4-DQPSK, 0.1% BER                      | –       | –                    | 0       | dB   |
| C/I 2 MHz adjacent channel                               | p/4-DQPSK, 0.1% BER                      | –       | –                    | –30.0   | dB   |
| C/I ≥ 3 MHz adjacent channel                             | 8-DPSK, 0.1% BER                         | –       | –                    | –40.0   | dB   |
| C/I image channel  | p/4-DQPSK, 0.1% BER                      | –       | –                    | –7.0    | dB   |
| C/I 1 MHz adjacent to image channel                      | p/4-DQPSK, 0.1% BER                      | –       | –                    | –20.0   | dB   |
| C/I cochannel  | 8-DPSK, 0.1% BER                         | –       | –                    | 21      | dB   |
| C/I 1 MHz adjacent channel                               | 8-DPSK, 0.1% BER                         | –       | –                    | 5       | dB   |
| C/I 2 MHz adjacent channel                               | 8-DPSK, 0.1% BER                         | –       | –                    | –25.0   | dB   |
| C/I ≥ 3 MHz adjacent channel                             | 8-DPSK, 0.1% BER                         | –       | –                    | –33.0   | dB   |
| C/I Image channel  | 8-DPSK, 0.1% BER                         | –       | –                    | 0       | dB   |
| C/I 1 MHz adjacent to image channel                      | 8-DPSK, 0.1% BER                         | –       | –                    | –13.0   | dB   |
| <b>Out-of-Band Blocking Performance (CW)<sup>f</sup></b> |  |         |                      |         |      |
| 30–2000 MHz  | 0.1% BER                                 | –       | –10.0                | –       | dBm  |
| 2000–2399 MHz  | 0.1% BER                                 | –       | –27                  | –       | dBm  |
| 2498–3000 MHz  | 0.1% BER                                 | –       | –27                  | –       | dBm  |
| 3000 MHz–12.75 GHz                                       | 0.1% BER                                 | –       | –10.0                | –       | dBm  |

**Table 21. Receiver RF Specifications<sup>a, b</sup> (Cont.)**

| Parameter   | Conditions | Minimum | Typical <sup>c</sup> | Maximum | Unit   |
|---|------------|---------|----------------------|---------|--------|
| <b>Out-of-Band Blocking Performance, Modulated Interferer</b> |            |         |                      |         |        |
| 776–764 MHz   | CDMA       | –       | –15                  | –       | dBm    |
| 824–849 MHz   | CDMA       | –       | –15                  | –       | dBm    |
| 1850–1910 MHz   | CDMA       | –       | –20                  | –       | dBm    |
| 824–849 MHz   | EDGE/GSM   | –       | –10                  | –       | dBm    |
| 880–915 MHz   | EDGE/GSM   | –       | –10                  | –       | dBm    |
| 1710–1785 MHz   | EDGE/GSM   | –       | –15                  | –       | dBm    |
| 1850–1910 MHz   | EDGE/GSM   | –       | –15                  | –       | dBm    |
| 1850–1910 MHz   | WCDMA      | –       | –25                  | –       | dBm    |
| 1920–1980 MHz   | WCDMA      | –       | –25                  | –       | dBm    |
| <b>Intermodulation Performance<sup>g</sup></b>                |            |         |                      |         |        |
| BT, Df = 5 MHz  | –          | –39.0   | –                    | –       | dBm    |
| <b>Spurious Emissions<sup>h</sup></b>                         |            |         |                      |         |        |
| 30 MHz to 1 GHz   | –          | –       | –                    | –57     | dBm    |
| 1 GHz to 12.75 GHz  | –          | –       | –                    | –47     | dBm    |
| 65 MHz to 108 MHz   | FM Rx      | –       | –145                 | –       | dBm/Hz |
| 746 MHz to 764 MHz  | CDMA       | –       | –145                 | –       | dBm/Hz |
| 851–894 MHz   | CDMA       | –       | –145                 | –       | dBm/Hz |
| 925–960 MHz   | EDGE/GSM   | –       | –145                 | –       | dBm/Hz |
| 1805–1880 MHz   | EDGE/GSM   | –       | –145                 | –       | dBm/Hz |
| 1930–1990 MHz   | PCS        | –       | –145                 | –       | dBm/Hz |
| 2110–2170 MHz   | WCDMA      | –       | –145                 | –       | dBm/Hz |

- a. All specifications are single ended. Unused inputs are left open.
- b. All specifications, except typical, are for industrial temperatures. For details see [Table 20 on page 33](#).
- c. Typical operating conditions are 1.22V operating voltage and 25°C ambient temperature.
- d. The receiver sensitivity is measured at BER of 0.1% on the device interface.
- e. Measured with the dirty transmitter OFF. Typically, there is approximately 1 dB less in Rx sensitivity when the dirty transmitter is ON.
- f. Meets this specification using front-end band pass filter.
- g. f0 = –64 dBm Bluetooth-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n\*1 MHz, where n is 3, 4, or 5. For the typical case, n = 5.
- h. Includes baseband radiated emissions.

**Table 22. Transmitter RF Specifications <sup>a, b</sup>**

| Parameter   | Conditions | Minimum | Typical | Maximum               | Unit   |
|---|------------|---------|---------|-----------------------|--------|
| <b>General</b>  |            |         |         |                       |        |
| Frequency range   | –          | 2402    | –       | 2480                  | MHz    |
| Class1: GFSK Tx power <sup>c</sup>  | –          | 6.5     | 10      | –                     | dBm    |
| Class1: EDR Tx power <sup>d</sup>   | –          | 4.5     | 8       | –                     | dBm    |
| Class 2: GFSK Tx power  | –          | –1.5    | 2       | –                     | dBm    |
| Power control step  | –          | 2       | 4       | 6                     | dB     |
| <b>Modulation Accuracy</b>  |            |         |         |                       |        |
| p/4-DQPSK Frequency Stability   | –          | –10     | –       | 10                    | kHz    |
| p/4-DQPSK RMS DEVM  | –          | –       | –       | 20                    | %      |
| p/4-QPSK Peak DEVM  | –          | –       | –       | 35                    | %      |
| p/4-DQPSK 99% DEVM  | –          | –       | –       | 30                    | %      |
| 8-DPSK frequency stability  | –          | –10     | –       | 10                    | kHz    |
| 8-DPSK RMS DEVM   | –          | –       | –       | 13                    | %      |
| 8-DPSK Peak DEVM  | –          | –       | –       | 25                    | %      |
| 8-DPSK 99% DEVM   | –          | –       | –       | 20                    | %      |
| <b>In-Band Spurious Emissions</b>   |            |         |         |                       |        |
| +500 kHz  | –          | –       | –       | –20                   | dBc    |
| 1.0 MHz <  M – N  < 1.5 MHz   | –          | –       | –       | –26                   | dBc    |
| 1.5 MHz <  M – N  < 2.5 MHz   | –          | –       | –       | –20                   | dBm    |
| M – N  ≥ 2.5 MHz  | –          | –       | –       | –40                   | dBm    |
| <b>Out-of-Band Spurious Emissions</b>                                     |            |         |         |                       |        |
| 30 MHz to 1 GHz   | –          | –       | –       | –36.0 <sup>e</sup>    | dBm    |
| 1 GHz to 12.75 GHz  | –          | –       | –       | –30.0 <sup>e, f</sup> | dBm    |
| 1.8 GHz to 1.9 GHz  | –          | –       | –       | –47.0                 | dBm    |
| 5.15 GHz to 5.3 GHz   | –          | –       | –       | –47.0                 | dBm    |
| <b>GPS Band Noise Emission (without a front-end band pass filter)</b>     |            |         |         |                       |        |
| 1572.92 MHz to 1577.92 MHz  | –          | –       | –150    | –127                  | dBm/Hz |
| <b>Out-of-Band Noise Emissions (without a front-end band pass filter)</b> |            |         |         |                       |        |
| 65 MHz to 108 MHz   | FM Rx      | –       | –145    | –                     | dBm/Hz |
| 746 MHz to 764 MHz  | CDMA       | –       | –145    | –                     | dBm/Hz |
| 869 MHz to 960 MHz  | CDMA       | –       | –145    | –                     | dBm/Hz |
| 925 MHz to 960 MHz  | EDGE/GSM   | –       | –145    | –                     | dBm/Hz |
| 1805 MHz to 1880 MHz  | EDGE/GSM   | –       | –145    | –                     | dBm/Hz |
| 1930 MHz to 1990 MHz  | PCS        | –       | –145    | –                     | dBm/Hz |
| 2110 MHz to 2170 MHz  | WCDMA      | –       | –145    | –                     | dBm/Hz |

- a. All specifications are for industrial temperatures. For details, see [Table 20 on page 33](#).
- b. All specifications are single-ended. Unused input are left open.
- c. +10 dBm output for GFSK measured with VDDTF = 2.9 V.
- d. +8 dBm output for EDR measured with VDDTF = 2.9 V.
- e. Maximum value is the value required for Bluetooth qualification.
- f. Meets this spec using a front-end band-pass filter.

### 8.3 Timing and AC Characteristics

In this section, use the numbers listed in the reference column to interpret the timing diagrams.

#### 8.3.1 Startup Timing

There are two basic startup scenarios. In one scenario, the chip startup and firmware boot is held off while the RST\_N pin is asserted. In the second scenario, the chip startup and firmware boot is directly triggered by the chip power-up. In this case, an internal power-on reset (POR) is held for a few ms, after which the chip commences startup.

The global reset signal in the CYW20713 is a logical OR (actually a wired AND, since the signals are active low) of the RST\_N input and the internal POR signals. The last signal to be released determines the time at which the chip is released from reset. The POR is typically asserted for 3 ms after VDDC crosses the 0.8V threshold, but it may be as soon as 1.5 ms after this event.

After the chip is released from reset, both startup scenarios follow the same sequence, as follows:

5. After approximately 120  $\mu$ s, the CLK\_REQ (GPIO\_5) signal is asserted.
6. The chip remains in sleep state for a minimum of 4.2 ms.
7. If present, the TCXO and LPO clocks must be oscillating by the end of the 4.2 ms period.

If a TCXO clock is not in the system, a crystal is assumed to be present at the XIN and XOUT pins. If an LPO clock is not used, the firmware will detect the absence of a clock at the LPO\_IN lead and use the internal LPO clock instead.

Figure 10 and Figure 11 on page 38 illustrate the two startup timing scenarios.

Figure 10. Startup Timing from RST\_N

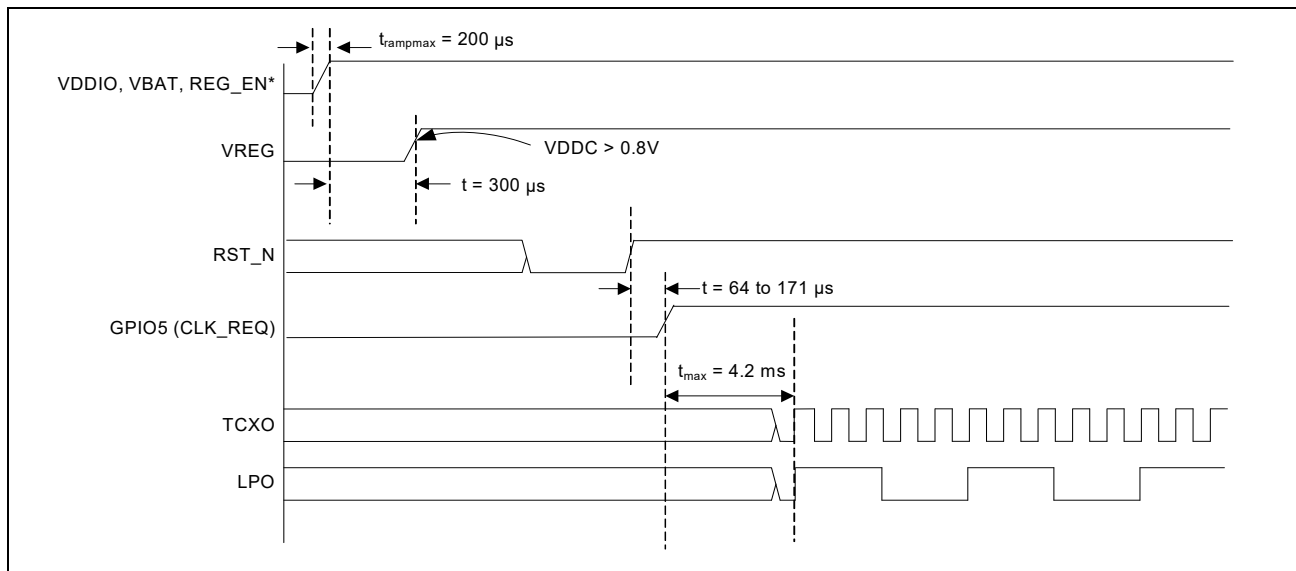
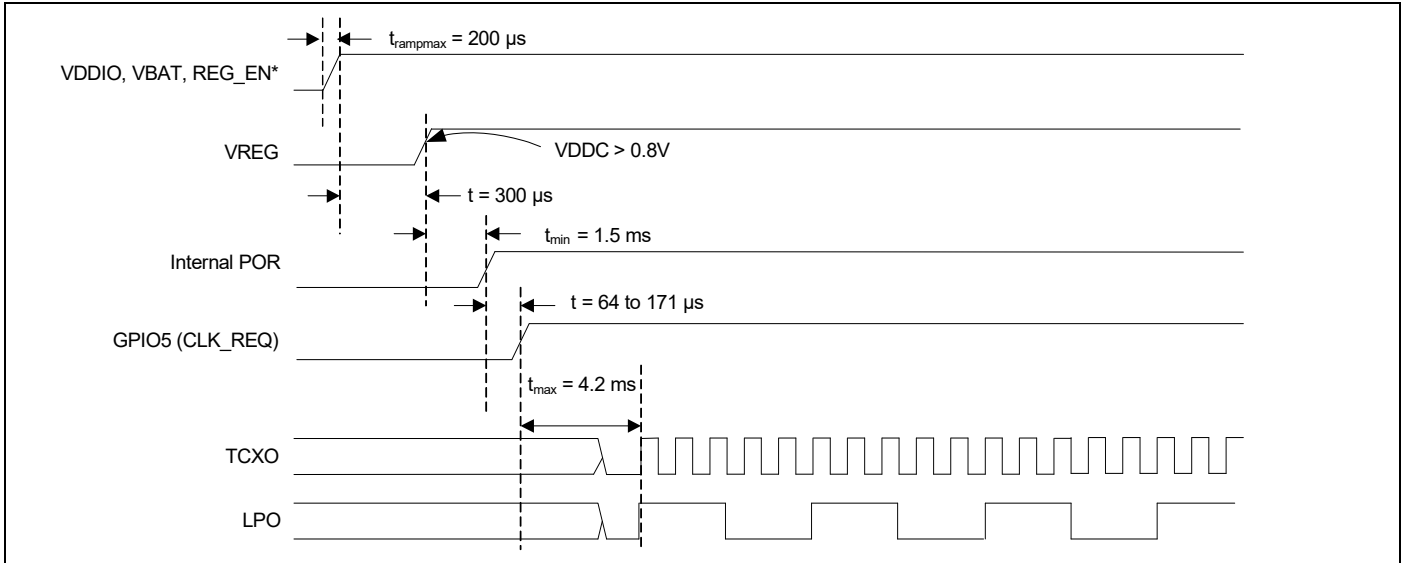


Figure 11. Startup Timing from Power-on Reset

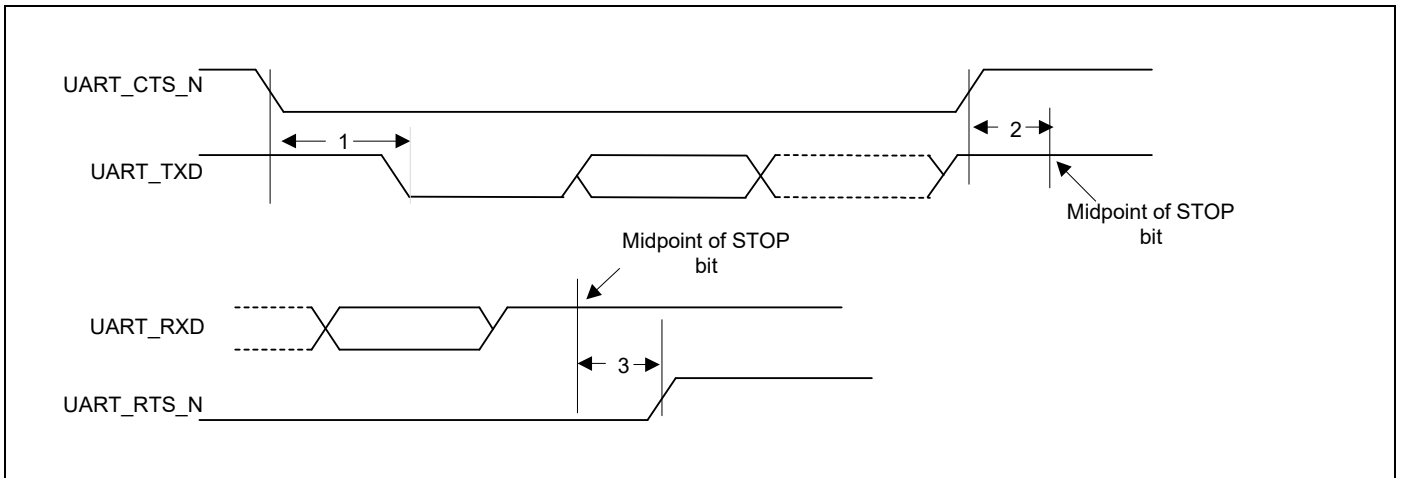


8.3.2 UART Timing

Table 23. UART Timing Specifications

| Reference | Characteristics   | Minimum | Maximum | Unit           |
|-----------|---|---------|---------|----------------|
| 1         | Delay time, UART_CTS_N low to UART_TXD valid            | –       | 24      | Baudout cycles |
| 2         | Setup time, UART_CTS_N high before midpoint of stop bit | –       | 10      | ns             |
| 3         | Delay time, midpoint of stop bit to UART_RTS_N high     | –       | 2       | Baudout cycles |

Figure 12. UART Timing

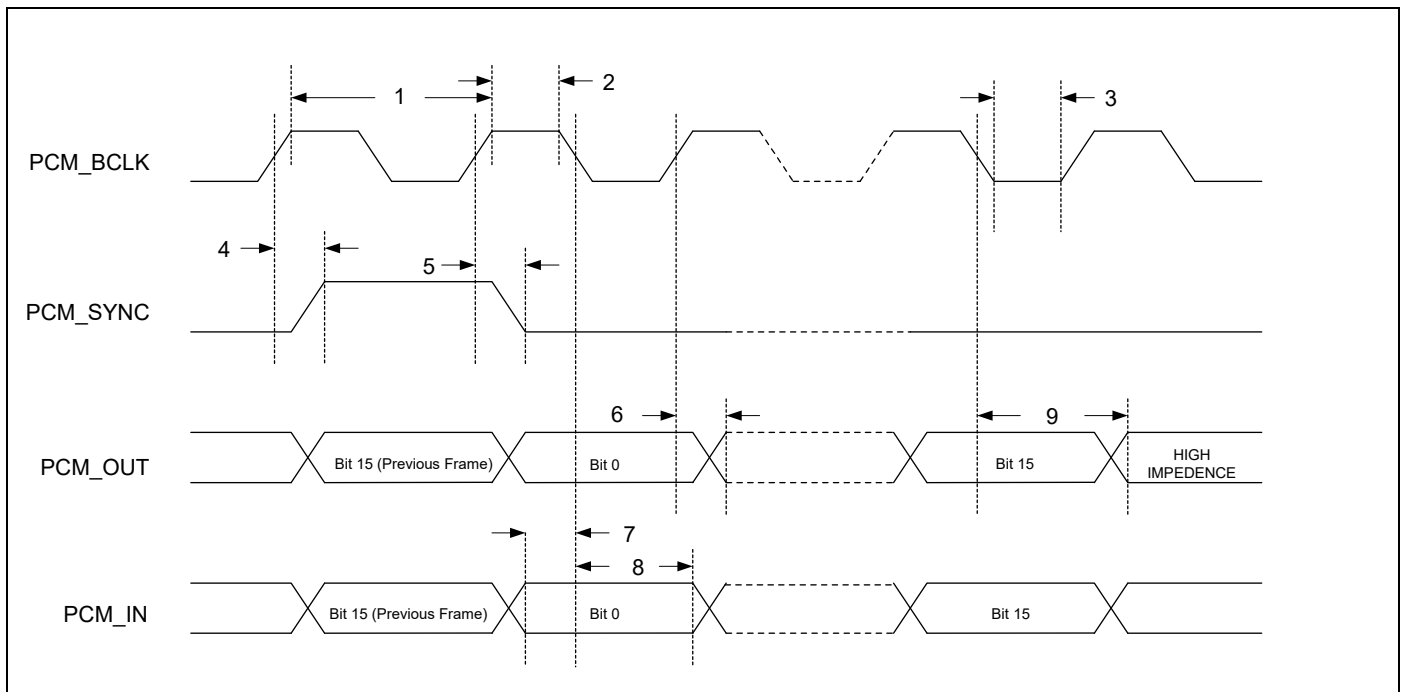


8.3.3 PCM Interface Timing

**Table 24. PCM Interface Timing Specifications (Short Frame Synchronization, Master Mode)**

| Reference | Characteristics   | Minimum | Maximum | Unit |
|-----------|---|---------|---------|------|
| 1         | PCM bit clock frequency   | 128     | 2048    | kHz  |
| 2         | PCM bit clock HIGH time   | 128     | –       | ns   |
| 3         | PCM bit clock LOW time  | 209     | –       | ns   |
| 4         | Delay from PCM_BCLK rising edge to PCM_SYNC high  | –       | 50      | ns   |
| 5         | Delay from PCM_BCLK rising edge to PCM_SYNC low   | –       | 50      | ns   |
| 6         | Delay from PCM_BCLK rising edge to data valid on PCM_OUT                                      | –       | 50      | ns   |
| 7         | Setup time for PCM_IN before PCM_BCLK falling edge  | 50      | –       | ns   |
| 8         | Hold time for PCM_IN after PCM_BCLK falling edge  | 10      | –       | ns   |
| 9         | Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | –       | 50      | ns   |

**Figure 13. PCM Interface Timing (Short Frame Synchronization, Master Mode)**

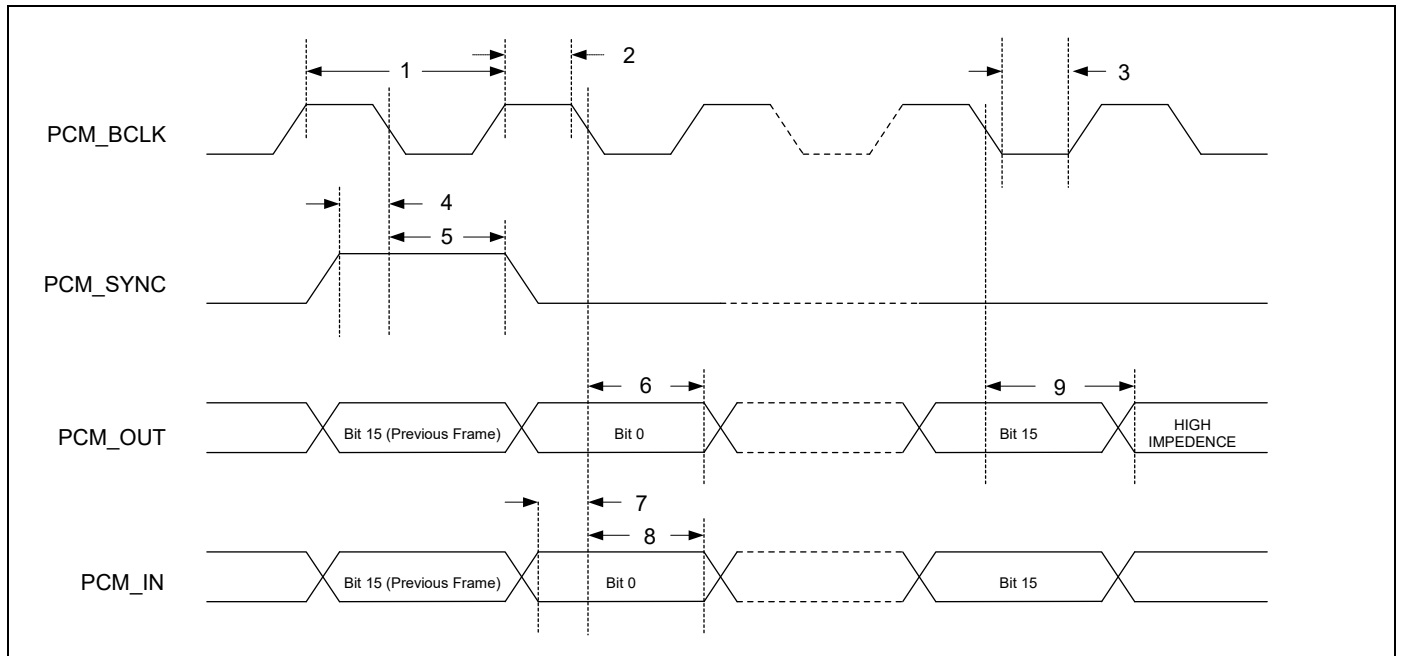




**Table 25. PCM Interface Timing Specifications (Short Frame Synchronization, Slave Mode)**

| Reference | Characteristics   | Minimum | Maximum | Unit |
|-----------|---|---------|---------|------|
| 1         | PCM bit clock frequency   | 128     | 2048    | kHz  |
| 2         | PCM bit clock HIGH time   | 209     | –       | ns   |
| 3         | PCM bit clock LOW time  | 209     | –       | ns   |
| 4         | Setup time for PCM_SYNC before falling edge of PCM_BCLK                                       | 50      | –       | ns   |
| 5         | Hold time for PCM_SYNC after falling edge of PCM_BCLK   | 10      | –       | ns   |
| 6         | Hold time of PCM_OUT after PCM_BCLK falling edge  | –       | 175     | ns   |
| 7         | Setup time for PCM_IN before PCM_BCLK falling edge  | 50      | –       | ns   |
| 8         | Hold time for PCM_IN after PCM_BCLK falling edge  | 10      | –       | ns   |
| 9         | Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | –       | 100     | ns   |

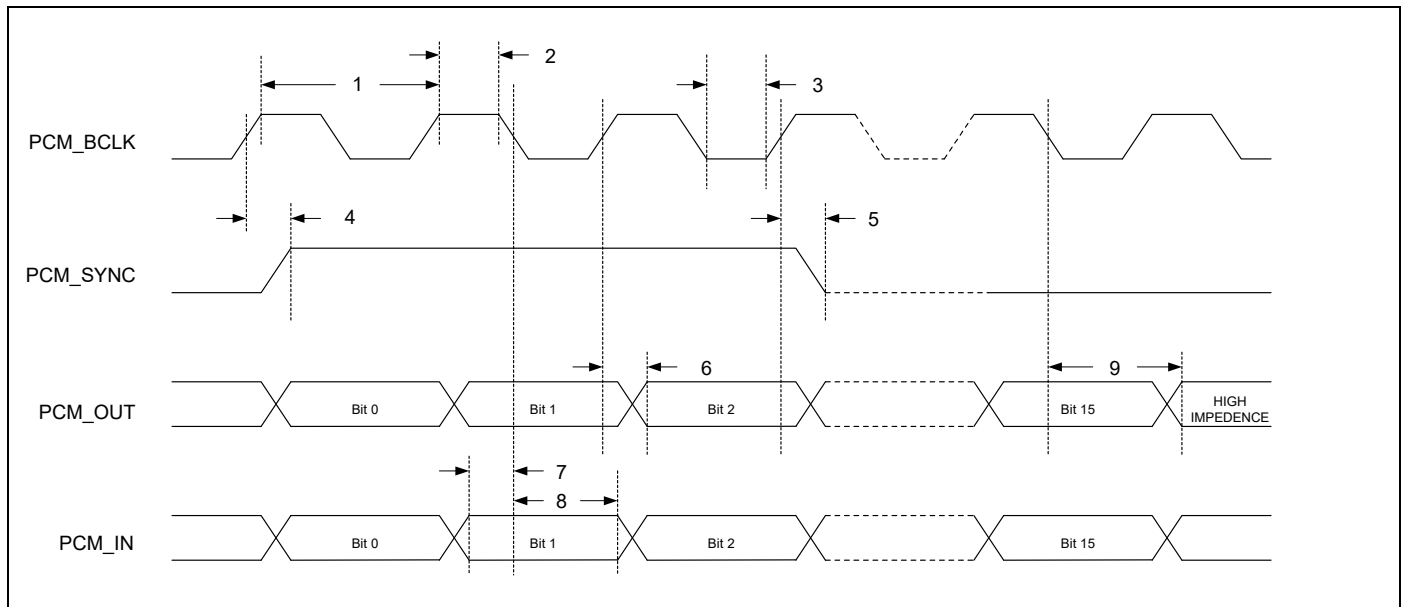
**Figure 14. PCM Interface Timing (Short Frame Synchronization, Slave Mode)**



**Table 26. PCM Interface Timing Specifications (Long Frame Synchronization, Master Mode)**

| Reference | Characteristics   | Minimum | Maximum | Unit |
|-----------|---|---------|---------|------|
| 1         | PCM bit clock frequency   | 128     | 2048    | kHz  |
| 2         | PCM bit clock HIGH time   | 209     | –       | ns   |
| 3         | PCM bit clock LOW time  | 209     | –       | ns   |
| 4         | Delay from PCM_BCLK rising edge to PCM_SYNC HIGH during first bit time                        | –       | 50      | ns   |
| 5         | Delay from PCM_BCLK rising edge to PCM_SYNC LOW during third bit time                         | –       | 50      | ns   |
| 6         | Delay from PCM_BCLK rising edge to data valid on PCM_OUT                                      | –       | 50      | ns   |
| 7         | Setup time for PCM_IN before PCM_BCLK falling edge  | 50      | –       | ns   |
| 8         | Hold time for PCM_IN after PCM_BCLK falling edge  | 10      | –       | ns   |
| 9         | Delay from falling edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | –       | 50      | ns   |

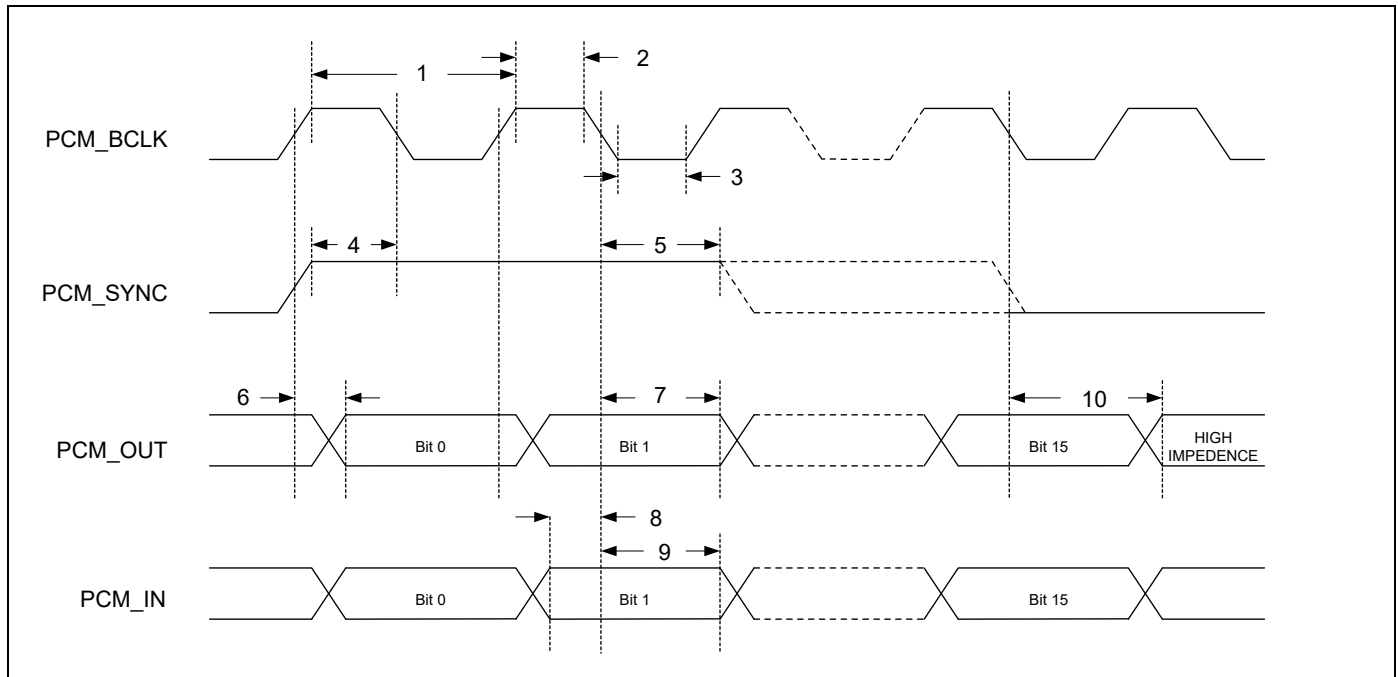
**Figure 15. PCM Interface Timing (Long Frame Synchronization, Master Mode)**



**Table 27. PCM Interface Timing Specifications (Long Frame Synchronization, Slave Mode)**

| Reference | Characteristics   | Minimum | Maximum | Unit |
|-----------|---|---------|---------|------|
| 1         | PCM bit clock frequency.  | 128     | 2048    | kHz  |
| 2         | PCM bit clock HIGH time.  | 209     | –       | ns   |
| 3         | PCM bit clock LOW time.   | 209     | –       | ns   |
| 4         | Setup time for PCM_SYNC before falling edge of PCM_BCLK during first bit time.  | 50      | –       | ns   |
| 5         | Hold time for PCM_SYNC after falling edge of PCM_BCLK during second bit period. (PCM_SYNC may go low any time from second bit period to last bit period). | 10      | –       | ns   |
| 6         | Delay from rising edge of PCM_BCLK or PCM_SYNC (whichever is later) to data valid for first bit on PCM_OUT.   | –       | 50      | ns   |
| 7         | Hold time of PCM_OUT after PCM_BCLK falling edge.   | –       | 175     | ns   |
| 8         | Setup time for PCM_IN before PCM_BCLK falling edge.   | 50      | –       | ns   |
| 9         | Hold time for PCM_IN after PCM_BCLK falling edge.   | 10      | –       | ns   |
| 10        | Delay from falling edge of PCM_BCLK or PCM_SYNC (whichever is later) during last bit in slot to PCM_OUT becoming high impedance.                          | –       | 100     | ns   |

**Figure 16. PCM Interface Timing (Long Frame Synchronization, Slave Mode)**



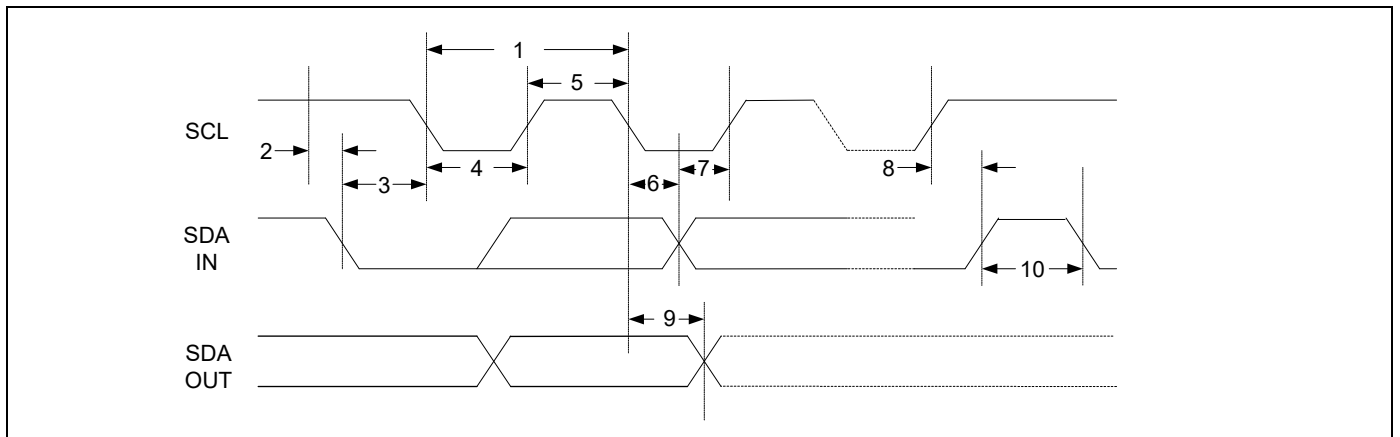
8.3.4 BSC Interface Timing

**Table 28. BSC Interface Timing Specifications**

| Reference | Characteristics                   | Minimum | Maximum                   | Unit |
|-----------|-----------------------------------|---------|---------------------------|------|
| 1         | Clock frequency                   | –       | 100<br>400<br>800<br>1000 | kHz  |
| 2         | START condition setup time        | 650     | –                         | ns   |
| 3         | START condition hold time         | 280     | –                         | ns   |
| 4         | Clock low time                    | 650     | –                         | ns   |
| 5         | Clock high time                   | 280     | –                         | ns   |
| 6         | Data input hold time <sup>a</sup> | 0       | –                         | ns   |
| 7         | Data input setup time             | 100     | –                         | ns   |
| 8         | STOP condition setup time         | 280     | –                         | ns   |
| 9         | Output valid from clock           | –       | 400                       | ns   |
| 10        | Bus free time <sup>b</sup>        | 650     | –                         | ns   |

- a. As a transmitter, 300 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions
- b. Time that the CBUS must be free before a new transaction can start.

**Figure 17. BSC Interface Timing Diagram**



## 8.4 I<sup>2</sup>S Interface

The CYW20713 supports two independent I<sup>2</sup>S digital audio ports. The I<sup>2</sup>S interface supports both master and slave modes. The I<sup>2</sup>S signals are:

- I<sup>2</sup>S clock: I<sup>2</sup>S SCK
- I<sup>2</sup>S Word Select: I<sup>2</sup>S WS
- I<sup>2</sup>S Data Out: I<sup>2</sup>S SDO
- I<sup>2</sup>S Data In: I<sup>2</sup>S SDI

I<sup>2</sup>S SCK and I<sup>2</sup>S WS become outputs in master mode and inputs in slave mode, while I<sup>2</sup>S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I<sup>2</sup>S bus, per the I<sup>2</sup>S specification. The MSB of each data word is transmitted one bit clock cycle after the I<sup>2</sup>S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I<sup>2</sup>S WS is low, and right-channel data is transmitted when I<sup>2</sup>S WS is high. Data bits sent by the CYW20713 are synchronized with the falling edge of I2S\_SCK and should be sampled by the receiver on the rising edge of I2S\_SCK.

The clock rate in master mode is either of the following:

$$48 \text{ kHz} \times 32 \text{ bits per frame} = 1.536 \text{ MHz}$$

$$48 \text{ kHz} \times 50 \text{ bits per frame} = 2.400 \text{ MHz}$$

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.

8.4.1 I<sup>2</sup>S Timing

**Note:** Timing values specified in Table 29 are relative to high and low threshold levels.

**Table 29. Timing for I<sup>2</sup>S Transmitters and Receivers**

|  | Transmitter         |                     |                     |      | Receiver            |                     |             |      | Notes |
|--|---------------------|---------------------|---------------------|------|---------------------|---------------------|-------------|------|-------|
|  | Lower Limit         |                     | Upper Limit         |      | Lower Limit         |                     | Upper Limit |      |       |
|  | Min.                | Max.                | Min.                | Max. | Min.                | Max.                | Min.        | Max. |       |
| Clock Period T   | T <sub>tr</sub>     | –                   | –                   | –    | T <sub>r</sub>      | –                   | –           | –    | a     |
| <b>Master Mode: Clock generated by transmitter or receiver</b> |                     |                     |                     |      |                     |                     |             |      |       |
| HIGH t <sub>HC</sub>   | 0.35T <sub>tr</sub> | –                   | –                   | –    | 0.35T <sub>tr</sub> | –                   | –           | –    | b     |
| LOW t <sub>LC</sub>  | 0.35T <sub>tr</sub> | –                   | –                   | –    | 0.35T <sub>tr</sub> | –                   | –           | –    | b     |
| <b>Slave Mode: Clock accepted by transmitter or receiver</b>   |                     |                     |                     |      |                     |                     |             |      |       |
| HIGH t <sub>HC</sub>   | –                   | 0.35T <sub>tr</sub> | –                   | –    | –                   | 0.35T <sub>tr</sub> | –           | –    | c     |
| LOW t <sub>LC</sub>  | –                   | 0.35T <sub>tr</sub> | –                   | –    | –                   | 0.35T <sub>tr</sub> | –           | –    | c     |
| Rise time t <sub>RC</sub>                                      | –                   | –                   | 0.15T <sub>tr</sub> | –    | –                   | –                   | –           | –    | d     |
| <b>Transmitter</b>   |                     |                     |                     |      |                     |                     |             |      |       |
| Delay t <sub>dtr</sub>   | –                   | –                   | –                   | 0.8T | –                   | –                   | –           | –    | e     |
| Hold time t <sub>htr</sub>                                     | 0                   | –                   | –                   | –    | –                   | –                   | –           | –    | d     |
| <b>Receiver</b>  |                     |                     |                     |      |                     |                     |             |      |       |
| Setup time t <sub>sr</sub>                                     | –                   | –                   | –                   | –    | –                   | 0.2T <sub>r</sub>   | –           | –    | f     |
| Hold time t <sub>hr</sub>                                      | –                   | –                   | –                   | –    | –                   | 0                   | –           | –    | f     |

- a. The system clock period T must be greater than T<sub>tr</sub> and T<sub>r</sub> because both the transmitter and receiver have to be able to handle the data transfer rate.
- b. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t<sub>HC</sub> and t<sub>LC</sub> are specified with respect to T.
- c. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than 0.35T<sub>r</sub>, any clock that meets the requirements can be used.
- d. Because the delay (t<sub>dtr</sub>) and the maximum transmitter speed (defined by T<sub>tr</sub>) are related, a fast transmitter driven by a slow clock edge can result in t<sub>dtr</sub> not exceeding t<sub>RC</sub> which means t<sub>htr</sub> becomes zero or negative. Therefore, the transmitter has to guarantee that t<sub>htr</sub> is greater than or equal to zero, so long as the clock rise-time t<sub>RC</sub> is not more than t<sub>RCmax</sub>, where t<sub>RCmax</sub> is not less than 0.15T<sub>tr</sub>.
- e. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
- f. The data setup and hold time must not be less than the specified receiver setup and hold time.

**Note:** The time periods specified in Figure 18 and Figure 19 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 18. I<sup>2</sup>S Transmitter Timing

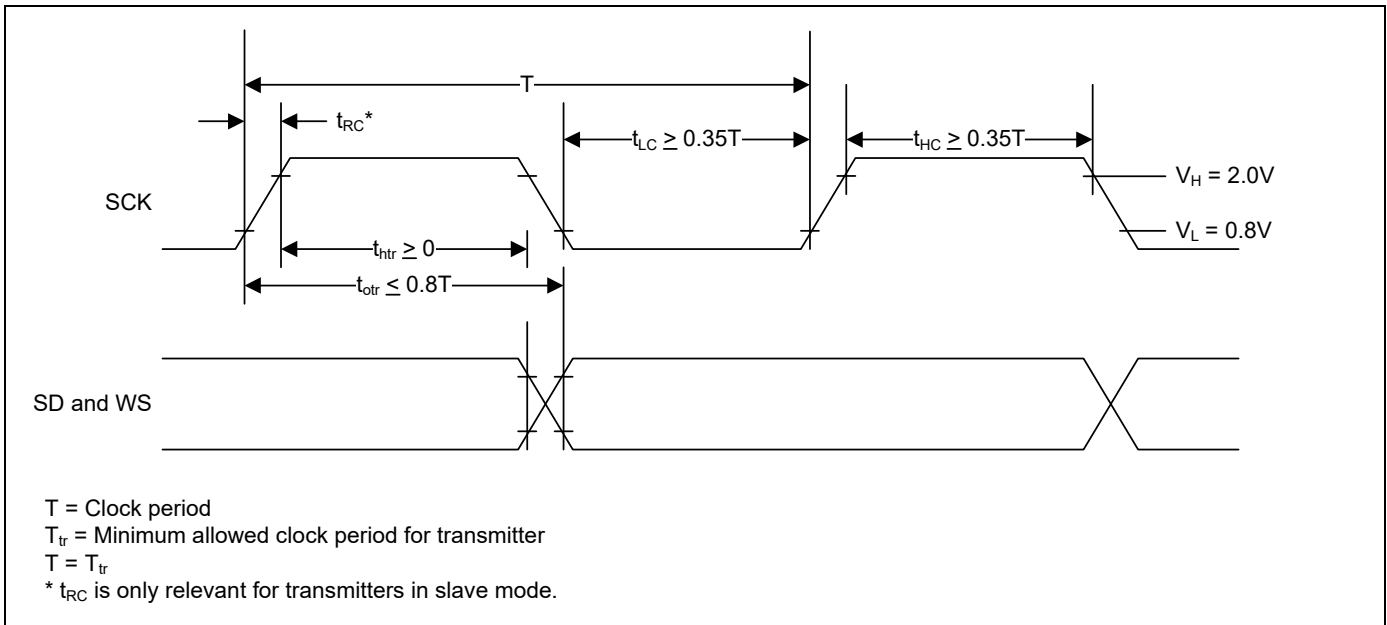
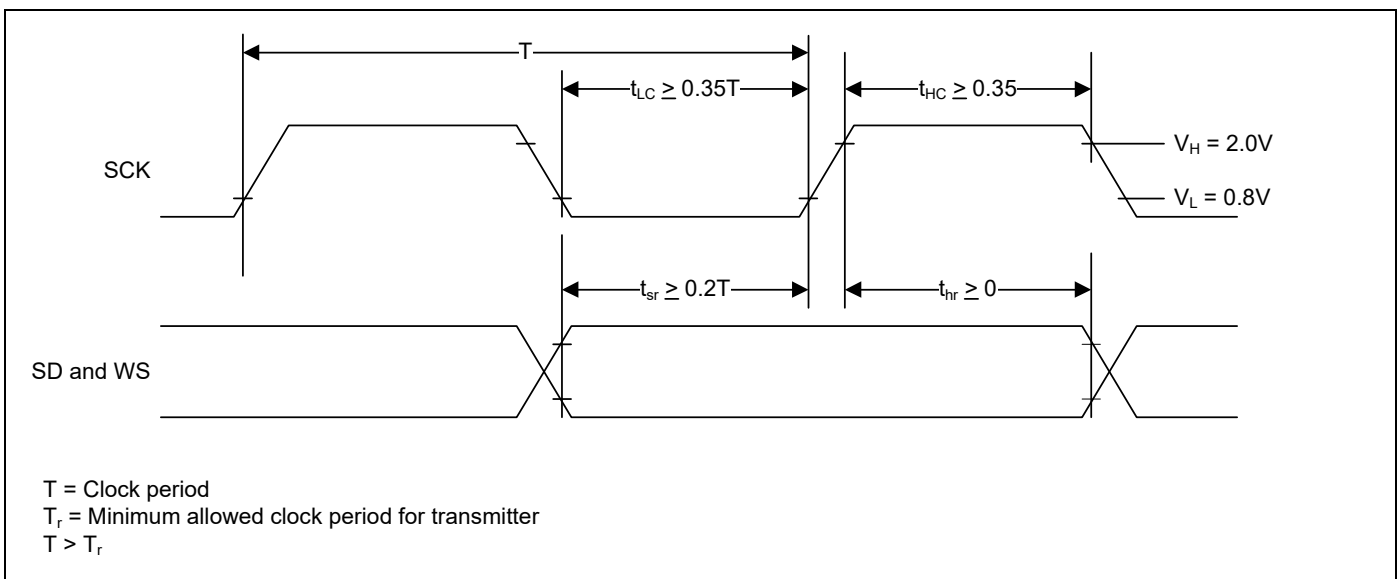


Figure 19. I<sup>2</sup>S Receiver Timing



9. Mechanical Information

Figure 20. CYW20713A1KUFBXG Mechanical Drawing

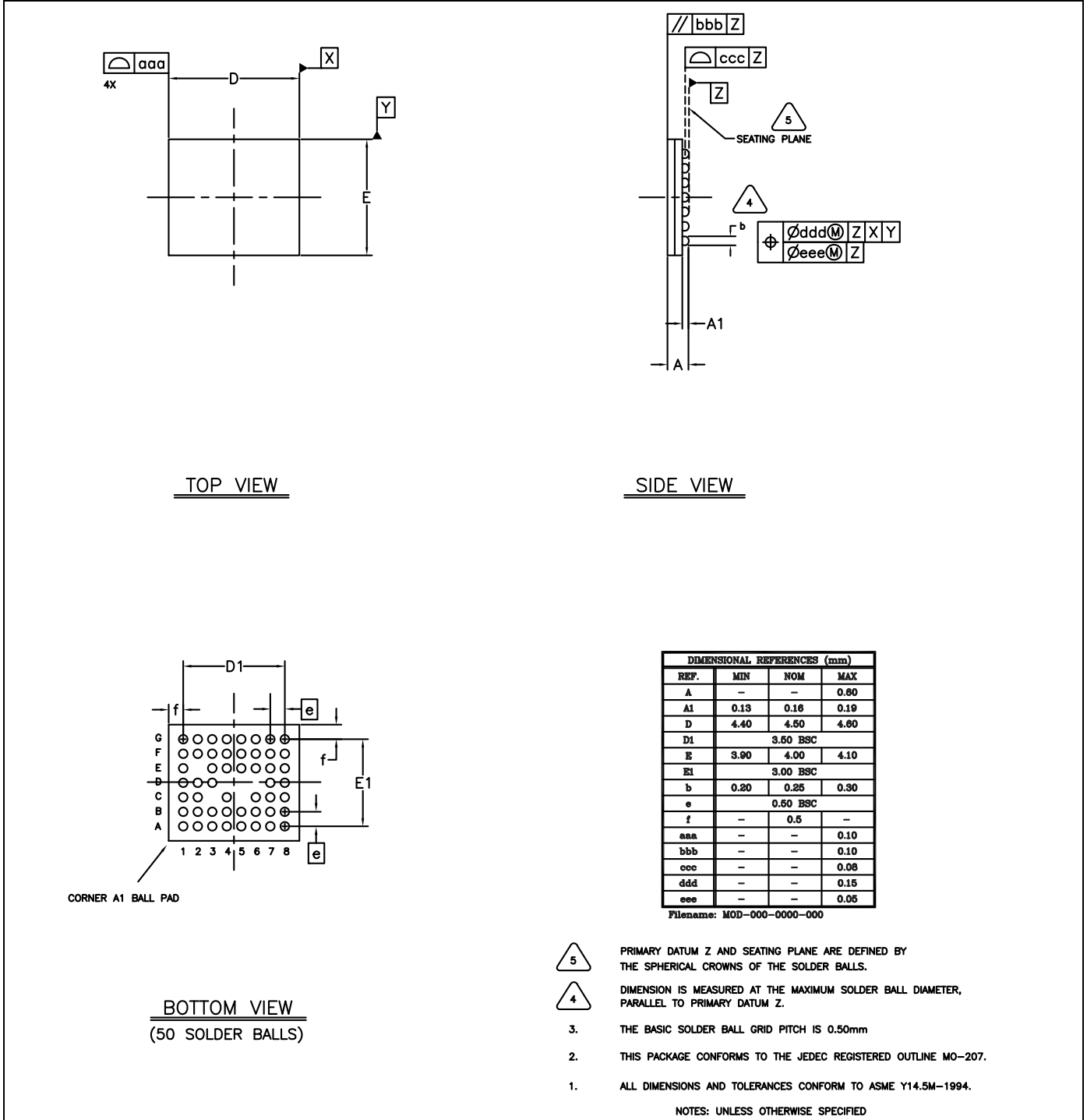
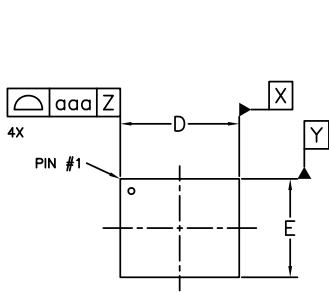
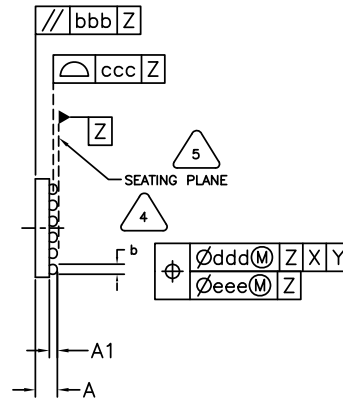




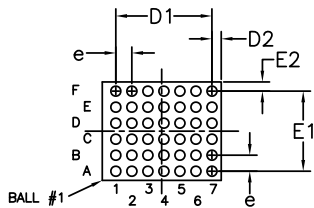
Figure 21. 42-Bump CYW20713A1KUBG Mechanical Drawing



TOP VIEW



SIDE VIEW



BOTTOM VIEW  
(42 SOLDER BALLS)

| DIMENSIONAL REFERENCES (mm) |            |       |       |
|-----------------------------|------------|-------|-------|
| REF.                        | MIN        | NOM   | MAX   |
| A                           | 0.500      | 0.550 | 0.600 |
| A1                          | 0.160      | 0.190 | 0.220 |
| D                           | 2.950      | 3.019 | 3.044 |
| E                           | 2.440      | 2.509 | 2.534 |
| D1                          | 2.400 REF. |       |       |
| E1                          | 2.000 REF. |       |       |
| D2                          | 0.255 REF. |       |       |
| E2                          | 0.255 REF. |       |       |
| b                           | 0.230      | 0.270 | 0.320 |
| e                           | 0.40 BSC   |       |       |
| f                           | -          | -     | -     |
| aaa                         | -          | -     | 0.10  |
| bbb                         | -          | -     | 0.10  |
| ccc                         | -          | -     | 0.03  |
| ddd                         | -          | -     | 0.15  |
| eee                         | -          | -     | 0.05  |

Filename: P-MOD-XXXX-000



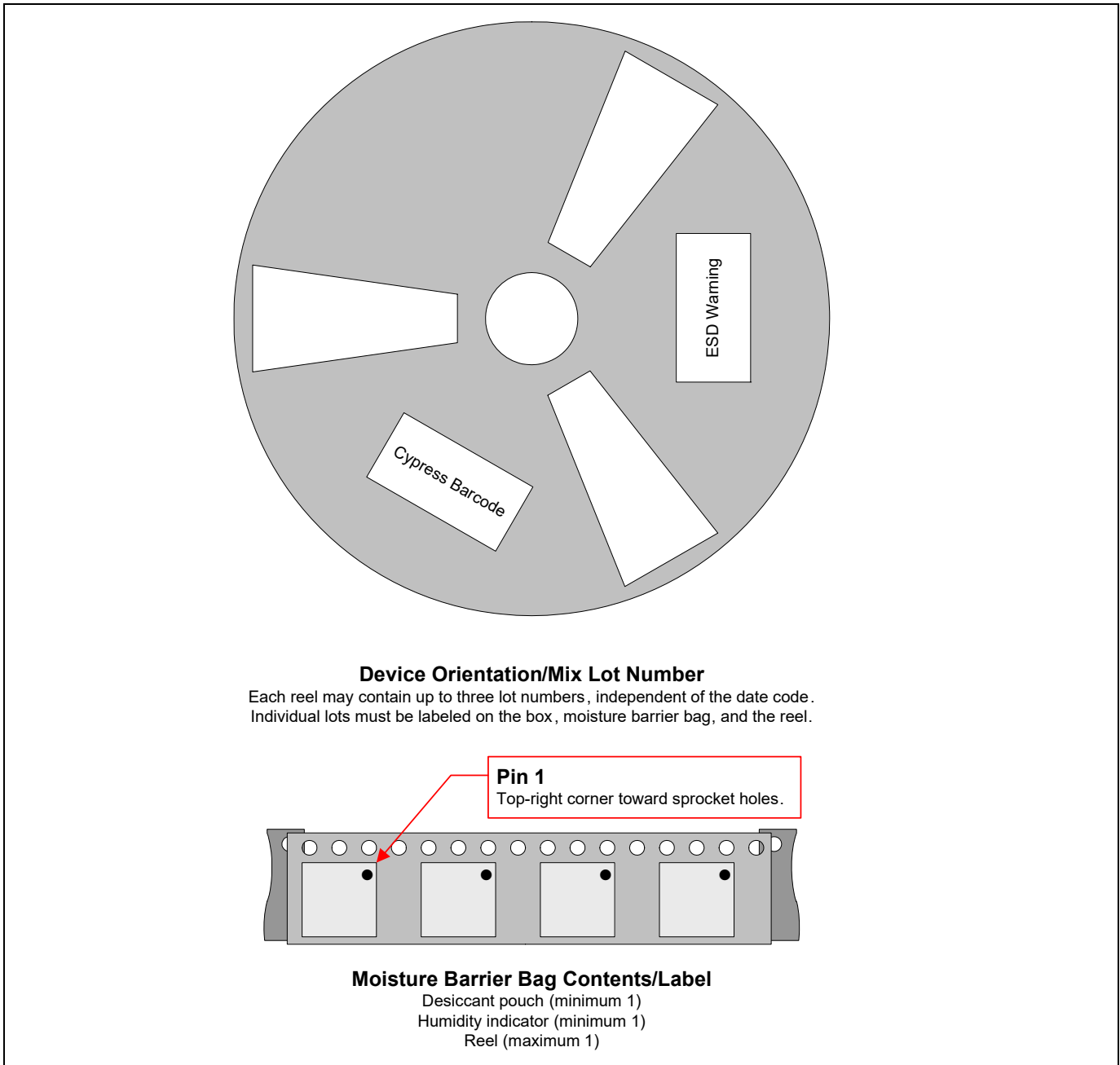
PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.



DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL PITCH IS 0.40mm
2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-225.
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

**9.1 Tape, Reel, and Packing Specification****Figure 22. Reel, Labeling, and Packing Specification**

## 10. Ordering Information

Table 30 lists available part numbers and describes differences in package type, available I/O, and functional configuration. See the referenced figures and tables for mechanical drawings and package I/O information.

All packages are rated from -40°C to +85°C.

**Table 30. Part Ordering Information**

| Part Number      | Package Type   | Functional I/O Features   | Strapped Configuration      |
|------------------|--|---|-----------------------------|
| CYW20713A1KUFBXG | 50-ball FPBGA,<br>4.5 mm x 4.0 mm x 0.6 mm.<br>See <a href="#">Figure 20 on page 47</a> .    | Dedicated Coex <sup>a</sup> , more GPIO, TM0 <sup>b</sup><br><a href="#">Table 9 on page 27</a> | TCXO AND/OR<br>mode enabled |
| CYW20713A1KUBG   | 42-bump WLPGA,<br>3.02 mm x 2.51 mm x 0.55 mm.<br>See <a href="#">Figure 21 on page 48</a> . | <a href="#">Table 10 on page 28</a>   | TCXO AND/OR<br>mode enabled |

- a. All packages support coexistence features through the ability to re-purpose most digital I/O based on the desired user configuration. Package include balls coexistence functionality (default).
- b. TM0 allows configuration of CLK\_REQ output polarity.

**Document History**

| Document Title: CYW20713 Single-Chip Bluetooth Transceiver and Baseband Processor |         |                 |   |
|---|---------|-----------------|---|
| Document Number: 002-14806  |         |                 |   |
| Revision  | ECN     | Submission Date | Description of Change   |
| **  | –       | 08/14/2014      | 20713-DS100-R<br>Initial release                              |
| *A  | –       | 10/16/2014      | 20713-DS101-R<br>Updated:<br>■ General description on page 1. |
| *B  | –       | 12/22/2015      | 20713-DS102-R<br>Added I2S Interface                          |
| *C  | 5482527 | 10/20/2016      | Updated to Cypress Template                                   |
| *D  | 5962278 | 11/09/2017      | Updated logo and copyright.                                   |
| *E  | 6659129 | 08/21/2019      | Added BT-SIG declaration and QDID numbers in page 1           |

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