SLG46855-A

Auto AEC-Q100 Qualified GreenPAK Programmable Mixed-Signal Matrix

General Description

The SLG46855-A provides a small, low power component for commonly used Mixed-Signal functions. The user creates their circuit design by programming the one time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, and the macrocells of the SLG46855-A. This highly versatile device allows a wide variety of Mixed-Signal functions to be designed within a very small, low power single integrated circuit.

Key Features

- Two High Speed General Purpose Analog Comparators (ACMPxH)
- Two Low Power General Purpose Analog Comparators (ACMPxL)
- Two Voltage References (Vref)
  - Two Vref Outputs
- Fifteen Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Nine Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter, or 3-bit LUT
  - One Selectable DFF/LATCH or 4-bit LUTs
- Eight Multi-Function Macrocells
  - Seven Selectable DFF/LATCH or 3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/LATCH or 4-bit LUT + 16-bit Delay/Counter
- Serial Communications
  - I^2C Protocol Interface
- Programmable Delay with Edge Detector Output
- Deglitch Filter or Edge Detector
- Three Oscillators (OSC)
  - 2.048 kHz Oscillator
  - 2.048 MHz Oscillator
  - 25 MHz Oscillator
- Analog Temperature Sensor
- Power-On Reset (POR)
- Read Back Protection (Read Lock)
- Power Supply
  - 2.5 V (±8 %) to 5 V (±10 %)
- Ambient Operating Temperature Range: -40 °C to 105 °C
- RoHS Compliant/Halogen-Free
- Available Package
- 14-pin FCQFN: 3.0 mm x 3.0 mm x 0.55 mm, 0.65 mm pitch
- AEC-Q100 (T_A = -40 °C to 105 °C) Qualified

Applications

- Infotainment
- Advanced Driver Assistance Systems (ADAS)
- Instrument clusters
- Audio, video, navigation

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1 Block Diagram

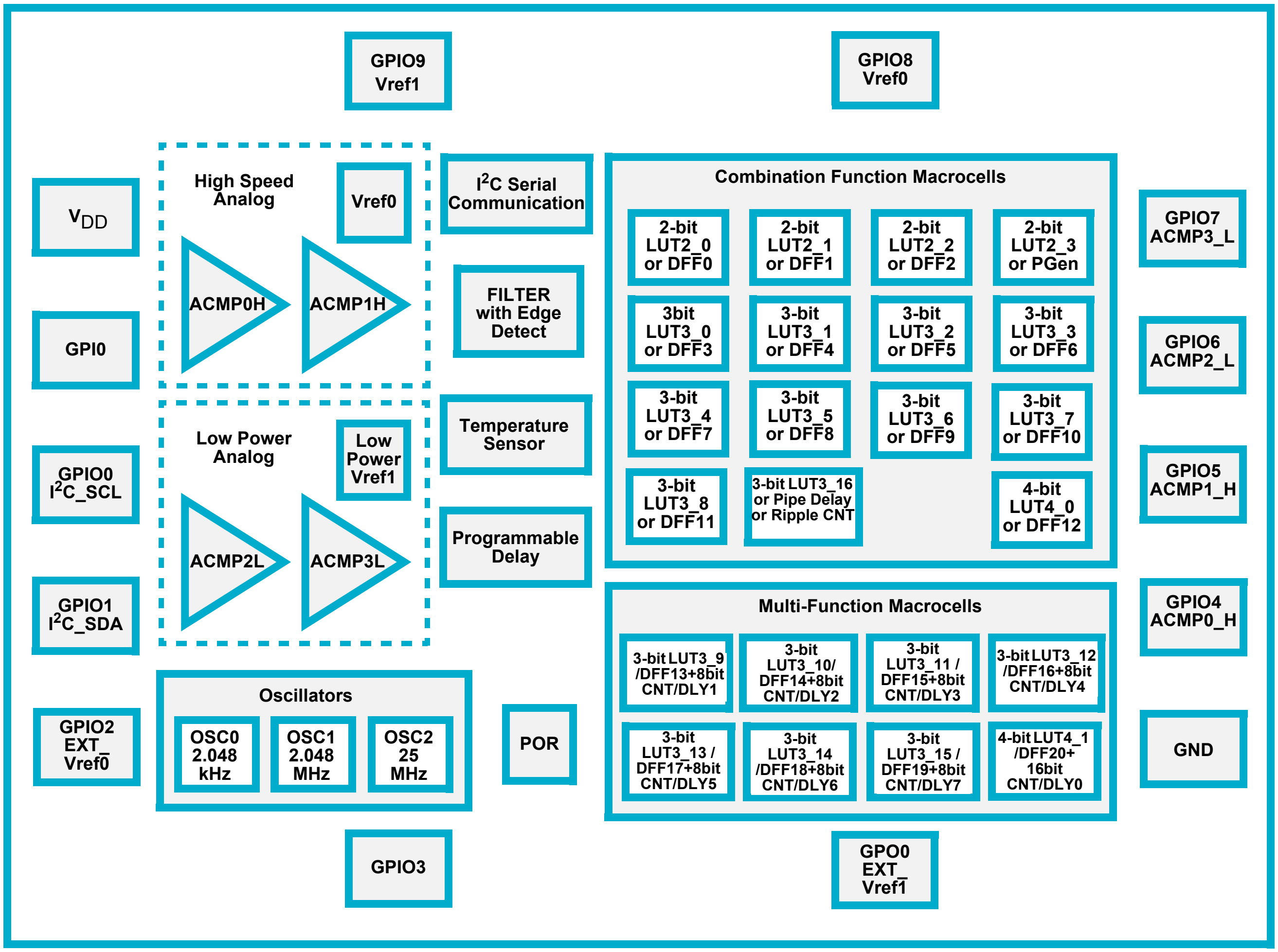
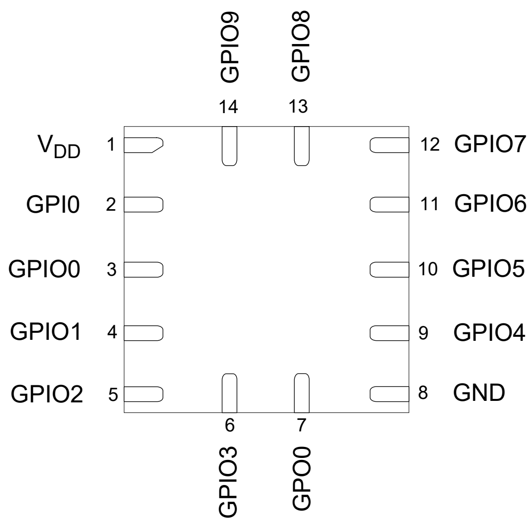


Figure 1: Block Diagram

2 Pinout

2.1 PIN CONFIGURATION - FCQFN- 14L



FCQFN-14L (Top View)

Pin #	Pin Name	Pin Functions
1	V_{DD}	Power Supply
2	GPI0	GPI, SLA_0
3	GPIO0	GPIO, SCL
4	GPIO1	GPIO, SDA
5	GPIO2	GPIO with OE, EXT_Vref0, SLA_1
6	GPIO3	GPIO with OE
7	GPO0	GPO, EXT_Vref1
8	GND	Ground
9	GPIO4	GPIO with OE, ACMP0_H+, SLA_2
10	GPIO5	GPIO with OE, ACMP1_H+, SLA_3
11	GPIO6	GPIO with OE, ACMP2_L+
12	GPIO7	GPIO with OE, ACMP3_L+
13	GPIO8	GPIO with OE, Vref0_OUT, TS_OUT
14	GPIO9	GPIO with OE, Vref1_OUT

Legend:

OE: Output Enable
ACMPx+: ACMPx Positive Input
ACMPx-: ACMPx Negative Input
SCL: I^2C Clock Input
SDA: I^2C Data Input/Output
Vrefx: Voltage Reference Output
EXT_CLKx: External Clock Input
SLA: Slave Address
TS_OUT: Temperature Output

Table 1: Functional Pin Description

FCQFN 14L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
1	V_{DD}	V_{DD}	Power Supply	--	--
		ACMP0_H+	Analog Comparator 0 Positive Input	Analog	--
		ACMP1_H+	Analog Comparator 1 Positive Input	Analog	--
		ACMP2_L+	Analog Comparator 2 Positive Input	Analog	--
		ACMP3_L+	Analog Comparator 3 Positive Input	Analog	--
2	GPI0	GPI0	General Purpose Input	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
		Slave Address 0		--	--

Table 1: Functional Pin Description(Continued)

FCQFN 14L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
3	GPIO0	GPIO0	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Open-Drain NMOS (3.2x)
				Digital Input with Schmitt Trigger	
				Low Voltage Digital Input	--
		SCL	I^{2}C Serial Clock	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
4	GPIO1	GPIO1	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS (3.2x)
				Digital Input with Schmitt Trigger	
				Low Voltage Digital Input	
		SDA	I^{2}C Serial Data	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
5	GPIO2	GPIO2	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		Slave Address 1		--	--
		EXT_VREF0	Analog Comparator Negative Input	Analog	--
6	GPIO3	GPIO3	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
7	GPO0	GPO0	General Purpose Output	--	Push-Pull (1x) (2x)
				--	Open-Drain NMOS (1x) (2x) (4x)
		EXT_VREF1	Analog Comparator Negative Input	Analog	--
8	GND	GND	Power Supply	--	--

Table 1: Functional Pin Description(Continued)

FCQFN 14L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
9	GPIO4	GPIO4	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x) (4x)
				Low Voltage Digital Input	--
		ACMP0_H+	Analog Comparator 0_H Positive Input	Analog	--
		Slave Address 2		--	--
10	GPIO5	GPIO5	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP1_H+	Analog Comparator 1_H Positive Input	Analog	--
		Slave Address 3		--	--
11	GPIO6	GPIO6	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP2_L+	Analog Comparator 2_L Positive Input	Analog	--
12	GPIO7	GPIO7	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP3_L+	Analog Comparator 3_L Positive Input	Analog	--
13	GPIO8	GPIO8	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		Vref0	Vref0 Output	Analog	--
14	GPIO9	GPIO9	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		Vref1	Vref1 Output	Analog	--

Note 1 General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure.

Table 2: Pin Type Definitions

Pin Type	Description
V_{DD}	Power Supply
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
GND	Ground

3 Characteristics

3.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage on V_{DD} relative to GND		-0.3	7	V
DC Input Voltage		GND - 0.5 V	V_{DD} + 0.5 V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)		--	90	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	Push-Pull 2x	--	16	
	Push-Pull 4x	--	32	
	OD 1x	--	11	
	OD 2x	--	21	
	OD 4x	--	43	
Current at Input Pin		-1.0	1.0	mA
Input Leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Moisture Sensitive Level		1		

3.2 ELECTROSTATIC DISCHARGE RATINGS

Table 4: Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V

3.3 RECOMMENDED OPERATING CONDITIONS

Table 5: Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		2.3	5.5	V
Operating Ambient Temperature		-40	105	°C
Maximal Voltage Applied to any PIN in High Impedance State		--	V_{DD}+ 0.3	V
Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	0	V_{DD}	V

3.4 ELECTRICAL CHARACTERISTICS

Table 6: EC at T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IH}	HIGH-Level Input Voltage	Logic Input (Note 1)	0.7x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with Schmitt Trigger	0.8x V_{DD}	--	V_{DD}+ 0.3	V
		Low-Level Logic Input (Note 1)	1.25	--	V_{DD}+ 0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input (Note 1)	GND- 0.3	--	0.3x V_{DD}	V
		Logic Input with Schmitt Trigger	GND- 0.3	--	0.2x V_{DD}	V
		Low-Level Logic Input (Note 1)	GND- 0.3	--	0.5	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull, 1x Drive, V_{DD} = 2.3 V, I_{OH} = 1 mA	2.17	--	--	V
		Push-Pull, 1x Drive, V_{DD} = 3.3 V, I_{OH} = 3 mA	3.02	--	--	V
		Push-Pull, 1x Drive, V_{DD} = 5.5 V, I_{OH} = 5 mA	5.19	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 2.3 V, I_{OH} = 1 mA	2.23	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 3.3 V, I_{OH} = 3 mA	3.16	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 5.5 V, I_{OH} = 5 mA	5.34	--	--	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, I_{OH} = 1 mA	2.27	--	--	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, I_{OH} = 3mA	3.23	--	--	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, I_{OH} = 5 mA	5.41	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, 1x Drive, V_{DD} = 2.3 V, I_{OL}= 1 mA	--	--	0.100	V
		Push-Pull, 1x Drive, V_{DD} = 3.3 V, I_{OL} = 3 mA	--	--	0.227	V
		Push-Pull, 1x Drive, V_{DD} = 5.5 V, I_{OL}= 5 mA	--	--	0.272	V
		Push-Pull, 2x Drive, V_{DD} = 2.3 V, I_{OL} = 1 mA	--	--	0.049	V
		Push-Pull, 2x Drive, V_{DD} = 3.3 V, I_{OL}= 3 mA	--	--	0.112	V

Table 6: EC at T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull, 2x Drive, V_{DD} = 5.5 V, I_{OL} = 5 mA	--	--	0.137	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, I_{OL} = 1 mA	--	--	0.023	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, I_{OL}= 3 mA	--	--	0.055	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, I_{OL} = 5 mA	--	--	0.067	V
		NMOS OD, 1x Drive, V_{DD} = 2.3 V, I_{OL} = 1 mA	--	--	0.042	V
		NMOS OD, 1x Drive, V_{DD} = 3.3 V, I_{OL} = 3 mA	--	--	0.093	V
		NMOS OD, 1x Drive, V_{DD} = 5.5 V, I_{OL} = 5 mA	--	--	0.117	V
		NMOS OD, 2x Drive, V_{DD} = 2.3 V, I_{OL} = 1 mA	--	--	0.020	V
		NMOS OD, 2x Drive, V_{DD} = 3.3 V, I_{OL} = 3 mA	--	--	0.047	V
		NMOS OD, 2x Drive, V_{DD} = 5.5 V, I_{OL} = 5 mA	--	--	0.058	V
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, I_{OL} = 1 mA	--	--	0.009	V
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, I_{OL} = 3 mA	--	--	0.022	V
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, I_{OL} = 5 mA	--	--	0.027	V
I_{OH}	HIGH-Level Output Pulse Current **(Note 2)**	Push-Pull, 1x Drive, V_{DD} = 2.3 V, V_{OH} = V_{DD} - 0.2 V	1.44	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 3.3 V, V_{OH} = 2.4 V	7.75	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 5.5 V, V_{OH} = 2.75 V	26.98	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 2.3 V, V_{OH} = V_{DD} - 0.2 V	2.82	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 3.3 V, V_{OH} = 2.4 V	15.12	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 5.5 V, V_{OH} = 2.75 V	51.97	--	--	mA
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, V_{OH} = V_{DD} - 0.2 V	5.47	--	--	mA
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, V_{OH} = 2.4 V	28.97	--	--	mA

Table 6: EC at T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	HIGH-Level Output Pulse Current (Note 2)	Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, V_{OH} = 2.75 V	97.85	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (Note 2)	Push-Pull, 1x Drive, V_{DD} = 2.3 V, V_{OL} = 0.2 V	1.92	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 3.3 V, V_{OL} = 0.4 V	5.01	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 5.5 V, V_{OL} = 0.4 V	7.10	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 2.3 V, V_{OL} = 0.2 V	3.84	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 3.3 V, V_{OL} = 0.4 V	9.96	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 5.5 V, V_{OL} = 0.4 V	13.96	--	--	mA
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, V_{OL} = 0.2 V	7.72	--	--	mA
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, V_{OL} = 0.4 V	20.12	--	--	mA
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, V_{OL} = 0.4 V	28.34	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 2.3 V, V_{OL} = 0.2 V	4.71	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 3.3 V, V_{OL} = 0.4 V	12.21	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 5.5 V, V_{OL} = 0.4 V	16.95	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 2.3 V, V_{OL} = 0.2 V	9.24	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 3.3 V, V_{OL} = 0.4 V	23.68	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 5.5 V, V_{OL} = 0.4 V	32.64	--	--	mA
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, V_{OL} = 0.2 V	18.96	--	--	mA
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, V_{OL} = 0.4 V	49.08	--	--	mA
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, V_{OL} = 0.4 V	68.27	--	--	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}, T_{RAMP} = 10 ms	--	1.4	2.1	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	1.56	1.84	2.03	V

Table 6: EC at T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.83	1.16	1.63	V
R_{PULL}	Pull-up or Pull-down Resistance	1 M for Pull-up: V_{IN} = GND	--	1	--	MΩ
		1 M for Pull-down: V_{IN} = V_{DD}	--	1	--	MΩ
		100 k for Pull-up: V_{IN} = GND	--	100	--	kΩ
		100 k for Pull-down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 k For Pull-up: V_{IN} = GND	--	10	--	kΩ
		10 k for Pull-down: V_{IN} = V_{DD}	--	10	--	kΩ
C_{IN}	Input Capacitance			4		pF
I_{LKG}	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = V_{DD}, V_{DD} = 2.3 V, All Pins	--	4.61	--	nA
		Vin = V_{DD}, V_{DD} = 3.3 V, All Pins	--	5.00	--	nA
		Vin = V_{DD}, V_{DD} = 5.5 V, All Pins	--	6.56	--	nA
		Vin = 0, V_{DD} = 2.3 V, All Pins	--	1.41	--	nA
		Vin = 0, V_{DD} = 3.3 V, All Pins	--	1.58	--	nA
		Vin = 0, V_{DD} = 5.5 V, All Pins	--	4.44	--	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = V_{DD}, V_{DD} = 2.3 V, All Pins	--	4.72	--	nA
		Vin = V_{DD}, V_{DD} = 3.3 V, All Pins	--	5.10	--	nA
		Vin = V_{DD}, V_{DD} = 5.5 V, All Pins	--	6.64	--	nA
		Vin = 0, V_{DD} = 2.3 V, All Pins	--	1.46	--	nA
		Vin = 0, V_{DD} = 3.3 V, All Pins	--	1.62	--	nA
		Vin = 0, V_{DD} = 5.5 V, All Pins	--	4.48	--	nA
	Low-Level Logic Input (Floating) Leakage	Vin = V_{DD}, V_{DD} = 2.3 V, All Pins	--	4.64	--	nA
		Vin = V_{DD}, V_{DD} = 3.3 V, All Pins	--	5.01	--	nA
		Vin = V_{DD}, V_{DD} = 5.5 V, All Pins	--	6.52	--	nA
		Vin = 0, V_{DD} = 2.3 V, All Pins	--	1.43	--	nA
		Vin = 0, V_{DD} = 3.3 V, All Pins	--	1.59	--	nA
		Vin = 0, V_{DD} = 5.5 V, All Pins	--	4.43	--	nA

Note 1 No hysteresis.
Note 2 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

3.5 I²C PINS ELECTRICAL CHARACTERISTICS

Table 7: EC of the I²C Pins for DI Mode at T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
V_{IL}	LOW-level Input Voltage		-0.5	0.3xV_{DD}	-0.5	0.3xV_{DD}	V
V_{IH}	HIGH-level Input Voltage		0.7xV_{DD}	5.5	0.7xV_{DD}	5.5	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05xV_{DD}	--	0.05xV_{DD}	--	V

Table 7: EC of the I²C Pins for DI Mode at T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
V_{OL1}	LOW-Level Output Voltage 1	(Open-Drain or open collector) at 3 mA sink current V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL2}	LOW-Level Output Voltage 2	(Open-Drain or open/ collector) at 2 mA sink current V_{DD} ≤ 2 V	0	0.2xV_{DD}	0	0.2xV_{DD}	V
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} **(Note 1)**		14x (V_{DD}/5.5V)	250	10x (V_{DD}/5.5V)	120	ns
I_i	Input Current each IO Pin	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	-10	+10	µA
C_i	Capacitance for each IO Pin		--	10	--	10	pF

Note 1 Does not meet standard I²C specifications: t_{of} = 20x(V_{DD}/5.5V) (min).
Note 2 For Fast-mode Plus SDA pin must be configured as NMOS 3.2x Open-Drain, see register [796] in section 17.

Table 8: EC of the I²C Pins for DILV Mode at T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Unit
			Min	Max	
V_{IL}	LOW-level Input Voltage **(Note 1)**		GND-0.3	0.5	V
V_{IH}	HIGH-level Input Voltage **(Note 1)**		1.25	V_{DD}+0.3	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05xV_{DD}	--	V
V_{OL1}	LOW-Level Output Voltage 1	(Open-Drain or open collector) at 3mA sink current V_{DD} > 2 V	0	0.4	V
V_{OL2}	LOW-Level Output Voltage 2	(Open-Drain or open collector) at 2 mA sink current V_{DD} ≤ 2 V	0	0.2xV_{DD}	V
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} **(Note 1)**		14x (V_{DD}/5.5V)	250	ns
I_i	Input Current each IO Pin	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	µA
C_i	Capacitance for each IO Pin		--	10	pF

Note 1 Does not meet standard I²C specifications: V_{IL} = -0.5 V (min), V_{IL} = 0.3xV_{DD} (max), V_{IH} = 0.7xV_{DD} (min), V_{IH} = 5.5 V (max), t_{of} = 20x(V_{DD}/5.5V) (min).

Table 9: I²C Pins Timing Characteristics, DI Mode, T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Speed						Unit
			400 kHz			1 MHz			
			Min	Typ	Max	Min	Typ	Max	
F_{SCL}	Clock Frequency, SCL		--	--	400	--	--	1000	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	--	500	--	--	ns

Table 9: I^{2}C Pins Timing Characteristics, DI Mode, T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Speed						Unit
			400 kHz			1 MHz			
			Min	Typ	Max	Min	Typ	Max	
t_{HIGH}	Clock Pulse Width High		600	--	--	260	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA) **(Note 1)**	V_{DD} = 2.3 V	--	--	90	--	--	87	ns
		V_{DD} = 3.3 V	--	--	90	--	--	87	
		V_{DD} = 5.5 V	--	--	90	--	--	87	
$t_{VD;ACK}$	Data Valid Acknowledge Time		--	--	900	--	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	--	500	--	--	ns
t_{HD_STA}	Start Hold Time		600	--	--	260	--	--	ns
t_{SU_STA}	Start Set-up Time		600	--	--	260	--	--	ns
t_{HD_DAT}	Data Hold Time	Rising Edge	0	--	--	0	--	--	ns
		Falling Edge	0	--	--	0	--	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	--	50	--	--	ns
t_R	Inputs Rise Time	C = 15 pF	--	--	300	--	--	120	ns
		C = 100 pF	--	--	300	--	--	120	ns
		C = 400 pF	--	--	300	--	--	120	ns
t_F	Inputs Fall Time	C = 15 pF	--	--	300	--	--	120	ns
		C = 100 pF	--	--	300	--	--	120	ns
		C = 400 pF	--	--	300	--	--	120	ns
t_{SU_STO}	Stop Set-up Time		600	--	--	260	--	--	ns
$t_{VD;DAT}$	Data Valid Time		50	--	--	50	--	--	ns

Note 1 Does not meet standard I^{2}C specifications: t_I = 95 ns for V_{DD} = 2.3 V, t_I = 95 ns for V_{DD} = 3.3 V, t_I = 111 ns for V_{DD} = 5.5V for 400 kHz; t_I = 168 ns for V_{DD} = 2.3 V, t_I = 157 ns for V_{DD} = 3.3 V, t_I = 156 ns for V_{DD} = 5.5 V for 1 MHz.
Note 2 Timing diagram can be found in the Figure 100.
Note 3 Please follow official I^{2}C spec UM10204.

Table 10: I^{2}C Pins Timing Characteristics, DILV Mode, T_A = -40°C to +105°C, V_{DD} = 2.3V to 5.5V Unless Otherwise Noted

Parameter	Description	Condition	Speed			Unit
			400 kHz			
			Min	Typ	Max	
F_{SCL}	Clock Frequency, SCL		--	--	400	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA) **(Note 1)**	V_{DD} = 2.3 V	--	--	300	ns
		V_{DD} = 3.3 V	--	--	235	
		V_{DD} = 5.5 V	--	--	185	
t_{AA}	Clock Low to Data Out Valid		--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	--	ns
t_{HD_STA}	Start Hold Time		600	--	--	ns

Table 10: I^2C Pins Timing Characteristics, DILV Mode, T_A = -40°C to +105°C, V_{DD} = 2.3V to 5.5V Unless Otherwise Noted

Parameter	Description	Condition	Speed 400 kHz Min	Speed 400 kHz Typ	Speed 400 kHz Max	Unit
t_{SU_STA}	Start Set-up Time		600	--	--	ns
t_{HD_DAT}	Data Hold Time **(Note 1)**	Rising Edge	255	--	--	ns
		Falling Edge	0	--	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	--	ns
t_R	Inputs Rise Time	C = 15 pF	--	--	300	ns
		C = 100 pF	--	--	300	ns
		C = 400pF	--	--	300	ns
t_F	Inputs Fall Time	C = 15 pF	--	--	300	ns
		C = 100 pF	--	--	300	ns
		C = 400 pF	--	--	300	ns
t_{SU_STO}	Stop Set-up Time		600	--	--	ns
t_{DH}	Data Out Hold Time		50	--	--	ns

Note 1 Does not meet standard I^2C specifications: t_I = 95 ns for V_{DD} = 2.3 V, t_I = 95 ns for V_{DD} = 3.3 V, t_I = 111 ns for V_{DD} = 5.5 V; t_{HD_DAT} = 0 ns (min) for Rising Edge.
Note 2 Timing diagram can be found in the Figure 100.
Note 3 Please follow official I^2C spec UM10204.
Note 4 When SCL Input is in Low-Level Logic mode max frequency is 400 kHz.

3.6 MACROCELLS CURRENT CONSUMPTION

Table 11: Typical Current Estimated for Each Macrocell at T_A = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I_{DD}	Current	Chip Quiescent	0.34	0.39	0.46	µA
		Vref0, SourceNone	7.61	7.67	7.88	µA
		Vref1, SourceNone	1.39	1.42	1.51	µA
		OSC2 25 MHz, pre-divider = 1, second divider = 1	50.46	62.63	90.60	µA
		OSC2 25 MHz, pre-divider = 4, second divider = 1	33.46	39.91	55.47	µA
		OSC2 25 MHz, pre-divider = 8, second divider = 1	30.35	35.75	49.03	µA
		OSC1 2.048 MHz, pre-divider = 1, second divider = 1	20.64	21.99	24.94	µA
		OSC1 2.048 MHz, pre-divider = 4, second divider = 1	18.56	19.21	20.61	µA
		OSC1 2.048 MHz, pre-divider = 8, second divider = 1	18.18	18.71	19.84	µA
		OSC0 2.048 kHz, pre-divider = 1, second divider = 1	0.62	0.66	0.77	µA
		OSC0 2.048 kHz, pre-divider = 4, second divider = 1	0.62	0.66	0.76	µA
		OSC0 2.048 kHz, pre-divider = 8, second divider = 1	0.61	0.66	0.76	µA
		Temperature Sensor, output range 1 (0.62 V to 0.99 V)	14.80	14.87	15.43	µA
		Temperature Sensor, output range 2 (0.75 V to 1.2 V)	14.94	15.02	15.43	µA
		All ACMPs (includes internal Vref, Vin+ = 0, Vref = 32 mV)	37.36	38.10	40.42	µA
		All ACMPxH (includes internal Vref, Vin+ = 0, Vref = 32 mV)	48.95	50.26	53.90	µA
		ACMP0H 100µA Enabled (includes internal Vref, Vin+ = 0, Vref = 32 mV)	35.95	36.65	38.92	µA
		Any ACMPxL (includes internal Vref, Vin+ = 0, Vref = 32 mV)	1.89	1.93	2.04	µA

3.7 TIMING CHARACTERISTICS

Table 12: Typical Delay Estimated for Each Macrocell at T_A = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital Input to PP 1x	23	26	17	19	12	15	ns
tpd	Delay	Digital Input to PP 2x	22	25	16	16	12	14	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1x	24	27	18	21	14	15	ns
tpd	Delay	Low Voltage Digital Input to PP 1x	38	241	26	164	18	104	ns
tpd	Delay	Digital input to NMOS 1x	--	24	--	18	--	13	ns

Table 12: Typical Delay Estimated for Each Macrocell at T_A = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital input to NMOS 2x	--	23	--	17	--	13	ns
tpd	Delay	Digital input to NMOS 4x	--	23	--	17	--	13	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 1	23	--	16	--	12	--	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 0	--	22	--	16	--	12	ns
tpd	Delay	PP 1x 3 State Hi-Z to 1	22	--	16	--	12	--	ns
tpd	Delay	PP 1x 3 State Hi-Z to 0	--	22	--	16	--	12	ns
tpd	Delay	PP 2x 3 State Hi-Z to 1	21	--	16	--	12	--	ns
tpd	Delay	PP 2x 3 State Hi-Z to 0	--	21	--	15	--	11	ns
tpd	Delay	LATCH Q	16	18	11	13	8	9	ns
tpd	Delay	LATCH nQ	19	15	14	11	9	7	ns
tpd	Delay	LATCH nRESET High Q	25	21	17	15	12	10	ns
tpd	Delay	LATCH nRESET High nQ	22	24	16	17	11	12	ns
tpd	Delay	LATCH nRESET Low Q	22	23	15	16	11	12	ns
tpd	Delay	LATCH nRESET Low nQ	24	21	17	15	12	10	ns
tpd	Delay	LATCH nSET High Q	19	21	14	15	9	10	ns
tpd	Delay	LATCH nSET High nQ	22	19	16	13	11	9	ns
tpd	Delay	LATCH nSET Low Q	22	18	16	13	11	9	ns
tpd	Delay	LATCH nSET Low nQ	19	21	14	15	9	10	ns
tpd	Delay	Multi-Function LATCH Q	19	22	14	16	9	11	ns
tpd	Delay	Multi-Function LATCH nQ	22	19	16	13	11	9	ns
tpd	Delay	Multi-Function LATCH nRESET Q	23	27	16	19	11	14	ns
tpd	Delay	Multi-Function LATCH nRESET nQ	27	23	20	17	14	11	ns
tpd	Delay	Multi-Function LATCH nSET Q	25	21	18	15	13	10	ns
tpd	Delay	Multi-Function LATCH nSET nQ	21	25	15	18	10	13	ns
tpd	Delay	LATCH3, LATCH12 First Q	17	19	12	14	8	9	ns
tpd	Delay	LATCH3, LATCH12 First nQ	20	17	14	12	10	8	ns
tpd	Delay	LATCH3, LATCH12 First nRESET High Q	26	23	18	16	13	11	ns
tpd	Delay	LATCH3, LATCH12 First nRESET High nQ	24	26	17	18	12	13	ns
tpd	Delay	LATCH3, LATCH12 First nRESET Low Q	23	25	16	18	11	12	ns
tpd	Delay	LATCH3, LATCH12 First nRESET Low nQ	26	23	18	16	13	11	ns
tpd	Delay	LATCH3, LATCH12 First nSET High Q	21	22	15	16	10	11	ns
tpd	Delay	LATCH3, LATCH12 First nSET High nQ	23	20	17	14	12	10	ns
tpd	Delay	LATCH3, LATCH12 First nSET Low Q	23	20	16	14	11	10	ns
tpd	Delay	LATCH3, LATCH12 First nSET Low nQ	21	23	15	16	10	11	ns
tpd	Delay	LATCH3, LATCH12 Second Q	19	19	13	13	9	9	ns
tpd	Delay	LATCH3, LATCH12 Second nQ	20	18	14	13	10	9	ns
tpd	Delay	LATCH3, LATCH12 Second nRESET High Q	--	22	--	16	--	11	ns

Table 12: Typical Delay Estimated for Each Macrocell at T_A = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	LATCH3, LATCH12 Second nRESET High nQ	23	--	17	--	12	--	ns
tpd	Delay	LATCH3, LATCH12 Second nRESET Low Q	--	25	--	18	--	12	ns
tpd	Delay	LATCH3, LATCH12 Second nRESET Low nQ	26	--	18	--	13	--	ns
tpd	Delay	LATCH3, LATCH12 Second nSET High Q	20	--	14	--	10	--	ns
tpd	Delay	LATCH3, LATCH12 Second nSET High nQ	--	20	--	14	--	10	ns
tpd	Delay	LATCH3, LATCH12 Second nSET Low Q	23	--	16	--	11	--	ns
tpd	Delay	LATCH3, LATCH12 Second nSET Low nQ	--	22	--	16	--	11	ns
tpd	Delay	2-bit LUT	15	16	11	11	7	8	ns
tpd	Delay	3-bit LUT	16	17	11	12	8	8	ns
tpd	Delay	4-bit LUT	19	17	13	12	9	9	ns
tpd	Delay	Multi-Function 3-bit LUT	18	21	13	15	9	11	ns
tpd	Delay	Multi-Function 3-bit LUT, CNT Delay	46	47	33	34	23	24	ns
tpd	Delay	Multi-Function 4-bit LUT	21	23	15	17	10	12	ns
tpd	Delay	Multi-Function 4-bit LUT, CNT Delay	48	46	34	34	23	24	ns
tpd	Delay	Edge detect	19	20	13	14	9	9	ns
tw	Width	Edge detect	211	212	156	157	115	115	ns
tpd	Delay	Edge detect Delayed	231	235	170	173	124	126	ns
tpd	Delay	Ripple CNT CLK DOWN Q0	18	16	13	11	9	8	ns
tpd	Delay	Ripple CNT CLK DOWN Q1	29	22	20	16	14	11	ns
tpd	Delay	Ripple CNT CLK DOWN Q2	27	29	20	21	14	14	ns
tpd	Delay	Ripple CNT CLK UP Q0	18	16	13	11	9	8	ns
tpd	Delay	Ripple CNT CLK UP Q1	24	24	17	17	12	12	ns
tpd	Delay	Ripple CNT CLK UP Q2	29	23	21	17	15	12	ns
tpd	Delay	Ripple CNT nSET DOWN Q0	26	33	19	23	14	16	ns
tpd	Delay	Ripple CNT nSET DOWN Q1	26	41	19	29	13	21	ns
tpd	Delay	Ripple CNT nSET DOWN Q2	25	41	18	29	13	20	ns
tpd	Delay	Ripple CNT nSET UP Q0	26	33	19	23	14	16	ns
tpd	Delay	Ripple CNT nSET UP Q1	26	38	19	27	13	19	ns
tpd	Delay	Ripple CNT nSET UP Q2	25	44	18	32	13	22	ns
tpd	Delay	DFF Q	17	17	12	12	8	8	ns
tpd	Delay	DFF nQ	18	16	13	11	9	8	ns
tpd	Delay	DFF nRESET High Q	--	20	--	14	--	10	ns
tpd	Delay	DFF nRESET High nQ	21	--	15	--	10	--	ns
tpd	Delay	DFF nRESET Low Q	--	22	--	16	--	11	ns
tpd	Delay	DFF nRESET Low nQ	23	--	17	--	12	--	ns
tpd	Delay	DFF nSET High Q	21	--	15	--	10	--	ns

Table 12: Typical Delay Estimated for Each Macrocell at T_A = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	DFF nSET High nQ	--	20	--	14	--	10	ns
tpd	Delay	DFF nSET Low Q	23	--	16	--	12	--	ns
tpd	Delay	DFF nSET Low nQ	--	22	--	16	--	11	ns
tpd	Delay	Multi-Function DFF Q	19	19	13	13	9	9	ns
tpd	Delay	Multi-Function DFF nQ	20	19	14	13	9	9	ns
tpd	Delay	Multi-Function DFF nRESET Q	--	26	--	19	--	13	ns
tpd	Delay	Multi-Function DFF nRESET nQ	26	--	19	--	13	--	ns
tpd	Delay	Multi-Function DFF nSET Q	26	--	19	--	13	--	ns
tpd	Delay	Multi-Function DFF nSET nQ	--	26	--	19	--	14	ns
tpd	Delay	DFF3, DFF12 First Q	18	18	13	13	9	9	ns
tpd	Delay	DFF3, DFF12 First nQ	19	18	14	13	9	9	ns
tpd	Delay	DFF3, DFF12 First nRESET High Q	--	22	--	15	--	11	ns
tpd	Delay	DFF3, DFF12 First nRESET High nQ	22	--	16	--	11	--	ns
tpd	Delay	DFF3, DFF12 First nRESET Low Q	--	24	--	17	--	12	ns
tpd	Delay	DFF3, DFF12 First nRESET Low nQ	25	--	18	--	12	--	ns
tpd	Delay	DFF3, DFF12 First nSET High Q	22	--	16	--	11	--	ns
tpd	Delay	DFF3, DFF12 First nSET High nQ	--	22	--	15	--	11	ns
tpd	Delay	DFF3, DFF12 First nSET Low Q	24	--	17	--	12	--	ns
tpd	Delay	DFF3, DFF12 First nSET Low nQ	--	24	--	17	--	12	ns
tpd	Delay	DFF3, DFF12 Second Q	20	21	14	15	10	10	ns
tpd	Delay	DFF3, DFF12 Second nQ	21	20	15	14	11	10	ns
tpd	Delay	DFF3, DFF12 Second nRESET High Q	--	21	--	15	--	10	ns
tpd	Delay	DFF3, DFF12 Second nRESET High nQ	22	--	16	--	11	--	ns
tpd	Delay	DFF3, DFF12 Second nRESET Low Q	--	23	--	17	--	12	ns
tpd	Delay	DFF3, DFF12 Second nRESET Low nQ	24	--	17	--	12	--	ns
tpd	Delay	DFF3, DFF12 Second nSET High Q	22	--	15	--	11	--	ns
tpd	Delay	DFF3, DFF12 Second nSET High nQ	--	21	--	15	--	10	ns
tpd	Delay	DFF3, DFF12 Second nSET Low Q	24	--	17	--	12	--	ns
tpd	Delay	DFF3, DFF12 Second nSET Low nQ	--	23	--	17	--	12	ns
tpd	Delay	PGen CLK	16	16	12	11	8	8	ns
tpd	Delay	PGen nRESET Hi-Z to 0	--	21	--	15	--	11	ns
tpd	Delay	PGen nRESET Hi-Z to 1	20	--	14	--	10	--	ns
tpd	Delay	Pipe Delay Out	23	20	16	15	11	10	ns
tpd	Delay	Pipe Delay nRESET Out	30	28	22	21	16	15	ns
tpd	Delay	Filter Q	160	140	109	98	68	65	ns
tpd	Delay	Filter nQ	141	159	99	108	66	68	ns

Table 13: Typical Propagations Delays and Pulse Widths at T_A = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
tw	Pulse Width, 1 cell	mode: (any)edge detect, edge detect output	221	163	119	ns
tw	Pulse Width, 2 cell	mode: (any)edge detect, edge detect output	438	322	234	ns
tw	Pulse Width, 3 cell	mode: (any)edge detect, edge detect output	652	480	349	ns
tw	Pulse Width, 4 cell	mode: (any)edge detect, edge detect output	869	639	464	ns
time1	Delay, 1 cell	mode: (any)edge detect, edge detect output	18	13	9	ns
time1	Delay, 2 cell	mode: (any)edge detect, edge detect output	18	13	9	ns
time1	Delay, 3 cell	mode: (any)edge detect, edge detect output	18	13	9	ns
time1	Delay, 4 cell	mode: (any)edge detect, edge detect output	18	13	9	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	240	176	128	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	455	334	243	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	672	493	358	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	888	673	473	ns

Table 14: Typical Filter Rejection Pulse Width at T_A = 25 °C

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width	< 127	< 86	< 54	ns
Inverter Filtered Pulse Width	< 109	< 77	< 52	ns

3.8 COUNTER/DELAY CHARACTERISTICS

Table 15: Typical Counter/Delay Offset at T_A = 25 °C

Parameter	OSC Freq	OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-On time	25 MHz	auto	0.14	0.14	0.14	µs
Power-On time	2.048 MHz	auto	0.5	0.5	0.4	µs
Power-On time	2.048 kHz	auto	628	544	466	µs
frequency settling time	25 MHz	auto	4	4	8	µs
frequency settling time	2.048 MHz	auto	0.3	0.4	0.4	µs
frequency settling time	2.048 kHz	auto	660	570	480	µs
variable (CLK period)	25 MHz	forced	0-40	0-40	0-40	ns
variable (CLK period)	2.048 MHz	forced	0-0.5	0-0.5	0-0.5	µs
variable (CLK period)	2.048 kHz	forced	0-488	0-488	0-488	µs
tpd (non-delayed edge)	25 MHz/ 2.048 kHz	either	35	14	10	ns

3.9 OSCILLATOR CHARACTERISTICS

Table 16: Oscillators Frequency Limits, V_{DD} = 2.3 V to 5.5 V

OSC	Temperature Range					
	+25 °C			-40 °C to +105 °C		
	Minimum Value, kHz	Maximum Value, kHz	Error, %	Minimum Value, kHz	Maximum Value, kHz	Error, %
2.048 kHz OSC0	2.0150	2.0685	+1.00	1.7799	2.1085	+2.95
			-1.61			-13.09
2.048 MHz OSC1	2019.42	2068.48	+1.00	1947.519	2080.775	+1.60
			-1.40			-4.91
25 MHz OSC2	24623	25250	+1.00	23655	25369	+1.48
			-1.51			-5.38

3.9.1 OSC Power-On Delay

Table 17: Oscillators Power-On Delay at T_A = -40 °C to +105 °C, OSC Power Setting: "Auto Power-On"

Power Supply Range (V_{DD}) V	OSC0 2.048 kHz		OSC1 2.048 MHz		OSC2 25 MHz		OSC2 25 MHz Start with Delay	
	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns	Typical Value, ns	Maximum Value, ns	Typical Value, ns	Maximum Value, ns
2.30	698.2	1063.8	527.6	562.7	44.9	61.2	144.5	166.0
2.50	663.6	993.6	505.5	542.8	39.7	53.9	142.5	164.9
3.00	601.9	866.9	471.0	510.7	31.2	42.1	140.3	164.8
3.30	576.1	812.0	457.7	498.1	28.0	37.8	139.8	165.4
3.60	555.7	768.3	447.3	487.7	25.5	34.6	139.6	166.2
4.00	533.8	721.1	436.0	475.7	23.1	31.8	139.6	167.2
5.00	492.0	637.1	415.6	454.1	19.2	26.9	139.9	170.1
5.50	468.7	598.1	408.3	446.4	18.0	26.2	139.9	171.3

3.10 ACMP CHARACTERISTICS

Table 18: ACMP Specifications at T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input		0	--	V_{DD}	V
		Negative Input		0	--	V_{DD}	V
V_{offset}	ACMP Input Offset	ACMPxH V_{HYS} = 0 mV, Gain = 1, Vref = 32 mV to 2016 mV		-6.4	--	6.4	mV
		ACMPxL V_{HYS} = 0 mV, Gain = 1, Vref = 32 mV to 2016 mV		-4.6	--	5.3	mV

Table 18: ACMP Specifications at T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
t_{start}	ACMP Startup Time	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxH		--	--	37	µs
		ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxL		--	--	294	µs
V_{HYS}	ACMP0H, ACMP1H Built-in Hysteresis **(Note 1)**	V_{HYS} = 32 mV	T = 25 °C	23.33	--	36.59	mV
		V_{HYS} = 64 mV	T = 25 °C	55.78	--	68.38	mV
		V_{HYS} = 192 mV	T = 25 °C	183.67	--	197.36	mV
		V_{HYS} = 32 mV		22.03	--	37.25	mV
		V_{HYS} = 64 mV		54.12	--	68.99	mV
		V_{HYS} = 192 mV		182.73	--	197.57	mV
	ACMP2L, ACMP3L Built-in Hysteresis **(Note 1)**	V_{HYS} = 32 mV	T = 25 °C	26.96	--	36.84	mV
		V_{HYS} = 64 mV	T = 25 °C	58.44	--	69.25	mV
		V_{HYS} = 192 mV	T = 25 °C	186.18	--	198.18	mV
		V_{HYS} = 32 mV		25.01	--	36.82	mV
		V_{HYS} = 64 mV		57.87	--	69.19	mV
		V_{HYS} = 192 mV		184.78	--	198.36	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	10	--	GΩ
		Gain = 0.5x		--	2	--	MΩ
		Gain = 0.33x		--	2	--	MΩ
		Gain = 0.25x		--	2	--	MΩ

Table 18: ACMP Specifications at T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
PROP	Propagation Delay, Response Time for ACMP0H, ACMP1H	Gain = 1, Vref = 32 mV to 2016 mV, Overdrive =10 mV	Low to High	--	1.85	13.55	μs
			High to Low	--	2.48	10.04	μs
		Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 100 mV	Low to High	--	0.54	2.03	μs
			High to Low	--	0.53	0.97	μs
		Gain = 1, T = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	1.46	--	μs
			High to Low	--	1.75	--	μs
		Gain = 1, T = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	0.55	--	μs
			High to Low	--	0.53	--	μs
	Propagation Delay, Response Time for ACMP2L, ACMP3L	Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 10 mV	Low to High	--	56.65	128.40	μs
			High to Low	--	63.01	141.48	μs
		Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 100 mV	Low to High	--	19.73	60.49	μs
			High to Low	--	19.33	60.93	μs
		Gain = 1, T = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	68.15	--	μs
			High to Low	--	66.31	--	μs
		Gain = 1, T = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	27.54	--	μs
			High to Low	--	27.01	--	μs
G	Gain error	G = 1, Vref = 32 mV		1	1	1	
		G = 0.5, Vref = 32 mV		0.484	0.502	0.526	
		G = 0.33, Vref = 32 mV		0.324	0.338	0.358	
		G = 0.25, Vref = 32 mV		0.238	0.250	0.263	
		G = 1, Vref = 480 mV		1	1	1	
		G = 0.5, Vref = 480 mV		0.497	0.501	0.504	
		G = 0.33, Vref = 480 mV		0.330	0.333	0.337	
		G = 0.25, Vref = 480 mV		0.248	0.250	0.253	
Vref	Internal Vref0 error Vref0 = 32 mV to 2016 mV, Buffer disabled	V_{DD} = 4.0 V	T = 25 °C	-0.85	--	4.95	%
	Internal Vref0 error Vref0 = 320 mV to 2016 mV, Buffer enabled		T = 25 °C I_{LOAD} = 1 μA	-7.96	--	2.39	%
			I_{LOAD} = 1 μA	-8.66	--	2.39	%
	Internal Vref1 error Vref1 = 32 mV to 2016 mV, Buffer disabled	V_{DD} = 4.0 V	T = 25 °C	-1.79	--	5.03	%
	Internal Vref1 error Vref1 = 320 mV to 2016 mV, Buffer enabled		T = 25 °C I_{LOAD} = 1 μA	-6.04	--	2.33	%
			I_{LOAD} = 1 μA	-6.79	--	2.51	%

Table 18: ACMP Specifications at T_A = -40 °C to +105 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted(Continued)

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
Is	Input Current Source		Vin = V_{DD} - 0.7 V, V_{DD} = 2.3 V	23.3	94.1	117.7	µA
			Vin = V_{DD} - 0.7 V, V_{DD} = 2.5 V	78.4	94.9	111.4	µA
			Vin = V_{DD} - 0.7 V, V_{DD} = 3.3 V	78.2	95.3	111.8	µA
			Vin = V_{DD} - 0.7 V, V_{DD} = 4.0 V	78.2	95.4	112.0	µA
			Vin = V_{DD} - 0.7 V, V_{DD} = 5.0 V	79.4	96.5	112.9	µA
			Vin = V_{DD} - 0.7 V, V_{DD} =5.5 V	81.7	98.7	116.4	µA

Note 1 V_{IL} = Vin - V_{HYS}, V_{IH} = Vin.

3.11 ANALOG TEMPERATURE SENSOR CHARACTERISTICS

Temperature Sensor typical nonlinearity ± 0.72 % for output range 1 and ± 0.42 % for output range 2 at V_{DD} = 2.3 V to 5.5 V.

Table 19: TS Output vs Temperature (Output Range 1), V_{DD} = 2.3 V to 5.5 V

T, °C	Buffer Enabled			Buffer Disabled		
	Min, mV	Typ, mV	Max, mV	Min, mV	Typ, mV	Max, mV
-40	992	997	1004	992	997	1005
-20	947	952	960	947	952	960
0	902	907	914	902	907	914
20	856	861	868	856	861	868
25	844	849	856	844	849	856
40	809	814	821	808	814	821
60	761	767	775	761	766	775
80	713	719	727	713	719	727
100	664	670	679	664	670	679
105	652	658	667	652	658	667

Table 20: TS Output vs Temperature (Output Range 2), V_{DD} = 2.3 V to 5.5 V

T, °C	Buffer Enabled			Buffer Disabled		
	Min, mV	Typ, mV	Max, mV	Min, mV	Typ, mV	Max, mV
-40	1192	1204	1212	1193	1204	1213
-20	1143	1150	1158	1143	1150	1158
0	1088	1095	1103	1088	1095	1103
20	1033	1040	1048	1033	1040	1048
25	1019	1025	1034	1019	1025	1034
40	976	983	992	976	983	991
60	919	926	935	919	926	935
80	861	868	878	861	868	878
100	802	810	820	802	810	820
105	788	795	806	787	795	806

Table 21: TS Output Error (Output Range 1), V_{DD} = 2.3 V to 5.5 V

T, °C	Buffer Enabled		Buffer Disabled	
	Min, %	Max, %	Min, %	Max, %
-40	-0.56	0.70	-0.57	0.73
-20	-0.56	0.75	-0.56	0.76
0	-0.58	0.78	-0.58	0.78
20	-0.59	0.81	-0.59	0.80
25	-0.61	0.84	-0.61	0.84
40	-0.64	0.92	-0.65	0.92
60	-0.72	1.03	-0.73	1.06
80	-0.79	1.15	-0.79	1.17
100	-0.89	1.33	-0.90	1.33
105	-0.91	1.40	-0.91	1.35

Table 22: TS Output Error (Output Range 2), V_{DD} = 2.3 V to 5.5 V

T, °C	Buffer Enabled		Buffer Disabled	
	Min, %	Max, %	Min, %	Max, %
-40	-0.99	0.70	-0.96	0.71
-20	-0.58	0.72	-0.59	0.72
0	-0.60	0.76	-0.60	0.74
20	-0.63	0.78	-0.63	0.77
25	-0.64	0.80	-0.64	0.81
40	-0.67	0.89	-0.67	0.90
60	-0.73	1.00	-0.73	0.99
80	-0.82	1.12	-0.82	1.12
100	-0.93	1.28	-0.93	1.28
105	-0.97	1.31	-0.97	1.32

4 User Programmability

The SLG46855-A is a user programmable device with one time programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

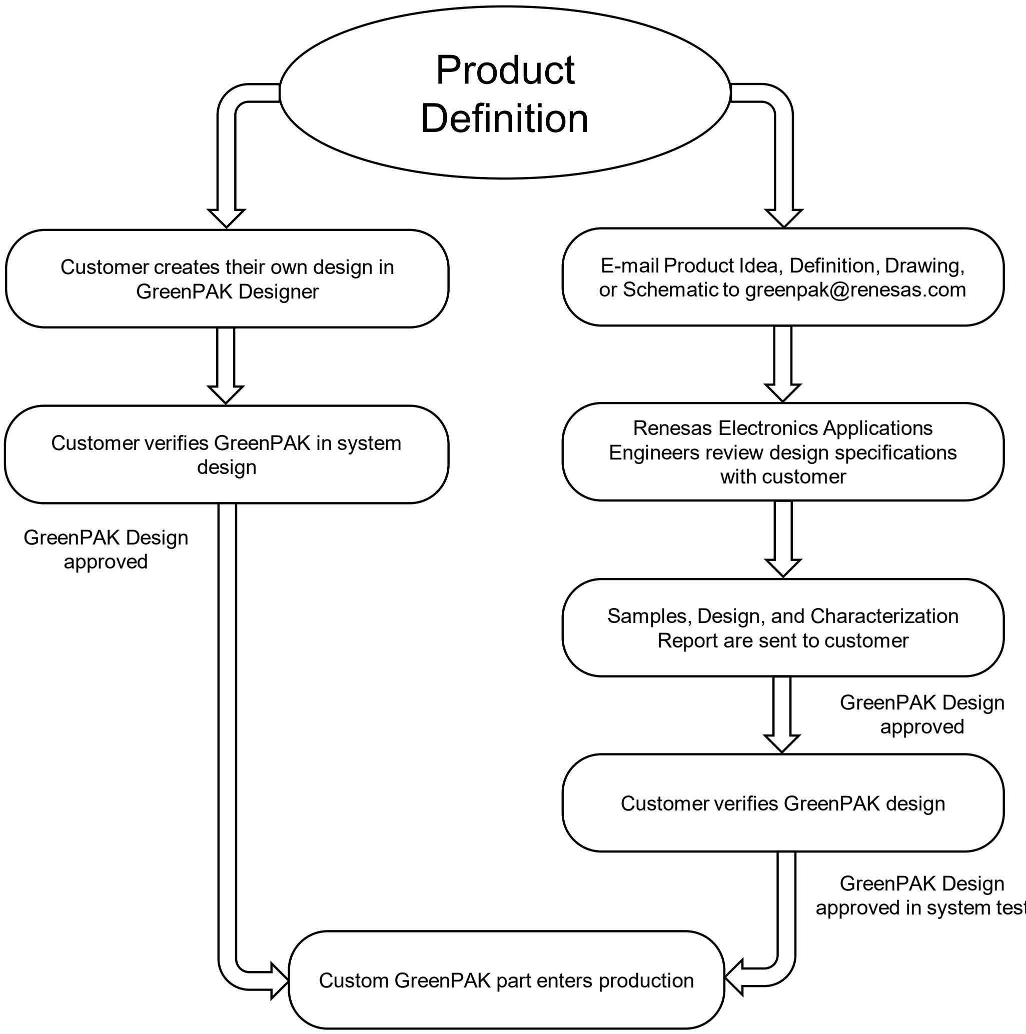


Figure 2: Steps to Create a Custom GreenPAK Device

5 IO Pins

The SLG46855-A has a total of 10 GPIO, 1 GPI, and 1 GPO Pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference).

5.1 GPIO PINS

GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8 and GPIO9 serve as General Purpose IO Pins.

5.2 GPI PINS

GPI0 serves as a General Purpose Input Pin.

5.3 GPO PINS

GPO0 serves as a General Purpose Output Pin.

5.4 PULL-UP/DOWN RESISTORS

All IO Pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as either Pull-up or Pull-downs.

5.5 FAST PULL-UP/DOWN DURING POWER-UP

During power-up, IO Pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to normal setting value. This function is enabled by register [778].

5.6 GPI STRUCTURE

5.6.1 GPI Structure (for GPI0)

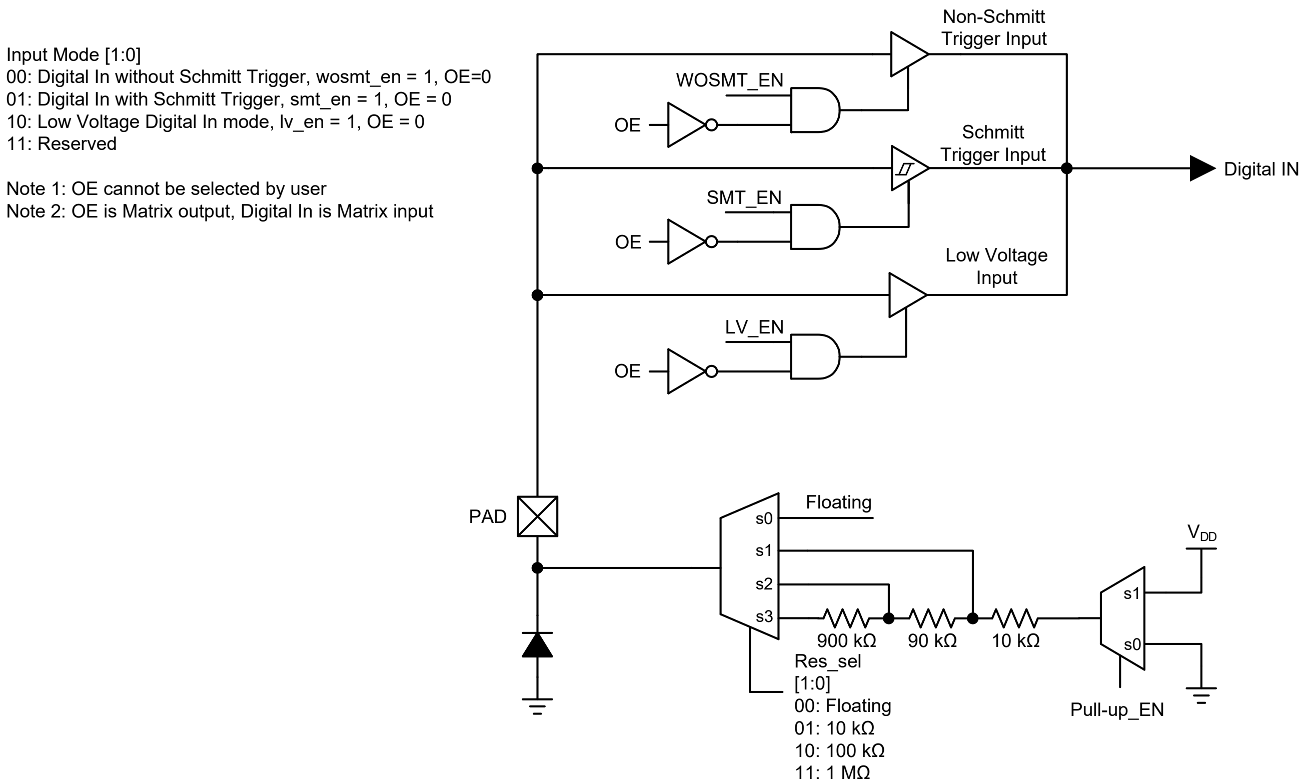


Figure 3: IO0 GPI Structure Diagram

5.7 GPIO WITH I²C MODE IO STRUCTURE

5.7.1 GPIO with I²C Mode Structure (for GPIO0 and GPIO1)

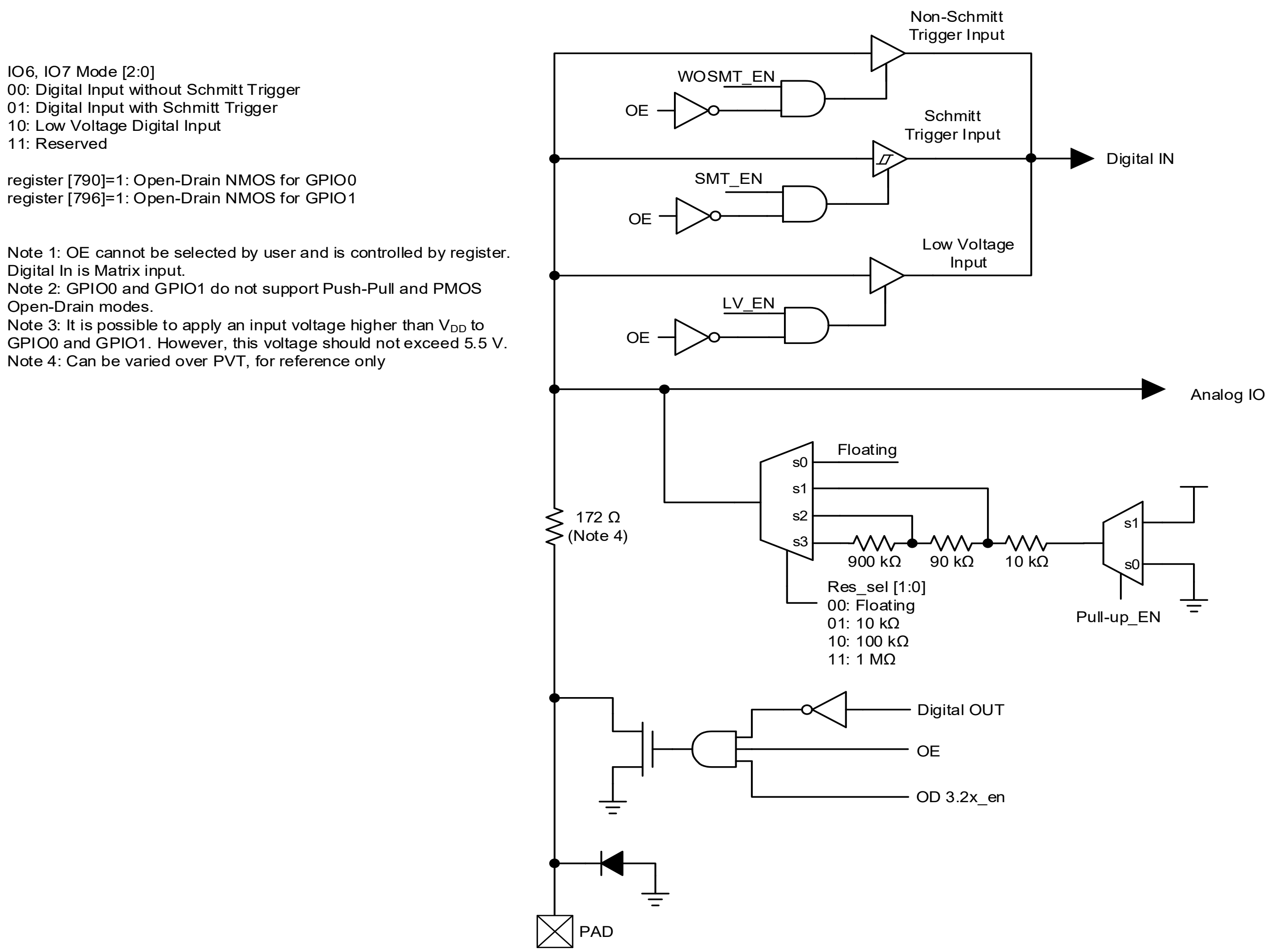


Figure 4: GPIO with I²C Mode IO Structure Diagram

5.8 MATRIX OE IO STRUCTURE

5.8.1 Matrix OE IO Structure (for GPIO2, GPIO3, GPIO5, GPIO6. GPIO7, GPIO8, and GPIO9)

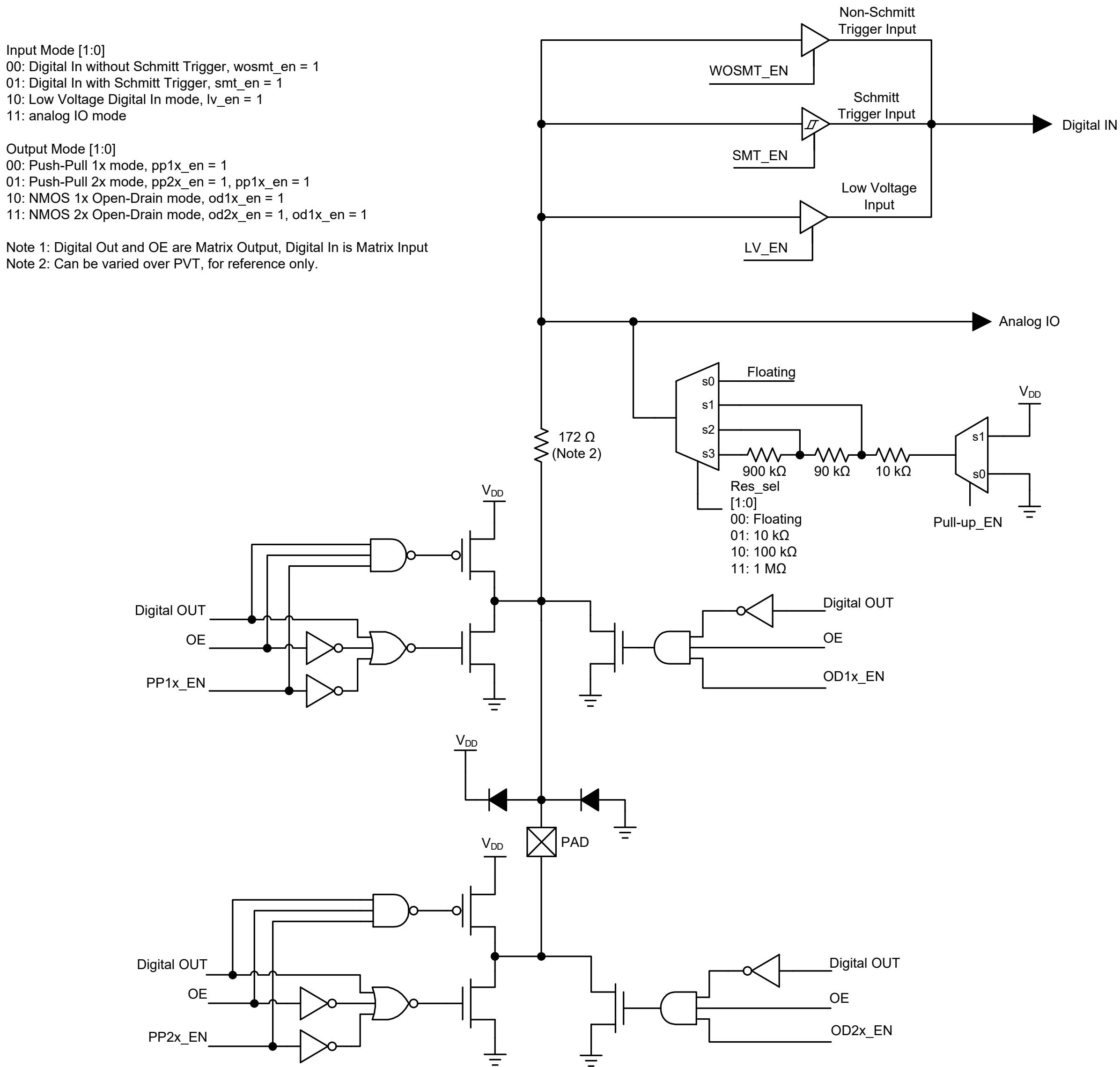


Figure 5: Matrix OE IO Structure Diagram

5.8.2 Matrix OE 4x Drive Structure (for GPIO4)

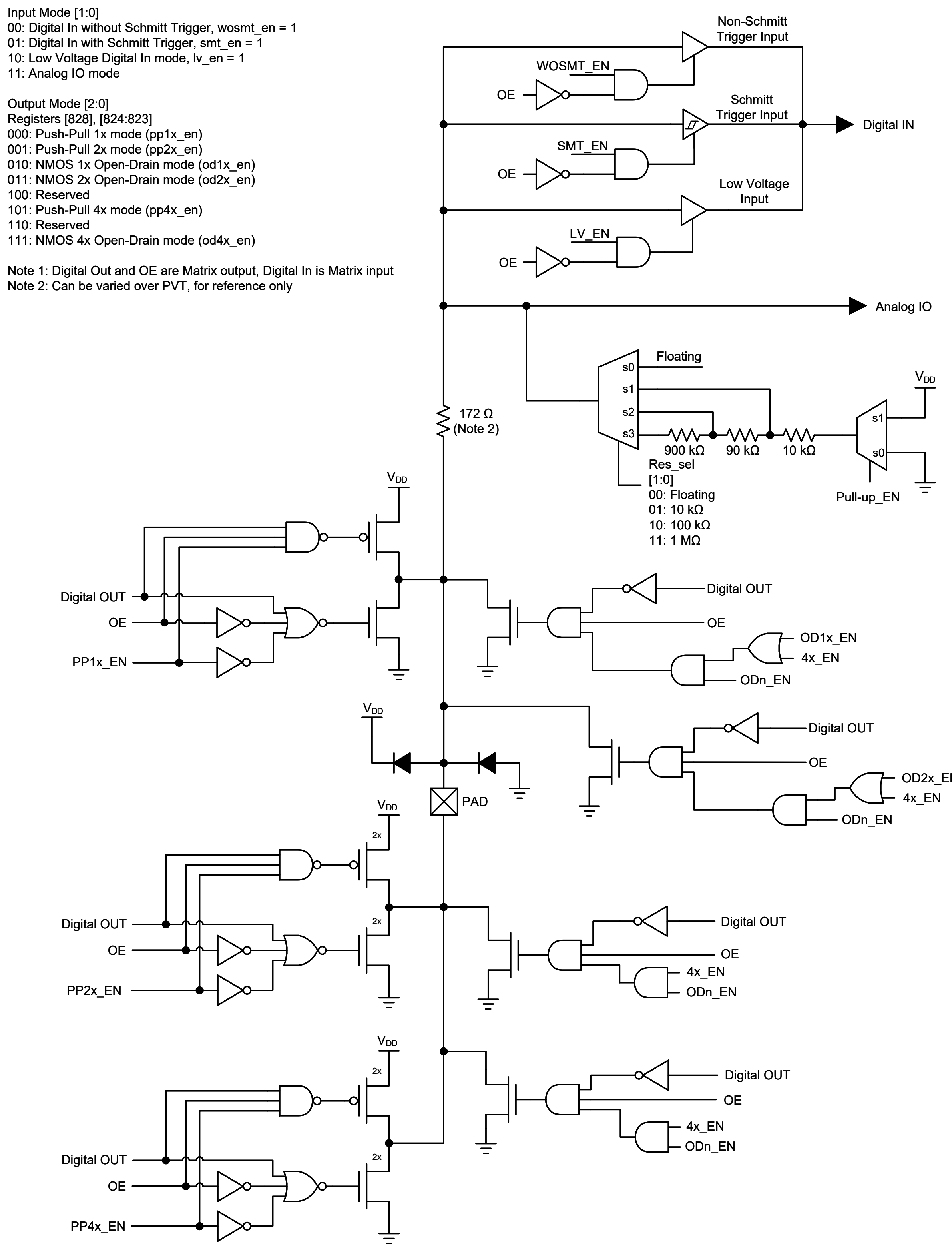


Figure 6: Matrix OE IO 4x Drive Structure Diagram

5.9 GPO STRUCTURE

5.9.1 GPO Register OE Structure (for GPO0)

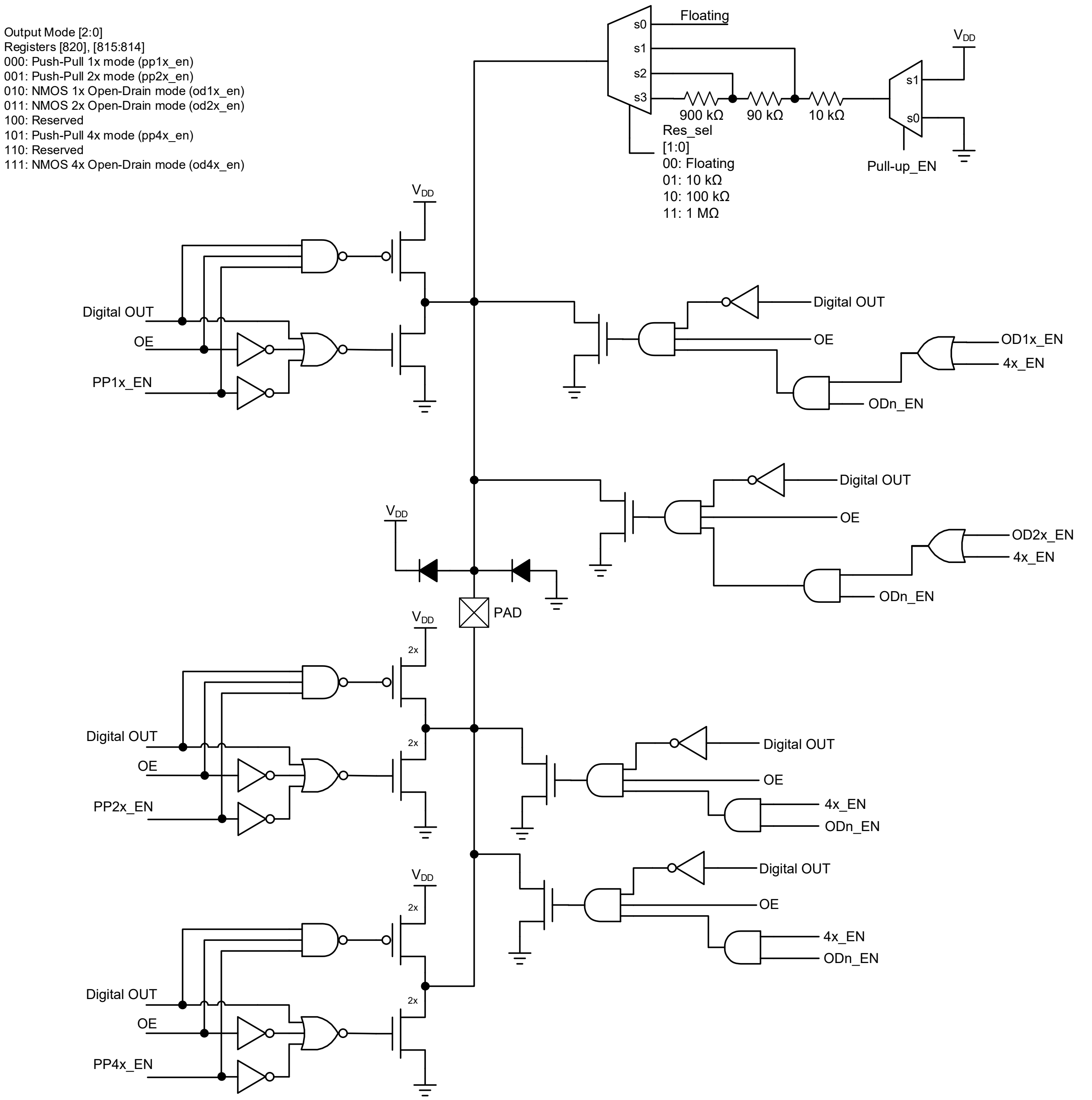


Figure 7: GPO Register OE 4x Drive Structure Diagram

5.10 IO TYPICAL PERFORMANCE

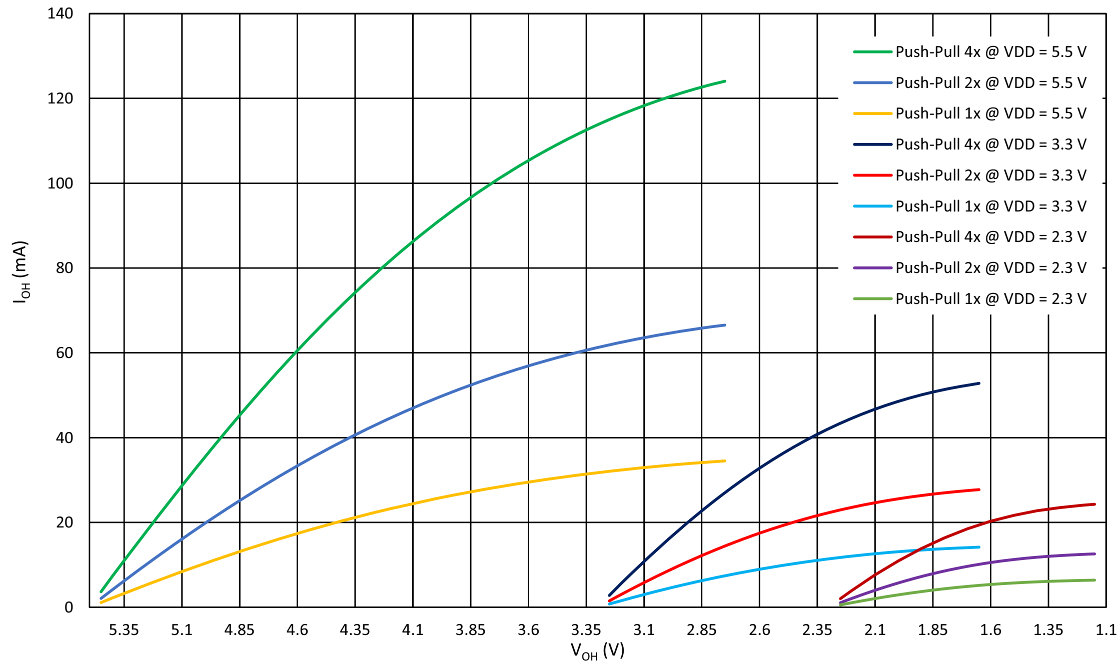


Figure 8: Typical High Level Output Current vs. High Level Output Voltage at T = 25 °C

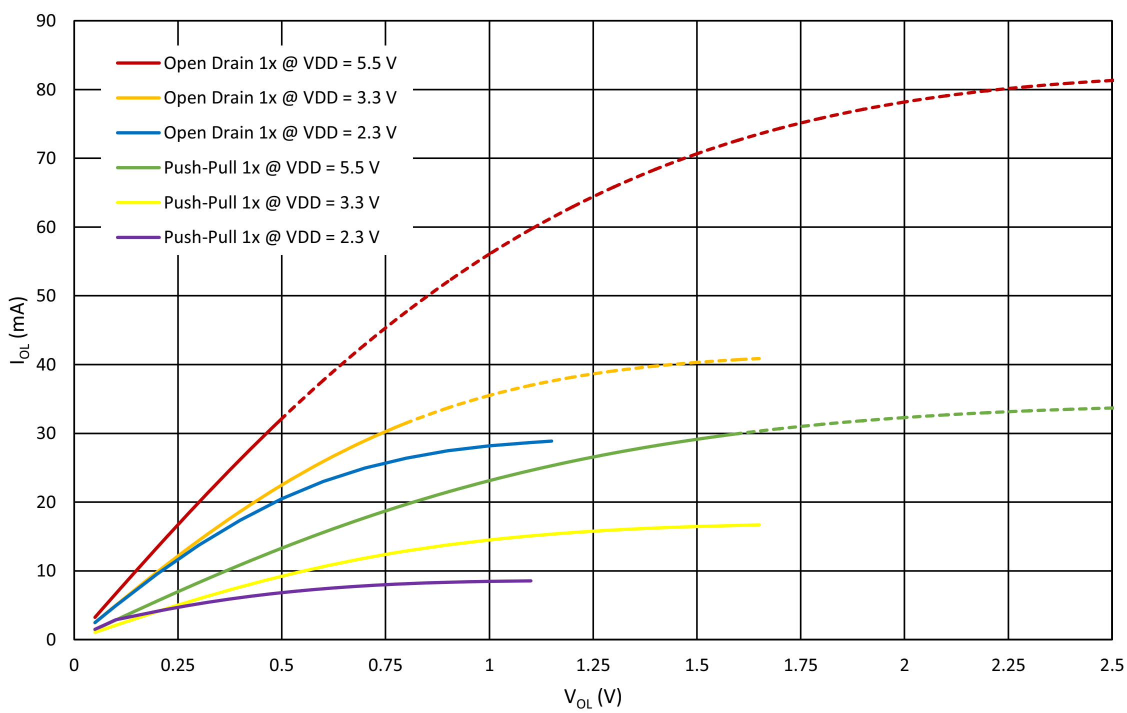


Figure 9: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C, Full Range

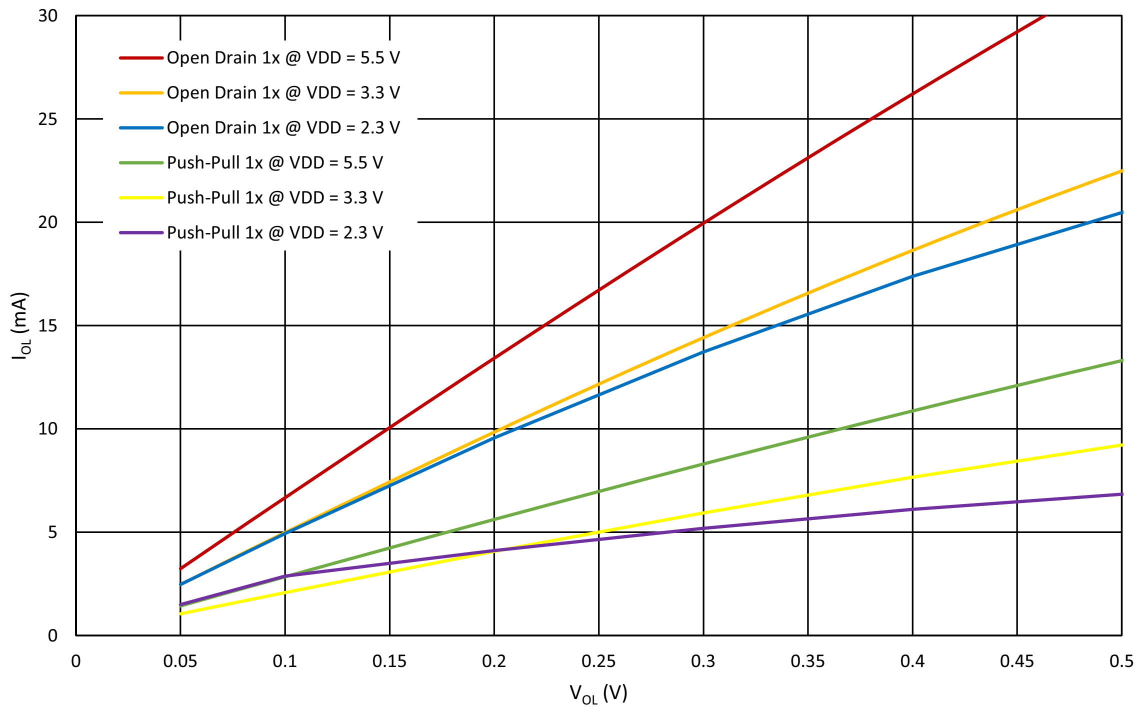


Figure 10: Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T = 25 °C

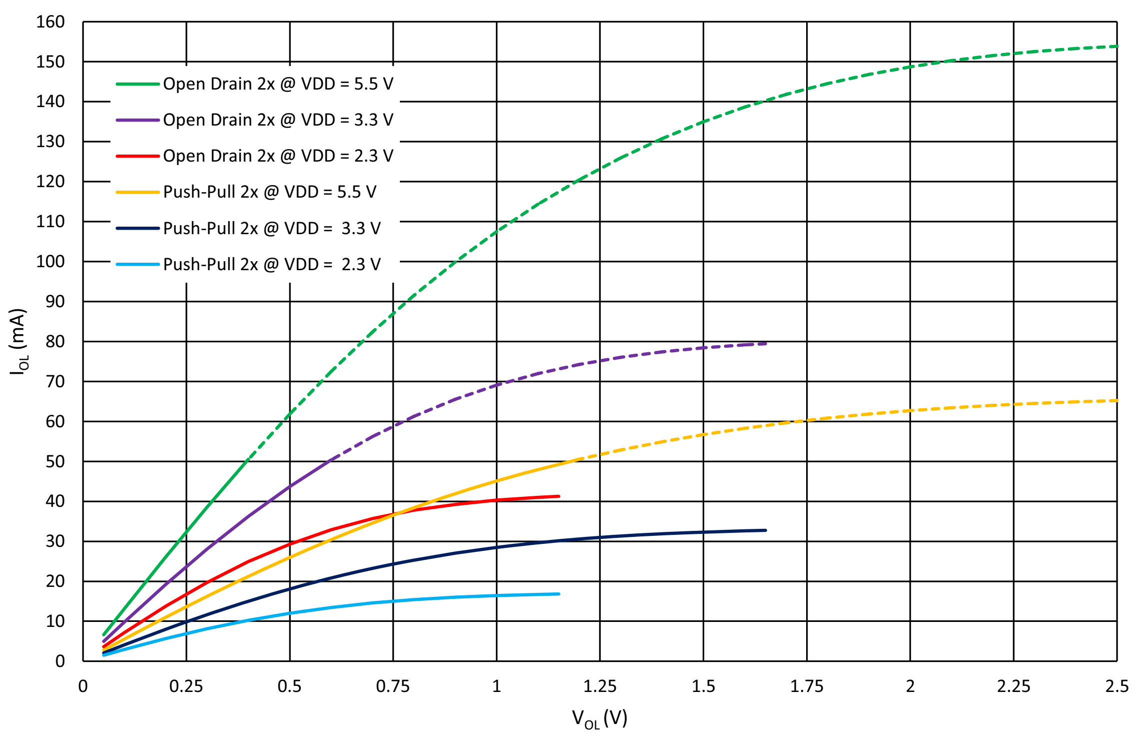


Figure 11: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C, Full Range

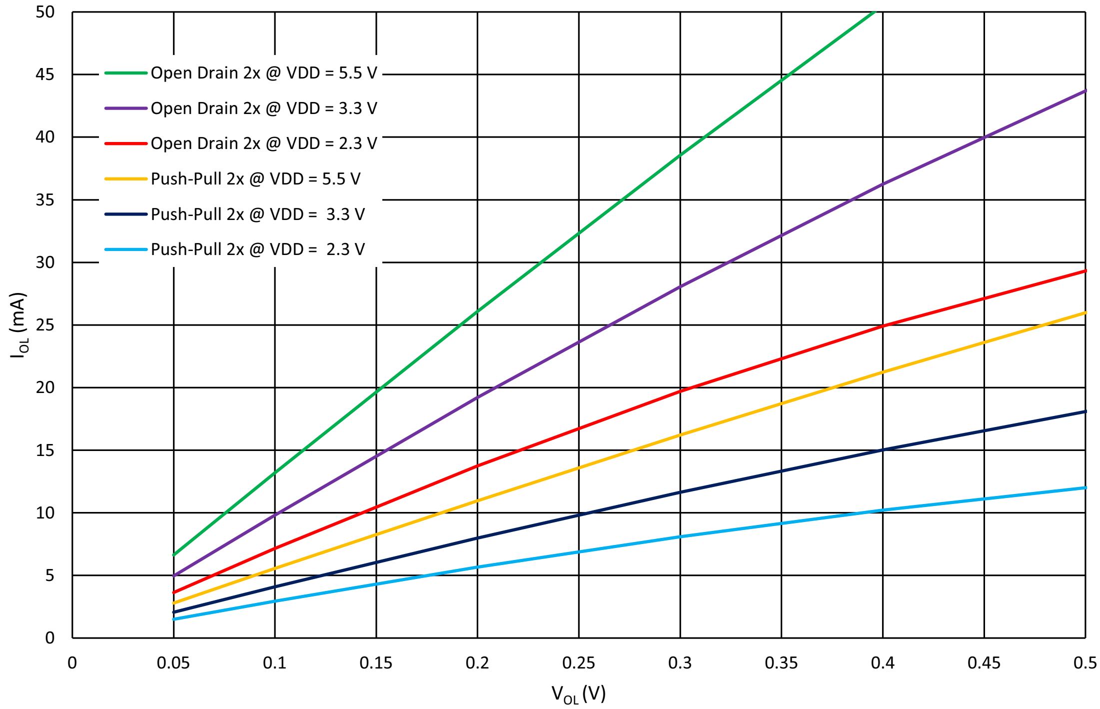


Figure 12: Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T = 25 °C

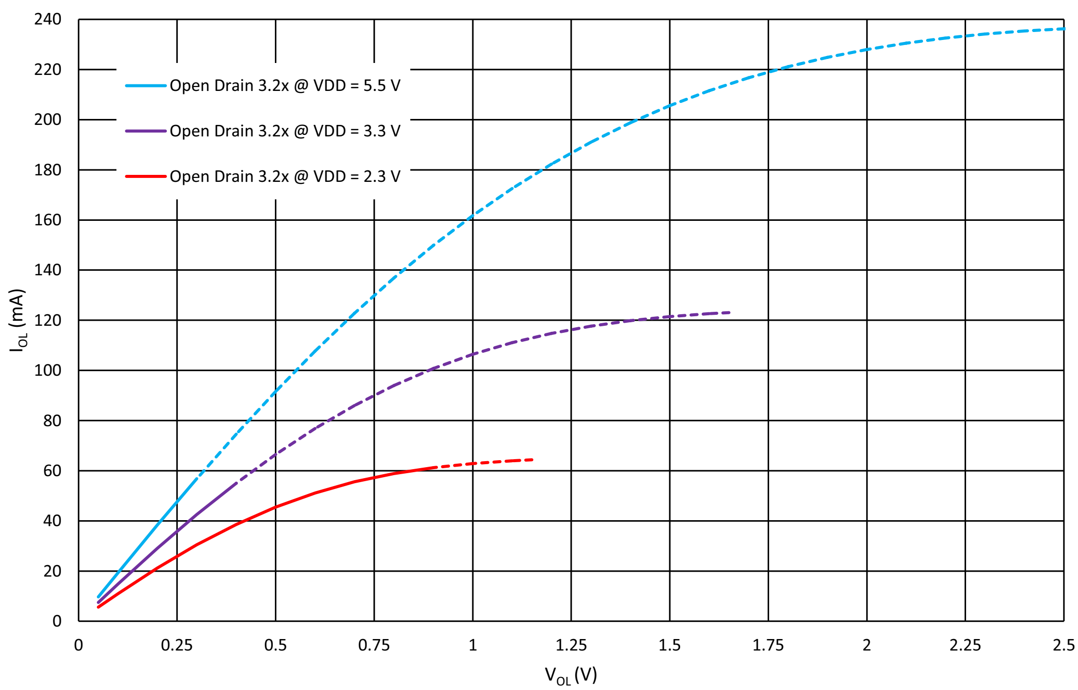


Figure 13: Typical Low Level Output Current vs. Low Level Output Voltage, 3.2x Drive at T = 25 °C, Full Range

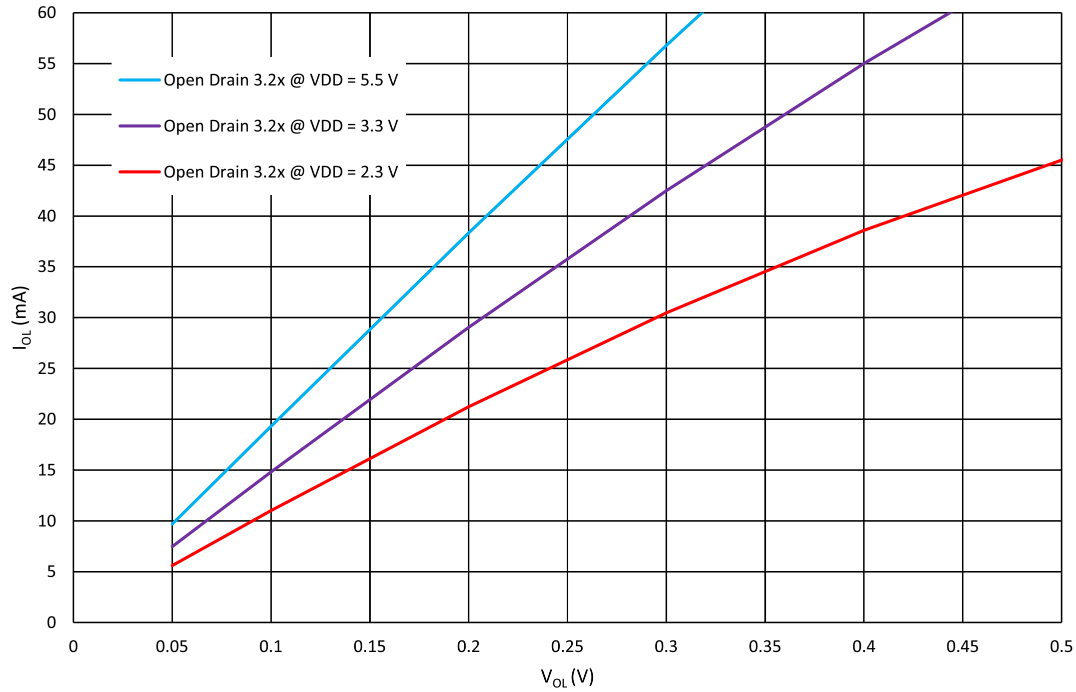


Figure 14: Typical Low Level Output Current vs. Low Level Output Voltage, 3.2x Drive at T = 25 °C

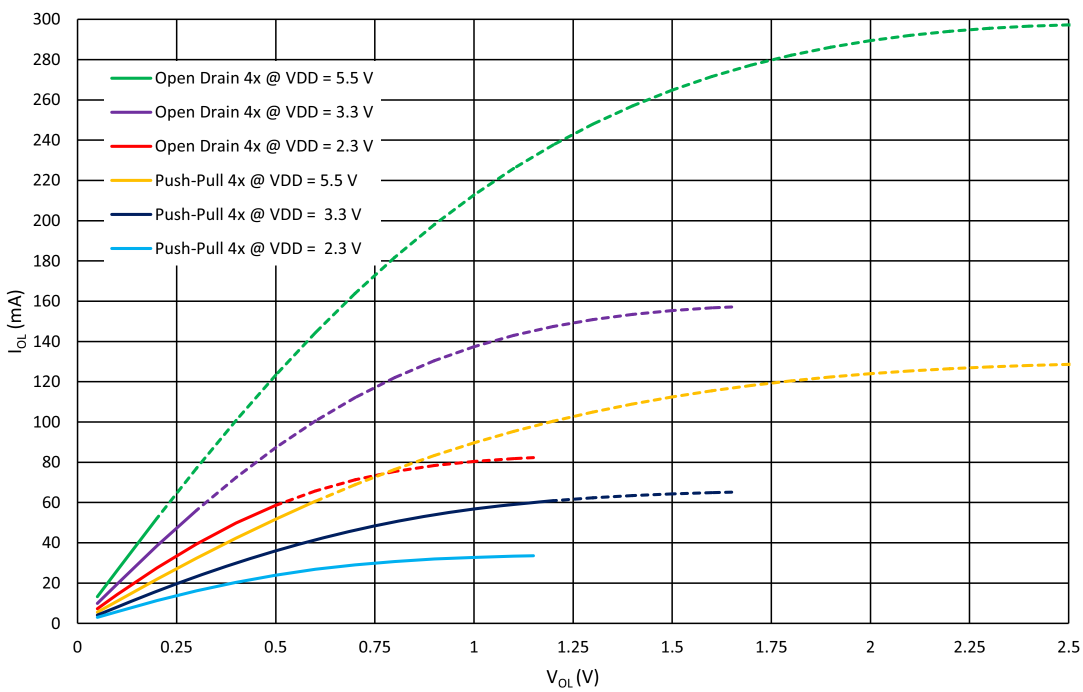


Figure 15: Typical Low Level Output Current vs. Low Level Output Voltage, 4x Drive at T = 25 °C, Full Range

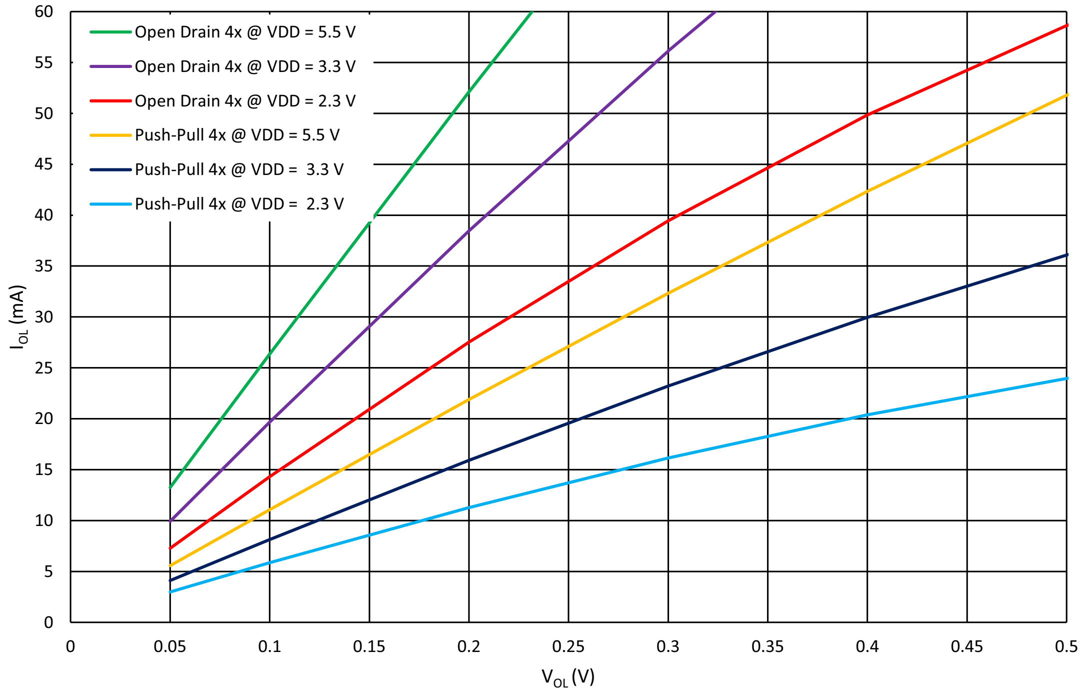


Figure 16: Typical Low Level Output Current vs. Low Level Output Voltage, 4x Drive at T = 25 °C

6 Connection Matrix

The Connection Matrix in the SLG46855-A is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one time programmable (OTP) NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46855-A has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low”, based on the design that is created. Once the 2048 register bits within the SLG46855-A are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 96 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46855-A’s register table, see Section 17.

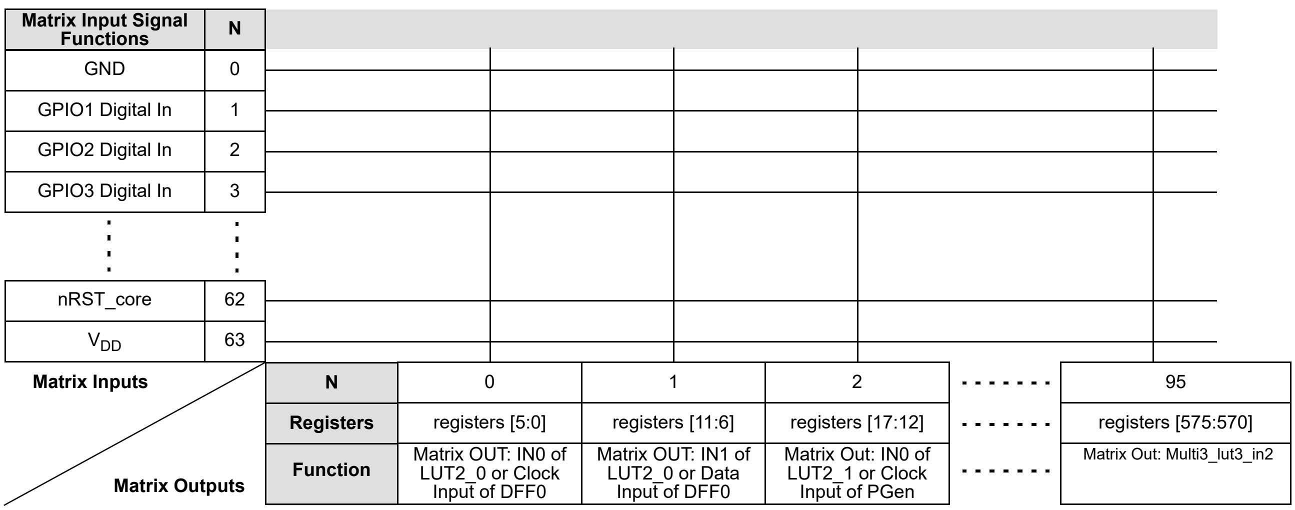


Figure 17: Connection Matrix

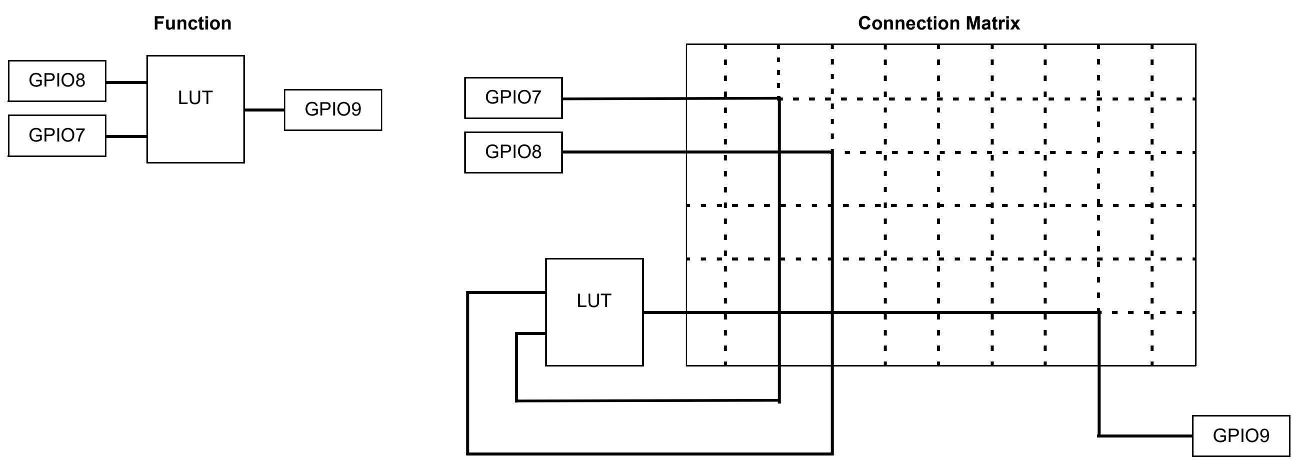


Figure 18: Connection Matrix Example

6.1 MATRIX INPUT TABLE

Table 23: Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	LUT2_0/DFF0 output	0	0	0	0	0	1
2	LUT2_1/DFF1 output	0	0	0	0	1	0
3	LUT2_2/DFF2 output	0	0	0	0	1	1
4	LUT2_3/PGen output	0	0	0	1	0	0
5	LUT3_0/DFF3 output	0	0	0	1	0	1
6	LUT3_1/DFF4 output	0	0	0	1	1	0
7	LUT3_2/DFF5 output	0	0	0	1	1	1
8	LUT3_3/DFF6 output	0	0	1	0	0	0
9	LUT3_4/DFF7 output	0	0	1	0	0	1
10	LUT3_5/DFF8 output	0	0	1	0	1	0
11	LUT3_6/DFF9 output	0	0	1	0	1	1
12	LUT3_7/DFF10 output	0	0	1	1	0	0
13	LUT3_8/DFF11 output	0	0	1	1	0	1
14	CNT0 output	0	0	1	1	1	0
15	MF0_LUT4/DFF_OUT	0	0	1	1	1	1
16	CNT1 output	0	1	0	0	0	0
17	MF1_LUT3/DFF_OUT	0	1	0	0	0	1
18	CNT2 output	0	1	0	0	1	0
19	MF2_LUT3/DFF_OUT	0	1	0	0	1	1
20	CNT3 output	0	1	0	1	0	0
21	MF3_LUT3/DFF_OUT	0	1	0	1	0	1
22	CNT4 output	0	1	0	1	1	0
23	MF4_LUT3/DFF_OUT	0	1	0	1	1	1
24	CNT5 output	0	1	1	0	0	0
25	MF5_LUT3/DFF_OUT	0	1	1	0	0	1
26	CNT6 output	0	1	1	0	1	0
27	MF6_LUT3/DFF_OUT	0	1	1	0	1	1
28	CNT7 output	0	1	1	1	0	0
29	MF7_LUT3/DFF_OUT	0	1	1	1	0	1
30	LUT3_16/Ripple CNT/Pipe Delay_out0	0	1	1	1	1	0
31	Ripple CNT/Pipe Delay_out1	0	1	1	1	1	1
32	GPIO0 digital input or I^2C_virtual_0 Input	1	0	0	0	0	0
33	GPIO1 digital input or I^2C_virtual_1 Input	1	0	0	0	0	1
34	I^2C_virtual_2 Input	1	0	0	0	1	0
35	I^2C_virtual_3 Input	1	0	0	0	1	1
36	I^2C_virtual_4 Input	1	0	0	1	0	0
37	I^2C_virtual_5 Input	1	0	0	1	0	1

Table 23: Matrix Input Table(Continued)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
38	I²C_virtual_6 Input	1	0	0	1	1	0
39	I²C_virtual_7 Input	1	0	0	1	1	1
40	Ripple CNT_out2	1	0	1	0	0	0
41	LUT4_0/DFF12 output	1	0	1	0	0	1
42	Programmable Delay Edge Detect Output	1	0	1	0	1	0
43	Edge Detect Filter Output	1	0	1	0	1	1
44	GPI0 Digital Input	1	0	1	1	0	0
45	GPIO2 Digital Input	1	0	1	1	0	1
46	GPIO3,Digital Input	1	0	1	1	1	0
47	GPIO4 Digital Input	1	0	1	1	1	1
48	GPIO5 Digital Input	1	1	0	0	0	0
49	GPIO6 Digital Input	1	1	0	0	0	1
50	GPIO7 Digital Input	1	1	0	0	1	0
51	GPIO8 Digital Input	1	1	0	0	1	1
52	GPIO9, Digital Input	1	1	0	1	0	0
53	Oscillator0 output 0	1	1	0	1	0	1
54	Oscillator1 output 0	1	1	0	1	1	0
55	Oscillator2 output	1	1	0	1	1	1
56	ACMP0 Output (normal speed)	1	1	1	0	0	0
57	ACMP1 Output (normal speed)	1	1	1	0	0	1
58	ACMP2 Output (low speed)	1	1	1	0	1	0
59	ACMP3 output (low speed)	1	1	1	0	1	1
60	Oscillator0 output 1	1	1	1	1	0	0
61	Oscillator1 output 1	1	1	1	1	0	1
62	POR OUT	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.2 MATRIX OUTPUT TABLE

Table 24: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[5:0]	IN0 of LUT2_0 or Clock Input of DFF0	0
[11:6]	IN1 of LUT2_0 or Data Input of DFF0	1
[17:12]	IN0 of LUT2_1 or Clock Input of DFF1	2
[23:18]	IN1 of LUT2_1 or Data Input of DFF1	3
[29:24]	IN0 of LUT2_2 or Clock Input of DFF2	4
[35:30]	IN1 of LUT2_2 or Data Input of DFF2	5
[41:36]	IN0 of LUT2_3 or Clock Input of PGen	6
[47:42]	IN1 of LUT2_3 or nRST of PGen	7
[53:48]	IN0 of LUT3_0 or CLK Input of DFF3	8
[59:54]	IN1 of LUT3_0 or Data of DFF3	9
[65:60]	IN2 of LUT3_0 or nRST (nSET) of DFF3	10
[71:66]	IN0 of LUT3_1 or CLK Input of DFF4	11
[77:72]	IN1 of LUT3_1 or Data of DFF4	12
[83:78]	IN2 of LUT3_1 or nRST (nSET) of DFF4	13
[89:84]	IN0 of LUT3_2 or CLK Input of DFF5	14
[95:90]	IN1 of LUT3_2 or Data of DFF5	15
[101:96]	IN2 of LUT3_2 or nRST (nSET) of DFF5	16
[107:102]	IN0 of LUT3_3 or CLK Input of DFF6	17
[113:108]	IN1 of LUT3_3 or Data of DFF6	18
[119:114]	IN2 of LUT3_3 or nRST (nSET) of DFF6	19
[125:120]	IN0 of LUT3_4 or CLK Input of DFF7	20
[131:126]	IN1 of LUT3_4 or Data of DFF7	21
[137:132]	IN2 of LUT3_4 or Data of DFF7	22
[143:138]	IN0 of LUT3_5 or CLK Input of DFF8	23
[149:144]	IN1 of LUT3_5 or Data of DFF8	24
[155:150]	IN2 of LUT3_5 or nRST (nSET) of DFF8	25
[161:156]	IN0 of LUT3_6 or CLK Input of DFF9	26
[167:162]	IN1 of LUT3_6 or Data of DFF9	27
[173:168]	IN2 of LUT3_6 or nRST (nSET) of DFF9	28
[179:174]	IN0 of LUT3_7 or CLK Input of DFF10	29
[185:180]	IN1 of LUT3_7 or Data of DFF10	30
[191:186]	IN2 of LUT3_7 or nRST (nSET) of DFF10	31
[197:192]	IN0 of LUT3_8 or CLK Input of DFF11	32
[203:198]	IN1 of LUT3_8 or CLK Input of DFF11	33
[209:204	IN2 of LUT3_8 or nRST (nSET) of DFF11	34
[215:210]	IN0 of LUT3_12 or CLK Input of DFF16 Delay4 Input (or Counter4 nRST Input)	35
[221:216]	IN1 of LUT3_12 or nRST (nSET) of DFF16 Delay4 Input (or Counter4 nRST Input)	36

Table 24: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[227:222]	IN2 of LUT3_12 or Data of DFF16 Delay4 Input (or Counter4 nRST Input)	37
[233:228]	IN0 of LUT3_13 or CLK Input of DFF17 Delay5 Input (or Counter5 nRST Input)	38
[239:234]	IN1 of LUT3_13 or nRST (nSET) of DFF17 Delay5 Input (or Counter5 nRST Input)	39
[245:240]	IN2 of LUT3_13 or Data of DFF17 Delay5 Input (or Counter5 nRST Input)	40
[251:246]	IN0 of LUT3_14 or CLK Input of DFF18 Delay6 Input (or Counter6 nRST Input)	41
[257:252]	IN1 of LUT3_14 or nRST (nSET) of DFF18 Delay6 Input (or Counter6 nRST Input)	42
[263:258]	IN2 of LUT3_14 or Data of DFF18 Delay6 Input (or Counter6 nRST Input)	43
[269:264]	IN0 of LUT3_15 or CLK Input of DFF19 Delay7 Input (or Counter7 nRST Input)	44
[275:270]	IN1 of LUT3_15 or nRST (nSET) of DFF19 Delay7 Input (or Counter7 nRST Input)	45
[281:276]	IN2 of LUT3_15 or Data of DFF19 Delay7 Input (or Counter7 nRST Input)	46
[287:282]	IN0 of LUT3_16 or Input of Pipe Delay or UP signal of RIPP CNT	47
[293:288]	IN1 of LUT3_16 or nRST of Pipe Delay or nSET of RIPP CNT	48
[299:294]	IN2 of LUT3_16 or Clock of Pipe Delay_RIPP CNT	49
[305:300]	IN0 of LUT4_0 or CLK Input of DFF12	50
[311:306]	IN1 of LUT4_0 or Data of DFF12	51
[317:312]	IN2 of LUT4_0 or nRST (nSET) of DFF12	52
[323:318]	IN3 of LUT4_0	53
[329:324]	Programmable delay/edge detect input	54
[335:330]	Filter/Edge detect input	55
[341:336]	GPIO0 Digital Output	56
[347:342]	GPIO1 Digital Output	57
[353:348]	GPIO2 Digital Output	58
[359:354]	GPIO2 Digital Output OE	59
[365:360]	GPIO3, Digital Output	60
[371:366]	GPIO3, Digital Output OE	61
[377:372]	GPO0 Digital Output	62
[383:378]	GPIO4 Digital Output	63
[389:384]	GPIO4 Digital Output OE	64
[395:390]	GPIO5 Digital Output	65
[401:396]	GPIO5 Digital Output OE	66
[407:402]	GPIO6 Digital Output	67
[413:408]	GPIO6 Digital Output OE	68

Table 24: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[419:414]	GPIO7 Digital Output	69
[425:420]	GPIO7 Digital Output OE	70
[431:426]	GPIO8 Digital Output	71
[437:432]	GPIO8 Digital Output OE	72
[443:438]	GPIO9, Digital Output	73
[449:444]	GPIO9 Digital Output OE	74
[455:450]	PWR UP of ACMP0_H	75
[461:456]	PWR UP of ACMP1_H	76
[467:462]	PWR UP of ACMP2_L	77
[473:468]	PWR UP of ACMP3_L	78
[479:474]	Temp sensor, Vref Out_0, Vref Out_1 Power Up	79
[485:480]	Oscillator0 ENABLE	80
[491:486]	Oscillator1 ENABLE	81
[497:492]	Oscillator2 ENABLE	82
[503:498]	IN0 of LUT4_1 or CLK Input of DFF20 Delay0 Input (or Counter0 nRST Input)	83
[509:504]	IN1 of LUT4_1 or nRST of DFF20 Delay0 Input (or Counter0 nRST Input)	84
[515:510]	IN2 of LUT4_1 or nSET of DFF20 Delay0 Input (or Counter0 nRST Input)	85
[521:516]	IN3 of LUT4_1 or Data of DFF20 Delay0 Input (or Counter0 nRST Input)	86
[527:522]	IN0 of LUT3_9 or CLK Input of DFF13 Delay1 Input (or Counter1 nRST Input)	87
[533:528]	IN1 of LUT3_9 or nRST (nSET) of DFF13 Delay1 Input (or Counter1 nRST Input)	88
[539:523]	IN2 of LUT3_9 or Data of DFF13 Delay1 Input (or Counter1 nRST Input)	89
[545:540]	IN0 of LUT3_10 or CLK Input of DFF14 Delay2 Input (or Counter2 nRST Input)	90
[551:546]	IN1 of LUT3_10 or nRST (nSET) of DFF14 Delay2 Input (or Counter2 nRST Input)	91
[557:552]	IN2 of LUT3_10 or Data of DFF14 Delay2 Input (or Counter2 nRST Input)	92
[563:558]	IN0 of LUT3_11 or CLK Input of DFF15 Delay3 Input (or Counter3 nRST Input)	93
[569:564]	IN1 of LUT3_11 or nRST (nSET) of DFF15 Delay3 Input (or Counter3 nRST Input)	94
[575:570]	IN2 of LUT3_11 or Data of DFF15 Delay3 Input (or Counter3 nRST Input)	95
Note 1 For each Address, the two most significant bits are unused.		

6.3 CONNECTION MATRIX VIRTUAL INPUTS

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at byte 0x4C (076).

Six of the eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Two of the eight Connection Matrix Virtual Inputs are shared with Pin digital inputs (GPIO0Digital or I^2C_virtual_0 Input), and (GPIO1 Digital or I^2C_virtual_1 Input). If the virtual input mode is selected, an I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened). The I^2C disable/enable register bit [2032] selects whether the Connection Matrix input comes from the Pin input or from the virtual register:

- Select SCL & Virtual Input 0 or GPIO0
- Select SDA & Virtual Input 1 or GPIO1

See Table 24 for Connection Matrix Virtual Inputs.

Table 25: Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I^2C_virtual_0 Input	[608]
33	I^2C_virtual_1 Input	[609]
34	I^2C_virtual_2 Input	[610]
35	I^2C_virtual_3 Input	[611]
36	I^2C_virtual_4 Input	[612]
37	I^2C_virtual_5 Input	[613]
38	I^2C_virtual_6 Input	[614]
39	I^2C_virtual_7 Input	[615]

6.4 CONNECTION MATRIX VIRTUAL OUTPUTS

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I^2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I^2C addresses for reading these register values are bytes 0x48 (072) to 0x4F (079). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at byte 0x4C (076)).

7 Combination Function Macrocells

The SLG46855-A has 15 combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Three macrocells that can serve as either 2-bit LUT or as D Flip-Flop
- Nine macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay/Ripple Counter
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen)
- One macrocell that can serve as either 4-bit LUT or as D Flip-Flop with Set/Reset Input

Inputs/Outputs for the 15 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of configuration bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-BIT LUT OR D FLIP-FLOP MACROCELLS

There is one macrocell that can serve as either 2-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

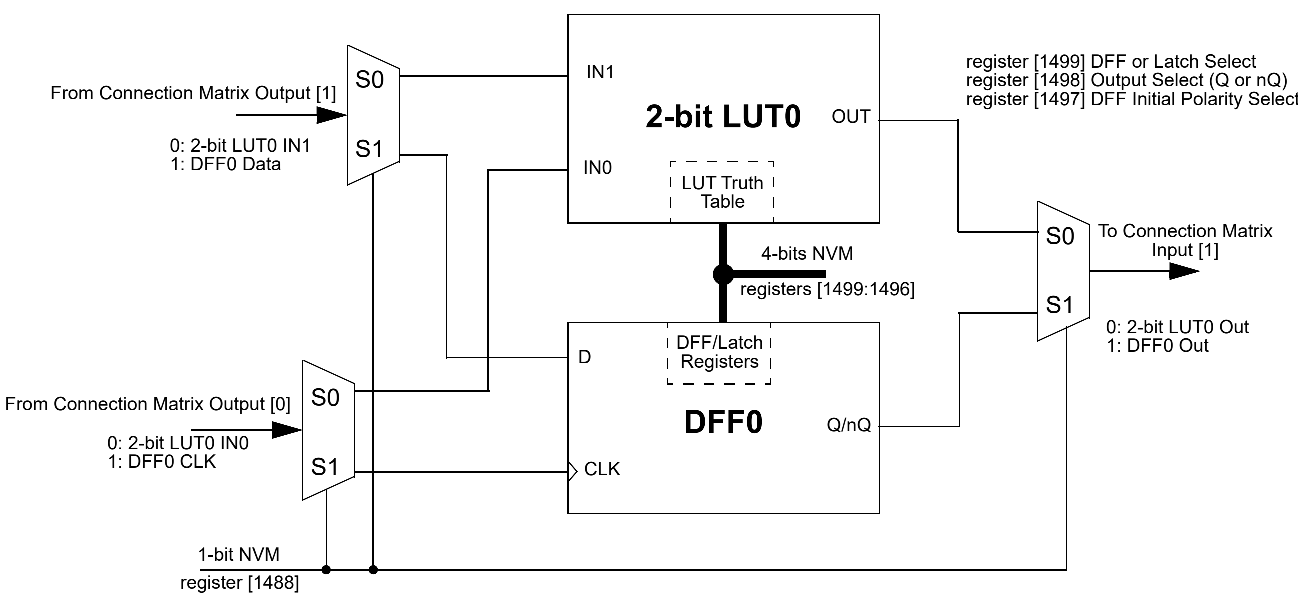


Figure 19: 2-bit LUT0 or DFF0

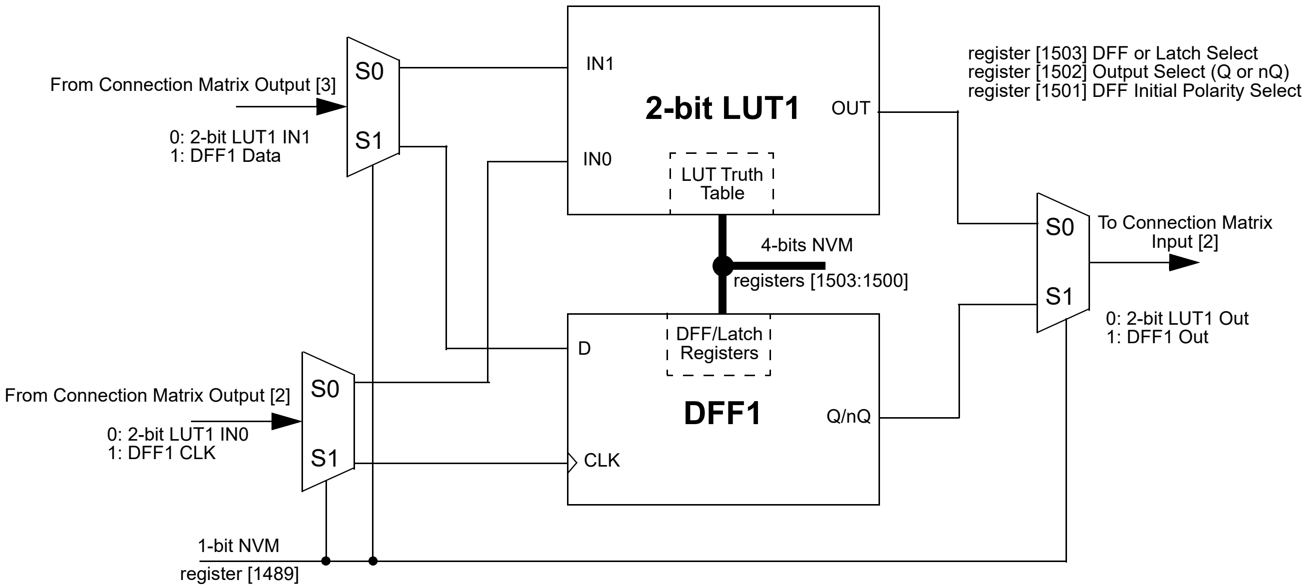


Figure 20: 2-bit LUT1 or DFF1

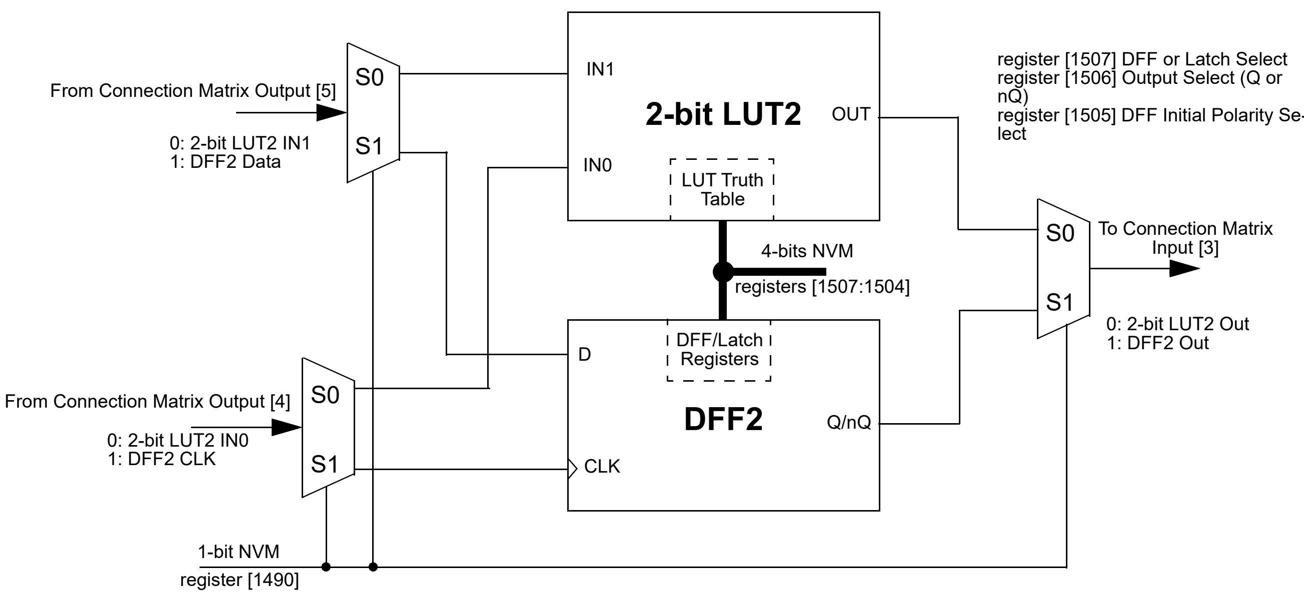


Figure 21: 2-bit LUT2 or DFF2

7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

Table 26: 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	register [1496]	LSB
0	1	register [1497]	
1	0	register [1498]	
1	1	register [1499]	MSB

Table 27: 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1500]	LSB
0	1	register [1501]	
1	0	register [1502]	
1	1	register [1503]	MSB

Table 28: 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	register [1504]	LSB
0	1	register [1505]	
1	0	register [1506]	
1	1	register [1507]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by registers [1499:1496]

2-Bit LUT1 is defined by registers [1503:1500]

2-Bit LUT2 is defined by registers [1507:1504]

Table 28 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells

Table 29: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.1.2 Initial Polarity Operations

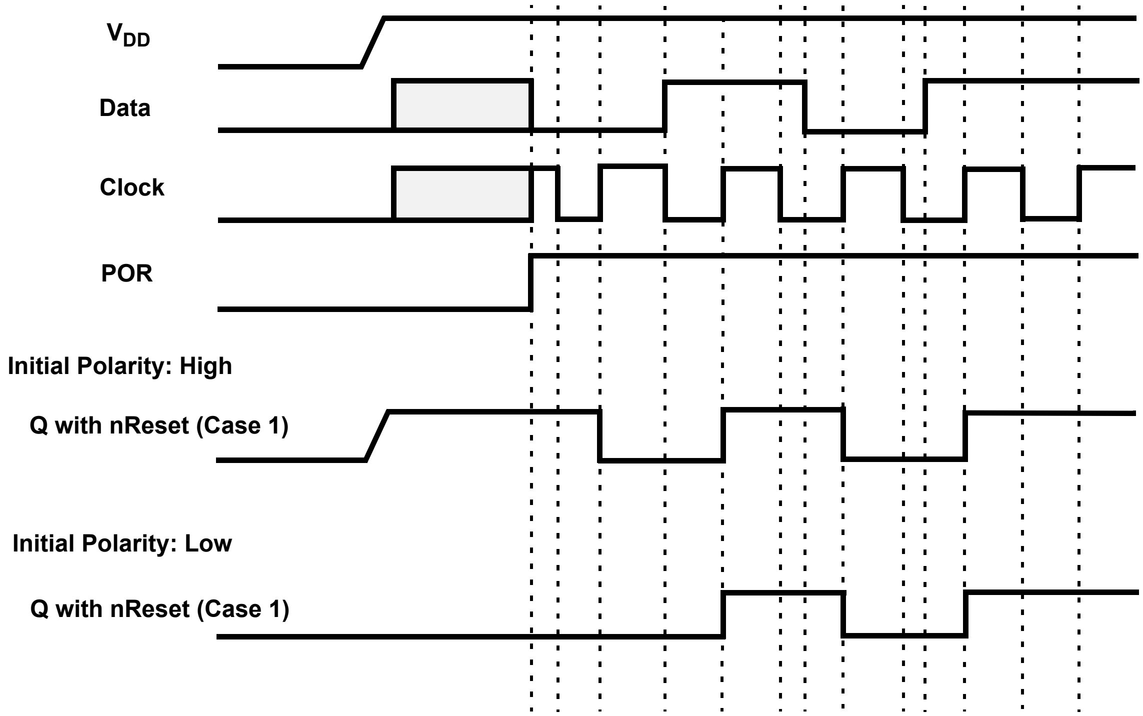


Figure 22: DFF Polarity Operations

7.2 2-BIT LUT OR PROGRAMMABLE PATTERN GENERATOR

The SLG46855-A has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

It is possible to define the RST level for the PGen macrocell. There are both high level reset (RST) and a low level reset (nRST) options available, which are selected by register [1409]. When operating as a Programmable Pattern Generator, the output of the macrocell will clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

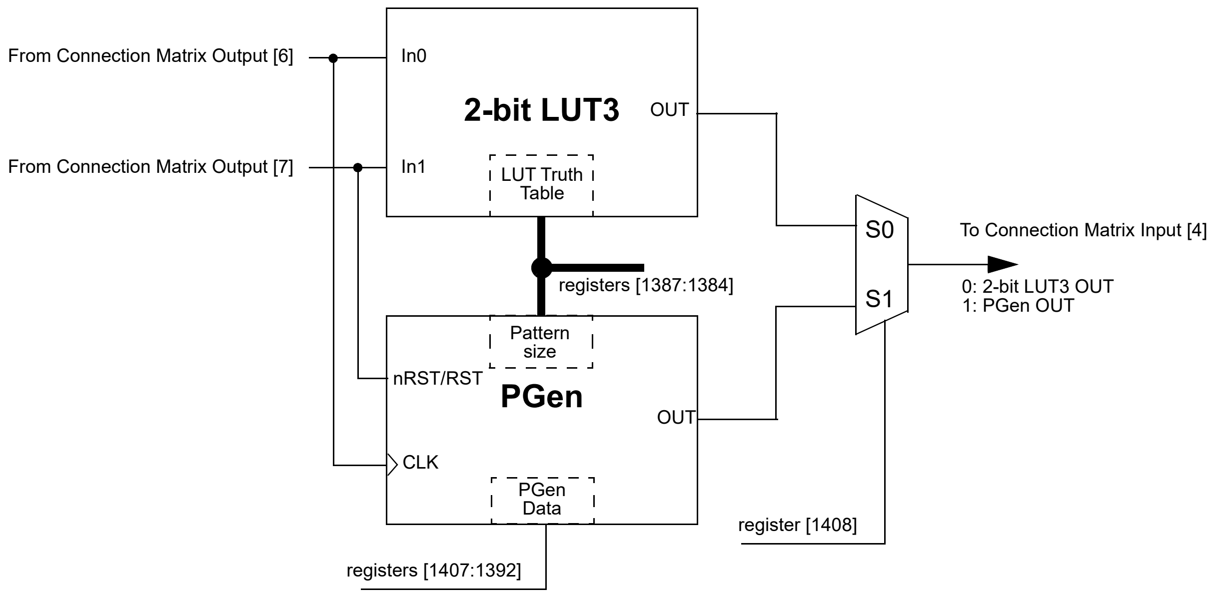


Figure 23: 2-bit LUT3 or PGen

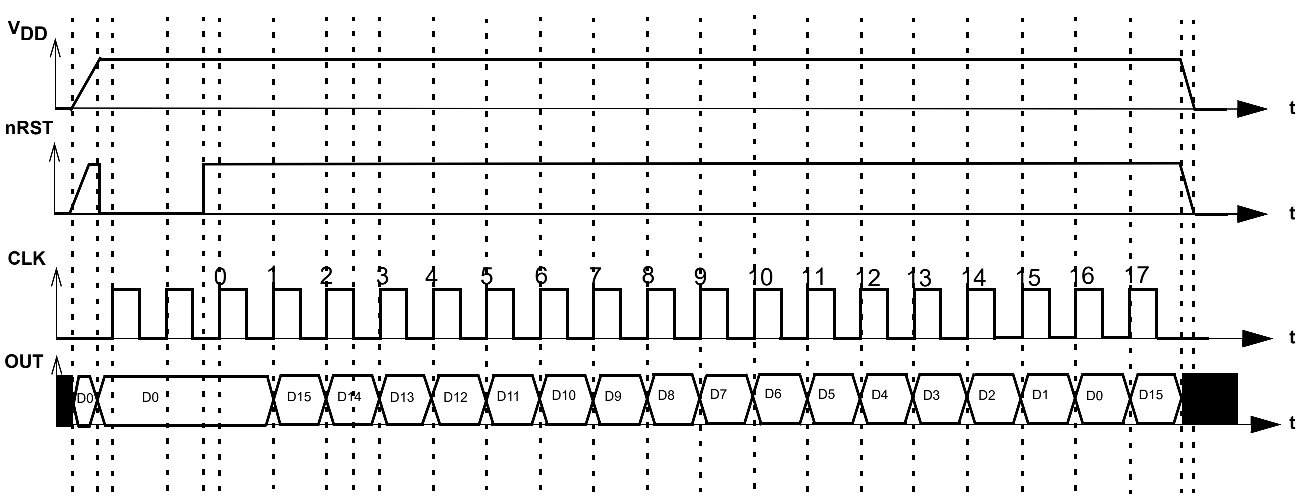


Figure 24: PGen Timing Diagram

7.2.1 2-Bit LUT or PGen Macrocell Used as 2-Bit LUT

Table 30: 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1384]	LSB
0	1	register [1385]	
1	0	register [1386]	
1	1	register [1387]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT3 is defined by registers [1387:1384]

Table 30 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 31: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.3 3-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELLS

There are nine macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available which are selected by register [1445].

DFF3 operation will flow the functional description below:

- If register [1443] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.
- If register [1443] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

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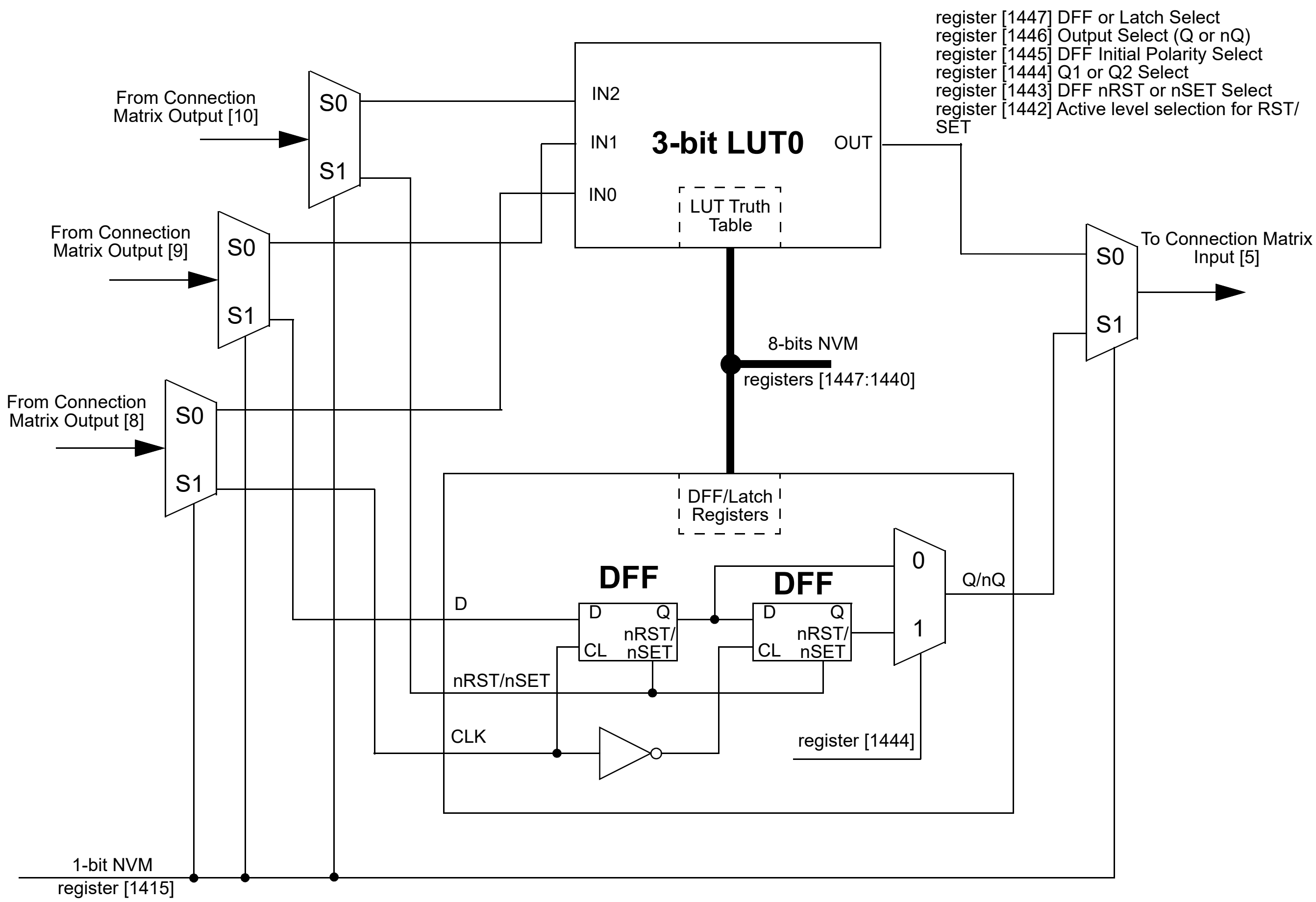

Figure 25: 3-bit LUT0 or DFF3

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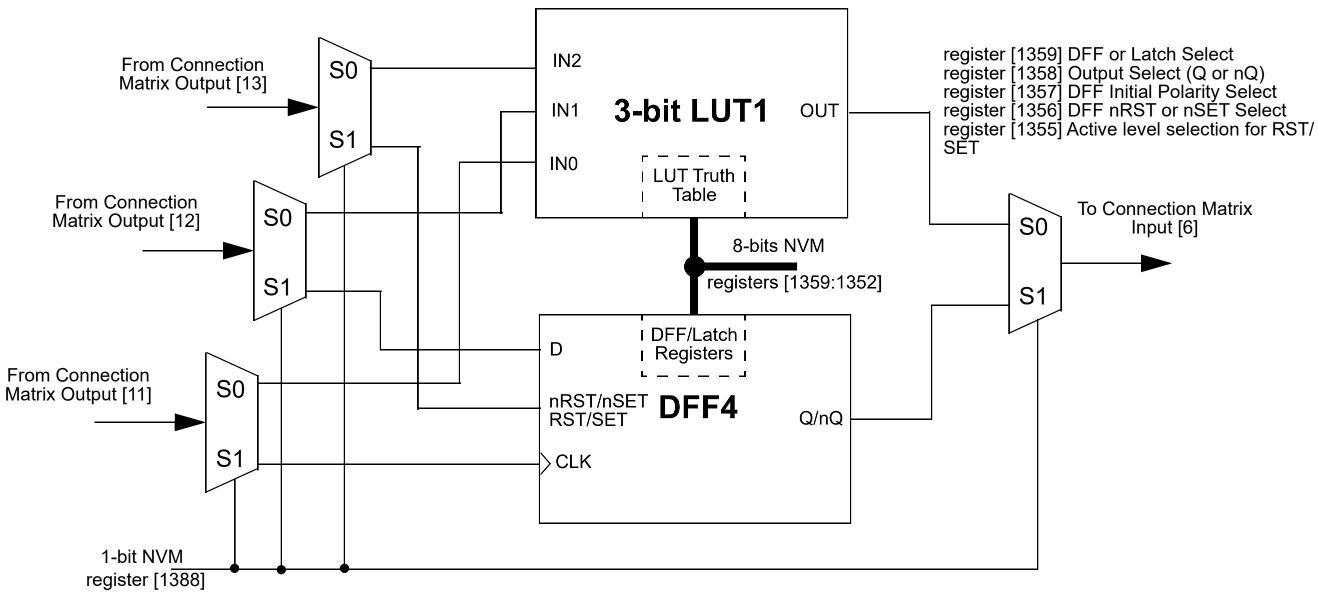

Figure 26: 3-bit LUT1 or DFF4

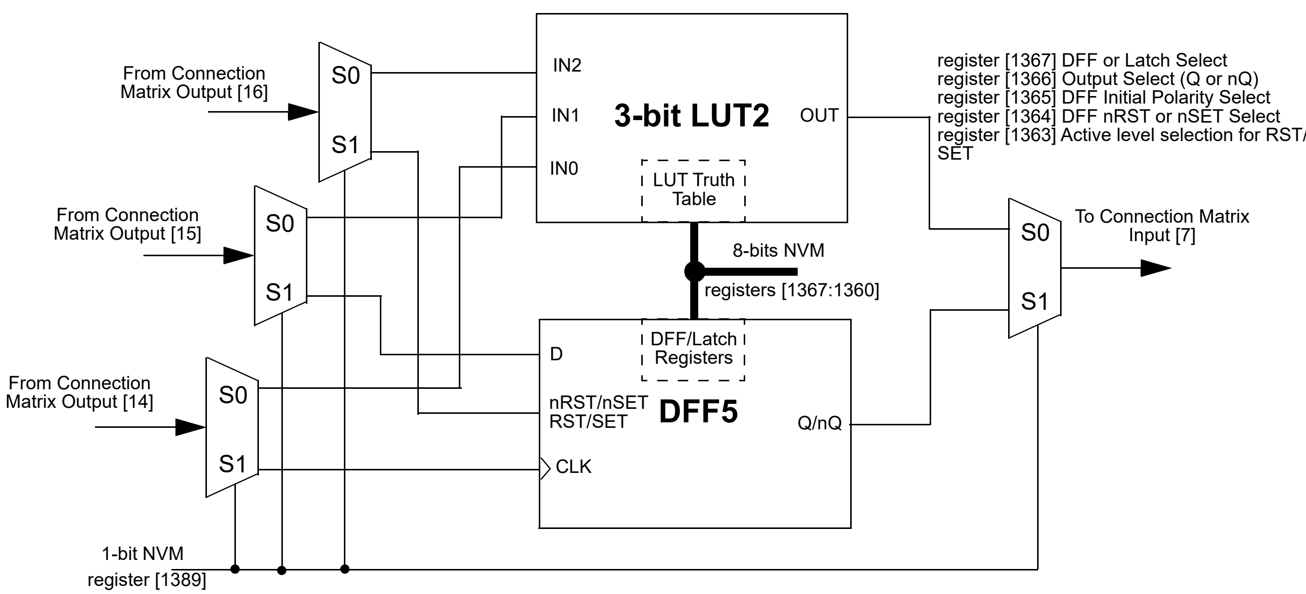

Figure 27: 3-bit LUT2 or DFF5

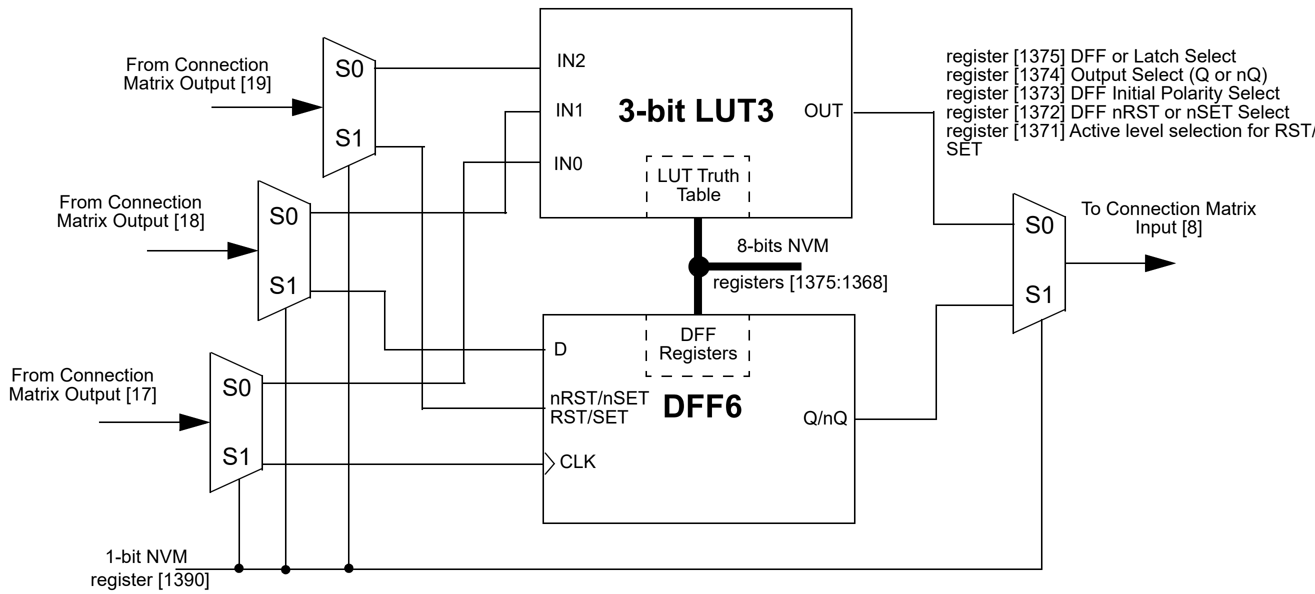

Figure 28: 3-bit LUT3 or DFF6

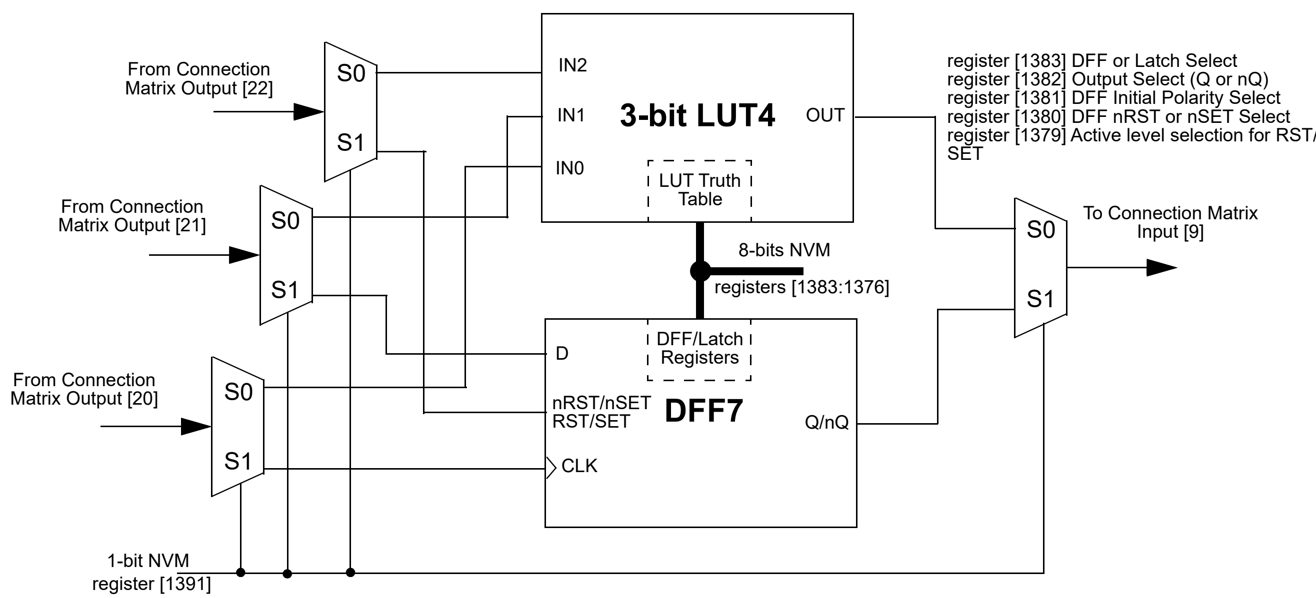

Figure 29: 3-bit LUT4 or DFF7

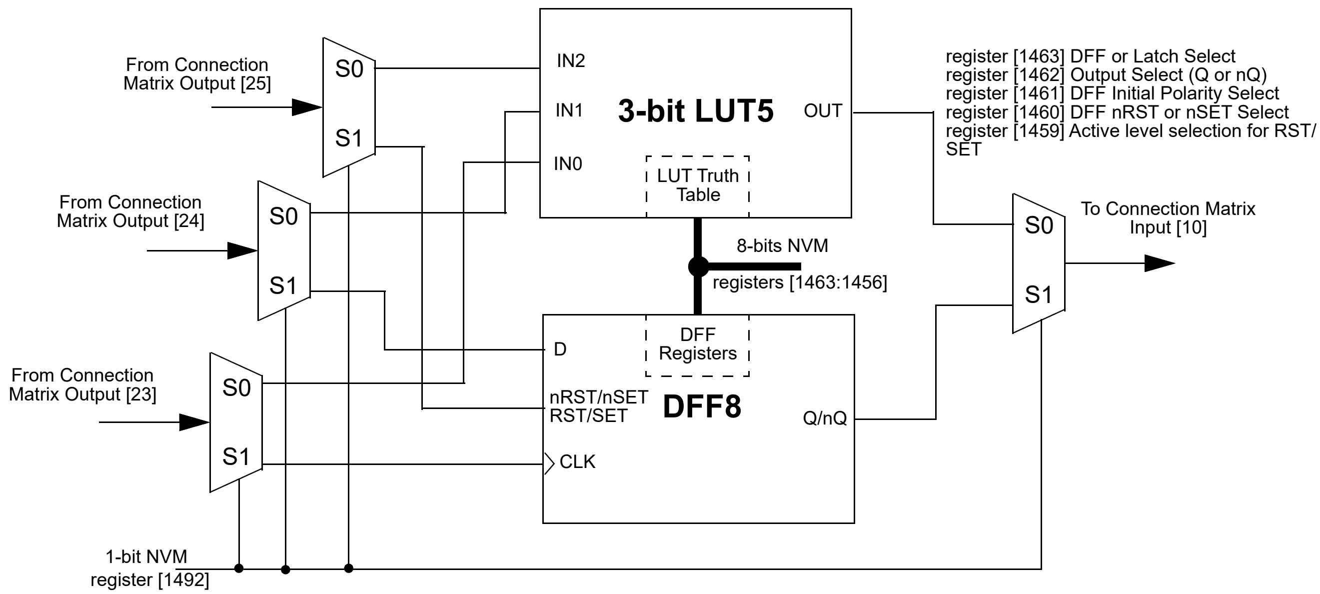

Figure 30: 3-bit LUT5 or DFF8

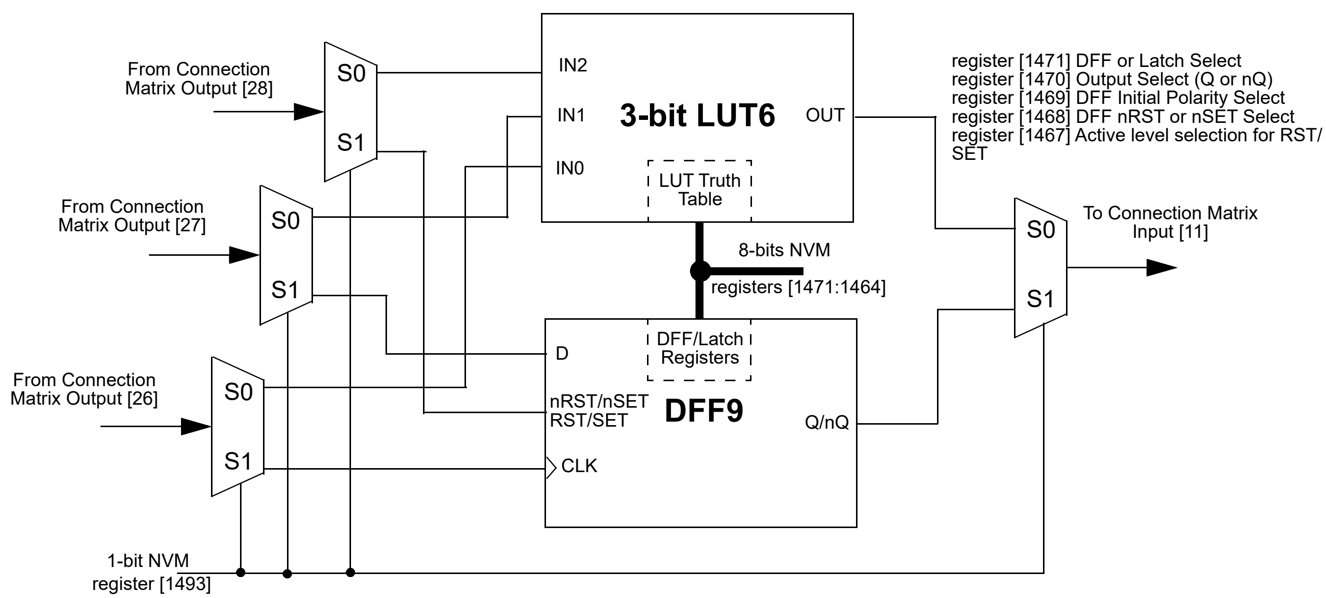

Figure 31: 3-bit LUT6 or DFF9

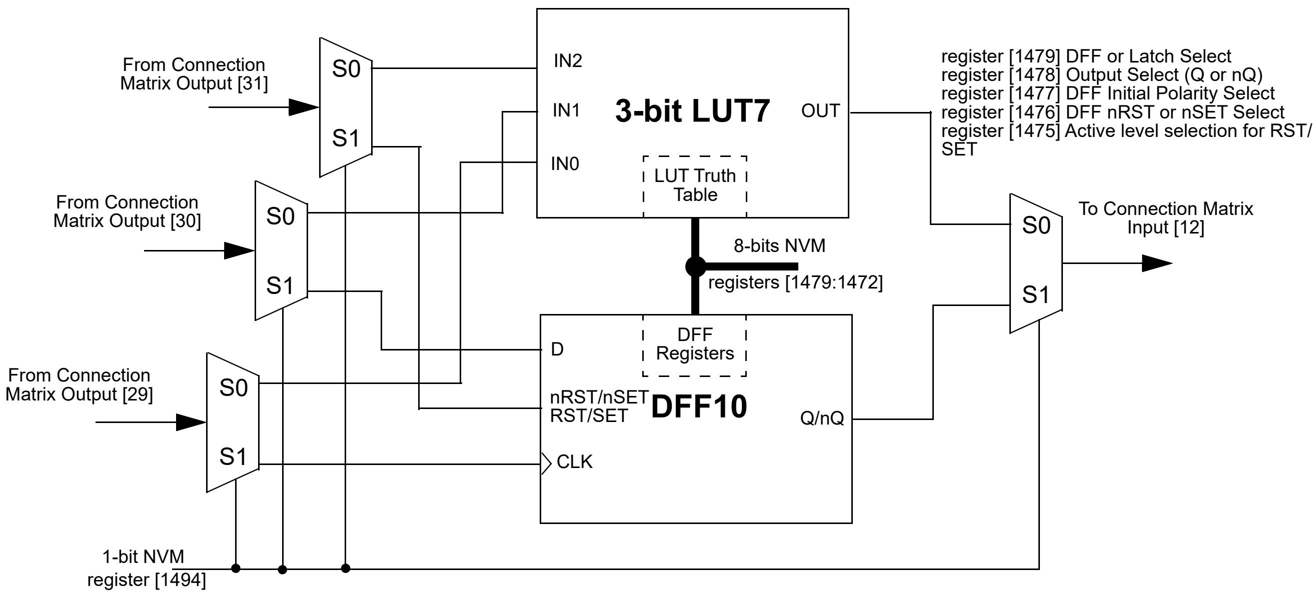

Figure 32: 3-bit LUT7 or DFF10

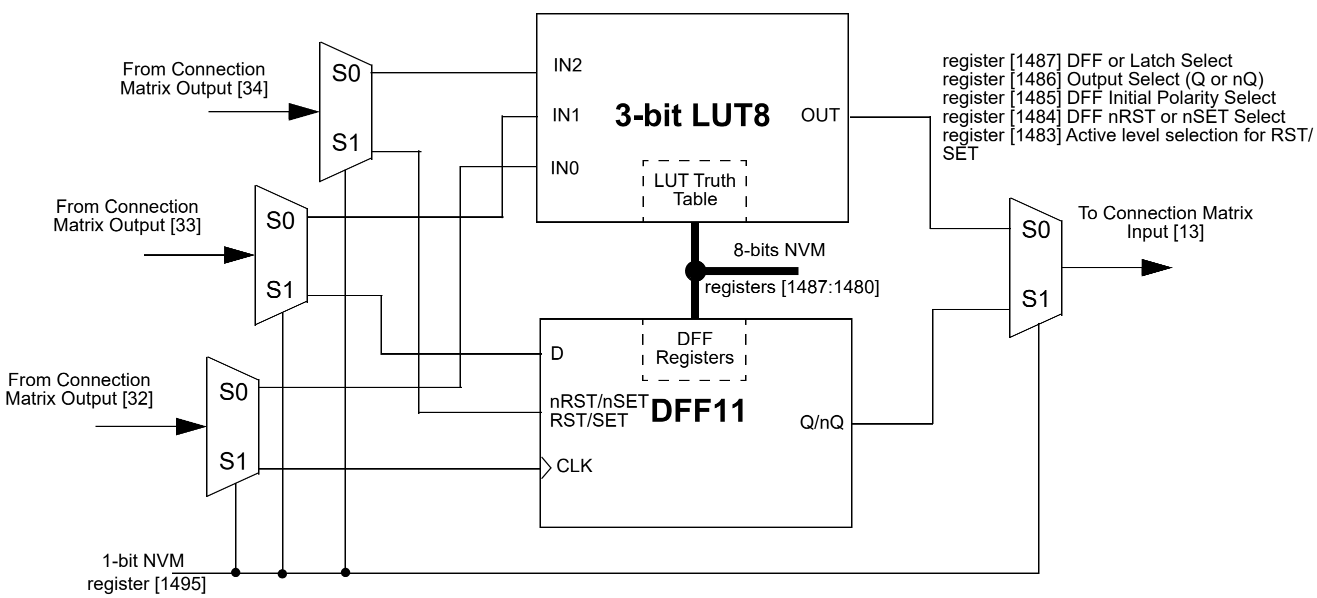

Figure 33: 3-bit LUT8 or DFF11

7.3.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 32: 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1440]	LSB
0	0	1	register [1441]	
0	1	0	register [1442]	
0	1	1	register [1443]	
1	0	0	register [1444]	
1	0	1	register [1445]	
1	1	0	register [1446]	
1	1	1	register [1447]	MSB

Table 33: 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1352]	LSB
0	0	1	register [1353]	
0	1	0	register [1354]	
0	1	1	register [1355]	
1	0	0	register [1356]	
1	0	1	register [1357]	
1	1	0	register [1358]	
1	1	1	register [1359]	MSB

Table 34: 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1360]	LSB
0	0	1	register [1361]	
0	1	0	register [1362]	
0	1	1	register [1363]	
1	0	0	register [1364]	
1	0	1	register [1365]	
1	1	0	register [1366]	
1	1	1	register [1367]	MSB

Table 35: 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1368]	LSB
0	0	1	register [1369]	
0	1	0	register [1370]	
0	1	1	register [1371]	
1	0	0	register [1372]	
1	0	1	register [1373]	
1	1	0	register [1374]	
1	1	1	register [1375]	MSB

Table 36: 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1376]	LSB
0	0	1	register [1377]	
0	1	0	register [1378]	
0	1	1	register [1379]	
1	0	0	register [1380]	
1	0	1	register [1381]	
1	1	0	register [1382]	
1	1	1	register [1383]	MSB

Table 37: 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1356]	LSB
0	0	1	register [1357]	
0	1	0	register [1358]	
0	1	1	register [1359]	
1	0	0	register [1360]	
1	0	1	register [1361]	
1	1	0	register [1362]	
1	1	1	register [1363]	MSB

Table 38: 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1364]	LSB
0	0	1	register [1365]	
0	1	0	register [1366]	
0	1	1	register [1367]	
1	0	0	register [1368]	
1	0	1	register [1369]	
1	1	0	register [1370]	
1	1	1	register [1371]	MSB

Table 39: 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1472]	LSB
0	0	1	register [1473]	
0	1	0	register [1474]	
0	1	1	register [1475]	
1	0	0	register [1476]	
1	0	1	register [1477]	
1	1	0	register [1478]	
1	1	1	register [1479]	MSB

Table 40: 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1480]	LSB
0	0	1	register [1481]	
0	1	0	register [1482]	
0	1	1	register [1483]	
1	0	0	register [1484]	
1	0	1	register [1485]	
1	1	0	register [1486]	
1	1	1	register [1487]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT0 is defined by registers [1447:1440]

3-Bit LUT1 is defined by registers [1359:1352]

3-Bit LUT2 is defined by registers [1367:1360]

3-Bit LUT3 is defined by registers [1375:1368]

3-Bit LUT4 is defined by registers [1383:1376]

3-Bit LUT5 is defined by registers [1463:1456]

3-Bit LUT6 is defined by registers [1471:1464]

3-Bit LUT7 is defined by registers [1479:1472]

3-Bit LUT8 is defined by registers [1487:1480]

Table 40 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 41: 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.3.2 Initial Polarity Operations

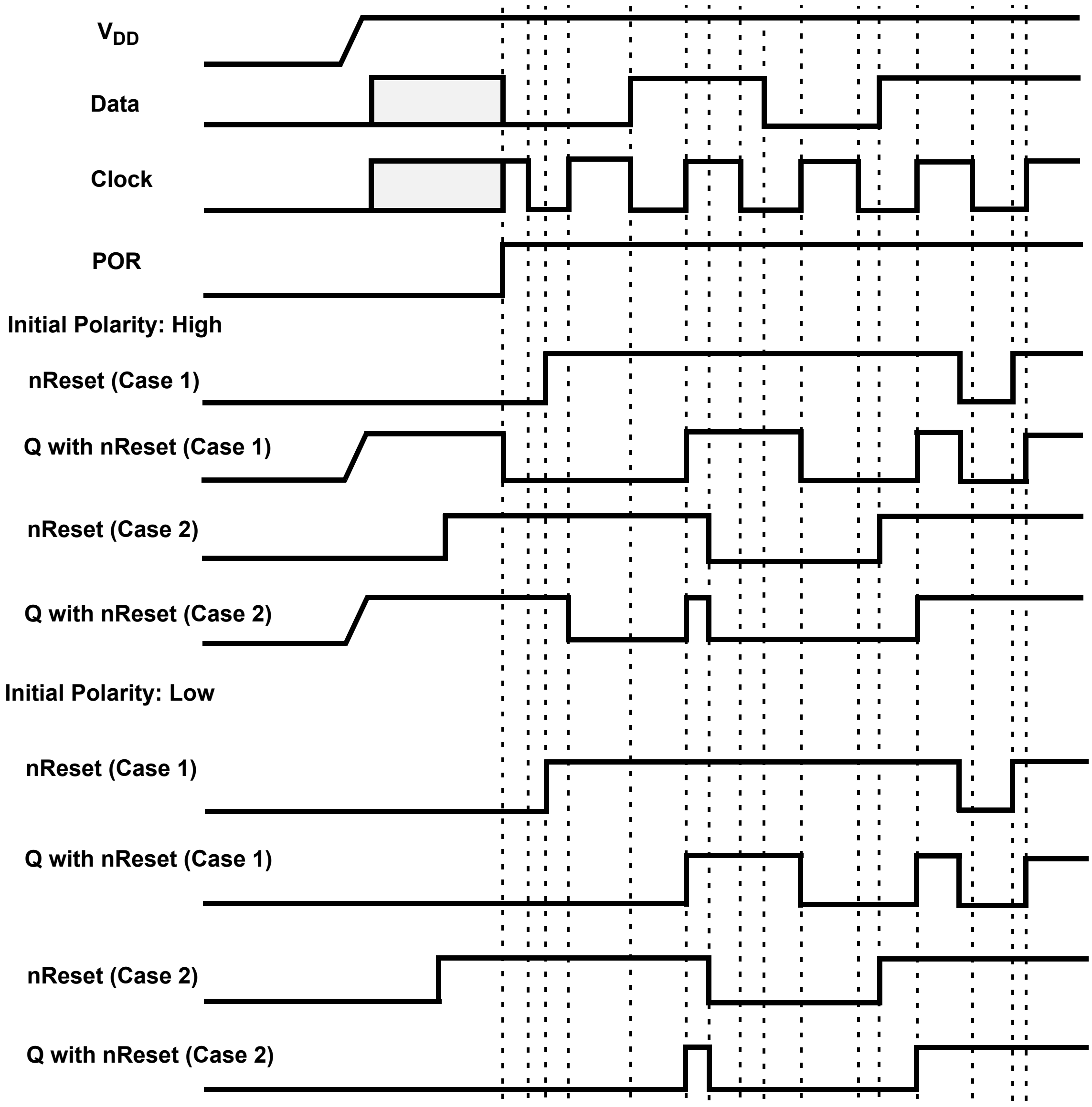

Figure 34: DFF Polarity Operations with nReset

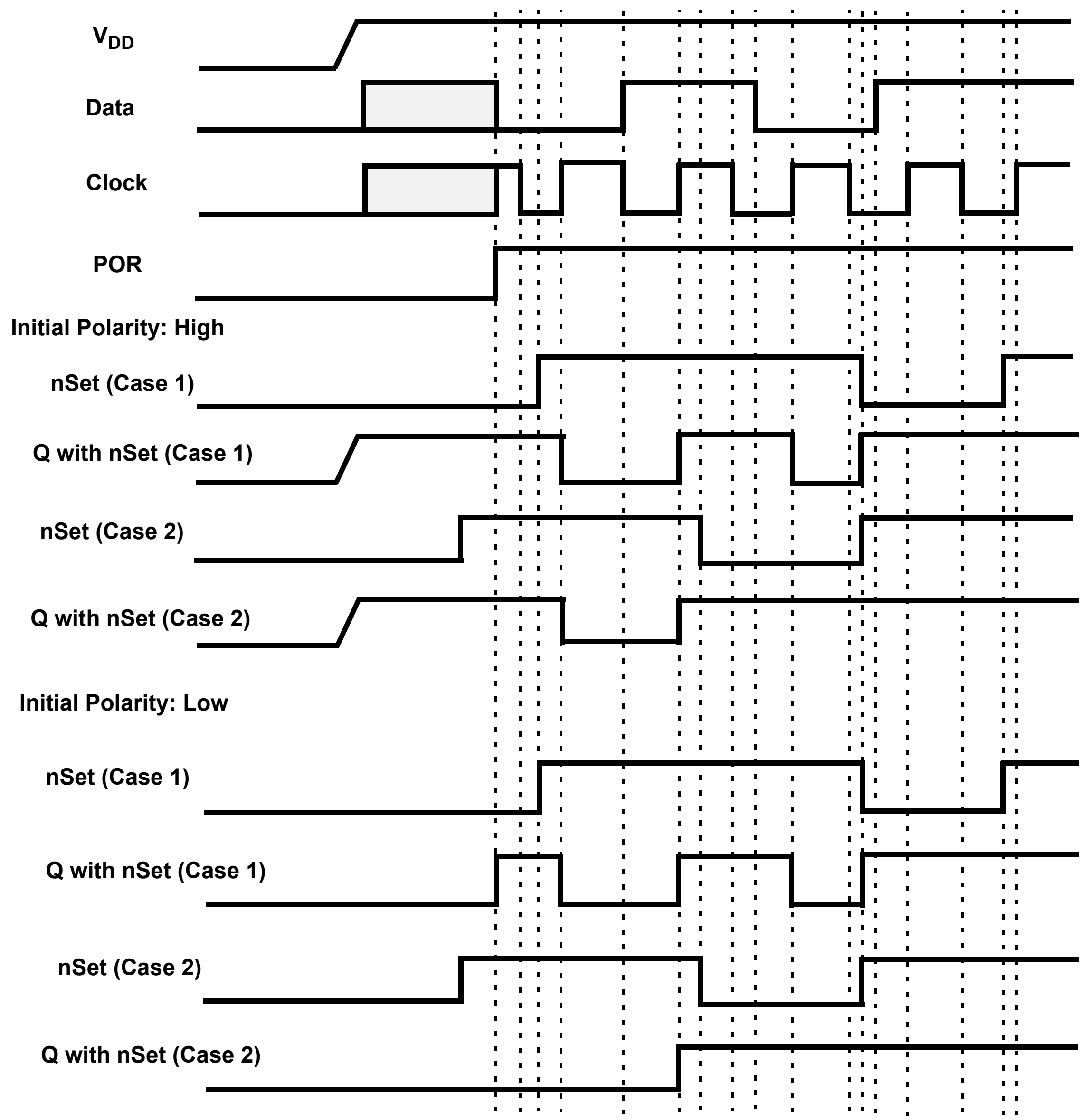

Figure 35: DFF Polarity Operations with nSet

7.4 4-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELL

There is one macrocell that can serve as either a 4-bit LUT or as a D Flip-Flop with Set/Reset inputs. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

- If register [1436] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.
- If register [1436] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available which are selected by register [1434].

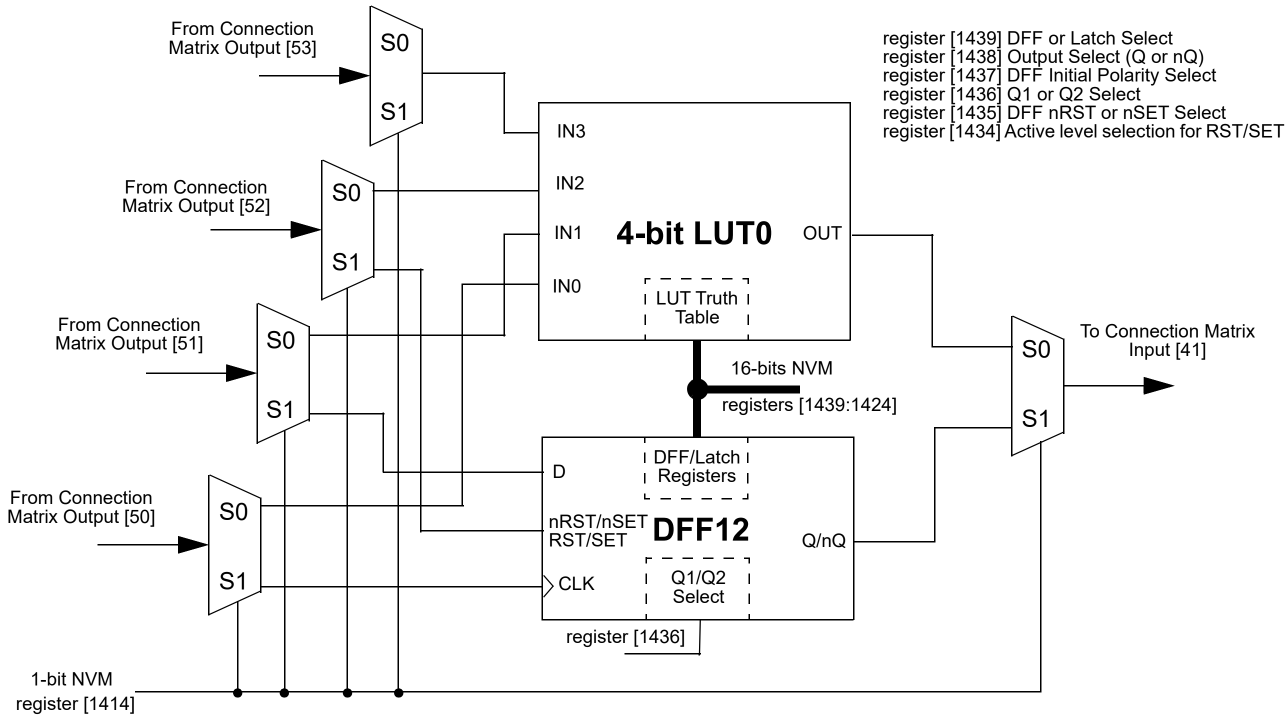

Figure 36: 4-bit LUT0 or DFF12

7.4.1 4-Bit LUT Macrocell Used as 4-Bit LUT

Table 42: 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1424]	LSB
0	0	0	1	register [1425]	
0	0	1	0	register [1426]	
0	0	1	1	register [1427]	
0	1	0	0	register [1428]	
0	1	0	1	register [1429]	
0	1	1	0	register [1430]	
0	1	1	1	register [1431]	
1	0	0	0	register [1432]	
1	0	0	1	register [1433]	
1	0	1	0	register [1434]	
1	0	1	1	register [1435]	
1	1	0	0	register [1436]	
1	1	0	1	register [1437]	
1	1	1	0	register [1438]	
1	1	1	1	register [1439]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by registers [1439:1424]

Table 43: 4-bit LUT Standard Digital Functions

Function	MSB														LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

7.5 3-BIT LUT OR PIPE DELAY/RIPPLE COUNTER MACROCELL

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay/Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a Pipe Delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK), and Reset (nRST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by registers [1419:1416] for OUT0 and registers [1423:1420] for OUT1. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46855-A design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the internal Oscillator within the SLG46855-A). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by register [1413]).

In the Ripple Counter mode there are 3 options for setting which use 7 bits. There are 3 bits to set **nSET value (SV)** in range from 0 to 7. This value will be set into the Ripple Counter outputs when nSET input goes LOW. **End value (EV)** will use 3 bits for setting output code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The **Functionality mode** option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

The user can select one of the functionality modes by register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV→EV→EV-1 to SV+1→SV, and others (if SV is smaller than EV), or SV→SV-1 to EV+1→EV→SV (if SV is bigger than EV). If UP input is HIGH, count starts from SV up to EV, and others.

In the FULL range configuration the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. Then current counter value jumps to EV and goes down to 0, and others.

If UP input is HIGH, count goes up starting from SV. Then current counter value jumps to 0 and counts up to EV, and others. See Ripple Counter functionality example in Figure 38.

Every step is executed by the rising edge on CLK input.

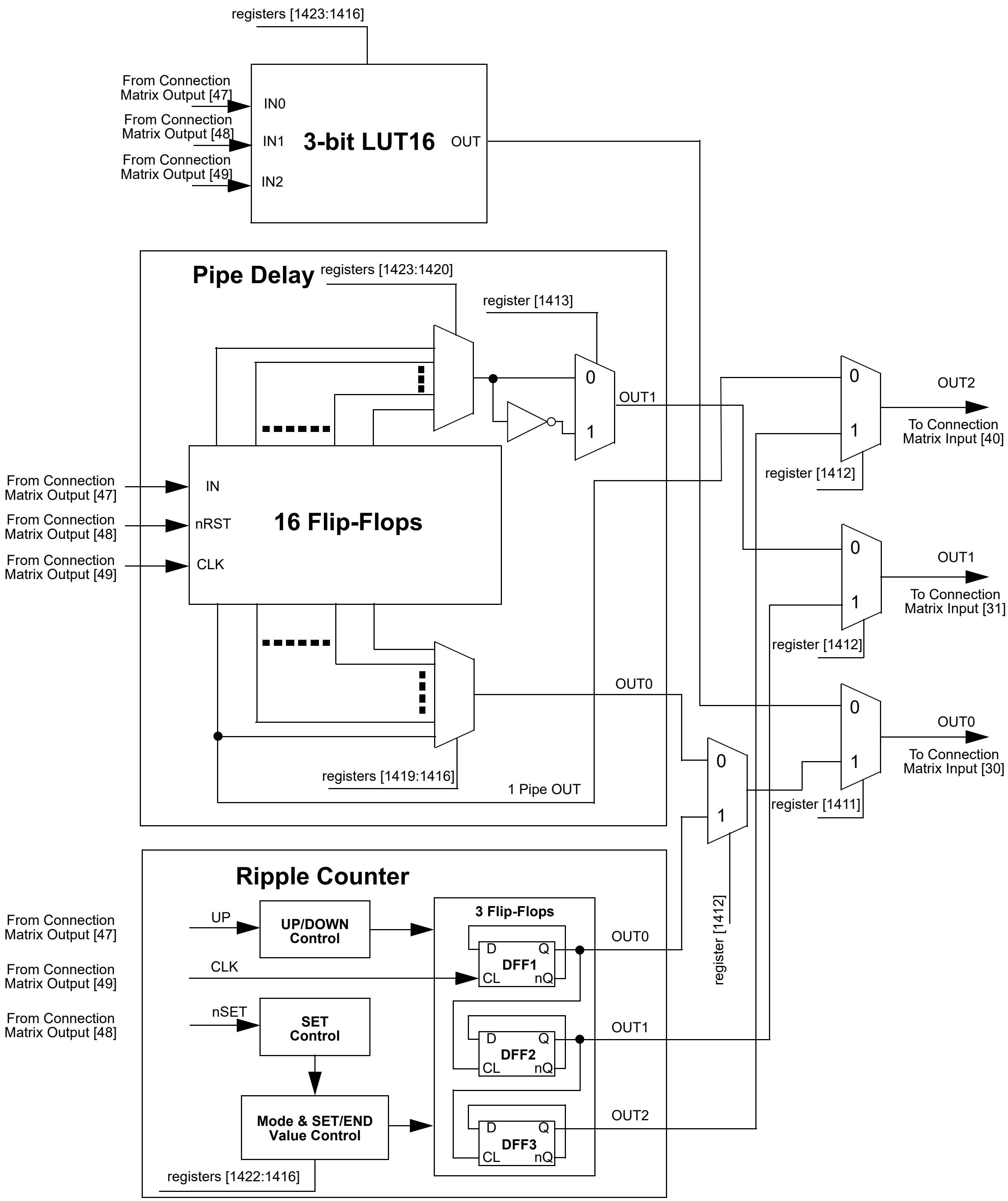

Figure 37: 3-bit LUT16/Pipe Delay/Ripple Counter

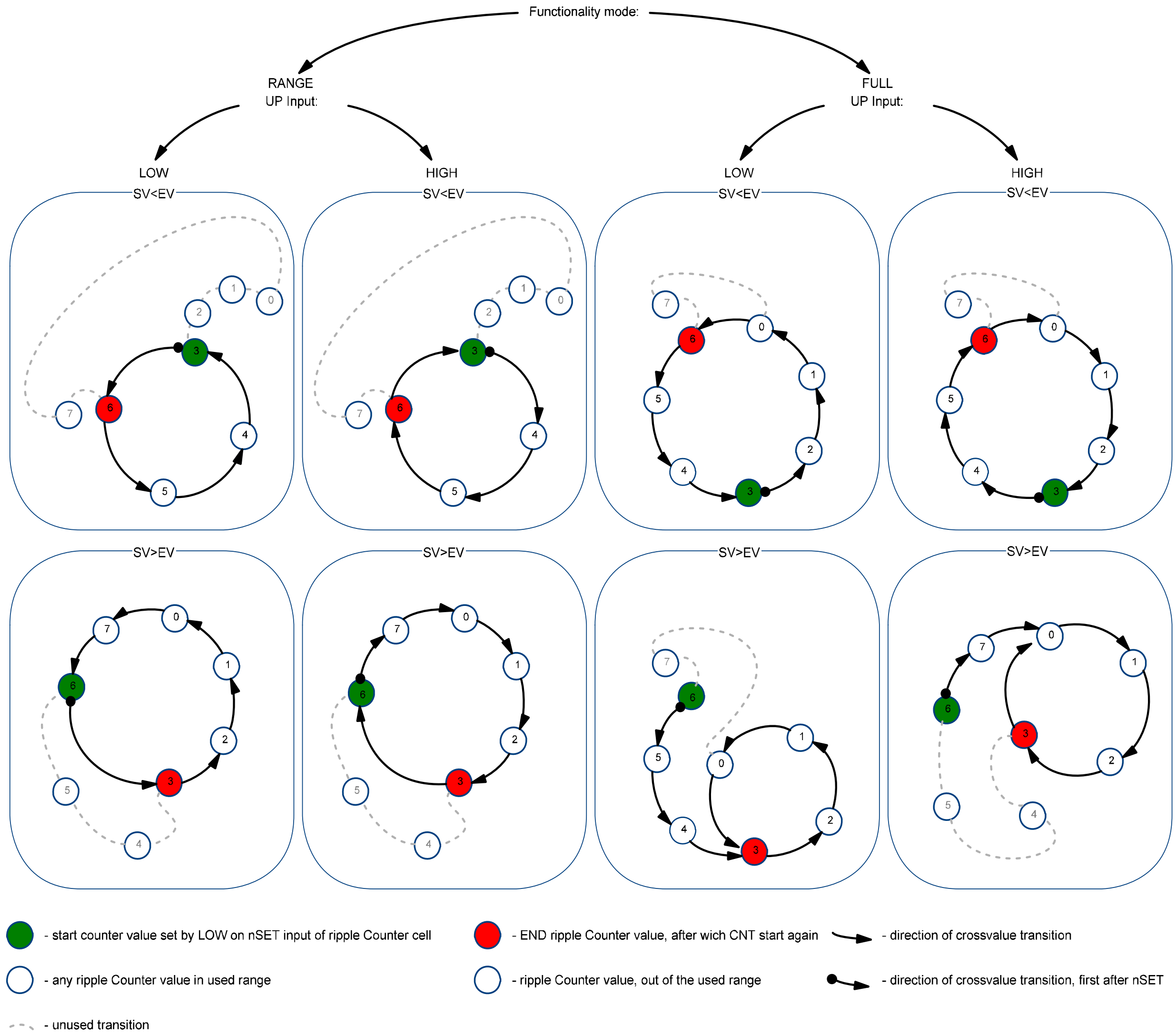

Figure 38: Example: Ripple Counter Functionality

7.5.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUT

Table 44: 3-bit LUT16 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [1416]
0	0	1	register [1417]
0	1	0	register [1418]
0	1	1	register [1419]
1	0	0	register [1420]
1	0	1	register [1421]
1	1	0	register [1422]
1	1	1	register [1423]

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT16 is defined by registers [1423:1416]

8 Multi-Function Macrocells

The SLG46855-A has 8 Multi-Function macrocells that can serve more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes, such as One Shot, Frequency Detect, Edge Detect, and others. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 39.

See the list below for the functions that can be implemented in these macrocells:

- Seven macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays
- One macrocell that can serve as a 4-bit LUT/D Flip-Flop and as 16-Bit Counter/Delay/FSM

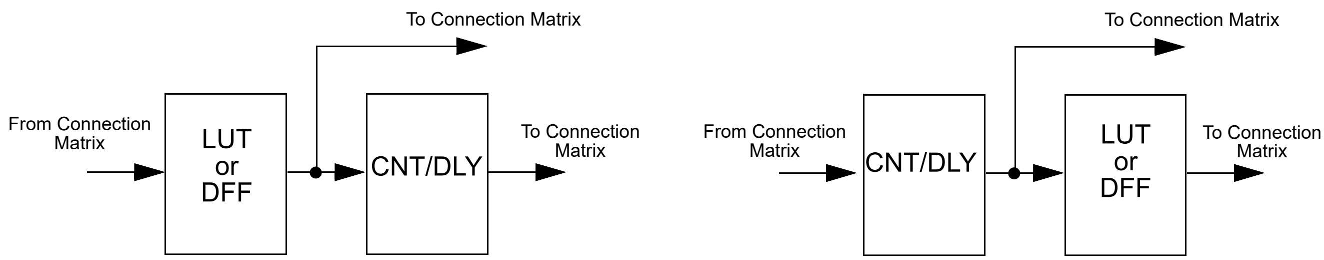

Figure 39: Possible Connections Inside Multi-Function Macrocell

Inputs/Outputs for the 8 Multi-Function function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

8.1 3-BIT LUT OR DFF/LATCH WITH 8-BIT COUNTER/DELAY MACROCELLS

There are seven macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays.

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Reset/Set (nRST/nSET) inputs of the Flip-Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When used to implement Counter/Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which define its initial value after GPAK is powered up. It is possible to select initial Low or initial High, as well as initial value defined by a Delay In signal.

For example, in case initial LOW option is used, the rising edge delay will start operation.

For timing diagrams refer to sections 7.1 and 8.3.

Note: After two DFF – counters initialize with counter data = 0 after POR.
Initial state = 1 – counters initialize with counter data = 0 after POR.Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

CNT6 and CNT7 current count value can be read via I²C. However, it is possible to change the counter data (value counter starts operating from) for any macrocell using I²C write commands. In this mode, it is possible to load count data immediately (after two DFF) or after counter ends counting. See Section 15.6.1 for further details.

8.1.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

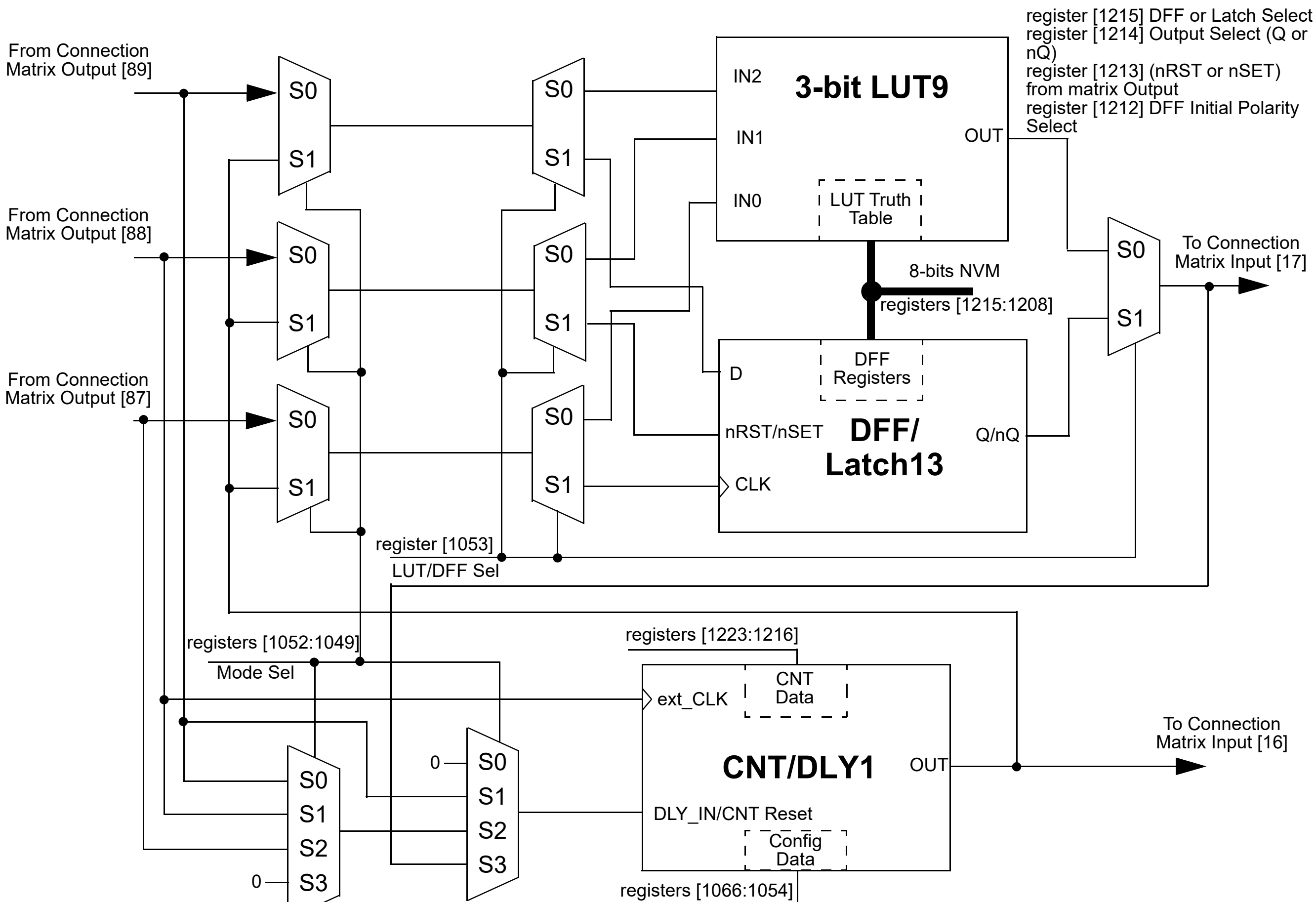

Figure 40: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF13, CNT/DLY1)

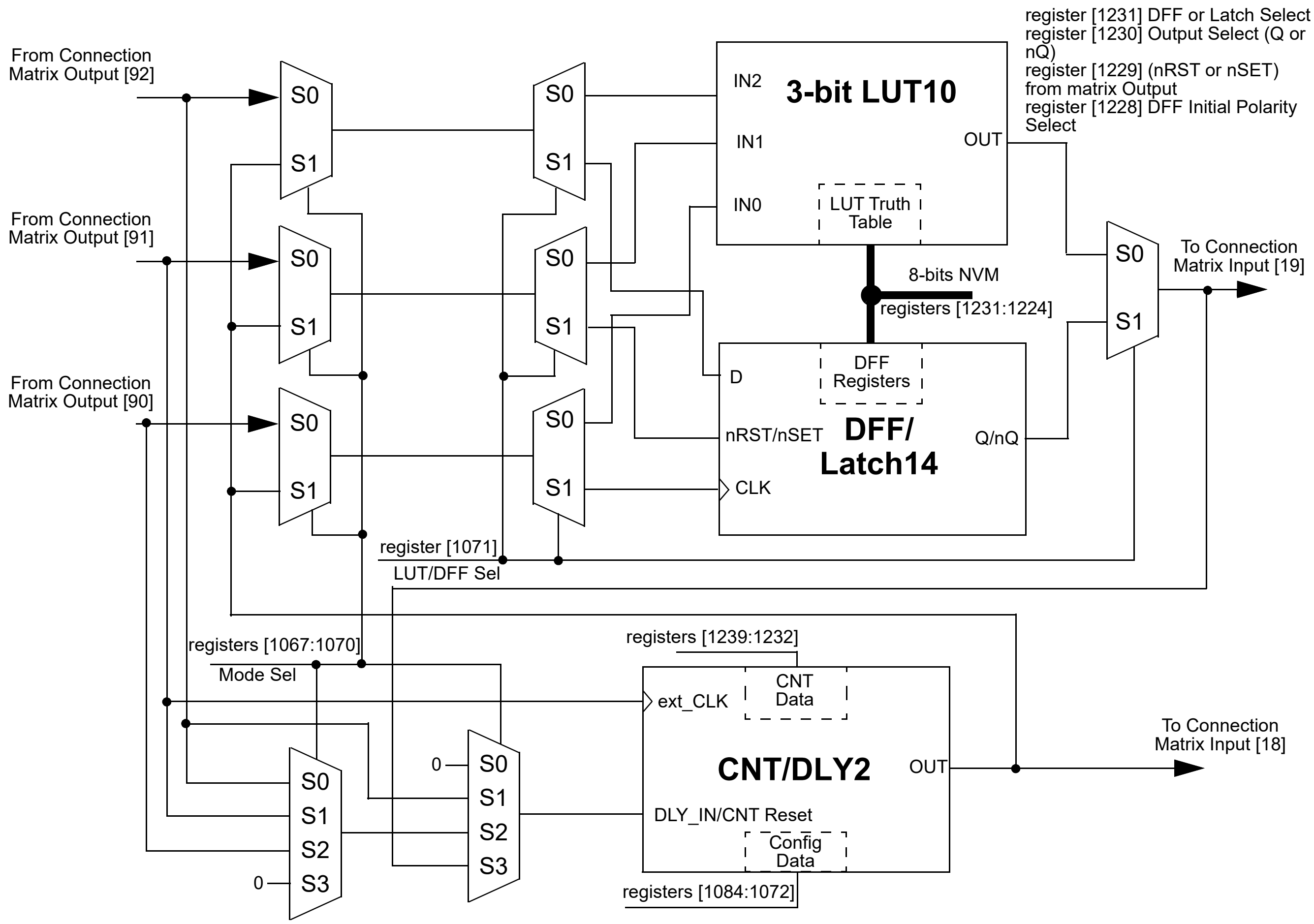

Figure 41: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF14, CNT/DLY2)

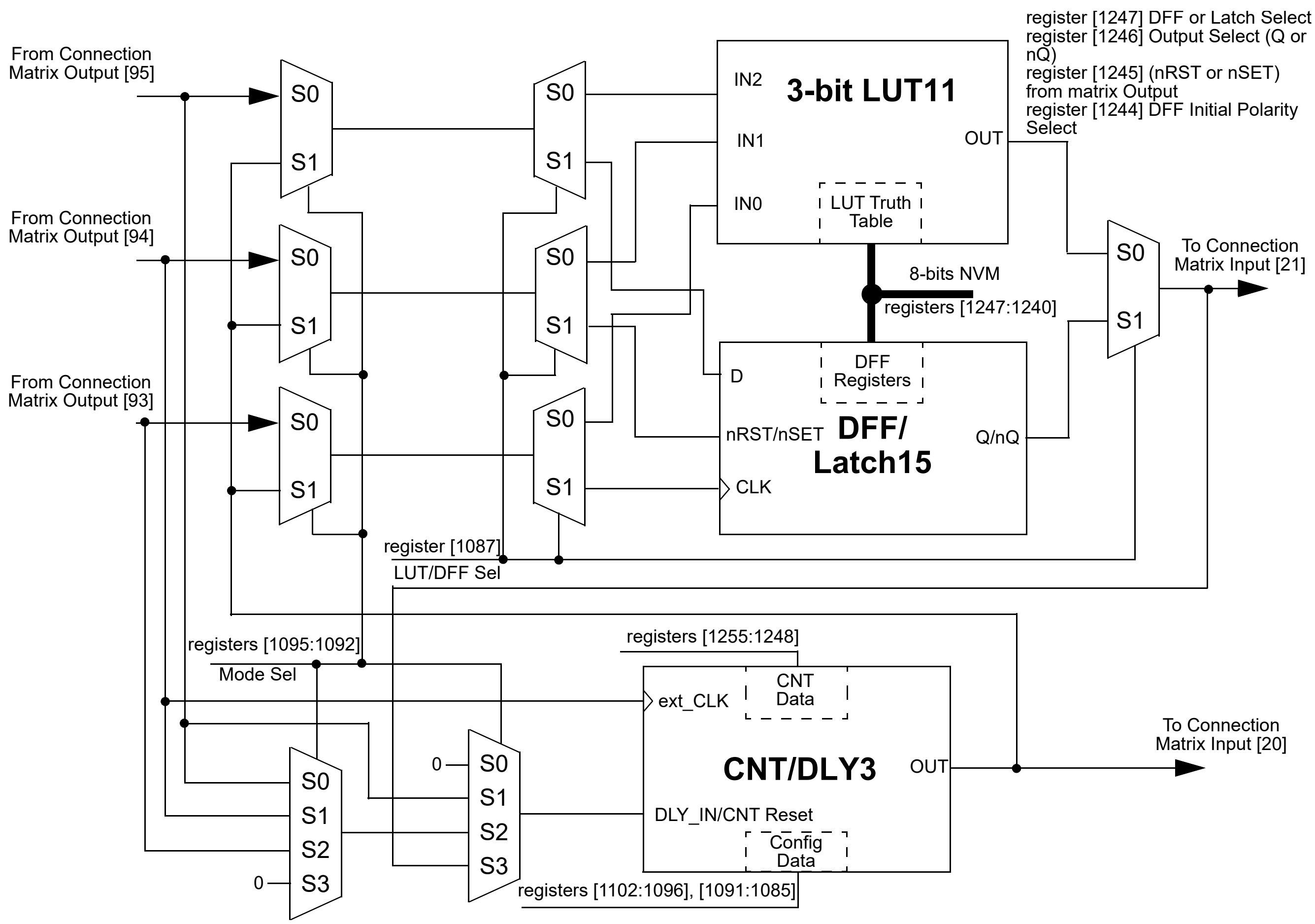

Figure 42: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF15, CNT/DLY3)

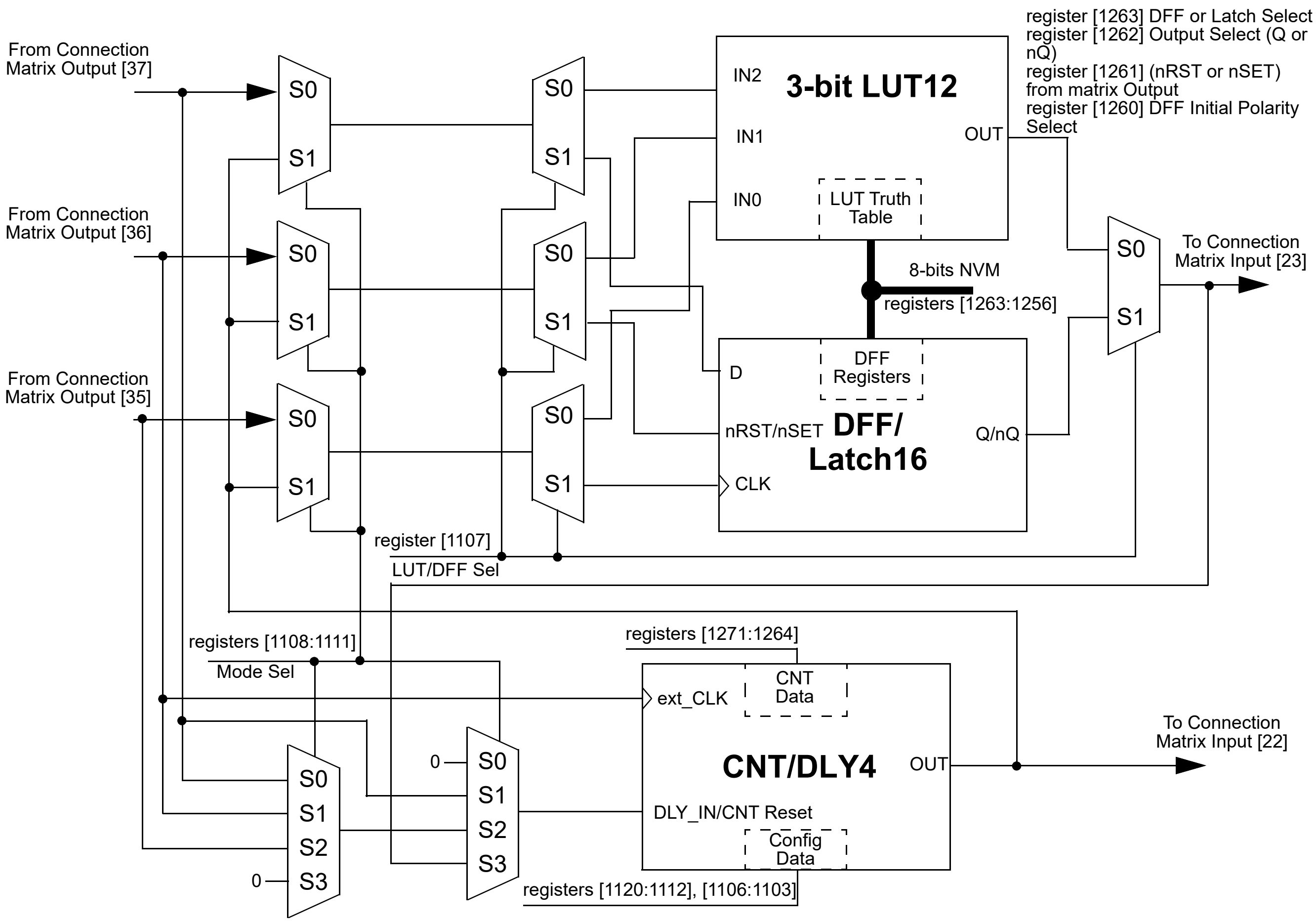

Figure 43: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF16, CNT/DLY4)

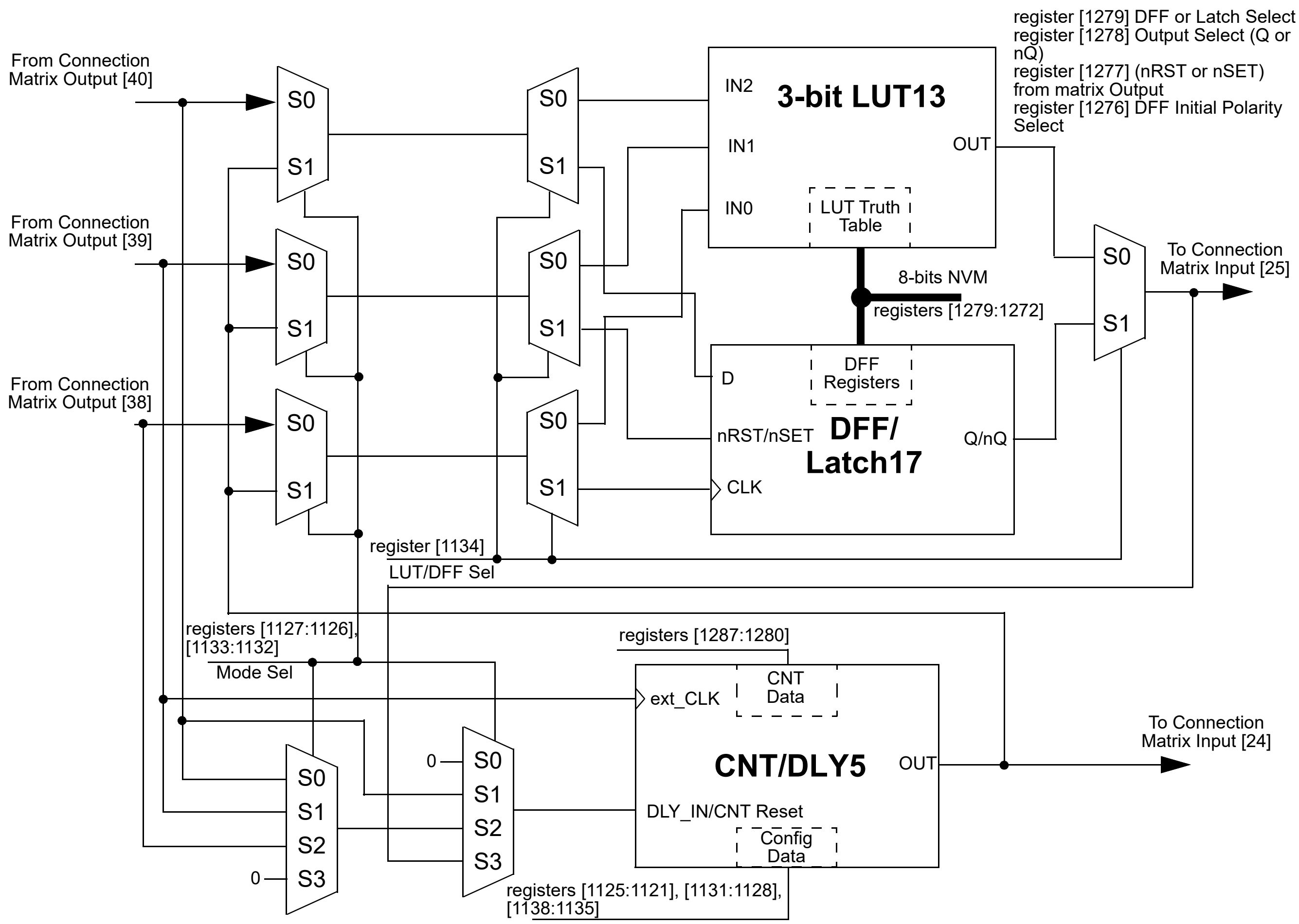

Figure 44: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT13/DFF17, CNT/DLY5)

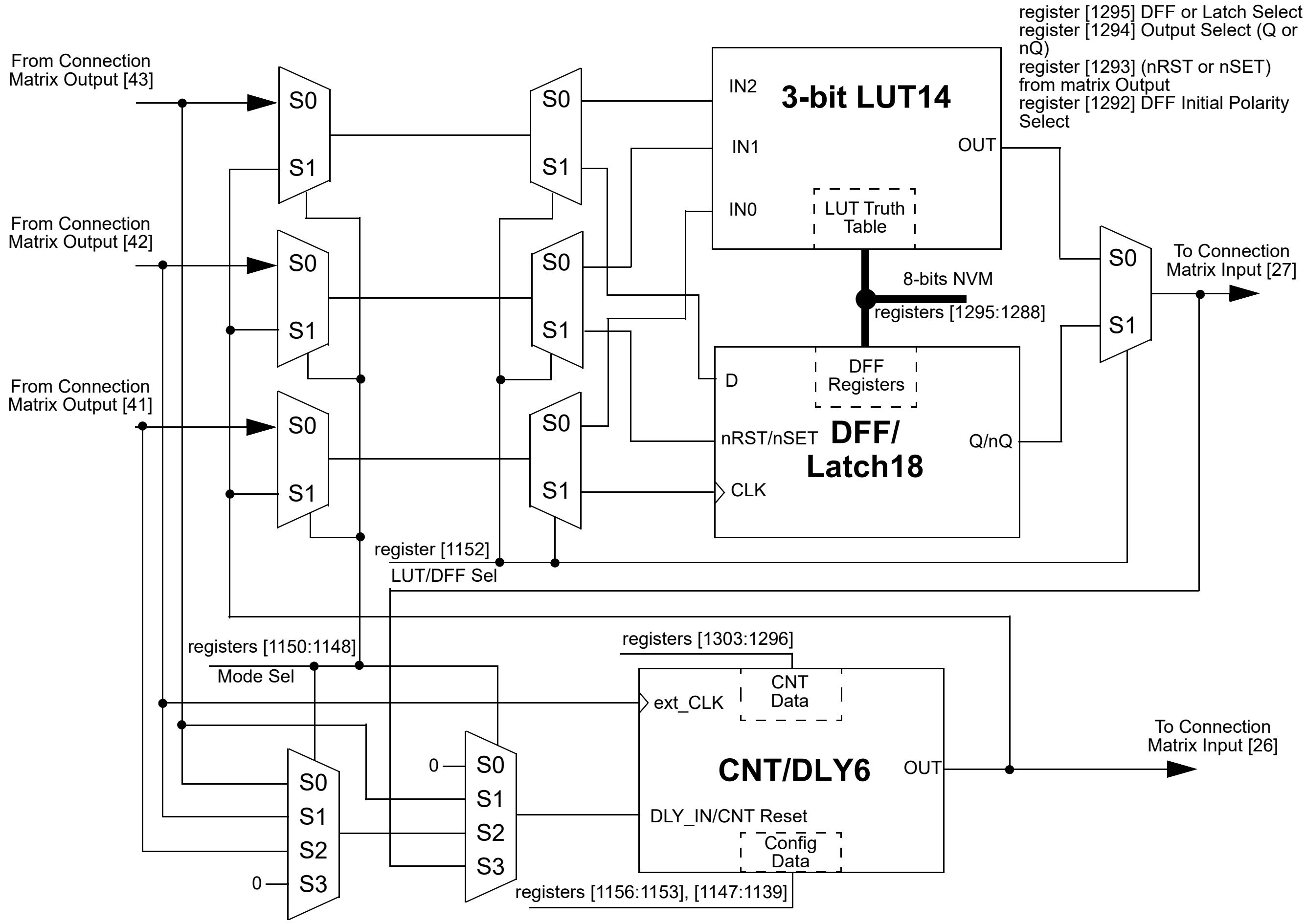

Figure 45: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT14/DFF18, CNT/DLY6)

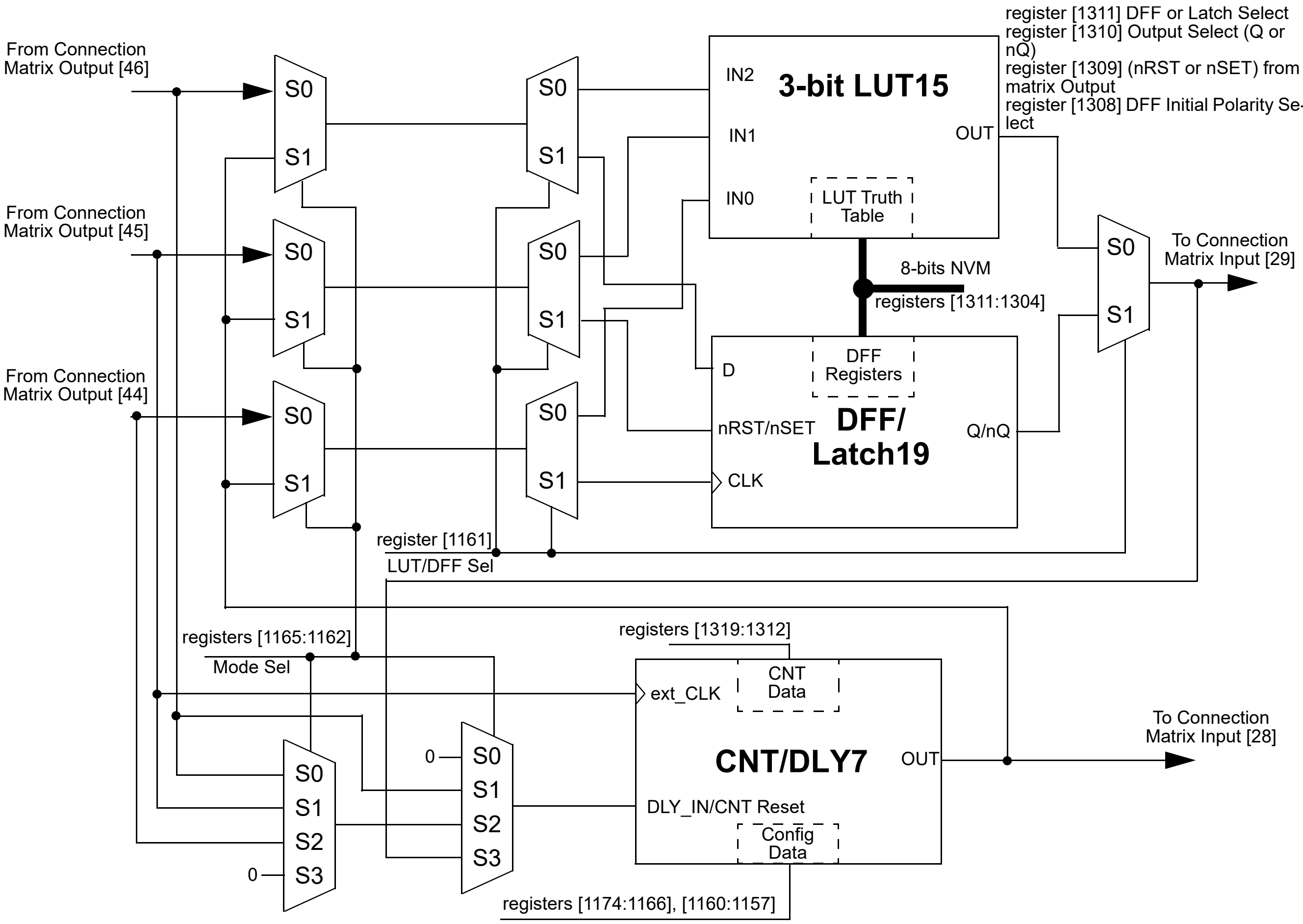

Figure 46: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT15/DFF19, CNT/DLY7)

As shown in Figures 24-30 there is a possibility to use LUT/DFF and CNT/DLY simultaneously.

Note: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter/Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CND/DLY's inputs (IN and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY. Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

8.1.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 45: 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1208]	LSB
0	0	1	register [1209]	
0	1	0	register [1210]	
0	1	1	register [1211]	
1	0	0	register [1212]	
1	0	1	register [1213]	
1	1	0	register [1214]	
1	1	1	register [1215]	MSB

Table 46: 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1224]	LSB
0	0	1	register [1225]	
0	1	0	register [1226]	
0	1	1	register [1227]	
1	0	0	register [1228]	
1	0	1	register [1229]	
1	1	0	register [1230]	
1	1	1	register [1231]	MSB

Table 47: 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1240]	LSB
0	0	1	register [1241]	
0	1	0	register [1242]	
0	1	1	register [1243]	
1	0	0	register [1244]	
1	0	1	register [1245]	
1	1	0	register [1246]	
1	1	1	register [1247]	MSB

Table 48: 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1256]	LSB
0	0	1	register [1257]	
0	1	0	register [1258]	
0	1	1	register [1259]	
1	0	0	register [1260]	
1	0	1	register [1261]	
1	1	0	register [1262]	
1	1	1	register [1263]	MSB

Table 49: 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1272]	LSB
0	0	1	register [1273]	
0	1	0	register [1274]	
0	1	1	register [1275]	
1	0	0	register [1276]	
1	0	1	register [1277]	
1	1	0	register [1278]	
1	1	1	register [1279]	MSB

Table 50: 3-bit LUT14 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1288]	LSB
0	0	1	register [1289]	
0	1	0	register [1290]	
0	1	1	register [1291]	
1	0	0	register [1292]	
1	0	1	register [1293]	
1	1	0	register [1294]	
1	1	1	register [1295]	MSB

Table 51: 3-bit LUT15 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1304]	LSB
0	0	1	register [1305]	
0	1	0	register [1306]	
0	1	1	register [1307]	
1	0	0	register [1308]	
1	0	1	register [1309]	
1	1	0	register [1310]	
1	1	1	register [1311]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT9 is defined by registers [1215:1208]

3-Bit LUT10 is defined by registers [1231:1224]

3-Bit LUT11 is defined by registers [1247:1240]

3-Bit LUT12 is defined by registers [1263:1256]

3-Bit LUT13 is defined by registers [1279:1272]

3-Bit LUT14 is defined by registers [1295:1288]

3-Bit LUT15 is defined by registers [1311:1304]

8.2 4-BIT LUT OR DFF/LATCH WITH 16-BIT COUNTER/DELAY MACROCELL

There is one macrocell that can serve as either 4-bit LUT/D Flip-Flops or as 16-bit Counter/Delay.

When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix.

When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

When used to implement 16-Bit Counter/Delay function, two of the four input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT Reset) for the Counter/Delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

This macrocell can also operate in a frequency detection or edge detection mode.

This macrocell can have its active count value read via I^2C. See Section 15.6.1 for further details.

Note: After two DFF – counters initialize with counter data = 0 after POR.
Initial state = 1 – counters initialize with counter data = 0 after POR.
Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

8.2.1 4-Bit LUT or DFF/LATCH with 16-Bit CNT/DLY Block Diagram

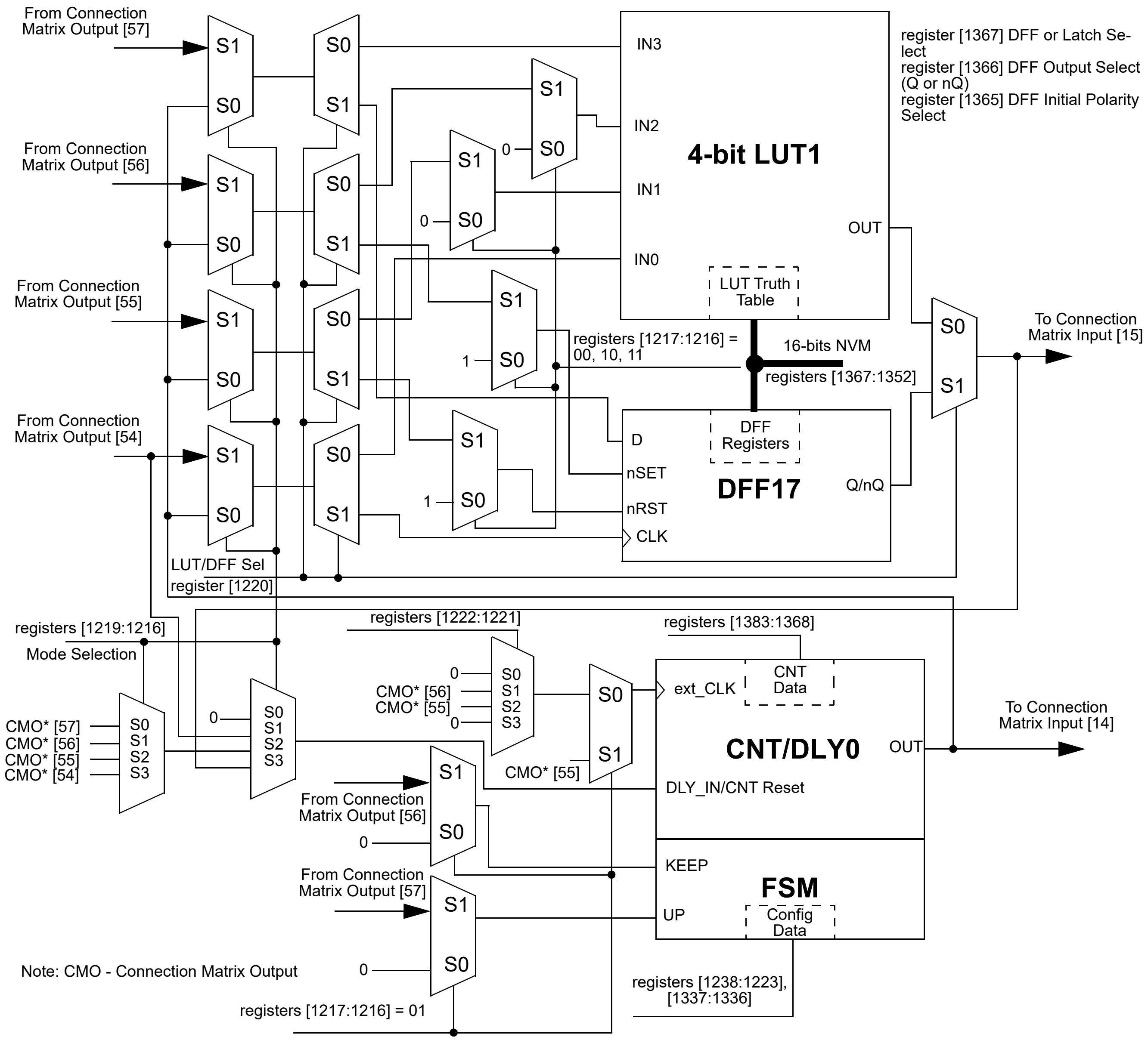

Figure 47: 4-bit LUT1 or CNT/DLY0

8.2.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Table 52: 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1176]	LSB
0	0	0	1	register [1177]	
0	0	1	0	register [1178]	
0	0	1	1	register [1179]	
0	1	0	0	register [1180]	
0	1	0	1	register [1181]	
0	1	1	0	register [1182]	
0	1	1	1	register [1183]	
1	0	0	0	register [1184]	
1	0	0	1	register [1185]	
1	0	1	0	register [1186]	
1	0	1	1	register [1187]	
1	1	0	0	register [1188]	
1	1	0	1	register [1189]	
1	1	1	0	register [1190]	
1	1	1	1	register [1191]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT1 is defined by registers [1191:1176]

Table 53: 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	1

8.3 CNT/DLY/FSM TIMING DIAGRAMS

8.3.1 Delay Mode CNT/DLY0 to CNT/DLY7

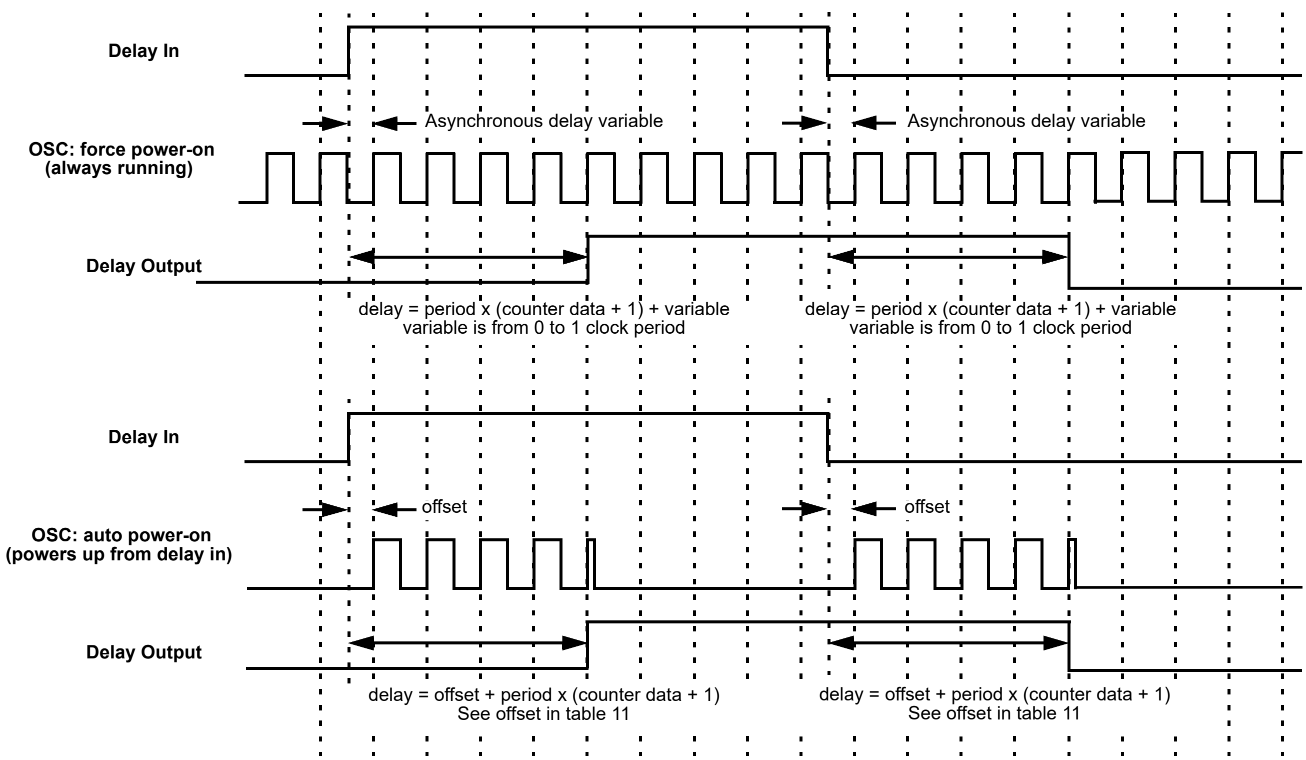

Figure 48: Delay Mode Timing Diagram, Edge Select: Both, Counter Data: 3

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter, if the input signal is shorter than the delay time.

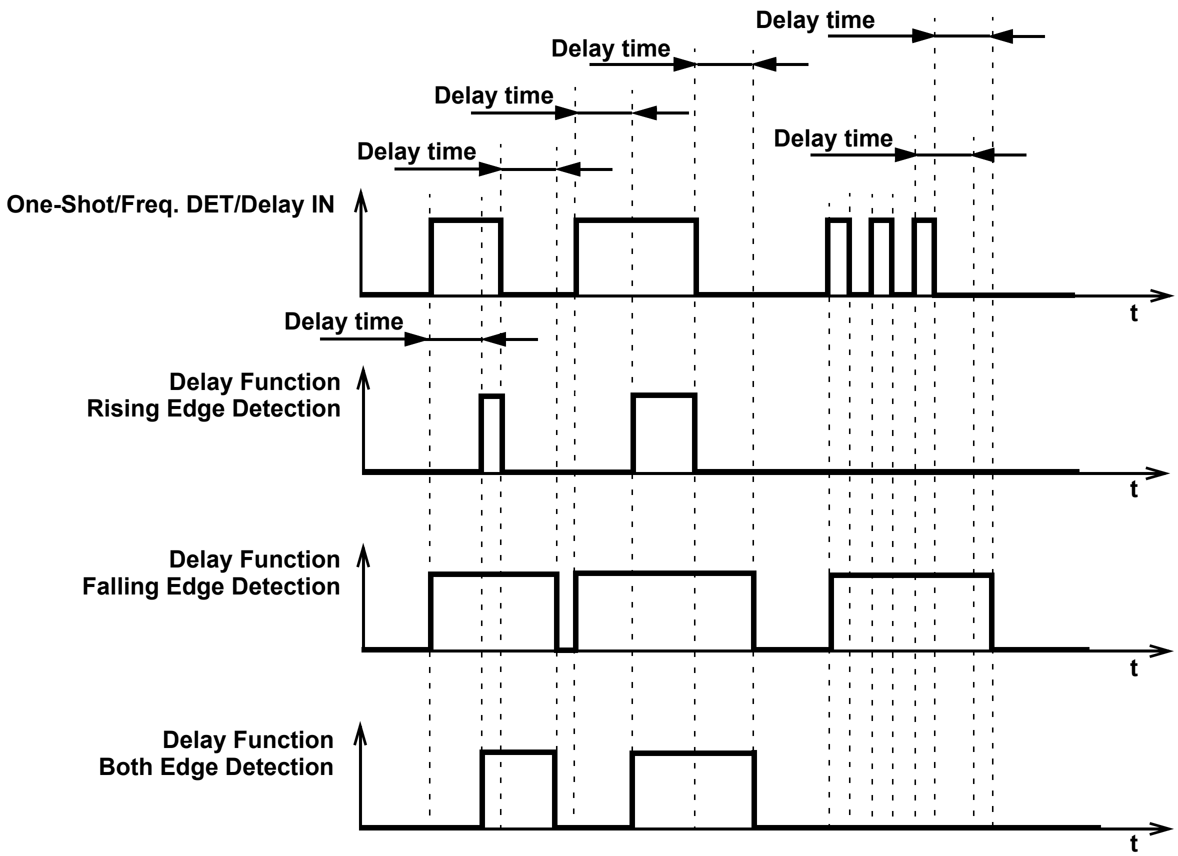

Figure 49: Delay Mode Timing Diagram for Different Edge Select Mode

8.3.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY0 to CNT/DLY7

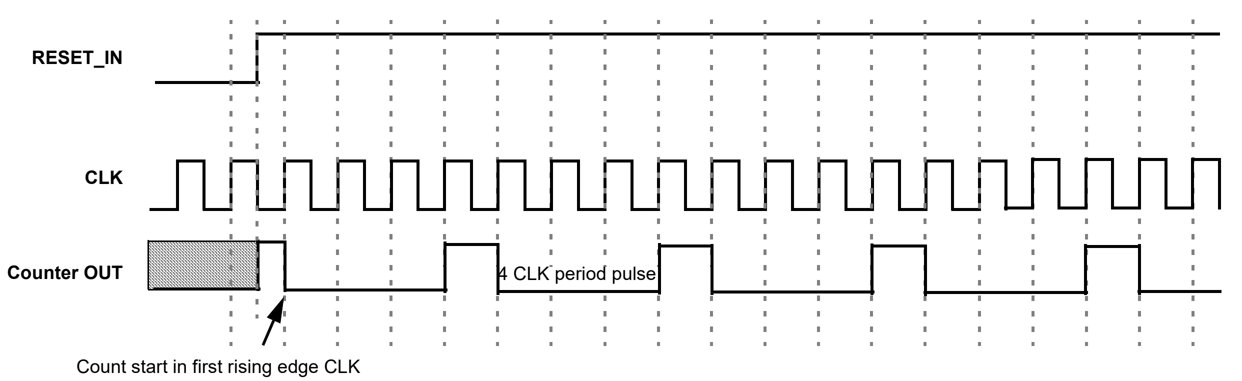

Figure 50: Counter Mode Timing Diagram without Two DFFs Synced Up

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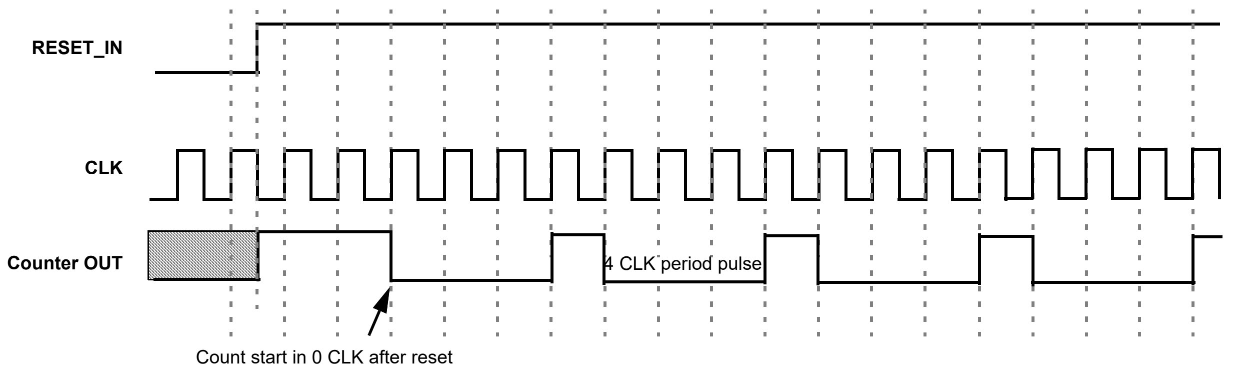


Figure 51: Counter Mode Timing Diagram with Two DFFs Synced Up

8.3.3 One-Shot Mode CNT/DLY0 to CNT/DLY7

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

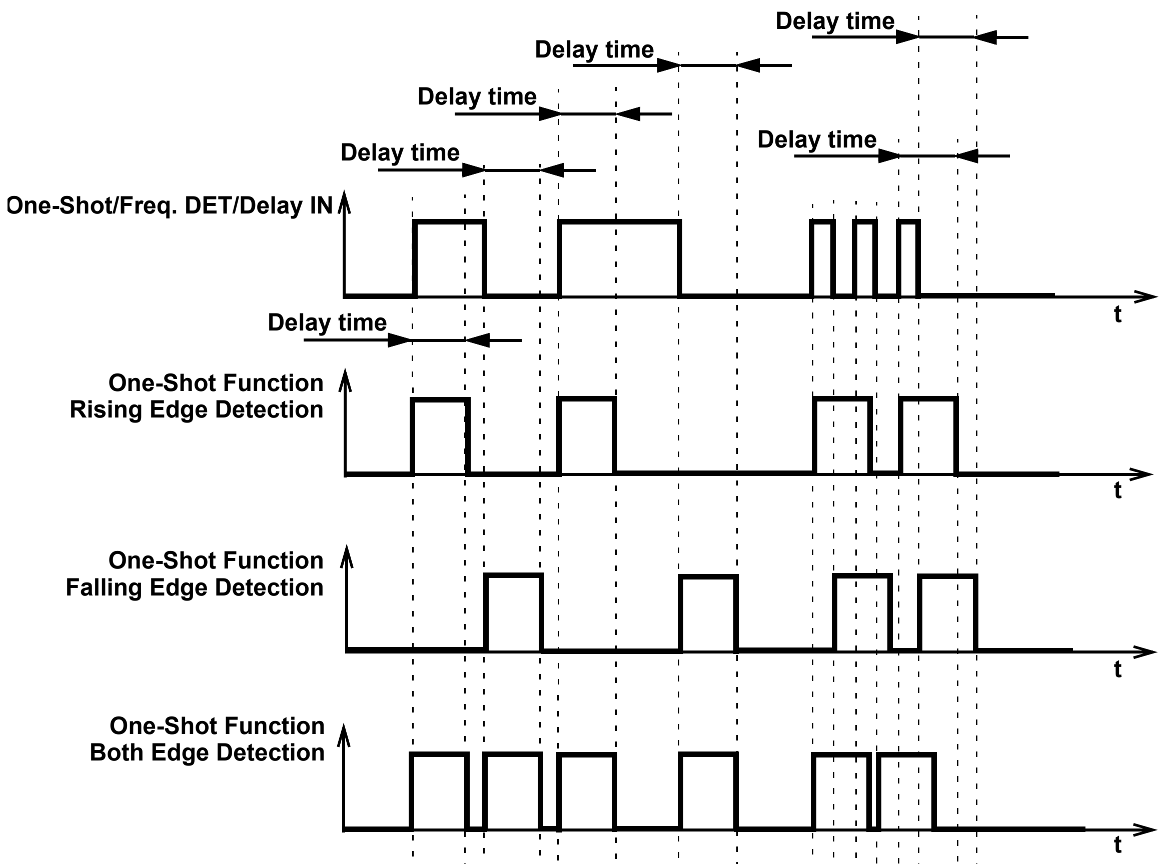


Figure 52: One-Shot Function Timing Diagram

This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

8.3.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY7

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

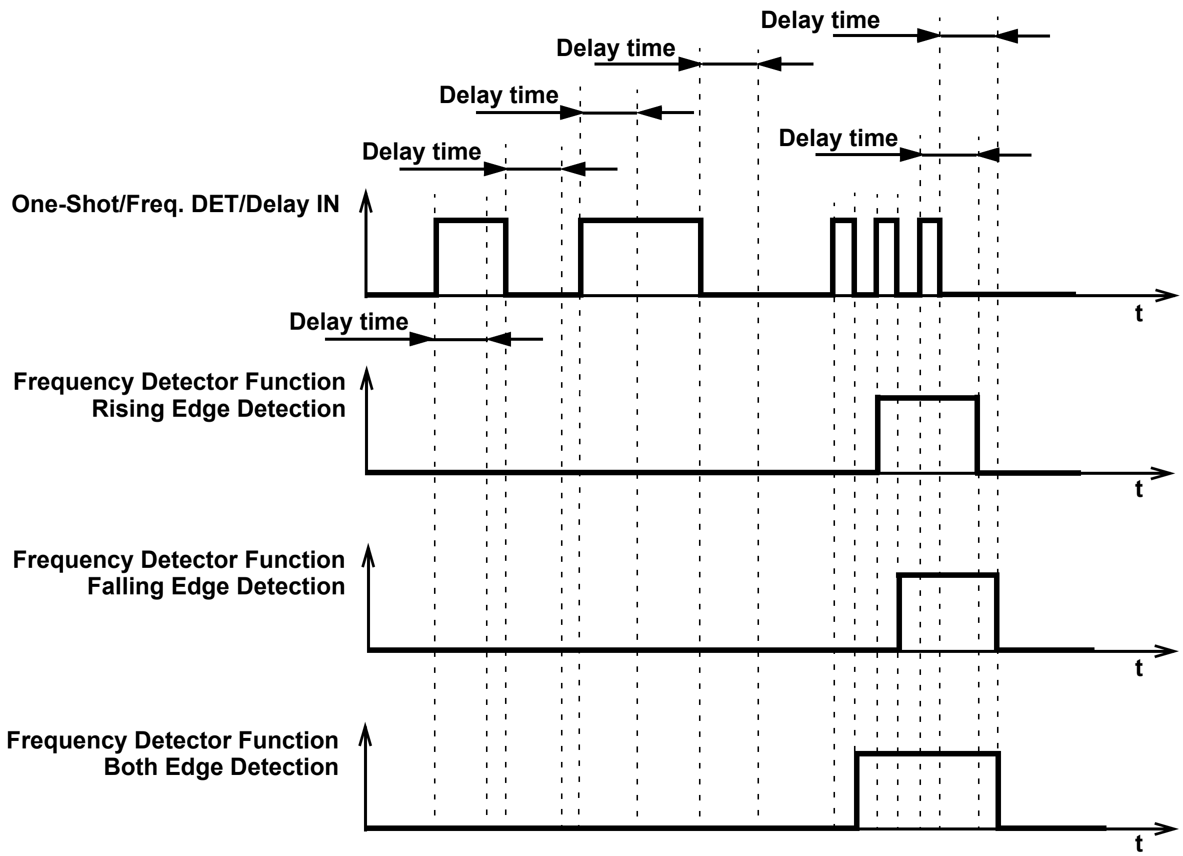


Figure 53: Frequency Detection Mode Timing Diagram

8.3.5 Edge Detection Mode CNT/DLY1 to CNT/DLY7

The macrocell generates high level short pulse when detecting the respective edge. See Table 12.

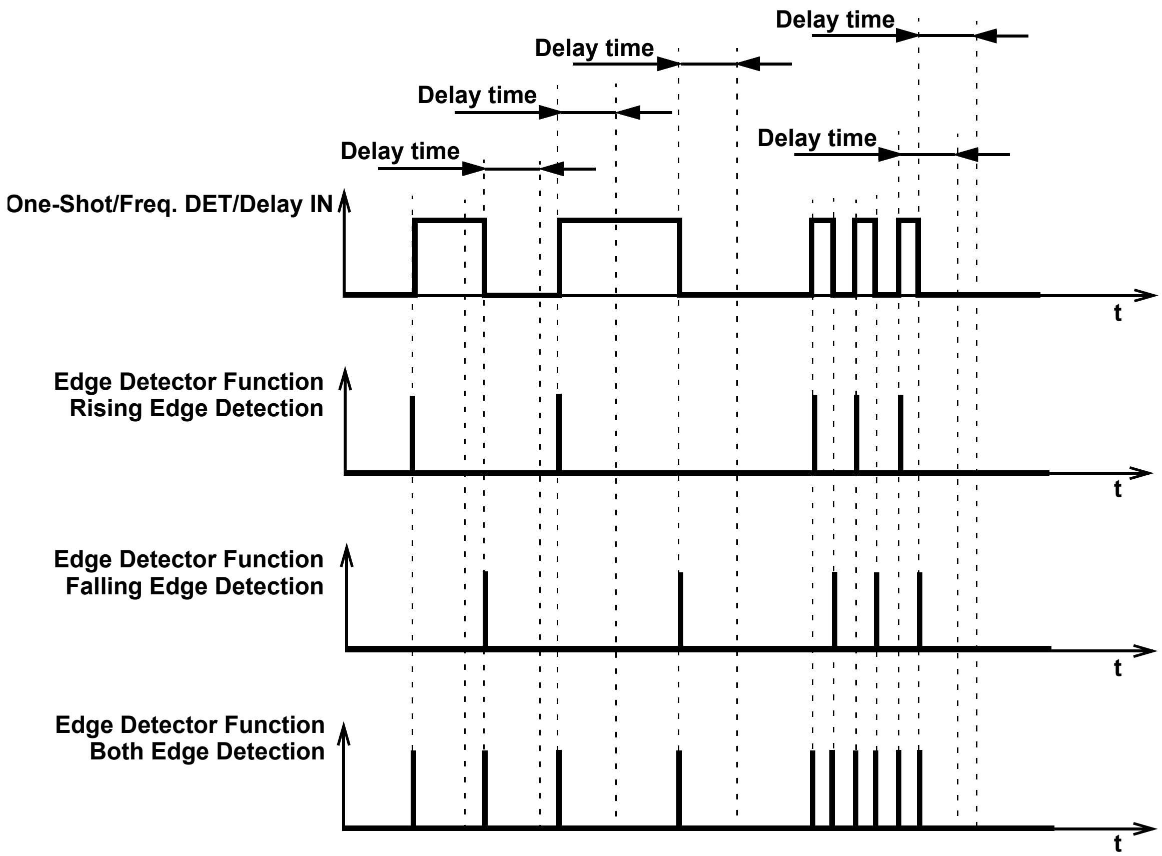


Figure 54: Edge Detection Mode Timing Diagram

8.3.6 Delayed Edge Detection Mode CNT/DLY0 to CNT/DLY7

In Delayed Edge Detection Mode, High level short pulses are generated on the macrocell output after the configured delay time, if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See Figure 55.

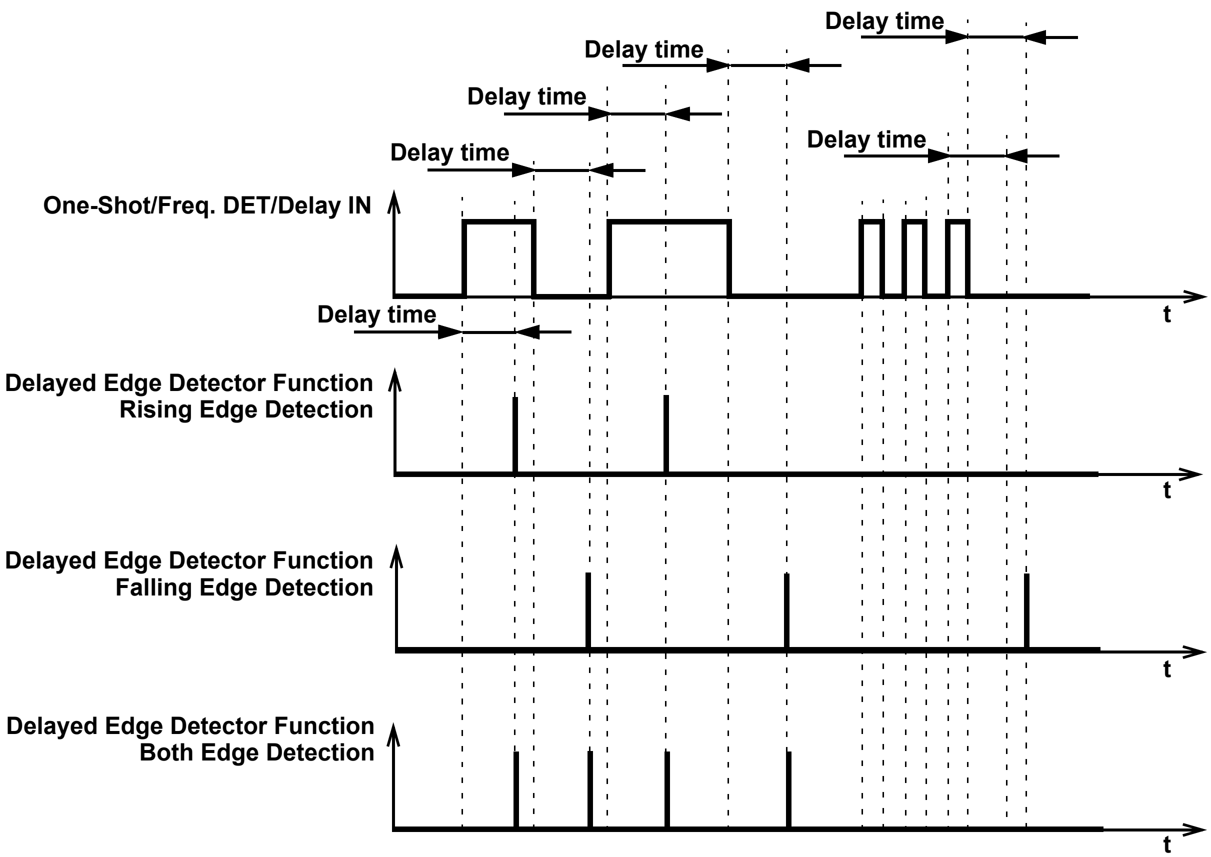


Figure 55: Delayed Edge Detection Mode Timing Diagram

8.3.7 CNT/FSM Mode CNT/DLY0

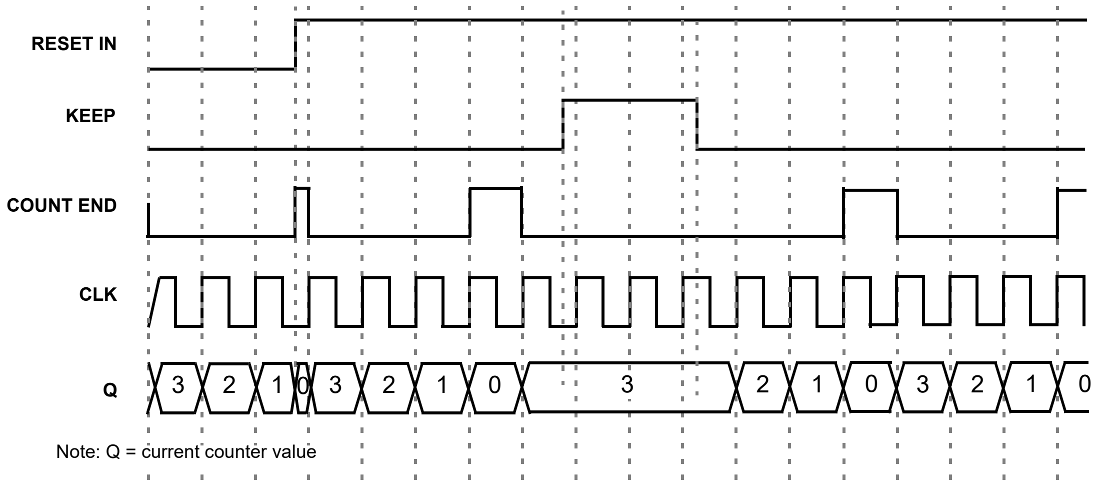


Figure 56: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

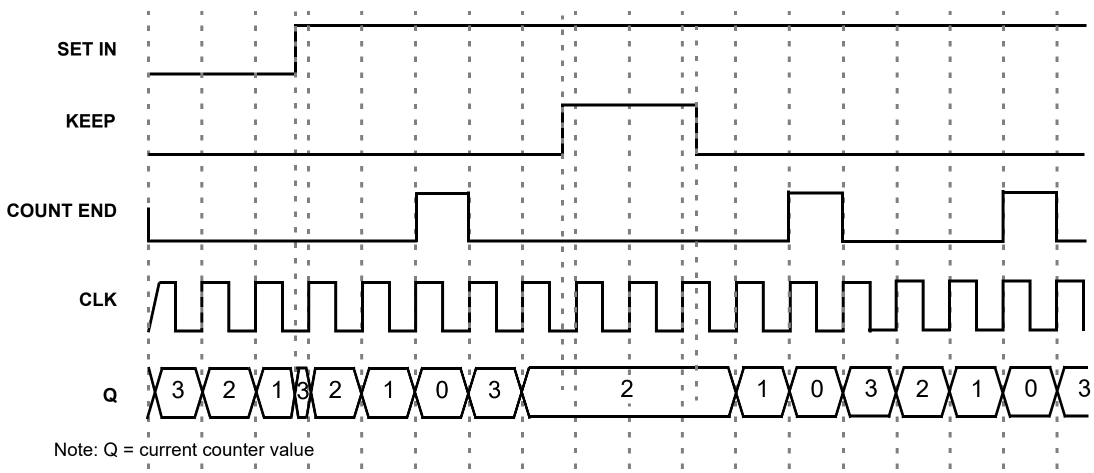


Figure 57: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

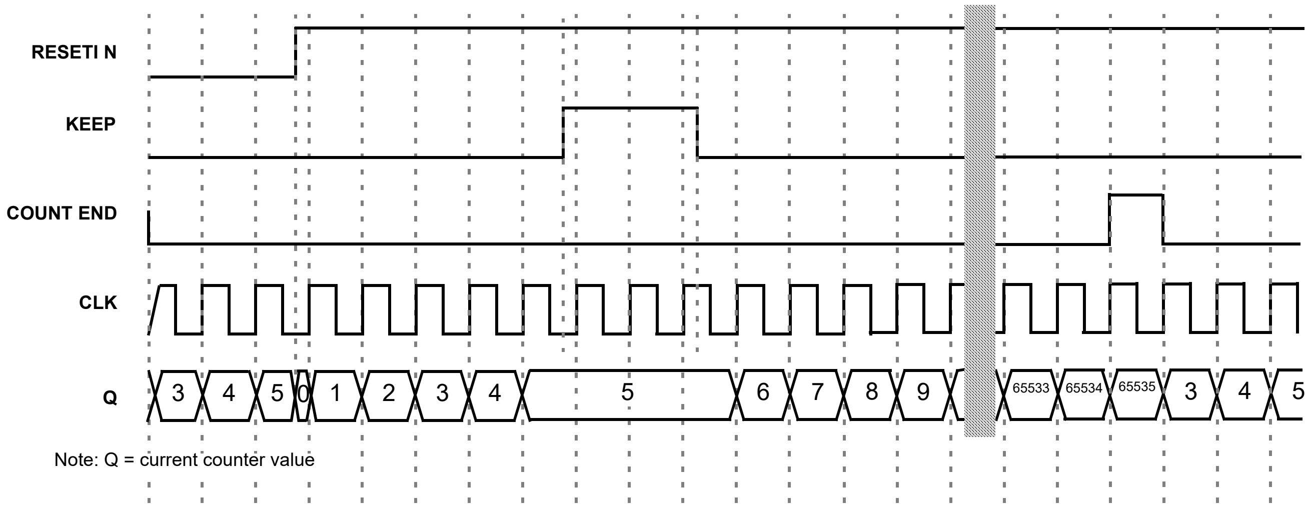


Figure 58: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

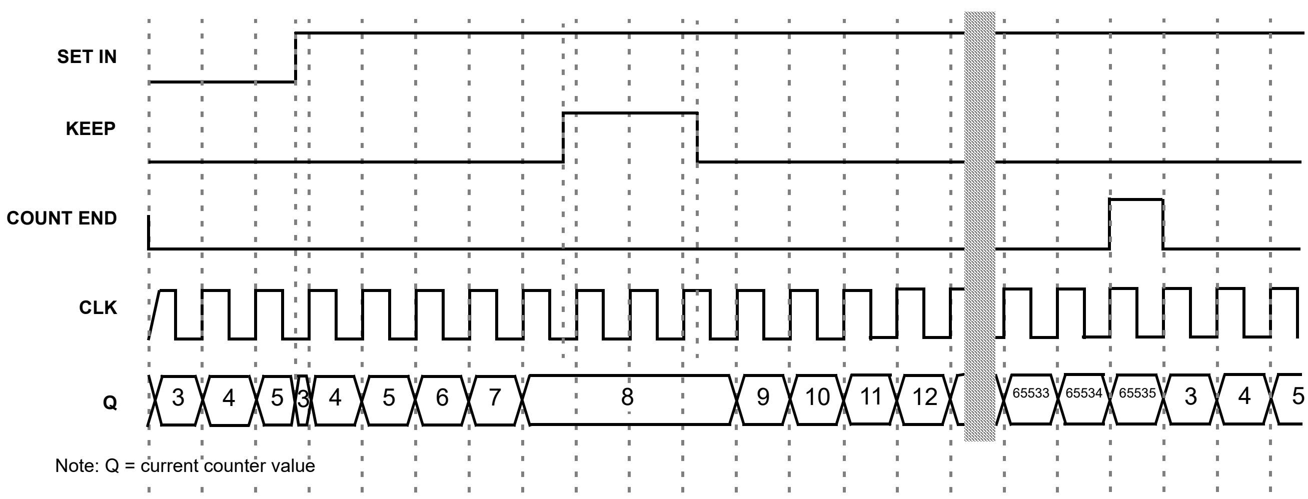


Figure 59: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator Is Forced On, UP = 1) for Counter Data = 3

8.3.8 Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. The counter value is shifted for two rising edges of the clock signal in Delay/One-Shot/Frequency Detect modes compared to Counter mode. See Figure 60:

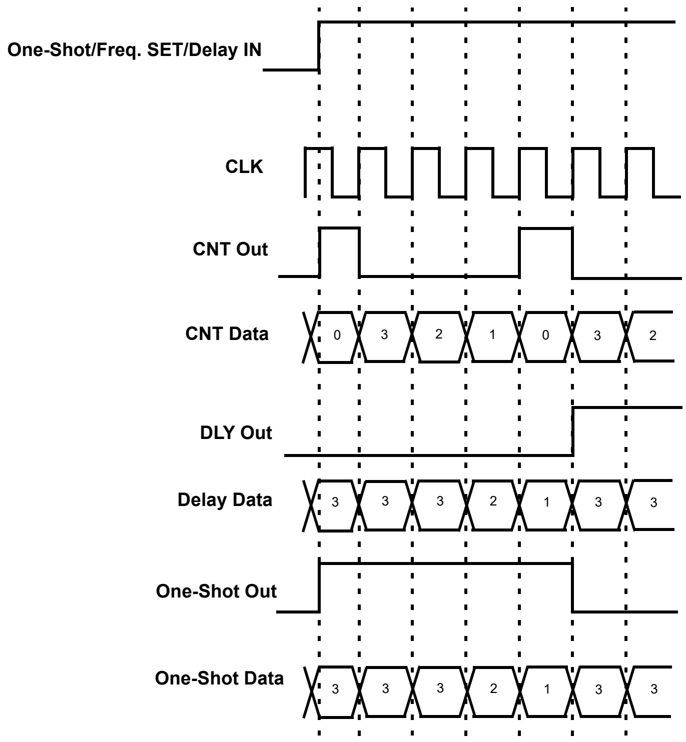


Figure 60: Counter Value, Counter Data = 3

8.4 WAKE AND SLEEP CONTROLLER

The SLG46855-A has a Wake and Sleep function for all ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose registers [1032:1031] = 11 and register [1046] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

Note 1: BG/Analog_Good time is long and should be considered in wake and sleep timing in case it dynamically powers on/off.

Note 2: Wake time should be long enough to make sure ACMP and Vref have enough time to get a sample before going to sleep.

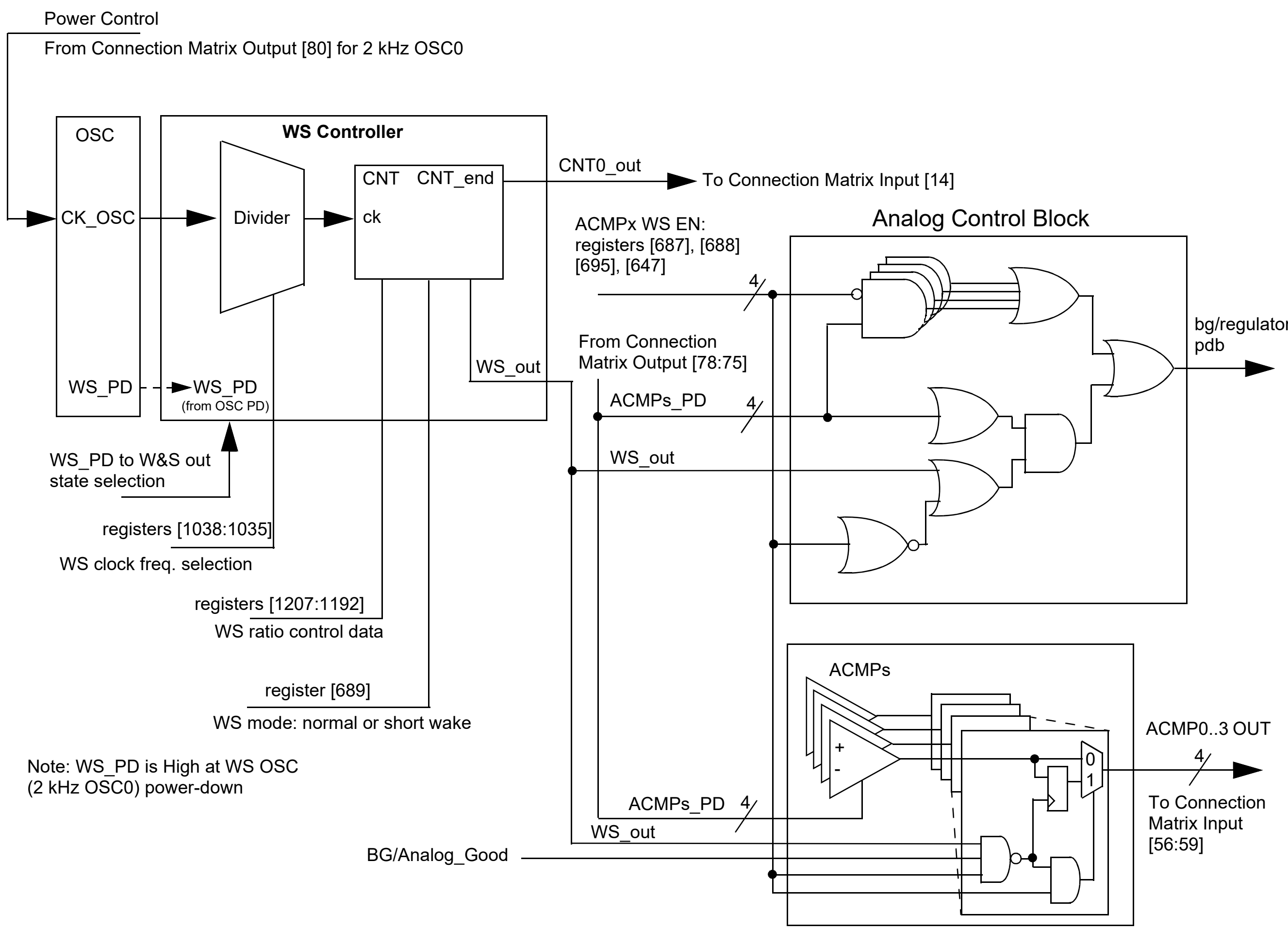


Figure 61: Wake/Sleep Controller

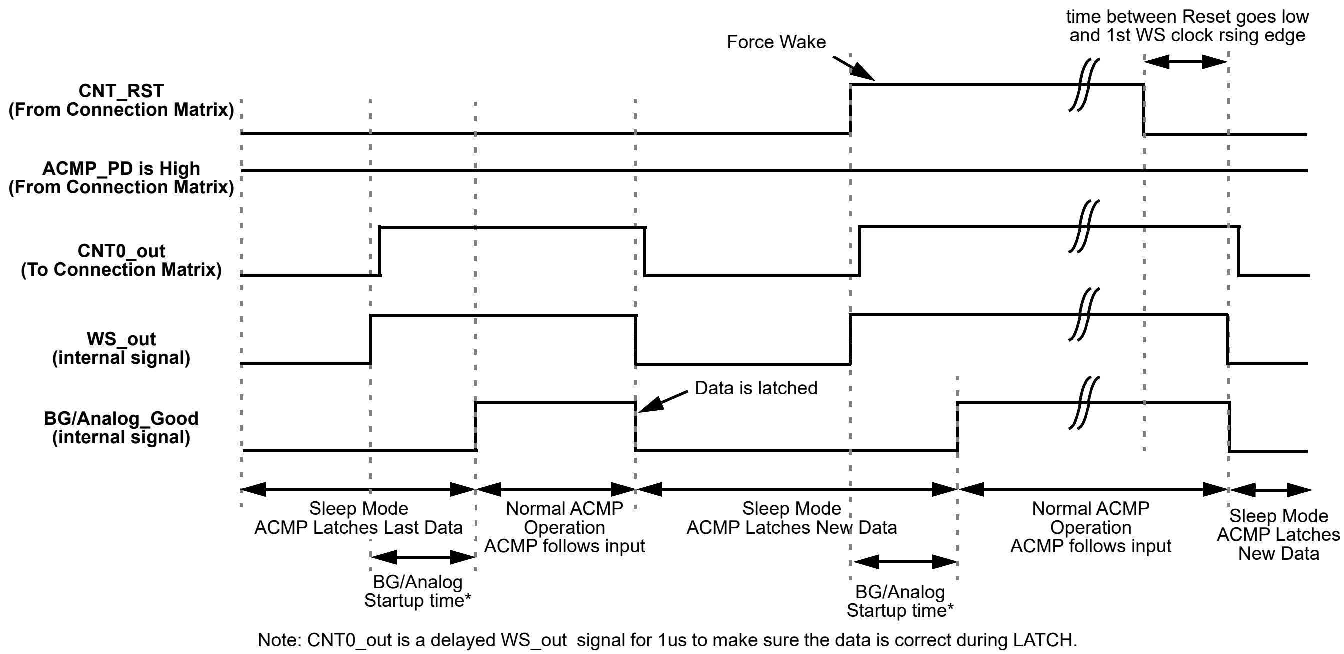


Figure 62: Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Reset is Used

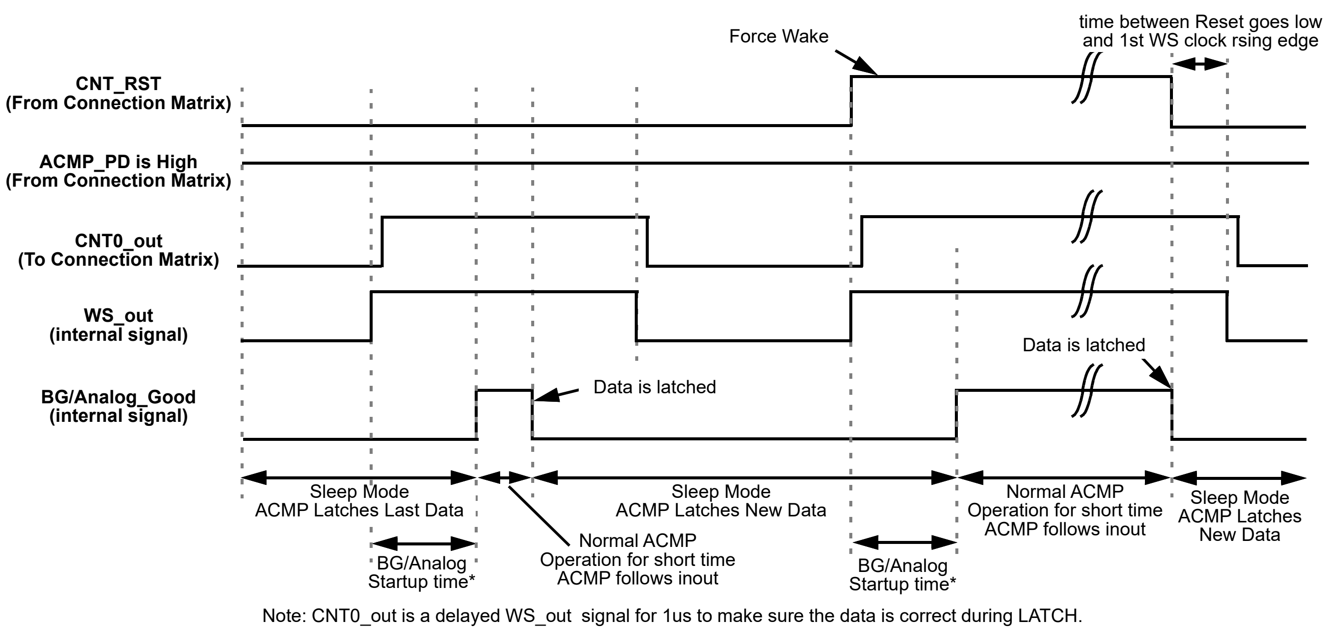


Figure 63: Wake/Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used

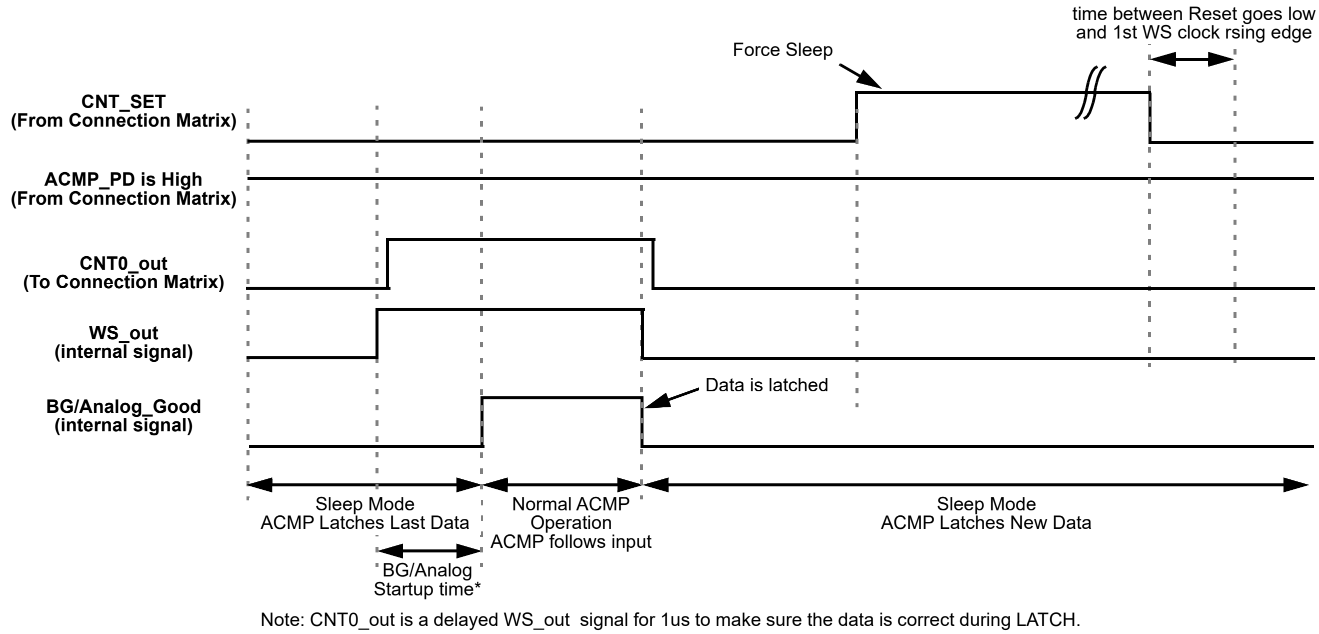


Figure 64: Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used

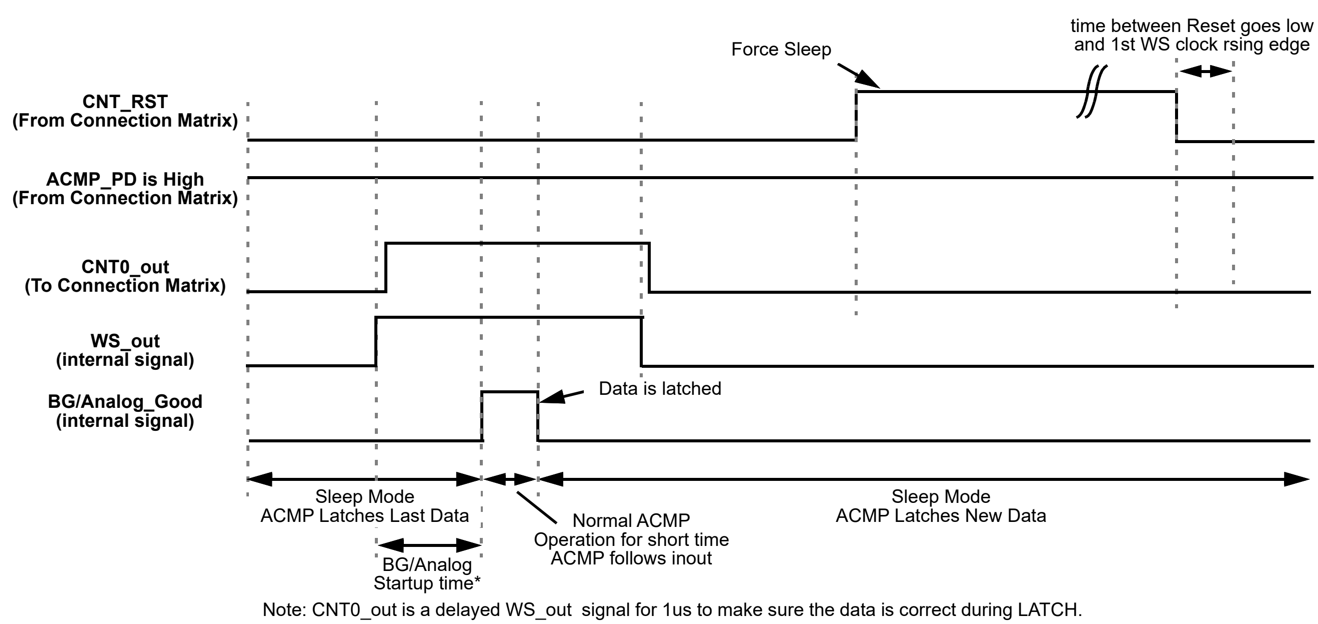


Figure 65: Wake/Sleep Timing Diagram, Short Wake Mode, Counter Set is Used

Note: If low power BG is powered on/off by WS, the wake time should be longer than 2.1 ms. The BG/analog start up time will take maximal 2 ms. Therefore, 8 periods of the Oscillator0 is recommended for the wake time, when BG is configured to Auto Power mode. If low power BG is always on, Oscillator0 period is longer than required wake time. The BG/analog start up time will take maximal 450 us for ACMP0/1 and a shorter time for ACMP2/3. The short wake mode can be used to reduce the current consumption.

To use any ACMP under WS controller, the following settings must be done:

- ACMP Power Up Input from matrix = 1 (for each ACMP separately);
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMP);
- Register WS → enable (for each ACMP separately);
- CNT/DLY0 set/reset input = 0 (for all ACMP).

The user can select a period of time while the ACMP is sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched, so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)
  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on.
  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off.
  Both cases WS function is turned off.

- Counter Data (Range: 1 - 65535)
  User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn on the ACMPs. When Reset signal goes out, the WS counter will go Low and turn off the ACMP until the counter counts up to the end. Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn off the ACMP. When Set signal goes out, the WS counter will go on counting and High level signal will turn on the ACMP while counter is counting up to the end.

Note: The OSC0 matrix power-down to control ACMP WS is not supported for short wait time option.

- Edge Select defines the edge for Q mode
  High level Set/Reset - switches mode Set/Reset when level is High

Note: Q mode operates only in case of "High Level Set/Reset”.

- Wake time selection - time required for wake signal to turn the ACMPxH on

  Normal Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.

  Short Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on for 1 μs and turn off regardless of WS signal. The WS signal width does not matter.

- Keep - pauses counting while Keep = 1
- Up - reverses counting
  If Up = 1, CNT is counting up from user selected value to 65535.

  If Up = 0, CNT is counting down from user selected value to 0.

9 Analog Comparators

There are two High Speed and two Low Power Rail-to-Rail General Purpose Analog Comparators (ACMP) macrocells in the SLG46855-A. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0H PWR UP, ACMP1H PWR UP, ACMP2L PWR UP, and ACMP3L PWR UP) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be ON continuously, OFF continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, its output is low.

Two of the four General Purpose Analog Comparators are optimized for high speed operation (ACMP0H and ACMP1H), and two other are optimized for low power operation (ACMP2L and ACMP3L).

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage (1x, 0.5x, 0.33x, 0.25x) before connection to the analog comparator. The gain divider is unbuffered and has input resistance of 2 MΩ (typ) for 0.5x, 0.33x, 0.25x, and 10 GΩ for 1x. Each of the ACMP cells has a negative input signal that is either created from an internal Vref or provided by any external source (GPIO2 and GPO0). Note that the external Vref signal is filtered with a 2nd order low pass filter with 8 kHz typical bandwidth, see Figure 66 to Figure 69.

Input bias current < 1 nA (typ).

PWR UP = 1 => ACMP is powered up.

PWR UP = 0 => ACMP is powered down.

During power-up, the ACMP output will remain LOW, and then becomes valid in 37 µs (max) after power up signal goes high for ACMP0H and ACMP1H, and becomes valid 294 µs (max) after power up signal goes high for ACMP2L and ACMP3L.

Each High Speed ACMP (ACMP0H and ACMP1H) has an optional Rail-to-Rail Input Buffer, which can be used along with the Gain divider to increase ACMP input resistance. However, Input buffer will increase an input offset voltage.

Each cell also has a hysteresis selection, to offer hysteresis of (0, 32, 64, 192) mV. The hysteresis option is available when using an internal Vref only.

The ACMP0H has an additional option of connecting an internal 100 µA current source to its positive input, register [690]. It is also possible to connect the 100 µA current source to each next ACMP via an internal analog MUX.

ACMP0H IN+ options are GPIO4, buffered GPIO4, V_{DD}, 100 µA Current Source
ACMP1H IN+ options are GPIO5, buffered GPIO5, ACMP0H IN+ MUX output
ACMP2L IN+ options are GPIO6, ACMP0H IN+ MUX output, ACMP1H IN+ MUX output
ACMP3L IN+ options are GPIO7, ACMP2L IN+ MUX output, Temp Sensor OUT

9.1 ACMP0H BLOCK DIAGRAM

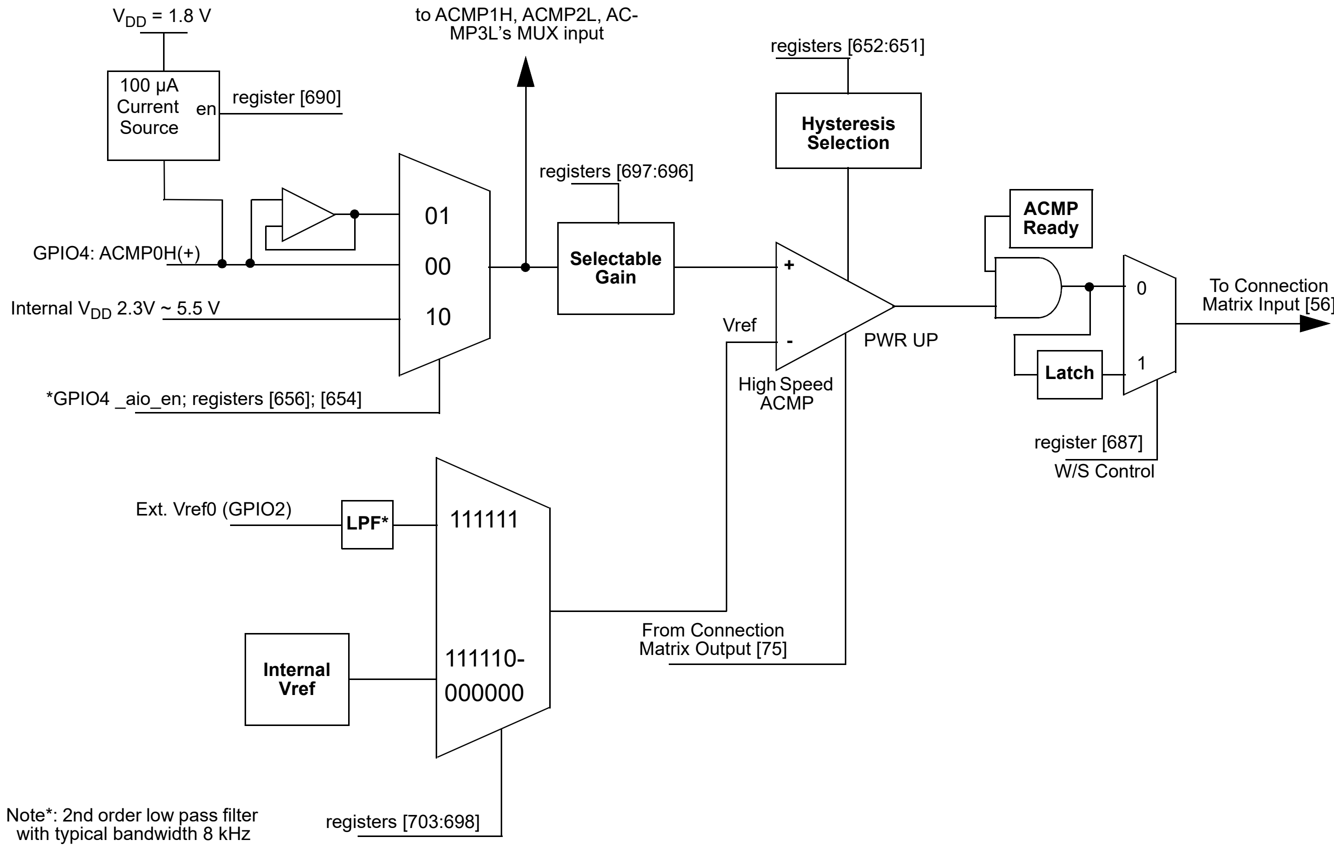


Figure 66: ACMP0H Block Diagram

9.2 ACMP1H BLOCK DIAGRAM

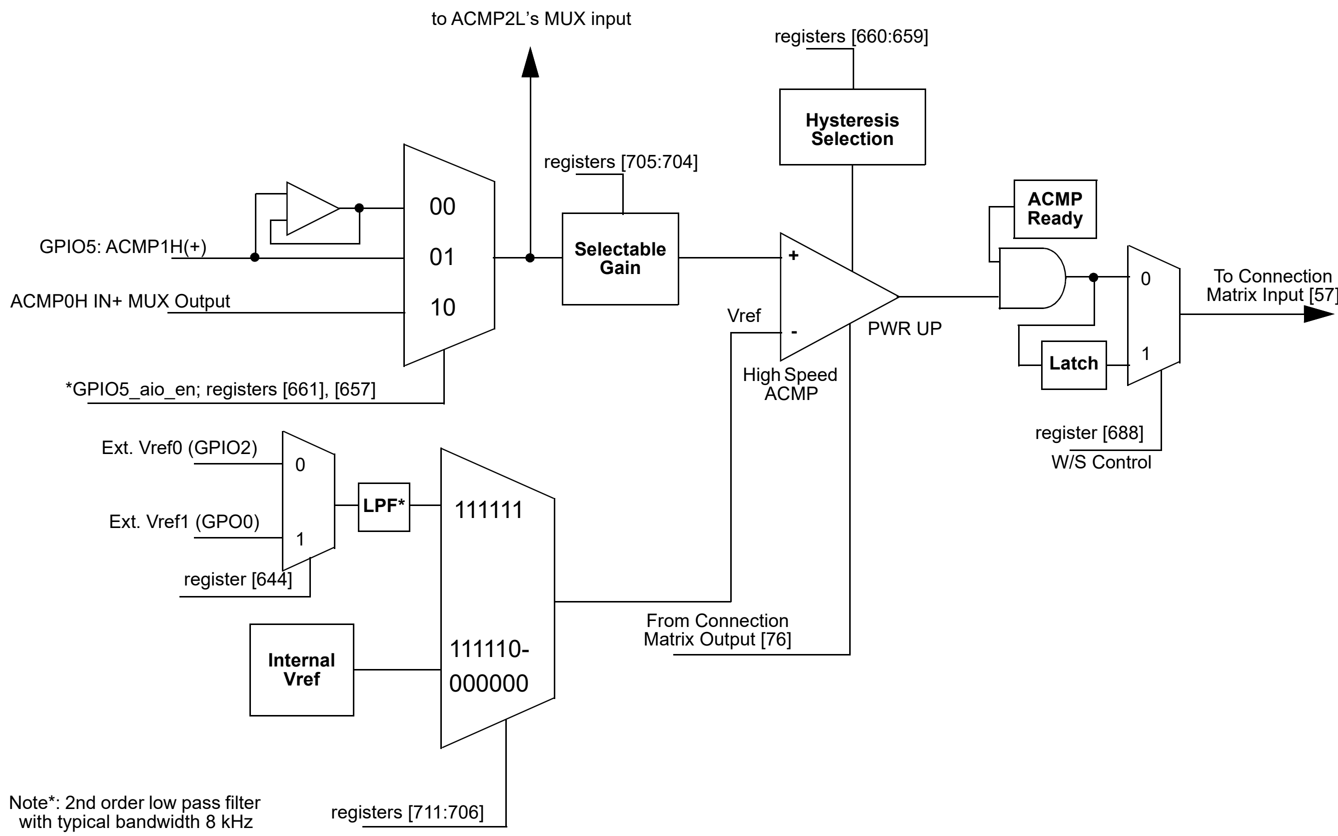


Figure 67: ACMP1H Block Diagram

9.3 ACMP2L BLOCK DIAGRAM

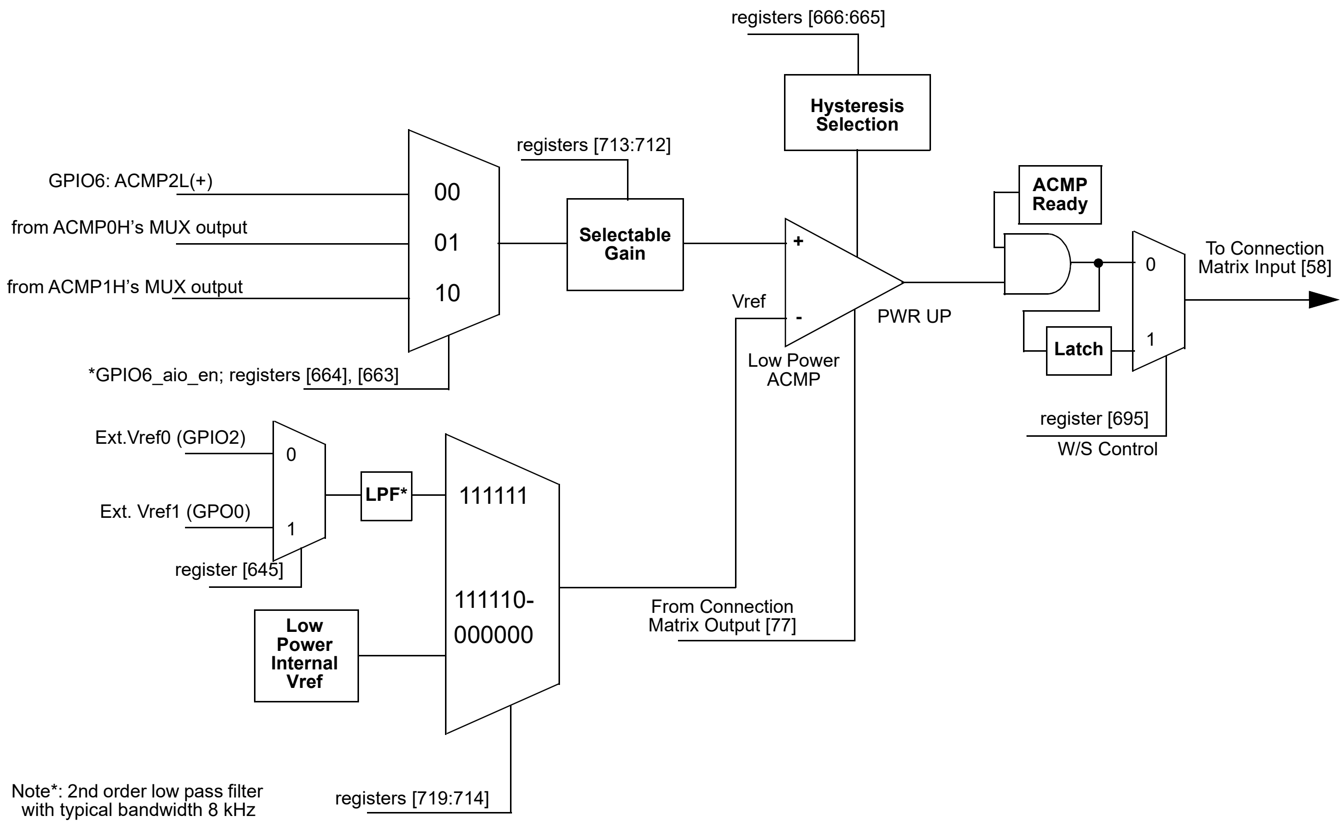


Figure 68: ACMP2L Block Diagram

9.4 ACMP3L BLOCK DIAGRAM

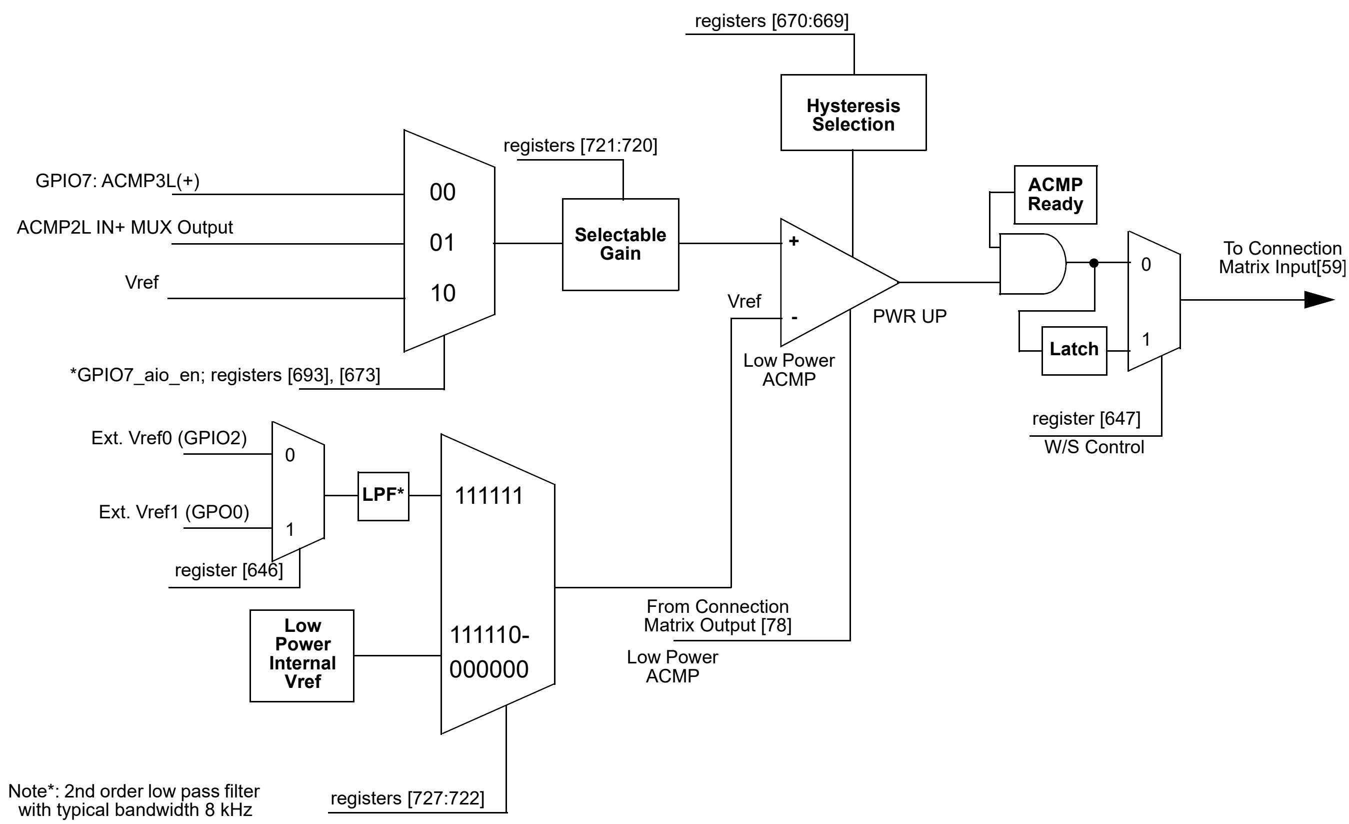


Figure 69: ACMP3L Block Diagram

9.5 ACMP TYPICAL PERFORMANCE

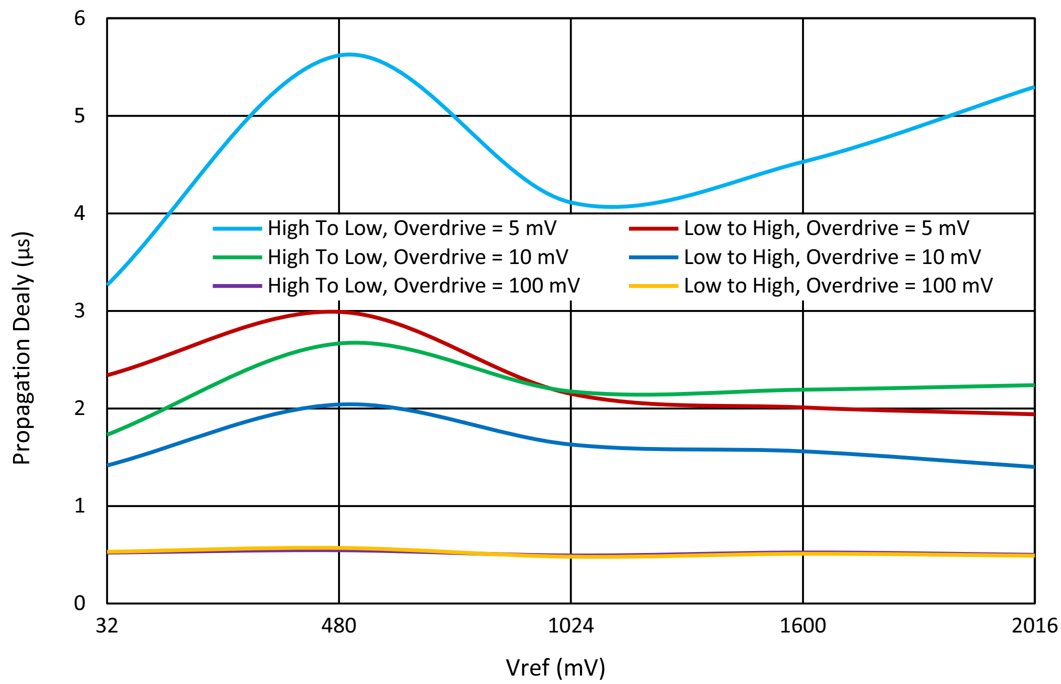


Figure 70: Typical Propagation Delay vs. Vref for ACMPxH at T = 25 °C, Gain = 1, Hysteresis = 0

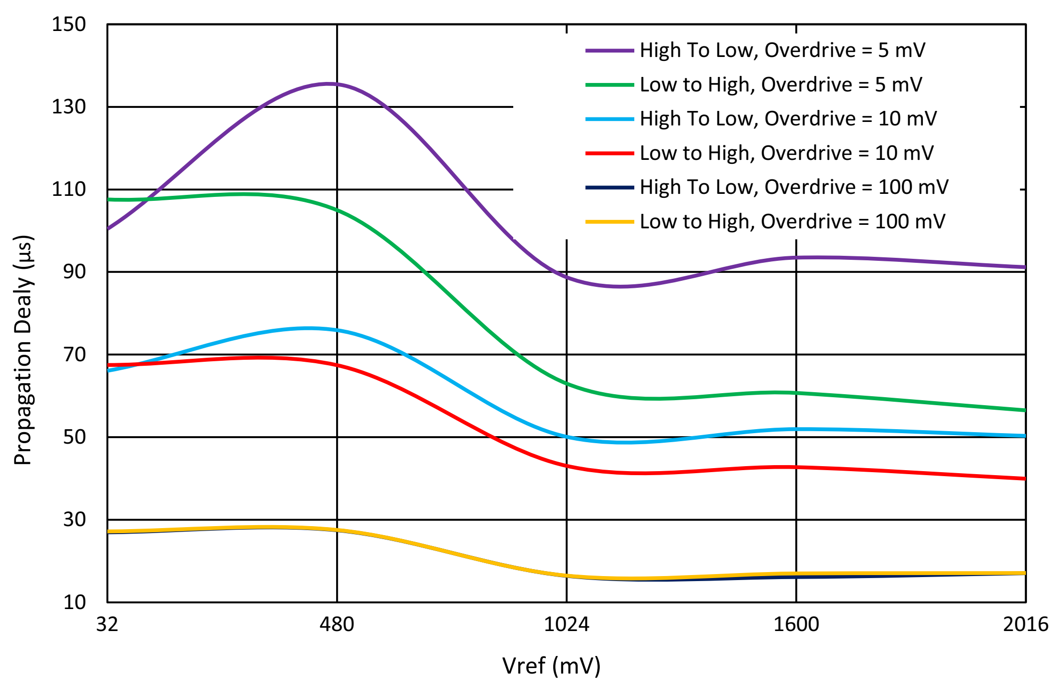


Figure 71: Typical Propagation Delay vs. Vref for ACMPxL at T = 25 °C, Gain = 1, Hysteresis = 0

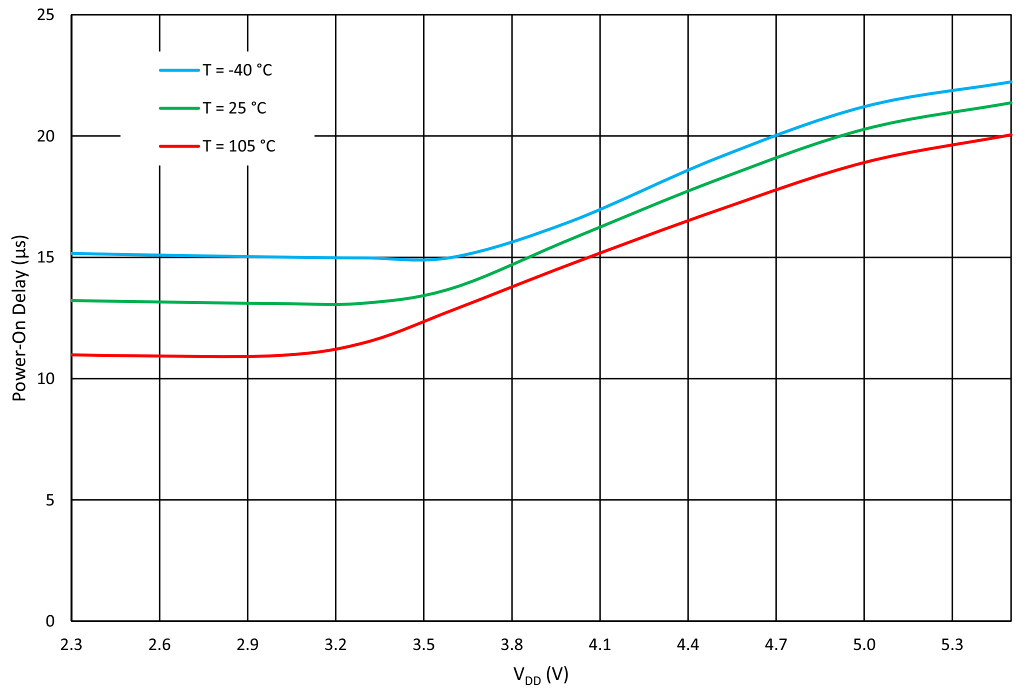


Figure 72: ACMPxH Power-On Delay vs. V_{DD}

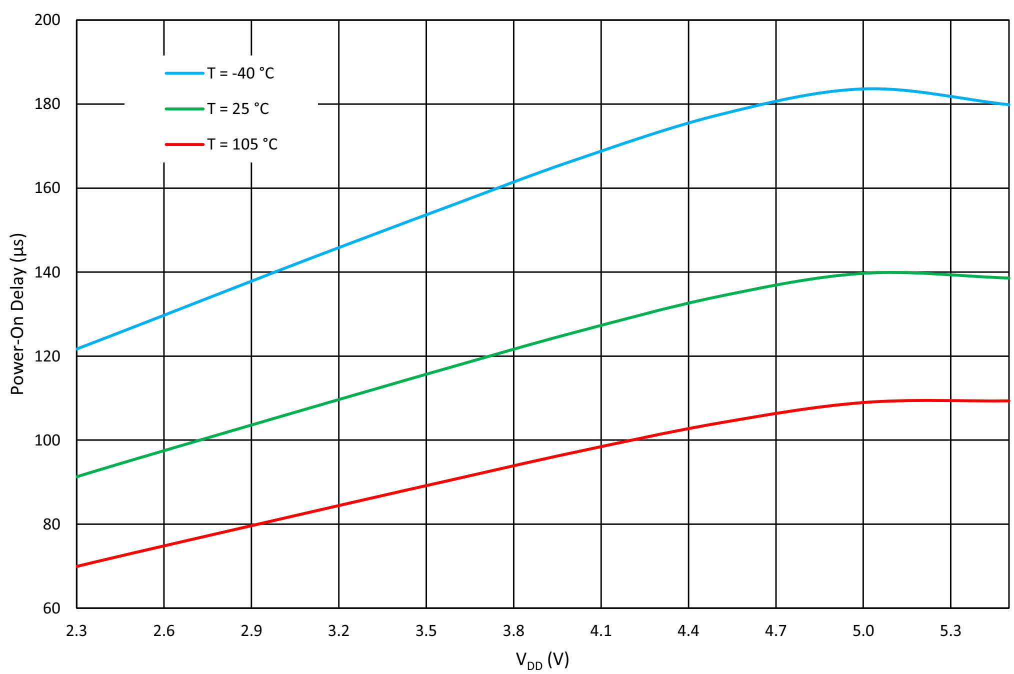


Figure 73: ACMPxL Power-On Delay vs. V_{DD}

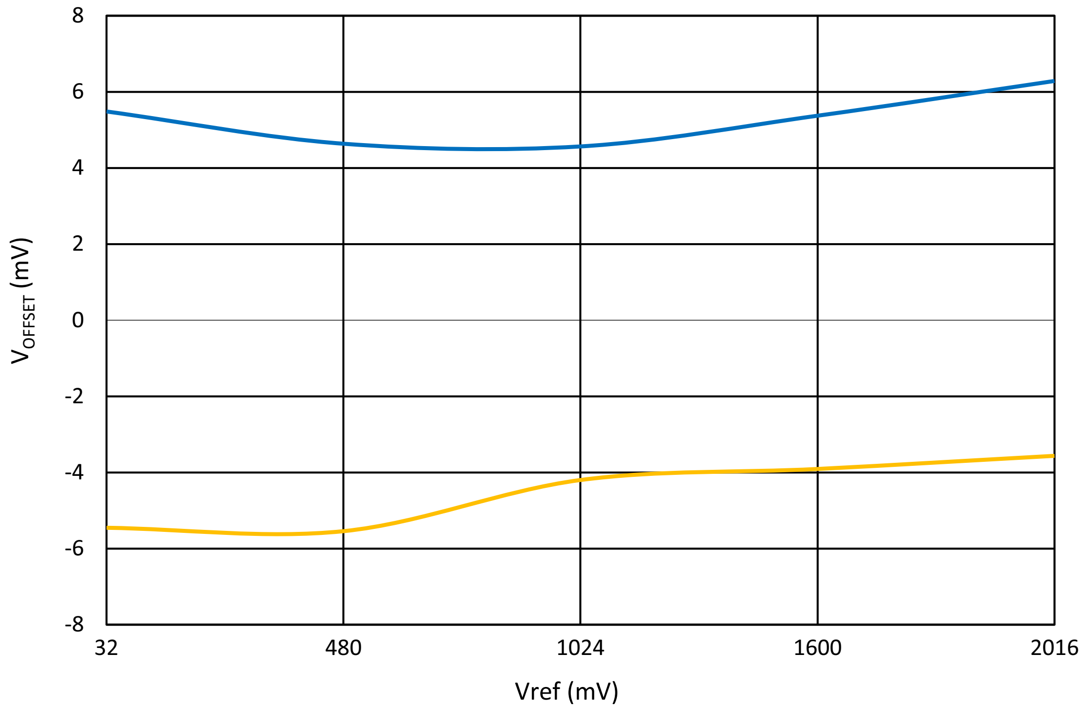


Figure 74: ACMPxH Input Offset Voltage vs. Vref at T = -40 °C to 105 °C

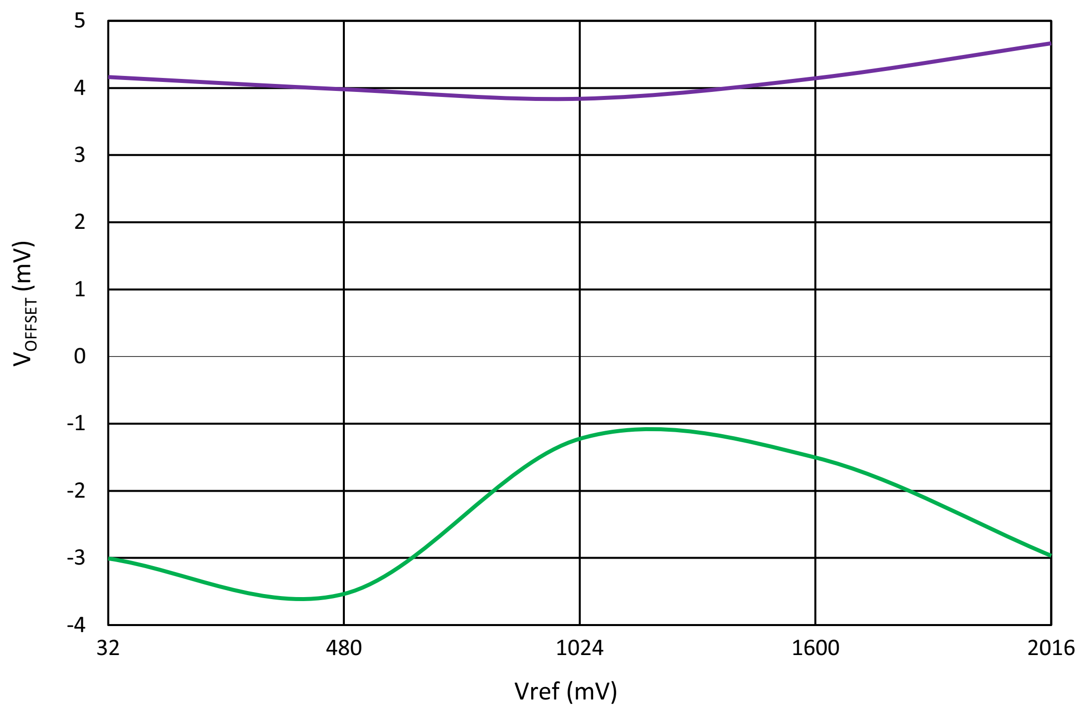


Figure 75: ACMPxL Input Offset Voltage vs. Vref at T = -40 °C to 105 °C

10 Programmable Delay/Edge Detector

The SLG46855-A has a programmable time delay logic cell that can generate a delay that is selectable from one of four timings (time2) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay, as well as glitch rejection during the delay period. See Figure 76 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

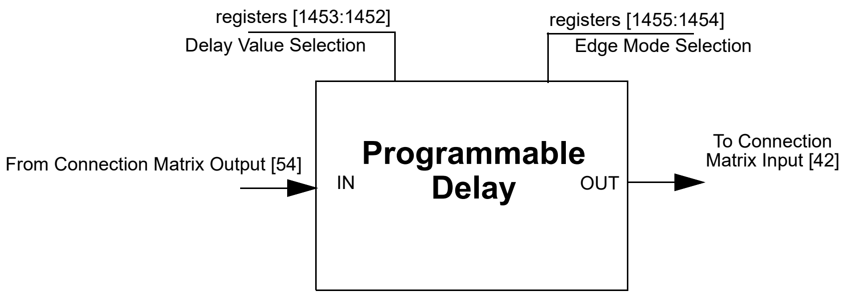


Figure 76: Programmable Delay

10.1 PROGRAMMABLE DELAY TIMING DIAGRAM - EDGE DETECTOR OUTPUT

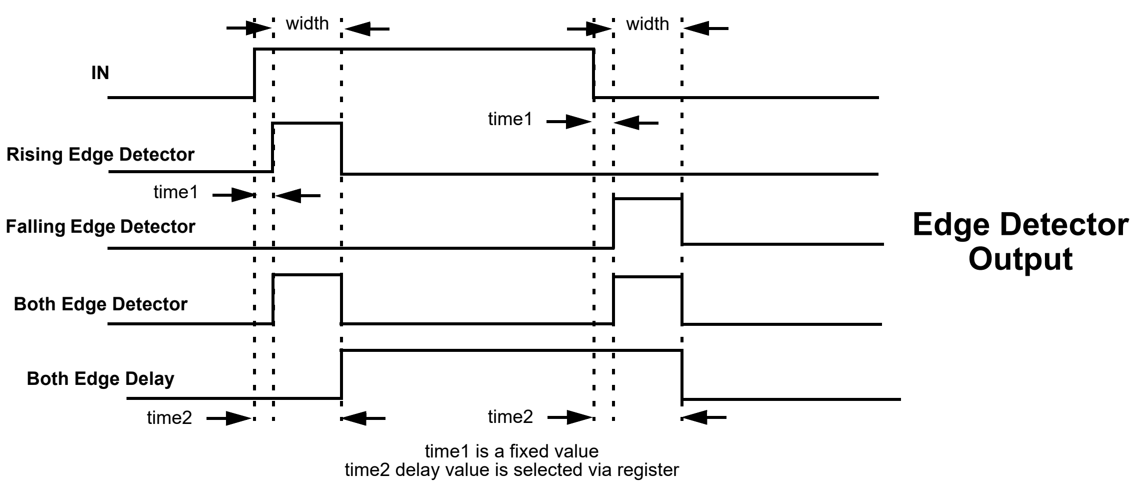


Figure 77: Edge Detector Output

Please refer to Table 12.

11 Additional Logic Function. Deglitch Filter

The SLG46855-A has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection Matrix inputs and outputs. In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay

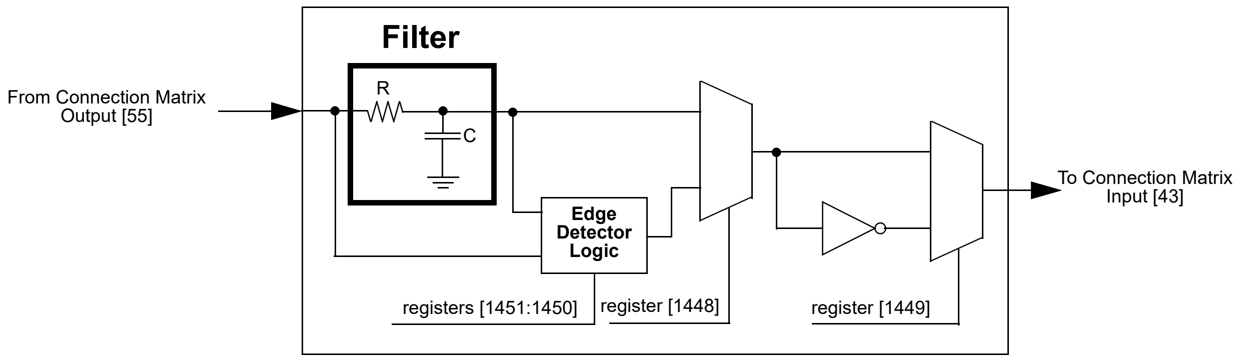


Figure 78: Deglitch Filter/Edge Detector

12 Voltage Reference

12.1 VOLTAGE REFERENCE OVERVIEW

The SLG46855-A has a Voltage Reference (Vref) macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, or temperature sensor output. The macrocell also has the option to output reference voltages on GPIO8 and GPIO9. See Table 53 for the available selections for each analog comparator.

Also see Figure 79, which shows the reference output structure.

12.2 VREF SELECTION TABLE

Table 54: Vref Selection Table

SEL[5:0]	Vref	SEL[5:0]	Vref
0	0.032	32	1.056
1	0.064	33	1.088
2	0.096	34	1.12
3	0.128	35	1.152
4	0.16	36	1.184
5	0.192	37	1.216
6	0.224	38	1.248
7	0.256	39	1.28
8	0.288	40	1.312
9	0.32	41	1.344
10	0.352	42	1.376
11	0.384	43	1.408
12	0.416	44	1.44
13	0.448	45	1.472
14	0.48	46	1.504
15	0.512	47	1.536
16	0.544	48	1.568
17	0.576	49	1.6
18	0.608	50	1.632
19	0.64	51	1.664
20	0.672	52	1.696
21	0.704	53	1.728
22	0.736	54	1.76
23	0.768	55	1.792
24	0.8	56	1.824
25	0.832	57	1.856
26	0.864	58	1.888
27	0.896	59	1.92
28	0.928	60	1.952
29	0.96	61	1.984
30	0.992	62	2.016
31	1.024	63	External

12.3 VREF BLOCK DIAGRAM

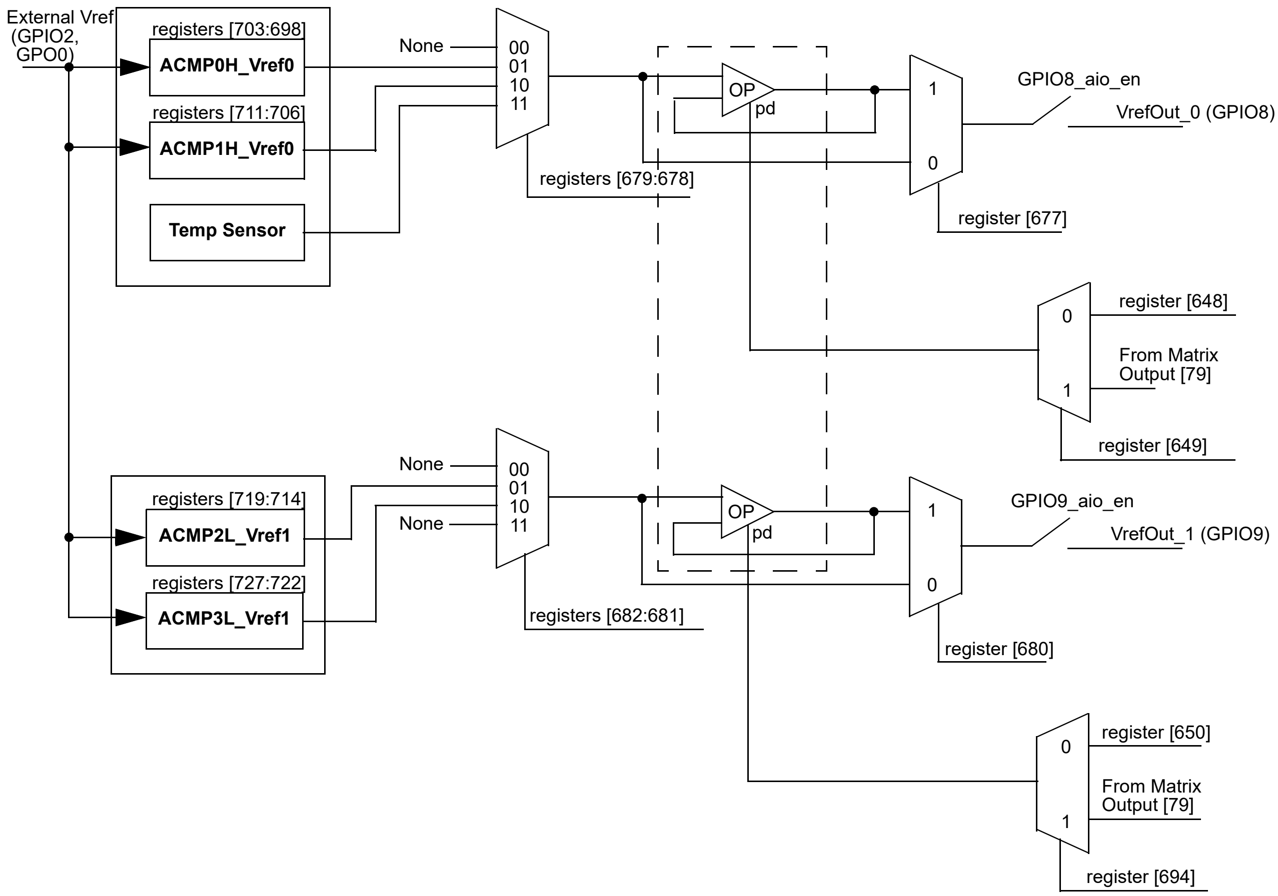


Figure 79: Voltage Reference Block Diagram

12.4 VREF LOAD REGULATION

Note 1 It is not recommended to use Vref connected to external pin without buffer.

Note 2 Vref buffer performance is not guaranteed at V_{DD} < 2.7 V.

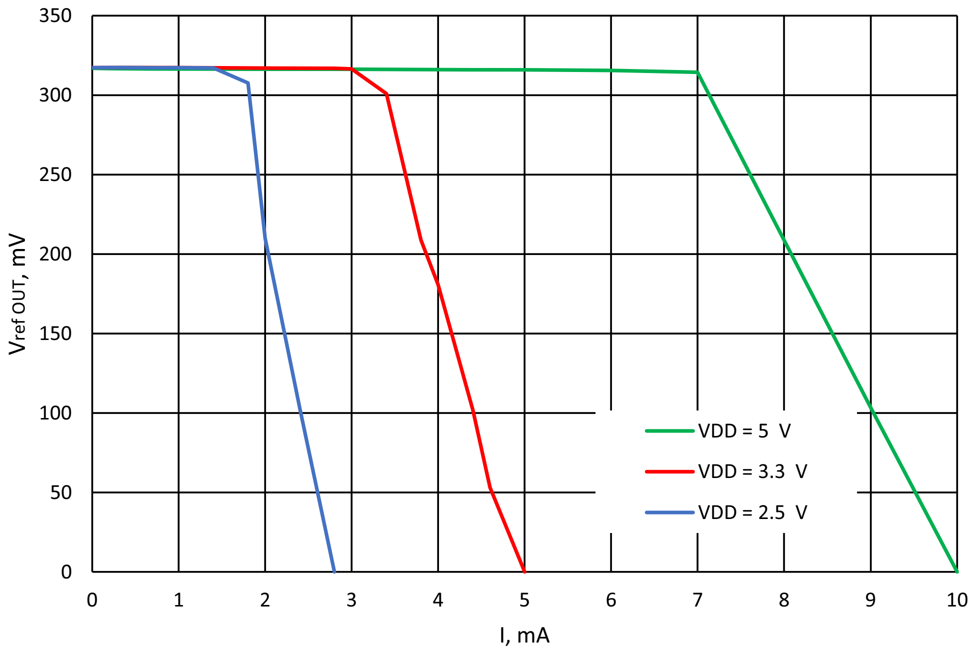


Figure 80: Typical Load Regulation, Vref = 320 mV, T = -40 °C to +105 °C, Buffer - Enabled

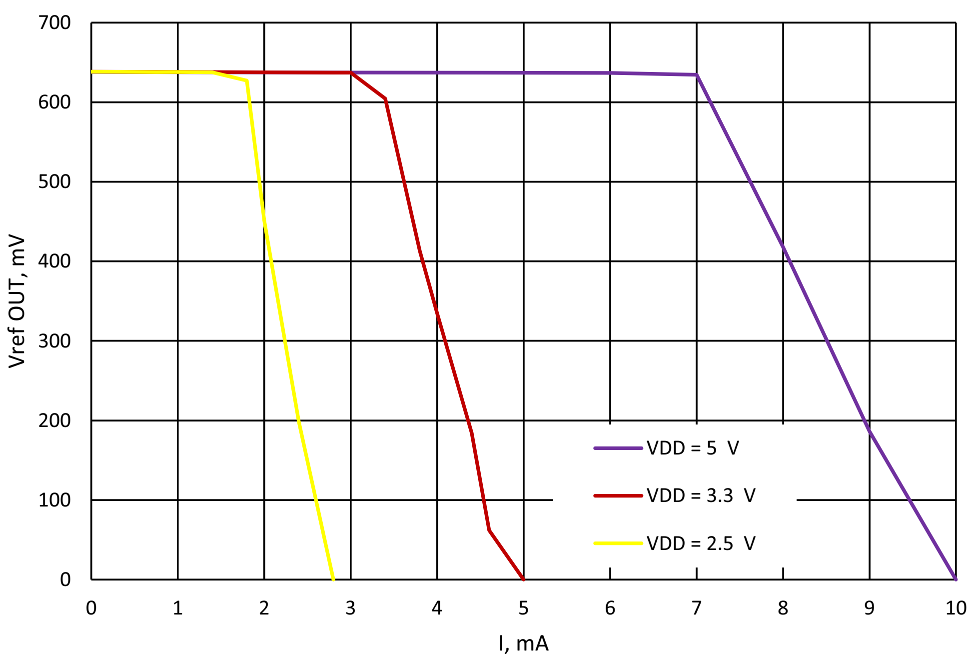


Figure 81: Typical Load Regulation, Vref = 640 mV, T = -40 °C to +105 °C, Buffer - Enabled

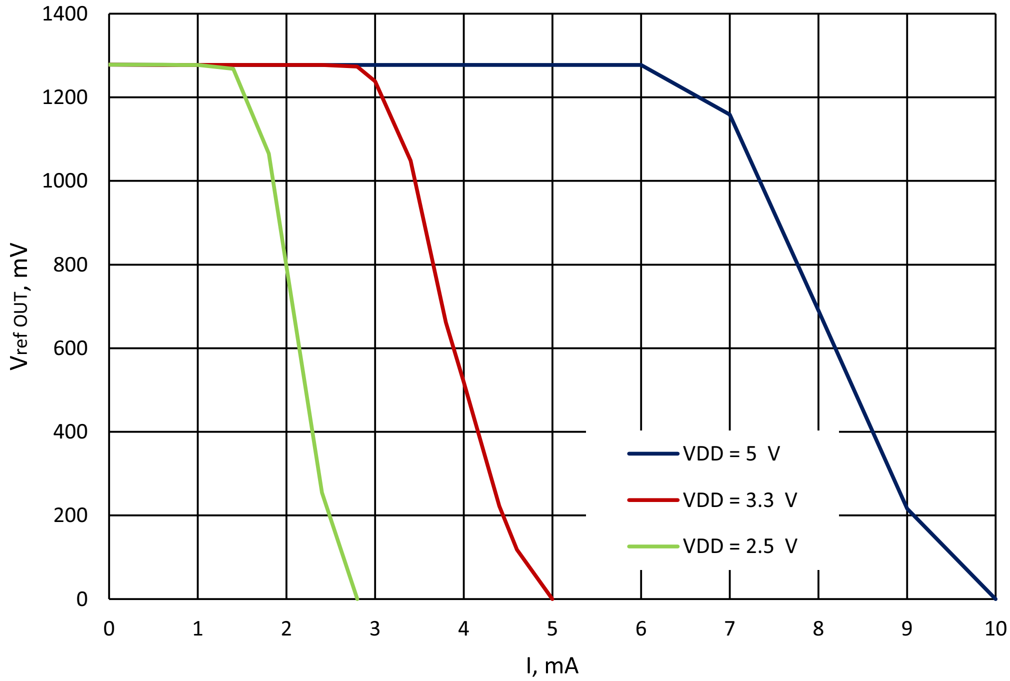


Figure 82: Typical Load Regulation, Vref = 1280 mV, T = -40 °C to +105 °C, Buffer - Enabled

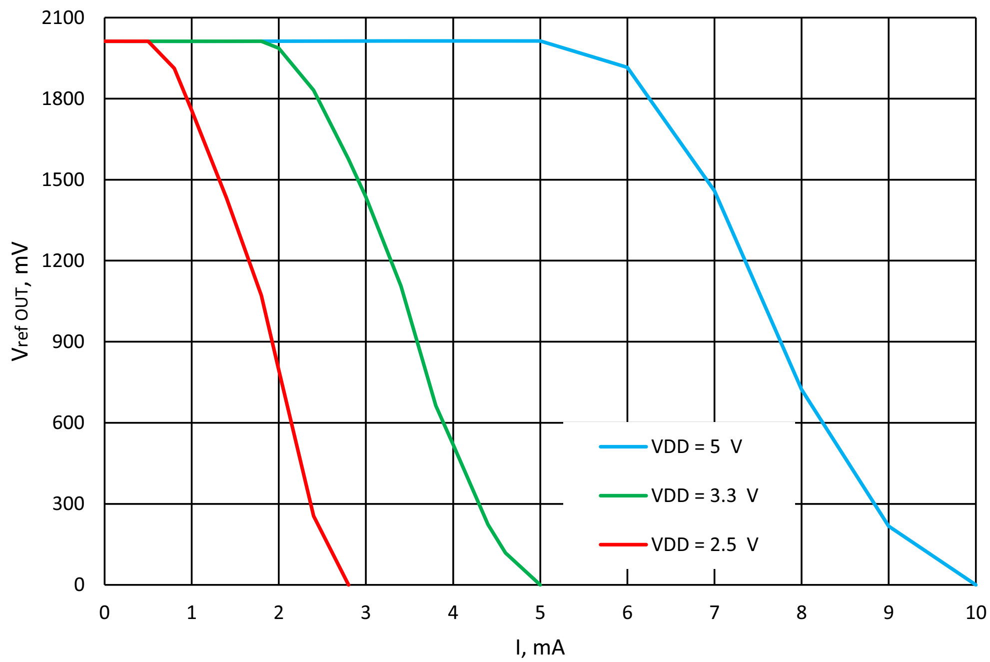


Figure 83: Typical Load Regulation, Vref = 2016 mV, T = -40 °C to +105 °C, Buffer - Enabled

13 Clocking

13.1 OSC GENERAL DESCRIPTION

The SLG46855-A has three internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (2.048 MHz)
- Oscillator2 (25 MHz).

There are two divider stages for each oscillator that gives the user flexibility for introducing clock signals to connection matrix, as well as various other macrocells. The pre-divider (first stage) for Oscillator allows the selection of /1, /2, /4 or /8 to divide down frequency from the fundamental. The second stage divider has an input of frequency from the pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24 or /64 on Connection Matrix Input lines [53], [54], and [55]. Please see Figure 87 for more details on the SLG46855-A clock scheme.

Oscillator2 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by register [749]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power-down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power-down/Force On (Connection Matrix Output [80], [81], [82]) signal has the highest priority. The OSC operates according to the following table:

Table 55: Oscillator Operation Mode Configuration Settings

POR	External Clock Selection	Signal From Connection Matrix	Register: Power-Down or Force On by Matrix Input	Register: Auto Power-On or Force On	OSC Enable Signal from CNT/DLY Macrocells	OSC Operation Mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF
Note 1 The OSC will run only when any macrocell that uses OSC is powered on.						

13.2 OSCILLATOR0 (2.048 KHZ)

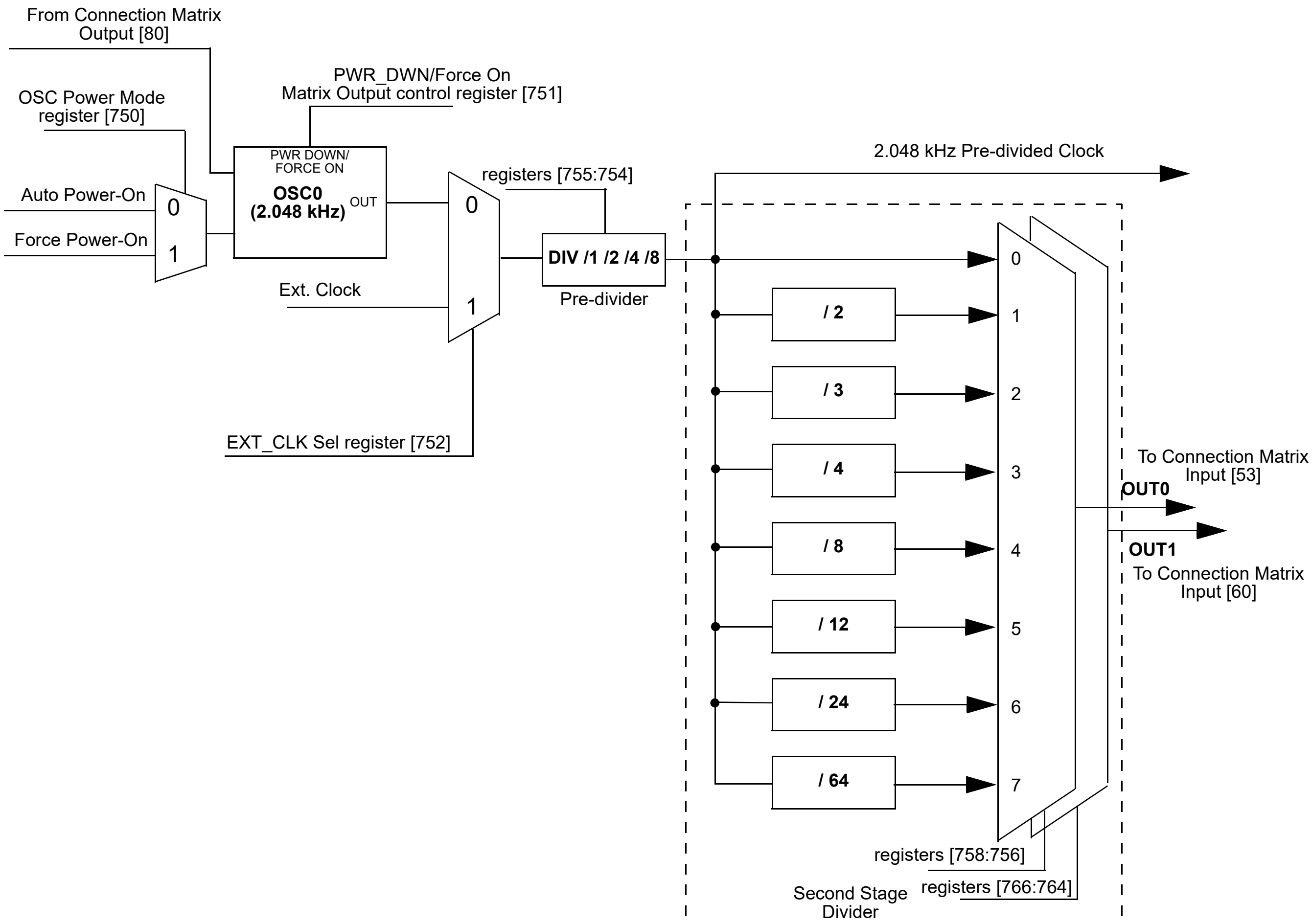


Figure 84: Oscillator0 Block Diagram

13.3 OSCILLATOR1 (2.048 MHZ)

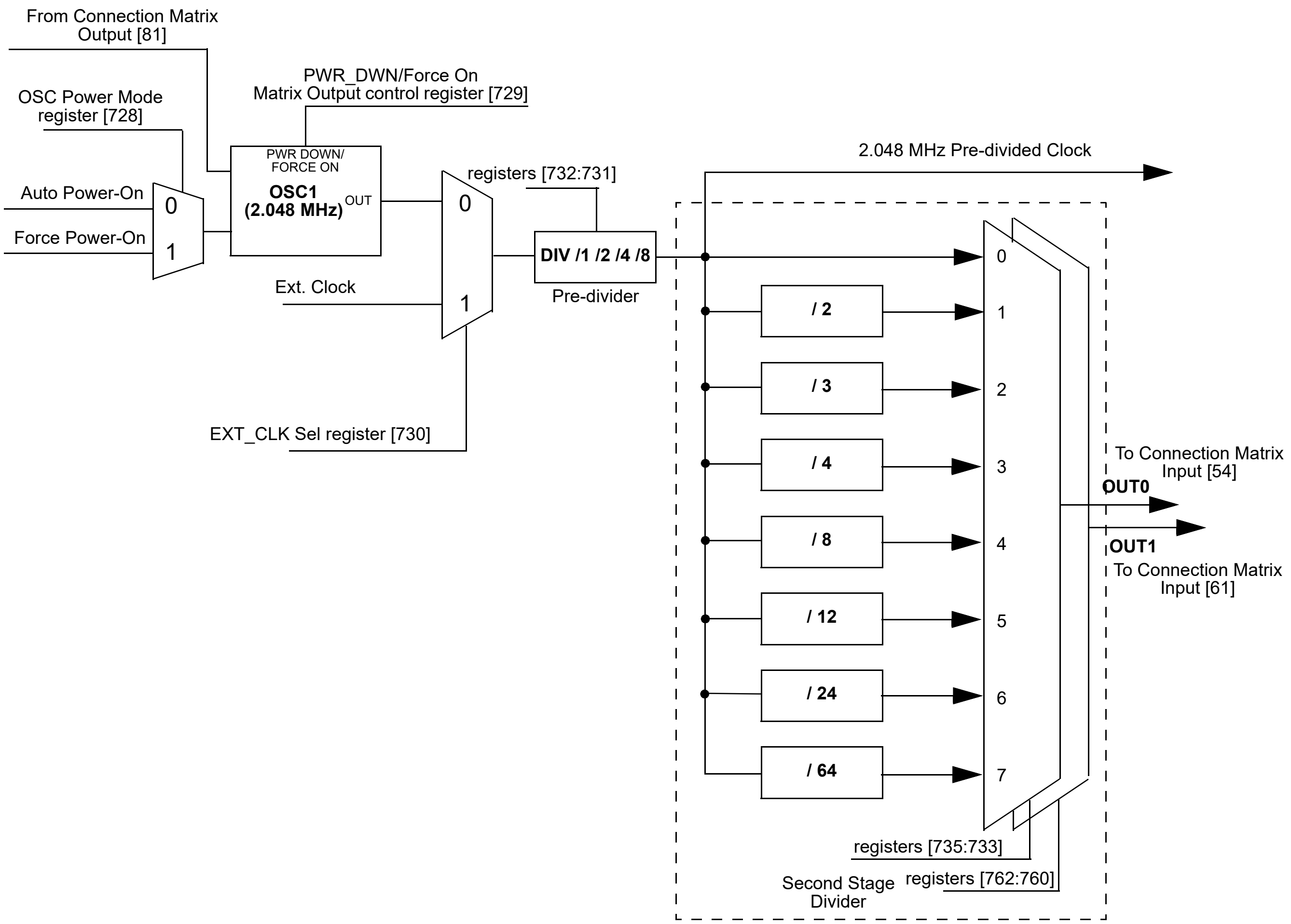


Figure 85: Oscillator1 Block Diagram

13.4 OSCILLATOR2 (25 MHZ)

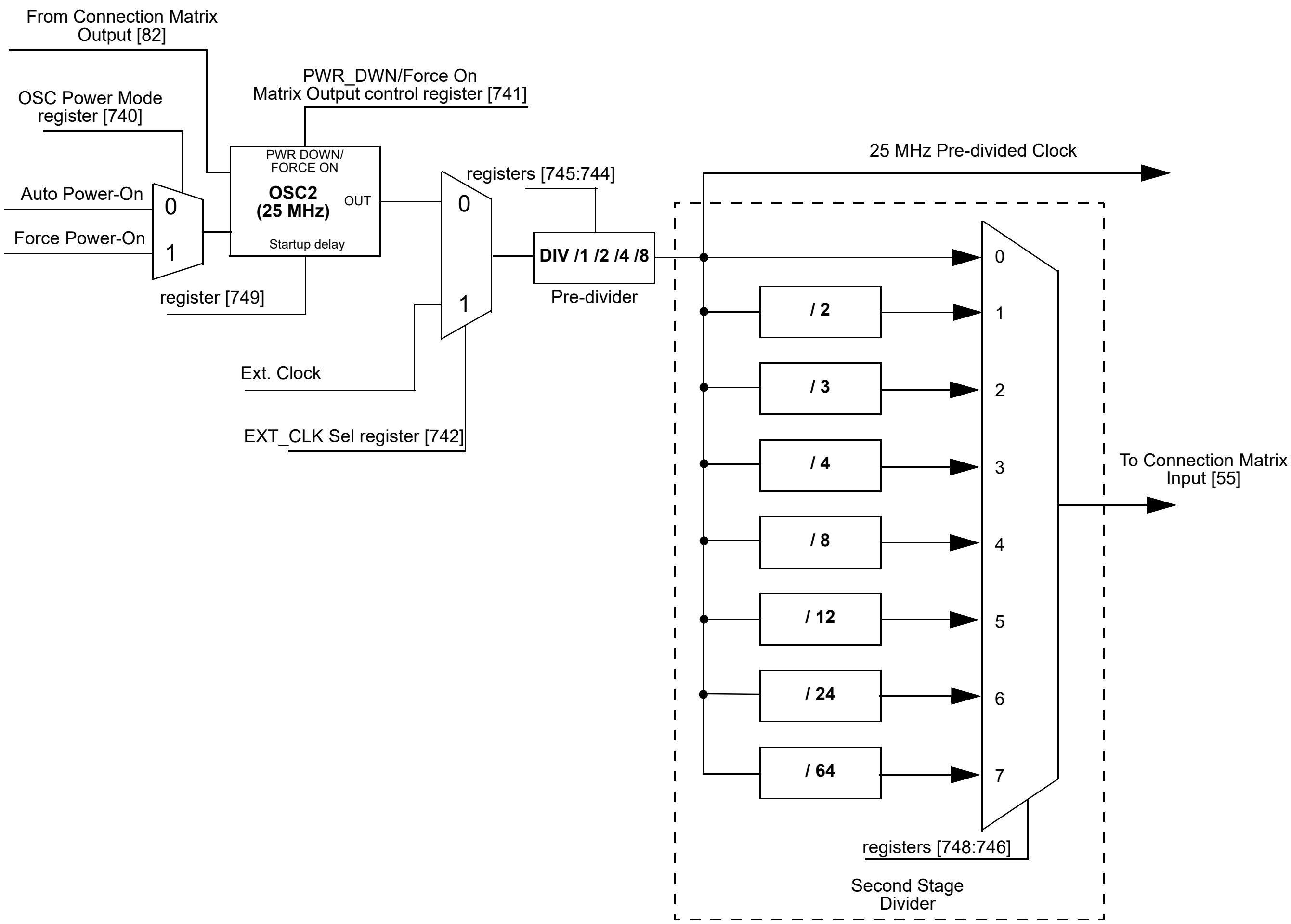


Figure 86: Oscillator2 Block Diagram

13.5 CNT/DLY CLOCK SCHEME

Each CNT/DLY within Multi-Function macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC0/1, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144
- OSC1/1, OSC1/8, OSC1/64, OSC1/512
- OSC2/1, OSC2/4

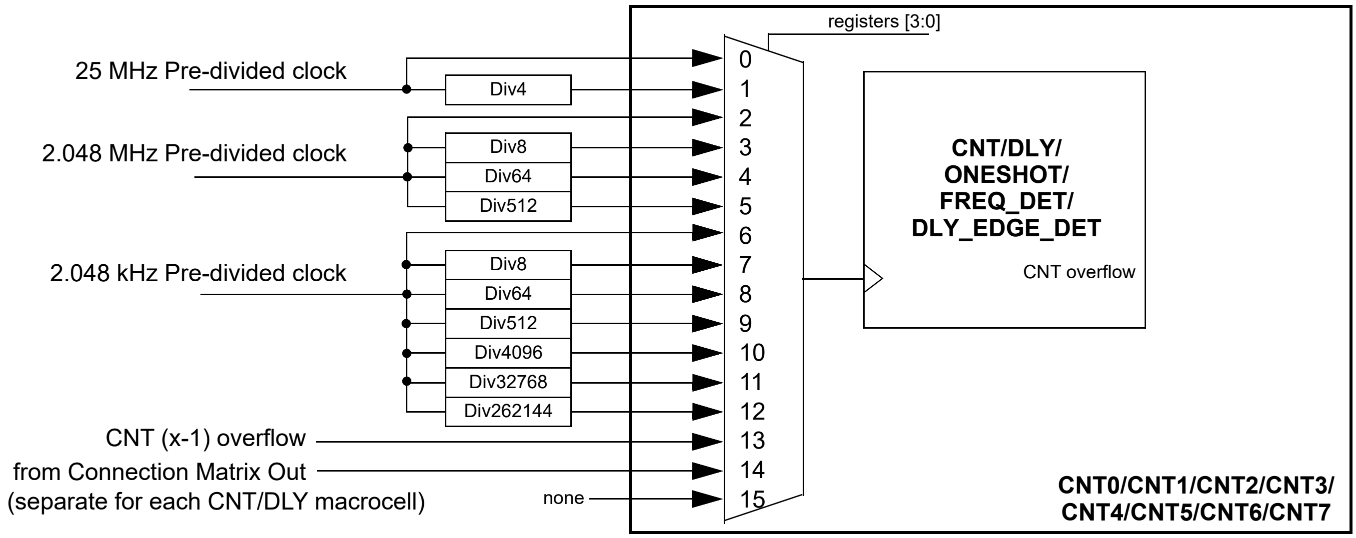


Figure 87: Clock Scheme

13.6 EXTERNAL CLOCKING

The SLG46855-A supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

13.6.1 GPI0 Source for Oscillator0 (2.048 kHz)

When register [752] is set to 1, an external clocking signal on GPI0 will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 84. The low and high limits for external frequency that can be selected are 0 MHz and 10 MHz.

13.6.2 GPIO2 Source for Oscillator1 (2.048 MHz)

When register [730] is set to 1, an external clocking signal on GPIO2 will be routed in place of the internal oscillator derived 2.048 MHz clock source. See Figure 85. The low and high limits for external frequency that can be selected are 0 MHz and 10 MHz.

13.6.3 GPIO8 Source for Oscillator 2 (25 MHz)

When register [742] is set to 1, an external clocking signal on GPIO8 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 86. The external frequency range is 0 MHz to 20 MHz at V_{DD} = 2.3 V, 30 MHz at V_{DD} = 3.3 V, 50 MHz at V_{DD} = 5.0 V. When an external clock is selected for OSC2, the oscillator's output signal will be inverted with respect to the GPIO8 input signal.

13.7 OSCILLATORS POWER-ON DELAY

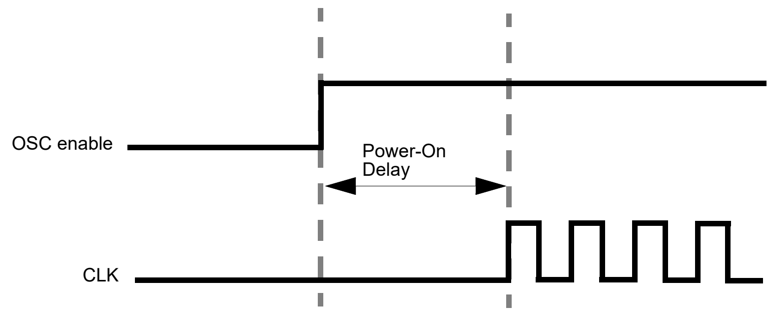


Figure 88: Oscillator Startup Diagram

Note 1 OSC power mode: “Auto Power-On”.

Note 2 “OSC enable” signal appears when any macrocell that uses OSC is powered on.

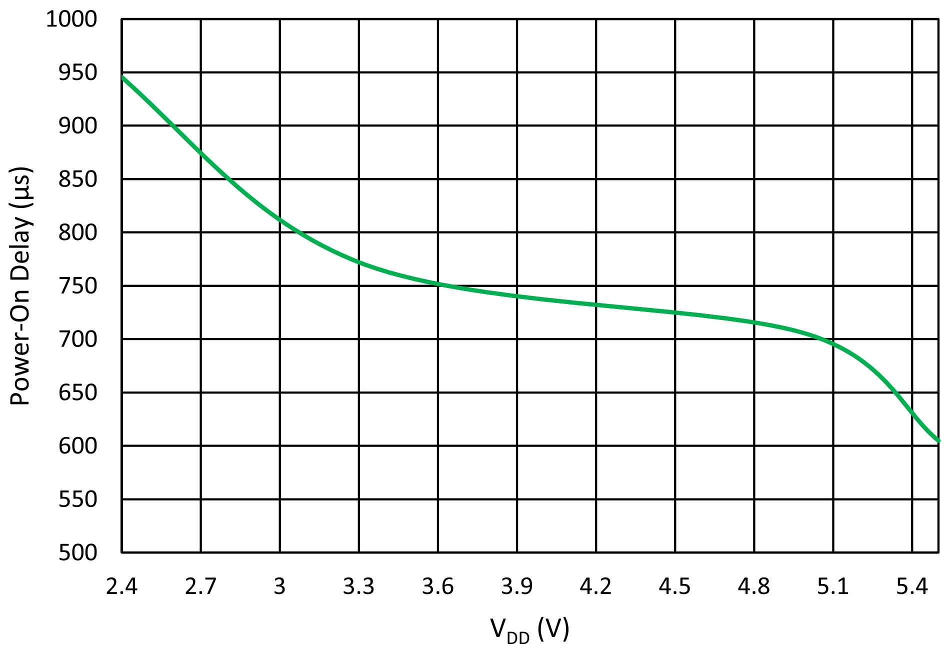


Figure 89: Oscillator0 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC0 = 2.048 kHz

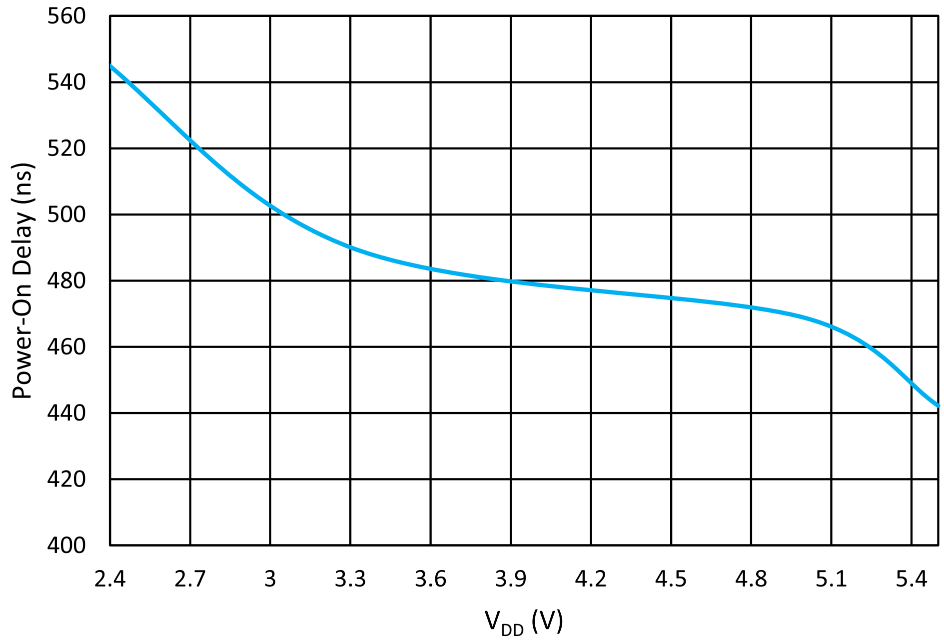


Figure 90: Oscillator1 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC1 = 2.048 MHz

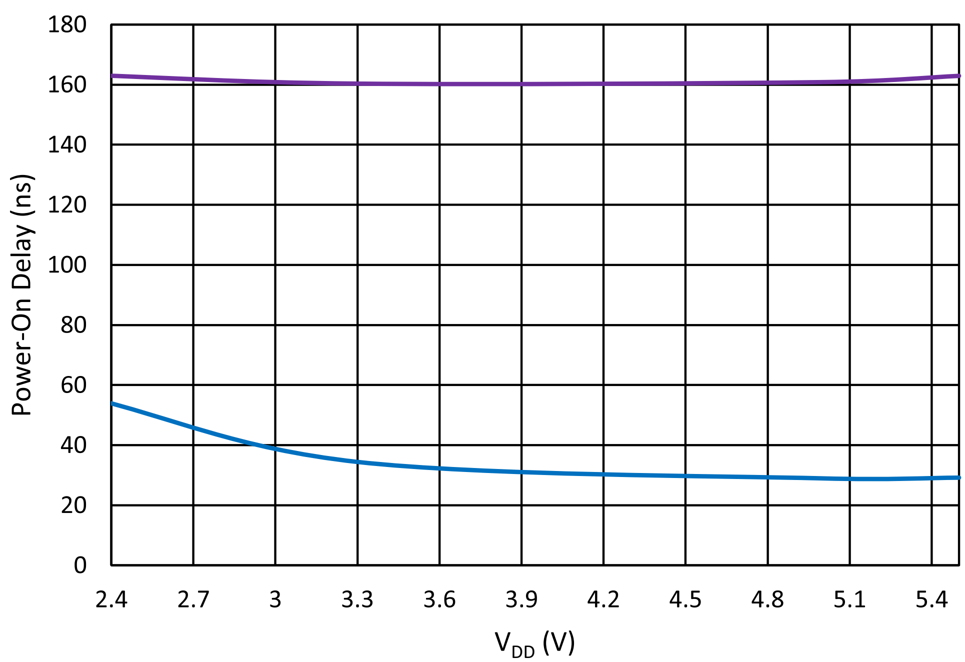


Figure 91: Oscillator2 Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC2 = 25 MHz

13.8 OSCILLATORS ACCURACY

Note: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

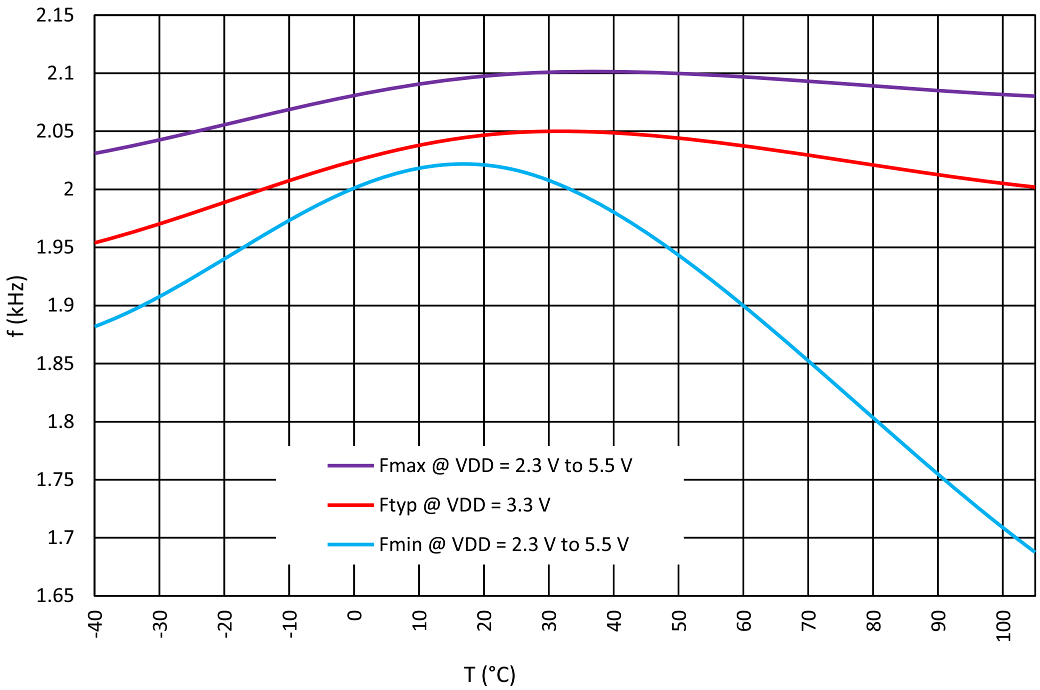


Figure 92: Oscillator0 Frequency vs. Temperature, OSC0 = 2.048 kHz

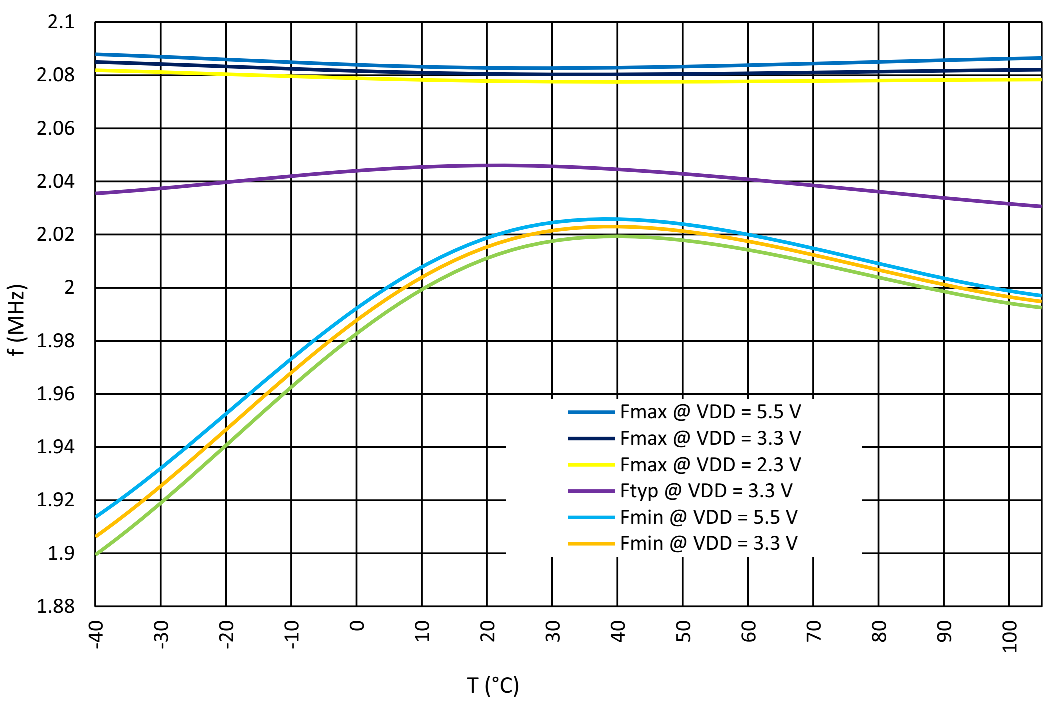


Figure 93: Oscillator1 Frequency vs. Temperature, OSC1 = 2.048 MHz

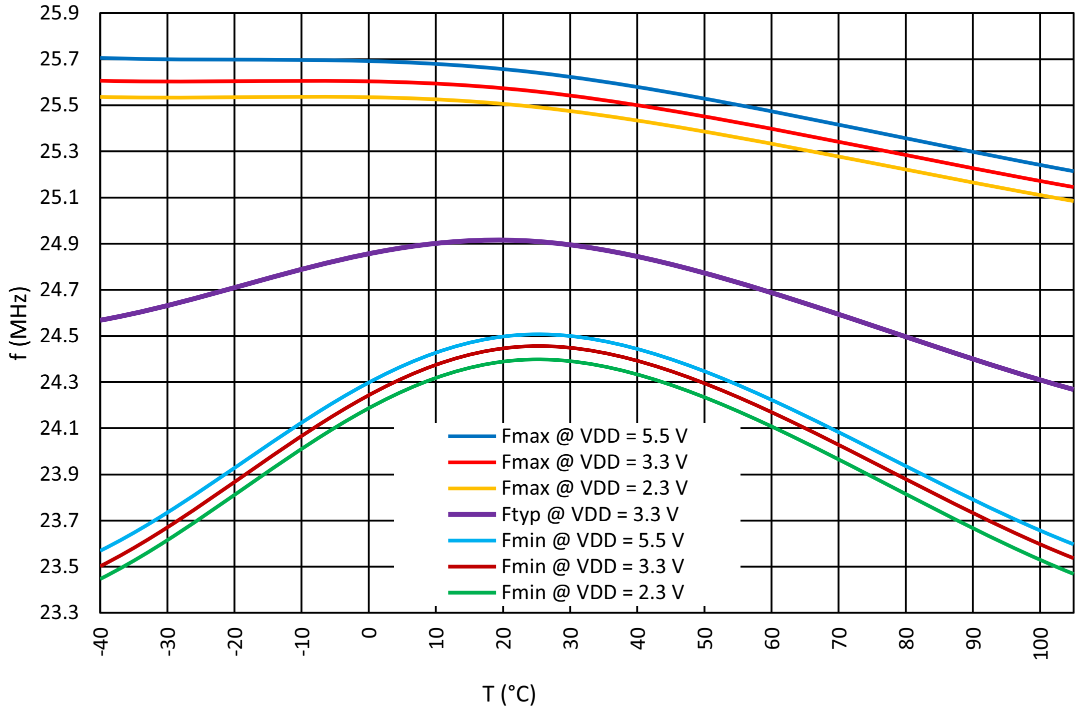


Figure 94: Oscillator2 Frequency vs. Temperature, OSC2 = 25 MHz

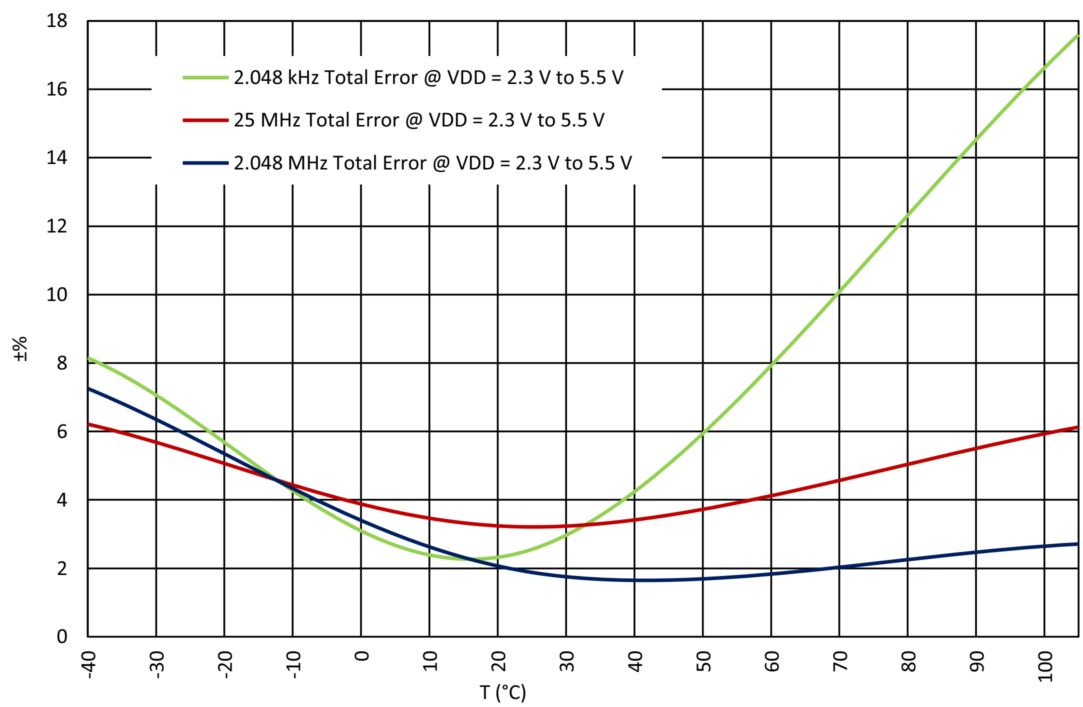


Figure 95: Oscillators Total Error vs. Temperature

Note: For more information see Section 3.9.

14 Power-On Reset

The SLG46855-A has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during Power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IOs.

14.1 GENERAL OPERATION

The SLG46855-A is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on PIN1) is less than Power-Off Threshold (see in Table 6), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (Note) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46855-A, the voltage applied on the V_{DD} should be higher than the Power-On threshold (Note). The full operational V_{DD} range for the SLG46855-A is 2.3 V to 5.5 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On threshold. After the POR sequence has started, the SLG46855-A will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

Note: The Power-On threshold is defined in Table 6.

To power down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power-Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before the voltage on PINs can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

14.2 POR SEQUENCE

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 96.

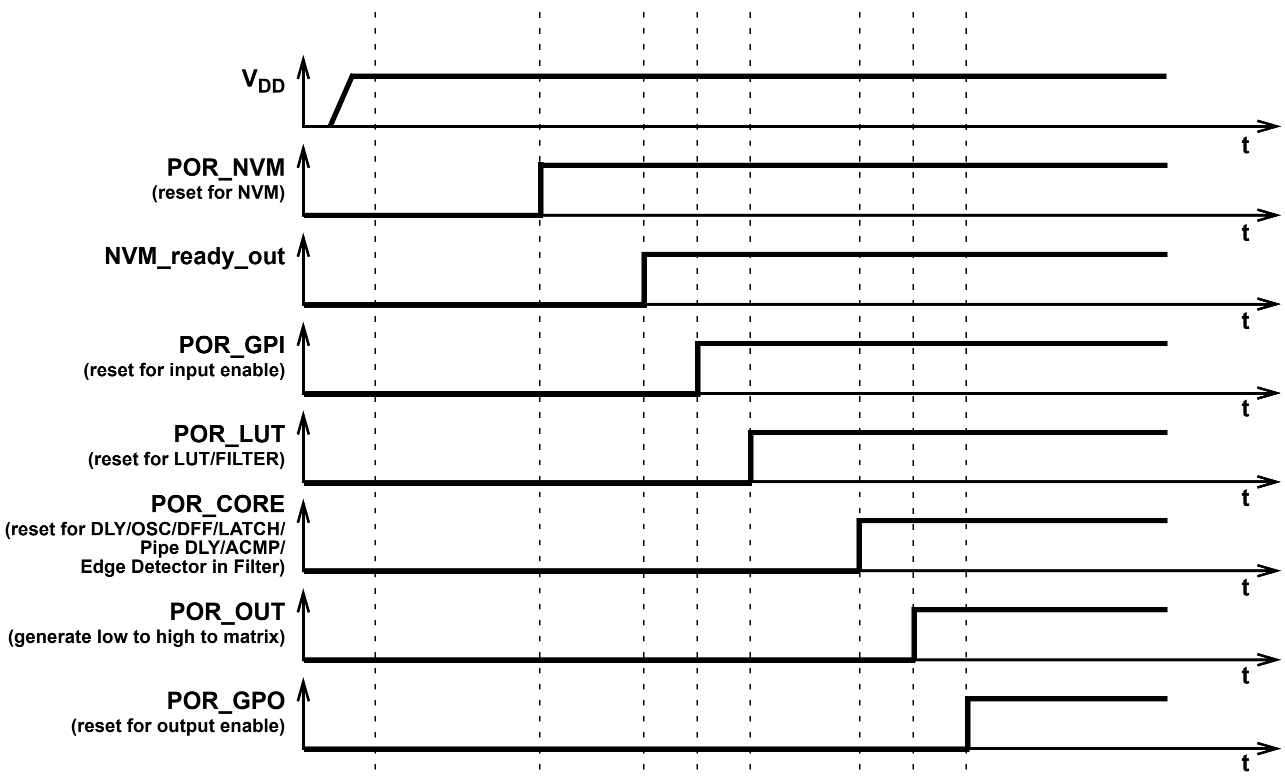


Figure 96: POR Sequence

As can be seen from Figure 96 after the V_{DD} has start ramping up and crosses the Power-On threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM, and transfers this information to a CMOS LATCH that serves to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, OSCs, DFFs, LATCHES, and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

14.3 MACROCELLS OUTPUT STATES DURING POR SEQUENCE

To have a full picture of SLG46855-A operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 97 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P_DLY macrocell configured as edge detector becomes active at this time. After that input pins are enabled.

Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

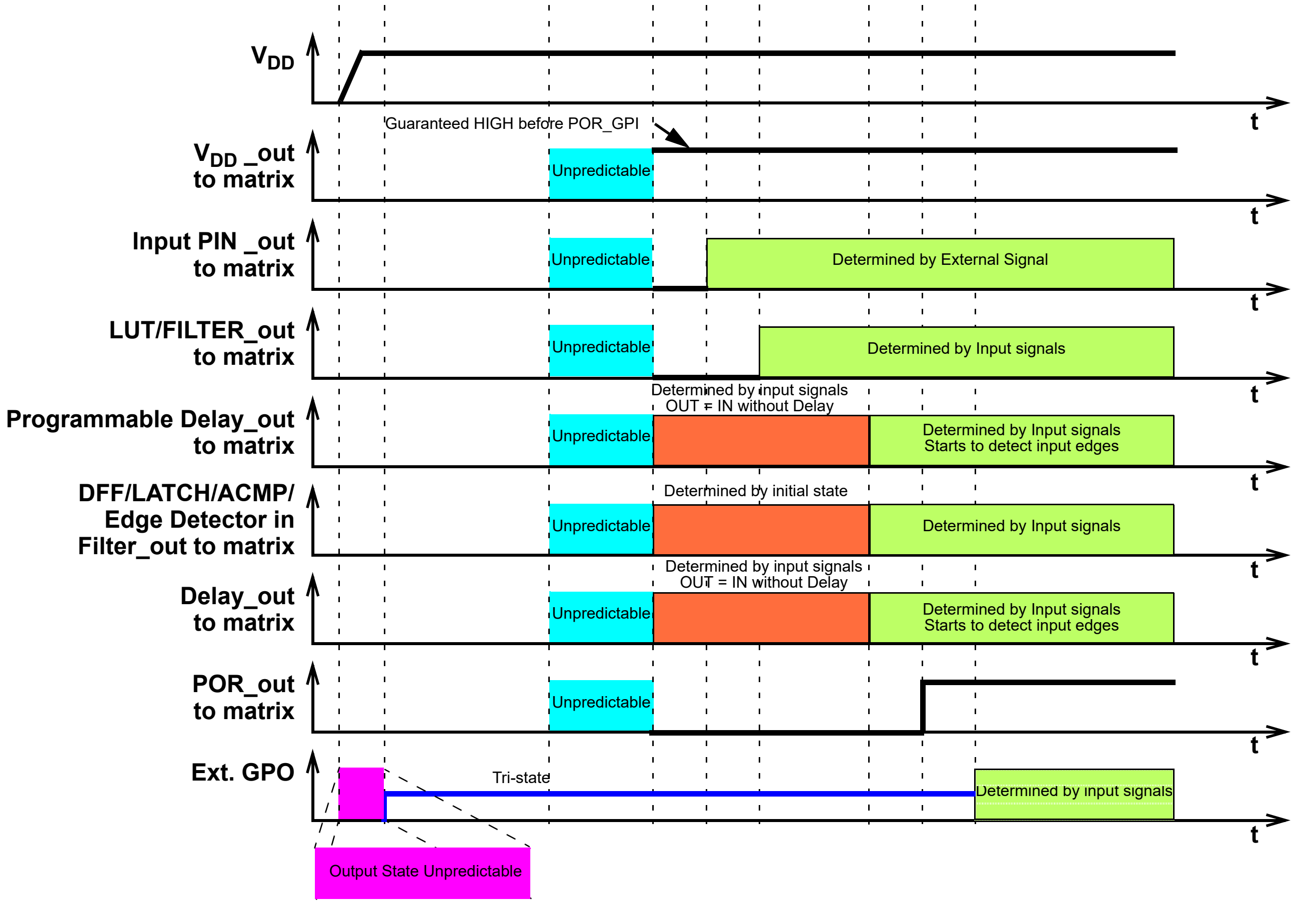


Figure 97: Internal Macrocell States During POR Sequence

14.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.56 V to 2.03 V, macrocells in SLG46855-A are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input pins, ACMP, Pull-up/down.
2. LUTs.
3. DFFs, Delays/Counters, Pipe Delay.
4. POR output to matrix.
5. Output pin corresponds to the internal logic.

The Vref output pin driving signal can precede POR output signal going high by 3 µs to 5 µs. The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin → V_{DD} and pin → GND on each pin. So, if the input signal applied to pin is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin.There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

14.3.2 Power-Down

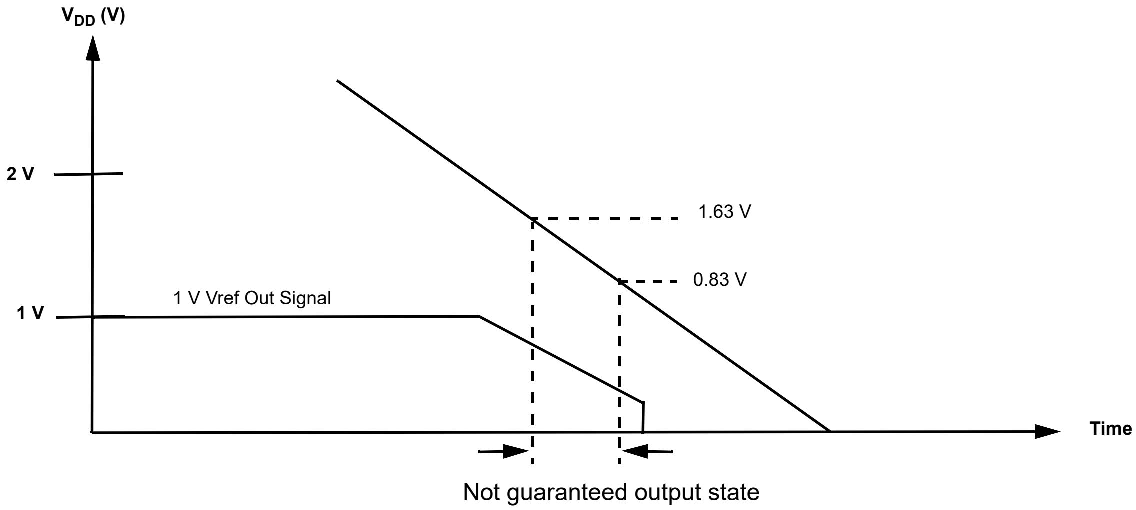


Figure 98: Power-Down

During power-down, macrocells in SLG46855-A are powered off after V_{DD} falling down below Power-Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

15 I^2C Serial Communications Macrocell

15.1 I^2C SERIAL COMMUNICATIONS MACROCELL OVERVIEW

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I^2C Serial Communications Macrocell in this device allows an I^2C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I^2C bus Master is also able to read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I^2C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits registers [1967:1965]. See Section 15.5 for more details on I^2C read/write memory protection.

15.2 I^2C SERIAL COMMUNICATIONS DEVICE ADDRESSING

Each command to the I^2C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 99. After the Start bit, the first four bits are a control code. Each bit in a control code can be sourced independently from the register or by value defined externally GPI0, GPIO2, GPIO4, and GPIO5. The LSB of the control code is defined by the value of GPI0, while the MSB is defined by the value of GPIO5. The address source (either register bit or PIN) for each bit in the control code is defined by registers [2027:2024]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I^2C bus. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I^2C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other slave device, please consult the I^2C-bus specification and user manual to understand the addressing and implementation of these special functions, to insure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I^2C Macrocell on the SLG46855-A are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be "0" for all commands to the SLG46855-A.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 99 shows this basic command structure.

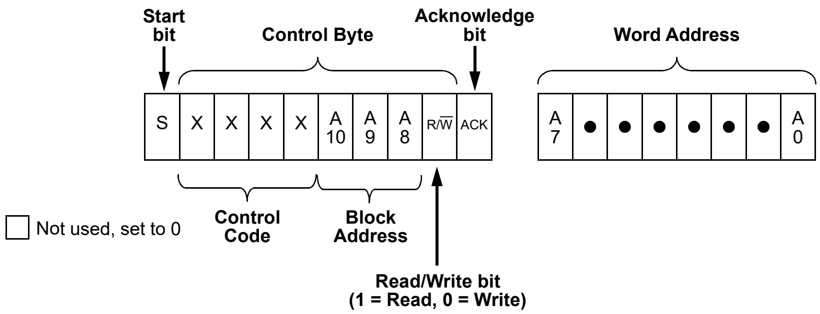


Figure 99: Basic Command Structure

15.3 I²C SERIAL GENERAL TIMING

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 100. Timing specifications can be found in the AC Characteristics section.

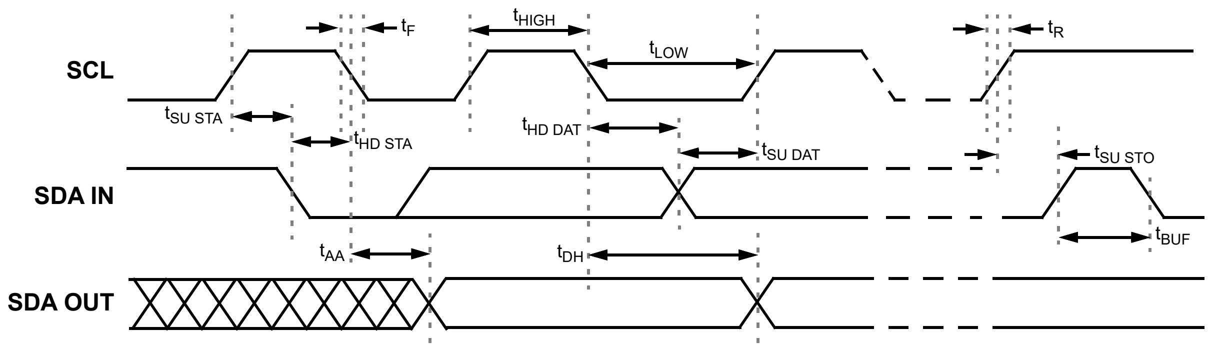


Figure 100: I²C General Timing Characteristics

15.4 I²C SERIAL COMMUNICATIONS COMMANDS

15.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to "0") are placed onto the I²C bus by the Master. After the SLG46855-A sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46855-A, where the data byte is to be written. After the SLG46855-A sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG46855-A again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46855-A generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command, register [1961] = 1 - Enable. It means that IOs will remain their state until the write command is done.

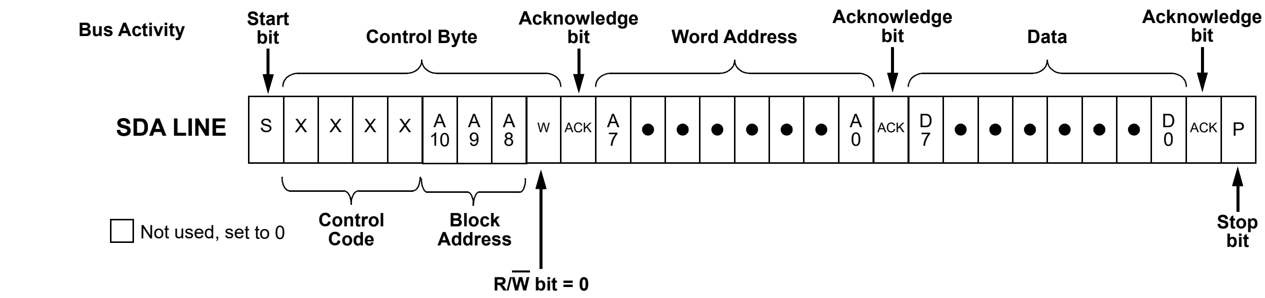


Figure 101: Byte Write Command, R/W = 0

15.4.2 Sequential Write Command

The write Control Byte, Word Address, and the first data byte are transmitted to the SLG46855-A in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Master continues to transmit data bytes to the SLG46855-A. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46855-A generates the Acknowledge bit.

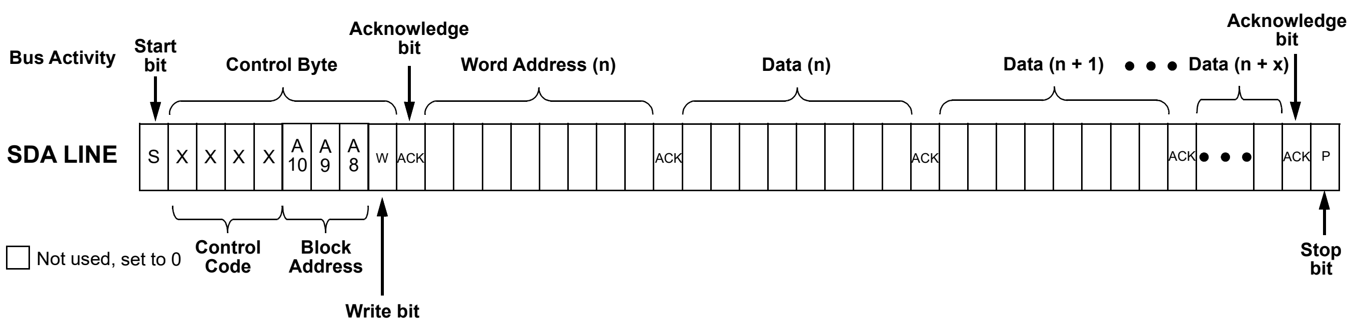


Figure 102: Sequential Write Command

15.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/W bit = "1". The SLG46855-A will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

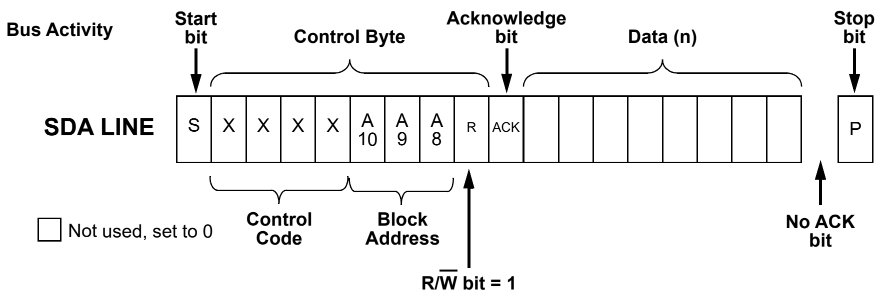


Figure 103: Current Address Read Command, R/W = 1

15.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to "0", indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to "1", after which the SLG46855-A issues an Acknowledge bit, followed by the requested eight data bits.

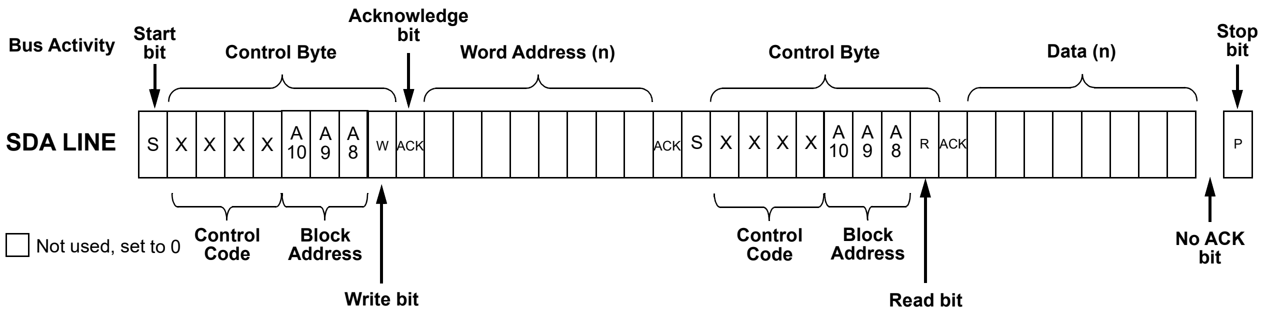


Figure 104: Random Read Command

15.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Random Read command, except that once the SLG46855-A transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

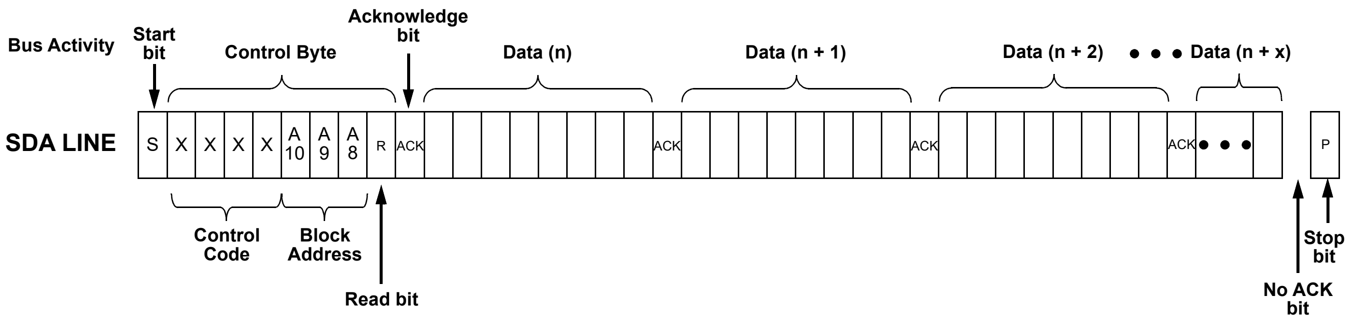


Figure 105: Sequential Read Command

15.4.6 I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [1960] I²C reset bit to "1", which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1960] will be set to "0" automatically. The Figure 106 illustrates the sequence of events for this reset function.

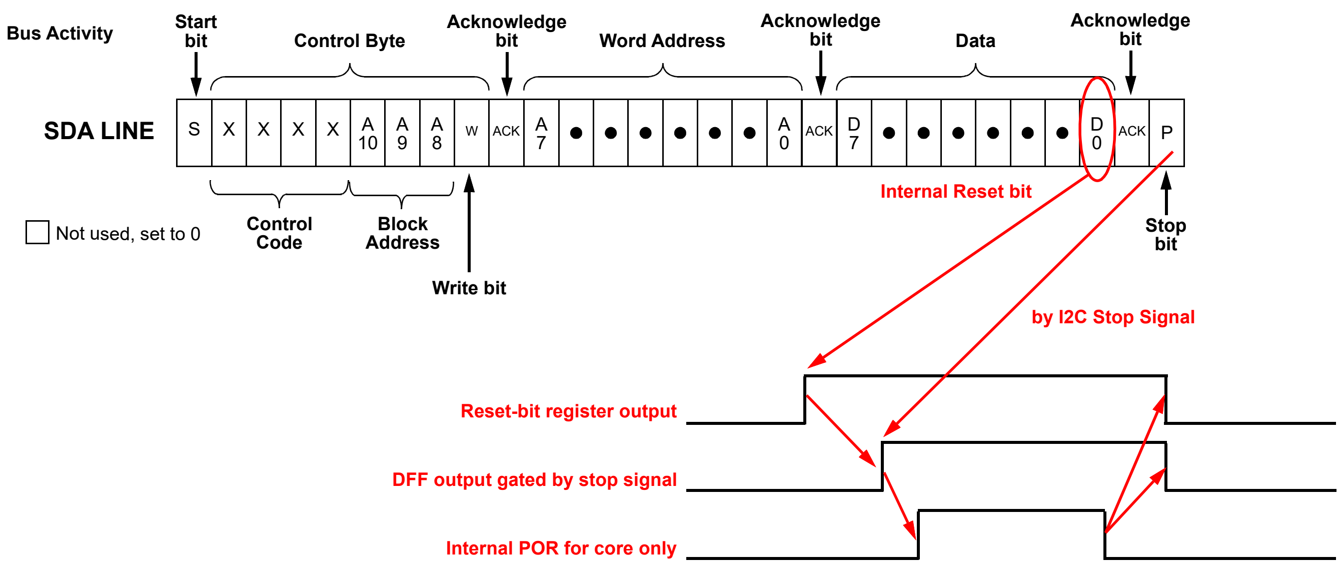


Figure 106: Reset Command Timing

15.5 I2C SERIAL COMMAND REGISTER MAP

There are seven read/write protect modes for the design sequence from being corrupted or copied. See Table 55 for details.

Table 56: Read/Write Protection Options

Configurations	Protection Modes Configuration							Data Output From	Register Address
	Unlocked	Partly Lock Read1	Partly Lock Read2	Partly Lock Read2/ Write	Lock Read	Lock Write	Lock Read/ Write		
	(Mode 0)	(Mode 1)	(Mode 2)	(Mode 3)	(Mode 4)	(Mode 5)	(Mode 6)		
I2C Byte Write Bit Masking (section 15.6.3)	R/W	R/W	R/W	R/W	W	R	-	Memory	F6
I2C Serial Reset Command (section 15.4.6)	R/W	R/W	R/W	R/W	W	R	-	Memory	F5,b'0
Outputs Latching During I2C Write	R/W	R/W	R/W	R/W	W	R	-	Memory	F5,b'1
Connection Matrix Virtual Inputs (section 6.3)	R/W	R/W	R/W	R/W	W	R	-	Macrocell	4C
Configuration Bits for All Macrocells (IO Pins, ACMPs, Combination Function Macrocells, etc.)	R/W	R/W	W	-	W	R	-	Memory	
Macrocells Inputs Configuration (Connection Matrix Outputs, section 6.2)	R/W	W	W	-	W	R	-	Memory	0~47
Protection Mode Enable	R	R	R	R	R	R	R	Memory	F5,b'3
Protection Mode Selection	R/W	R	R	R	R	R	R	Memory	F5,b'7~5
Macrocells Output Values (Connection Matrix Inputs, section 6.1)	R	R	R	R	-	R	-	Macrocell	48~4B; 4D~4F
Counter Current Value (for 16-bit CNT)	R	R	R	R	-	R	-	Macrocell	A5,A6
Counter Current Value (for 8-bit CNT)	R	R	R	R	-	R	-	Macrocell	A7,A8
I2C Control Code (section 15.2)	R	R	R	R	R	R	R	Memory	FD,b'3~0
Pin Slave Address Select	R	R	R	R	R	R	R	Memory	FD,b'7~4
I2C Disable/Enable	R	R	R	R	R	R	R	Memory	FE,b'0

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

It is possible to read some data from macrocells, such as counter current value, connection matrix, and connection matrix virtual inputs. The I^2C write will not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allows identifying silicon family, its revision, and others.

See Section 17 for detailed information on all registers.

15.6 I^2C ADDITIONAL OPTIONS

When Output latching during I^2C write, register [1961] = 1 allows all PINs output value to be latched until I^2C write is done. It will protect the output change due to configuration process during I^2C write in case multiple register bytes are changed. Inputs and internal macrocells retain their status during I^2C write.

If the user sets GPIO0 and GPIO1 function to a selection other than SDA and SCL, all access via I^2C will be disabled.

Note: Any write commands that come to the device via I^2C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

See Section 17 for detailed information on all registers.

15.6.1 Reading Counter Data via I^2C

The current count value in three counters in the device can be read via I^2C. The counters that have this additional functionality are 16-bit CNT0, and 8-bit counters CNT6 and CNT7.

15.6.2 I^2C Expander

In addition to the eight Connection Matrix Virtual Inputs, the SLG46855-A chip has four pins which can be used as an I^2C Expander. These four pins are GPO0, GPIO6, GPIO7, and GPIO8.

Each of these pins can be used as an I^2C Expander output or used as a normal pin. Also, each of these four expander outputs have initial state settings which are specified in registers [1959:1952].

15.6.3 I^2C Byte Write Bit Masking

The I^2C macrocell inside SLG46855-A supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see Section 15.4.1 for details) on the I^2C Byte Write Mask Register (address 0F6H) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to “1” in the I^2C Byte Write Mask Register will mask the effect of changing that particular bit in the target register, during the next Byte Write Command. The contents of the I^2C Byte Write Mask Register are reset (set to 00h) after valid Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I^2C Byte Write Mask Register will be reset with no effect. Figure 107 shows an example of this function.

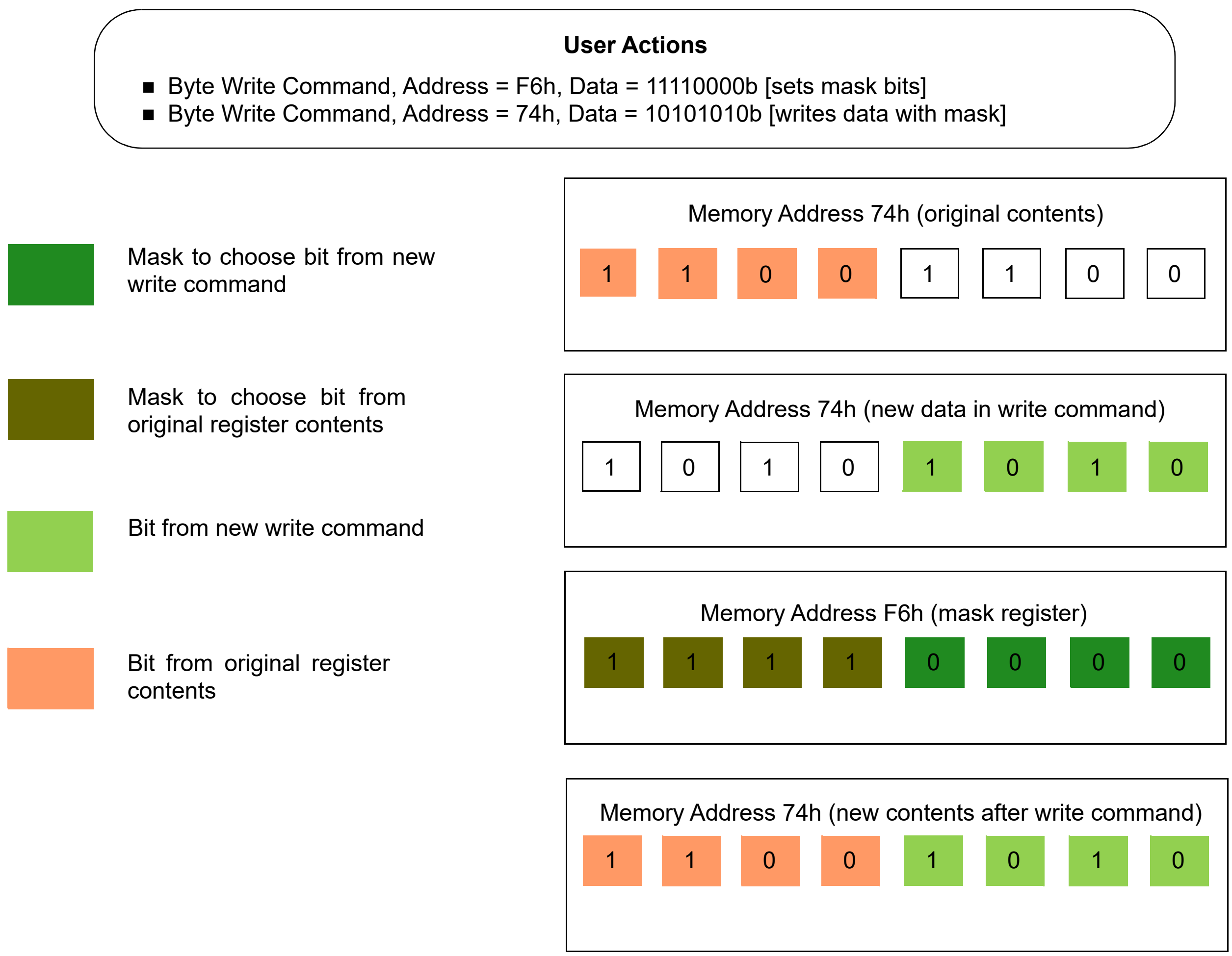


Figure 107: Example of I^2C Byte Write Bit Masking

16 Analog Temperature Sensor

The SLG46855-A has an Analog Temperature sensor (TS) with an output voltage linearly-proportional to the Centigrade temperature. The TS cell shares buffer with Vref 0, so it is impossible to use both cells simultaneously, its output can be connected directly to the GPIO8 or to the ACPM3_L positive input. Using buffer causes low-output impedance, linear output, and makes interfacing to readout or control circuitry especially easy. The TS is rated to operate over a -40 °C to 105 °C temperature range. The error in the whole temperature range does not exceed ±1.5 %. For more detail refer to section 3.11.

The equation below calculates the typical analog voltage passed from the TS to the ACMPs' IN+ source input for V_{DD} = 2.3 V to 5.5 V. It is important to note that there will be a chip to chip variation of about ±2 °C.

$$V_{TS1} = -2.3 \times T + 906.2$$

$$V_{TS2} = -2.8 \times T + 1094.3$$

where:

V_{TS1} (mV) - TS Output Voltage, range 1

V_{TS2} (mV) - TS Output Voltage, range 2

T (°C) - Temperature

Temperature hysteresis can be setup by enabling the GreenPAK's internal ACMP hysteresis.

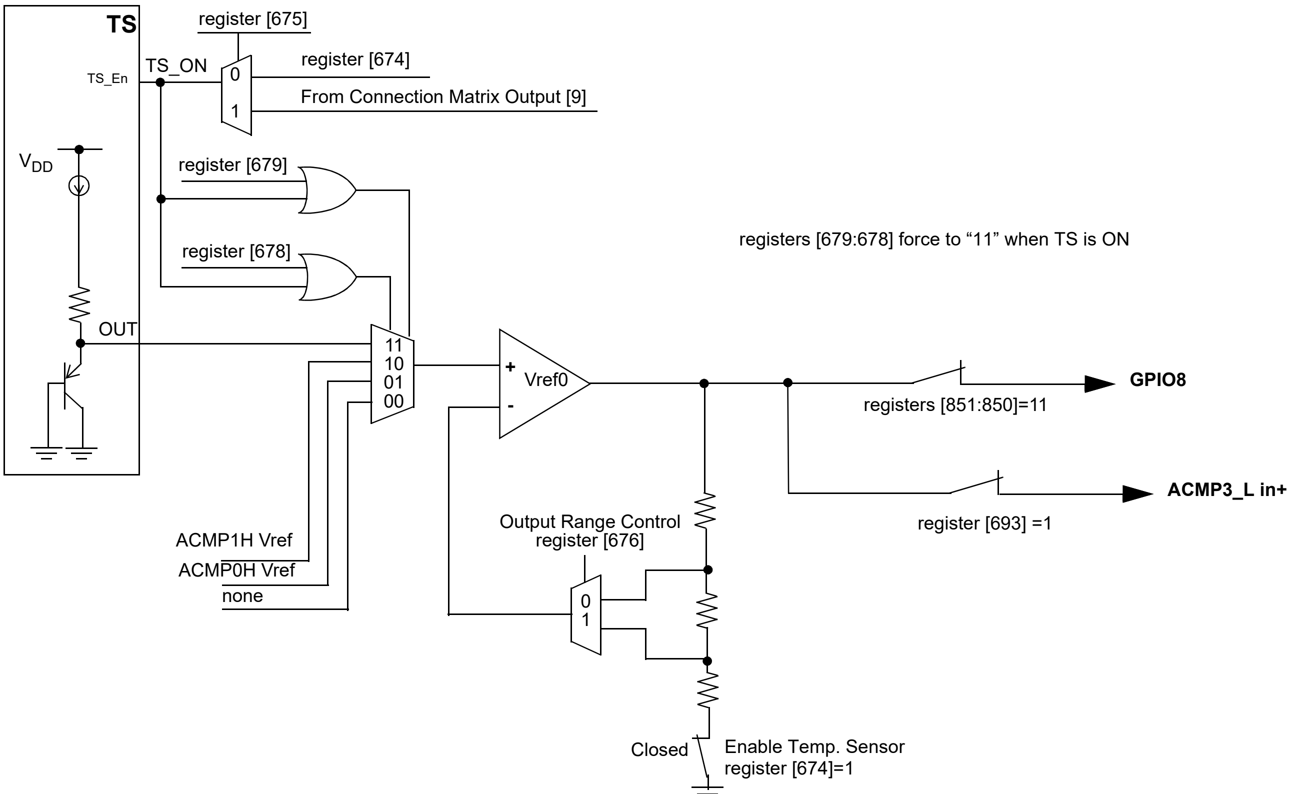


Figure 108: Analog Temperature Sensor Structure Diagram

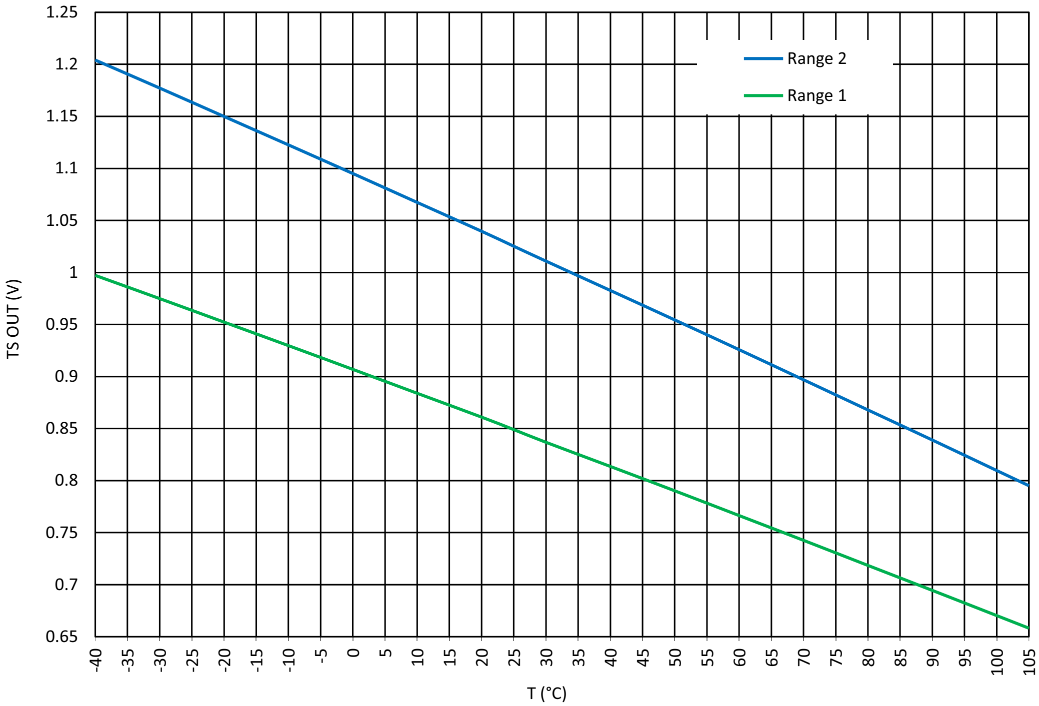


Figure 109: TS Output vs. Temperature, V_{DD} = 2.3 V to 5.5 V

17 Register Definitions

17.1 REGISTER MAP

Table 57: Register Map

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
Matrix Output			
0	0	LUT2_0 & DFF0	OUT0: IN0 of LUT2_0 or Clock Input of DFF0
	1		
	2		
	3		
	4		
	5		
	6		OUT1 IN1 of LUT2_0 or Data Input of DFF0
	7		
1	8		
	9		
	10		
	11		
	12	LUT2_1 & DFF1	OUT2: IN0 of LUT2_1 or Clock Input of DFF1
	13		
	14		
	15		
2	16		
	17		
	18		OUT3: IN1 of LUT2_1 or Data Input of DFF1
	19		
	20		
	21		
	22		
	23		

Table 57: Register Map (Continued)

Address: Byte	Address: Register Bit	Signal Function	Register Bit Definition
3	24	LUT2_2 & DFF2	OUT4: IN0 of LUT2_2 or Clock Input of DFF2
	25		
	26		
	27		
	28		
	29		
	30		OUT5: IN1 of LUT2_2 or Data Input of DFF2
	31		
4	32		
	33		
	34		
	35		
	36	LUT2_3 & PGen	OUT6: IN0 of LUT2_3 or Clock Input of PGen
	37		
	38		
	39		
5	40		
	41		
	42		OUT7: IN1 of LUT2_3 or nRST of PGen
	43		
	44		
	45		
	46		
	47		
6	48	LUT3_0 & DFF3	OUT8: IN0 of LUT3_0 or CLK Input of DFF3
	49		
	50		
	51		
	52		
	53		
	54		OUT9: IN1 of LUT3_0 or Data of DFF3
	55		
7	56		
	57		
	58		
	59		
	60		OUT10: IN2 of LUT3_0 or nRST (nSET) of DFF3
	61		
	62		
	63		
8	64		
	65		
	66	LUT3_1 & DFF4	OUT11: IN0 of LUT3_1 or CLK Input of DFF4
	67		
	68		
	69		
	70		
	71		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
9	72	LUT3_1 & DFF4	OUT12: IN1 of LUT3_1 or Data of DFF4
	73		
	74		
	75		
	76		
	77		
	78		
	79		
A	80		OUT13: IN2 of LUT3_1 or nRST (nSET) of DFF4
	81		
	82		
	83		
	84	LUT3_2 & DFF5	OUT14: IN0 of LUT3_2 or CLK Input of DFF5
	85		
	86		
	87		
B	88		
	89		
	90		OUT15: IN1 of LUT3_2 or Data of DFF5
	91		
	92		
	93		
	94		
	95		
C	96		OUT16: IN2 of LUT3_2 or nRST (nSET) of DFF5
	97		
	98		
	99		
	100		
	101		
	102	LUT3_3 & DFF6	OUT17: IN0 of LUT3_3 or CLK Input of DFF6
	103		
D	104		
	105		
	106		
	107		
	108		OUT18: IN1 of LUT3_3 or Data of DFF6
	109		
	110		
	111		
E	112		
	113		
	114		OUT19: IN2 of LUT3_3 or nRST (nSET) of DFF6
	115		
	116		
	117		
	118		
	119		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F	120	LUT3_4 & DFF7	OUT20: IN0 of LUT3_4 or CLK Input of DFF7
	121		
	122		
	123		
	124		
	125		
	126		OUT21: IN1 of LUT3_4 or Data of DFF7
	127		
10	128		
	129		
	130		
	131		
	132		OUT22: IN2 of LUT3_4 or nRST (nSET) of DFF7
	133		
	134		
	135		
11	136		
	137		
	138	LUT3_5 & DFF8	OUT23: IN0 of LUT3_5 or CLK Input of DFF8
	139		
	140		
	141		
	142		
	143		
12	144		OUT24: IN1 of LUT3_5 or Data of DFF8
	145		
	146		
	147		
	148		
	149		
	150		OUT25: IN2 of LUT3_5 or nRST (nSET) of DFF8
	151		
13	152		
	153		
	154		
	155		
	156	LUT3_6 & DFF9	OUT26: IN0 of LUT3_6 or CLK Input of DFF9
	157		
	158		
	159		
14	160		
	161		
	162		OUT27: IN1 of LUT3_6 or Data of DFF9
	163		
	164		
	165		
	166		
	167		

Table 57: Register Map (Continued)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Signal Function</th><th rowspan="2">Register Bit Definition</th></tr>
<tr><th>Byte</th><th>Register Bit</th></tr>
<tr><td rowspan="8">15</td><td>168</td><td rowspan="6">LUT3_6 & DFF9</td><td rowspan="6">OUT28:
IN2 of LUT3_6 or nRST (nSET) of DFF9</td></tr>
<tr><td>169</td></tr>
<tr><td>170</td></tr>
<tr><td>171</td></tr>
<tr><td>172</td></tr>
<tr><td>173</td></tr>
<tr><td>174</td><td rowspan="18">LUT3_7 & DFF10</td><td rowspan="6">OUT29:
IN0 of LUT3_7 or CLK Input of DFF10</td></tr>
<tr><td>175</td></tr>
<tr><td rowspan="8">16</td><td>176</td></tr>
<tr><td>177</td></tr>
<tr><td>178</td></tr>
<tr><td>179</td></tr>
<tr><td>180</td><td rowspan="6">OUT30:
IN1 of LUT3_7 or Data of DFF10</td></tr>
<tr><td>181</td></tr>
<tr><td>182</td></tr>
<tr><td>183</td></tr>
<tr><td rowspan="8">17</td><td>184</td></tr>
<tr><td>185</td></tr>
<tr><td>186</td><td rowspan="6">OUT31:
IN2 of LUT3_7 or nRST (nSET) of DFF10</td></tr>
<tr><td>187</td></tr>
<tr><td>188</td></tr>
<tr><td>189</td></tr>
<tr><td>190</td></tr>
<tr><td>191</td></tr>
<tr><td rowspan="8">18</td><td>192</td><td rowspan="18">LUT3_8 & DFF11</td><td rowspan="6">OUT32:
IN0 of LUT3_8 or CLK Input of DFF11</td></tr>
<tr><td>193</td></tr>
<tr><td>194</td></tr>
<tr><td>195</td></tr>
<tr><td>196</td></tr>
<tr><td>197</td></tr>
<tr><td>198</td><td rowspan="6">OUT33:
IN1 of LUT3_8 or Data of DFF11</td></tr>
<tr><td>199</td></tr>
<tr><td rowspan="8">19</td><td>200</td></tr>
<tr><td>201</td></tr>
<tr><td>202</td></tr>
<tr><td>203</td></tr>
<tr><td>204</td><td rowspan="6">OUT34:
IN2 of LUT3_8 or nRST (nSET) of DFF11</td></tr>
<tr><td>205</td></tr>
<tr><td>206</td></tr>
<tr><td>207</td></tr>
<tr><td rowspan="8">1A</td><td>208</td></tr>
<tr><td>209</td></tr>
<tr><td>210</td><td rowspan="6">Multi_function4</td><td rowspan="6">OUT35:
IN0 of LUT3_12 or CLK Input of DFF16
Delay4 Input (or Counter4 nRST Input)</td></tr>
<tr><td>211</td></tr>
<tr><td>212</td></tr>
<tr><td>213</td></tr>
<tr><td>214</td></tr>
<tr><td>215</td></tr>
</table>

Table 57: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
1B	216	Multi_function4	OUT36: IN1 of LUT3_12 or nRST (nSET) of DFF16 Delay4 Input (or Counter4 nRST Input)
	217		
	218		
	219		
	220		
	221		
	222		OUT37: IN2 of LUT3_12 or Data of DFF16 Delay4 Input (or Counter4 nRST Input)
	223		
1C	224		
	225		
	226		
	227		
	228	Multi_function5	OUT38: IN0 of LUT3_13 or CLK Input of DFF17 Delay5 Input (or Counter5 nRST Input)
	229		
	230		
	231		
1D	232		
	233		
	234		OUT39: IN1 of LUT3_13 or nRST (nSET) of DFF17 Delay5 Input (or Counter5 nRST Input)
	235		
	236		
	237		
	238		
	239		
1E	240		OUT40: IN2 of LUT3_13 or Data of DFF17 Delay5 Input (or Counter5 nRST Input)
	241		
	242		
	243		
	244		
	245		
	246	Multi_function6	OUT41: IN0 of LUT3_14 or CLK Input of DFF18 Delay6 Input (or Counter6 nRST Input)
	247		
1F	248		
	249		
	250		
	251		
	252		OUT42: IN1 of LUT3_14 or nRST (nSET) of DFF18 Delay6 Input (or Counter6 nRST Input)
	253		
	254		
	255		
20	256		
	257		
	258		OUT43: IN2 of LUT3_14 or Data of DFF18 Delay6 Input (or Counter6 nRST Input)
	259		
	260		
	261		
	262		
	263		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
21	264	Multi_function7	OUT44: IN0 of LUT3_15 or CLK Input of DFF19 Delay7 Input (or Counter7 nRST Input)
	265		
	266		
	267		
	268		
	269		
	270		OUT45: IN1 of LUT3_15 or nRST (nSET) of DFF19 Delay7 Input (or Counter7 nRST Input)
	271		
22	272		
	273		
	274		
	275		
	276		OUT46: IN2 of LUT3_15 or Data of DFF19 Delay7 Input (or Counter7 nRST Input)
	277		
	278		
	279		
23	280		
	281		
	282	LUT3_16 & Pipe Delay (RIPP CNT)	OUT47: IN0 of LUT3_16 or Input of Pipe Delay or UP signal of RIPP CNT
	283		
	284		
	285		
	286		
	287		
24	288		OUT48: IN1 of LUT3_16 or nRST of Pipe Delay or nSET of RIPP CNT
	289		
	290		
	291		
	292		
	293		
	294		OUT49: IN2 of LUT3_16 or Clock of Pipe Delay_RIPP CNT
	295		
25	296		
	297		
	298		
	299		
	300	LUT4_DFF12	OUT50: IN0 of LUT4_0 or CLK Input of DFF12
	301		
	302		
	303		
26	304		
	305		
	306		OUT51: IN1 of LUT4_0 or Data of DFF12
	307		
	308		
	309		
	310		
	311		

Table 57: Register Map (Continued)

Address Byte	Register Bit	Signal Function	Register Bit Definition
27	312	LUT4_DFF12	OUT52: IN2 of LUT4_0 or nRST (nSET) of DFF12
	313		
	314		
	315		
	316		
	317		
	318		
	319		
28	320		OUT53: IN3 of LUT4_0
	321		
	322		
	323		
	324	Programmable delay	OUT54: Programmable delay/edge detect input
	325		
	326		
	327		
29	328		
	329		
	330	Filter/Edge Detect	OUT55: Filter/Edge detect input
	331		
	332		
	333		
	334		
	335		
2A	336	GPIO0	OUT56: GPIO0 DOUT
	337		
	338		
	339		
	340		
	341		
	342	GPIO1	OUT57: GPIO1 DOUT
	343		
2B	344		
	345		
	346		
	347		
	348	GPIO2	OUT58: GPIO2 DOUT
	349		
	350		
	351		
2C	352		
	353		
	354		OUT59: GPIO2 DOUT OE
	355		
	356		
	357		
	358		
	359		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
2D	360	GPIO3 DOUT and Input of Power Switch ON0	OUT60: GPIO3 DOUT and Input of Power Switch ON0
	361		
	362		
	363		
	364		
	365		
	366		OUT61: GPIO3 DOUT OE
	367		
2E	368		
	369		
	370		
	371		
	372	GPO0 and Input of Power Switch ON1	OUT62: GPO0 DOUT and Input of Power Switch ON1
	373		
	374		
	375		
2F	376		
	377		
	378	GPIO4	OUT63: GPIO4 DOUT
	379		
	380		
	381		
	382		
	383		
30	384		OUT64: GPIO4 DOUT OE
	385		
	386		
	387		
	388		
	389		
	390	GPIO5	OUT65: GPIO5 DOUT
	391		
31	392		
	393		
	394		
	395		
	396		OUT66: GPIO5 DOUT OE
	397		
	398		
	399		
32	400		
	401		
	402	GPIO6	OUT67: GPIO6 DOUT
	403		
	404		
	405		
	406		
	407		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
33	408	GPIO6	OUT68: GPIO6 DOUT OE
	409		
	410		
	411		
	412		
	413		
	414	GPIO7	OUT69: GPIO7 DOUT
	415		
34	416		
	417		
	418		
	419		
	420		OUT70: GPIO7 DOUT OE
	421		
	422		
	423		
35	424		
	425		
	426	GPIO8	OUT71: GPIO8 DOUT
	427		
	428		
	429		
	430		
	431		
36	432		OUT72: GPIO8 DOUT OE
	433		
	434		
	435		
	436		
	437		
	438	GPIO9	OUT73: GPIO9 DOUT
	439		
37	440		
	441		
	442		
	443		
	444		OUT74: GPIO9 DOUT OE
	445		
	446		
	447		
38	448		
	449		
	450	ACMP0H	OUT75: PWR UP of ACMP0H
	451		
	452		
	453		
	454		
	455		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
39	456	ACMP1H	OUT76: PWR UP of ACMP1H
	457		
	458		
	459		
	460		
	461		
	462	ACMP2L	OUT77: PWR UP of ACMP2L
	463		
3A	464		
	465		
	466		
	467		
	468	ACMP3L	OUT78: PWR UP of ACMP3L
	469		
	470		
	471		
3B	472		
	473		
	474	Temp Sensor	OUT79: Temp sensor, Vref Out_0, Vref Out_1 Power Up
	475		
	476		
	477		
	478		
	479		
3C	480	OSC0	OUT80: OSC0 ENABLE
	481		
	482		
	483		
	484		
	485		
	486	OSC1	OUT81: OSC1 ENABLE
	487		
3D	488		
	489		
	490		
	491		
	492	OSC2	OUT82: OSC2 ENABLE
	493		
	494		
	495		
3E	496		
	497		
	498	Multi_function0	OUT83: IN0 of LUT4_1 or CLK Input of DFF20 Delay0 Input (or Counter0 nRST Input)
	499		
	500		
	501		
	502		
	503		

Table 57: Register Map (Continued)

Address Byte	Register Bit	Signal Function	Register Bit Definition
3F	504	Multi_function0	OUT84: IN1 of LUT4_1 or nRST of DFF20 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source
	505		
	506		
	507		
	508		
	509		
	510		OUT85: IN2 of LUT4_1 or nSET of DFF20 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source KEEP Input of FSM0
	511		
40	512		
	513		
	514		
	515		
	516		OUT86: IN3 of LUT4_1 or Data of DFF20 Delay0 Input (or Counter0 nRST Input) UP Input of FSM0
	517		
	518		
	519		
41	520		
	521		
	522	Multi_function1	OUT87: IN0 of LUT3_9 or CLK Input of DFF13 Delay1 Input (or Counter1 nRST Input)
	523		
	524		
	525		
	526		
	527		
42	528		OUT88: IN1 of LUT3_9 or nRST (nSET) of DFF13 Delay1 Input (or Counter1 nRST Input)
	529		
	530		
	531		
	532		
	533		
	534		OUT89: IN2 of LUT3_9 or Data of DFF13 Delay1 Input (or Counter1 nRST Input)
	535		
43	536		
	537		
	538		
	539		
	540	Multi_function2	OUT90: IN0 of LUT3_10 or CLK Input of DFF14 Delay2 Input (or Counter2 nRST Input)
	541		
	542		
	543		
44	544		
	545		
	546		OUT91: IN1 of LUT3_10 or nRST (nSET) of DFF14 Delay2 Input (or Counter2 nRST Input)
	547		
	548		
	549		
	550		
	551		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
45	552	Multi_function2	OUT92: IN2 of LUT3_10 or Data of DFF14 Delay2 Input (or Counter2 nRST Input)
	553		
	554		
	555		
	556		
	557		
	558	Multi_function3	OUT93: IN0 of LUT3_11 or CLK Input of DFF15 Delay3 Input (or Counter3 nRST Input)
	559		
46	560		
	561		
	562		
	563		
	564		OUT94: IN1 of LUT3_11 or nRST (nSET) of DFF15 Delay3 Input (or Counter3 nRST Input)
	565		
	566		
	567		
47	568		
	569		
	570		OUT95: IN2 of LUT3_11 or Data of DFF15 Delay3 Input (or Counter3 nRST Input)
	571		
	572		
	573		
	574		
	575		
48	576	Matrix Input 0	GND
	577	Matrix Input 1	LUT2_0/DFF0 output
	578	Matrix Input 2	LUT2_1/DFF1 output
	579	Matrix Input 3	LUT2_2/DFF2 output
	580	Matrix Input 4	LUT2_3/PGen output
	581	Matrix Input 5	LUT3_0/DFF3 output
	582	Matrix Input 6	LUT3_1/DFF4 output
	583	Matrix Input 7	LUT3_2/DFF5 output
49	584	Matrix Input 8	LUT3_3/DFF6 output
	585	Matrix Input 9	LUT3_4/DFF7 output
	586	Matrix Input 10	LUT3_5/DFF8 output
	587	Matrix Input 11	LUT3_6/DFF9 output
	588	Matrix Input 12	LUT3_7/DFF10 output
	589	Matrix Input 13	LUT3_8/DFF11 output
	590	Matrix Input 14	CNT0 output
	591	Matrix Input 15	MF0_LUT4/DFF_OUT
4A	592	Matrix Input 16	CNT1 output
	593	Matrix Input 17	MF1_LUT3/DFF_OUT
	594	Matrix Input 18	CNT2 output
	595	Matrix Input 19	MF2_LUT3/DFF_OUT
	596	Matrix Input 20	CNT3 output
	597	Matrix Input 21	MF3_LUT3/DFF_OUT
	598	Matrix Input 22	CNT4 output
	599	Matrix Input 23	MF4_LUT3/DFF_OUT

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
4B	600	Matrix Input 24	CNT5 output
	601	Matrix Input 25	MF5_LUT3/DFF_OUT
	602	Matrix Input 26	CNT6 output
	603	Matrix Input 27	MF6_LUT3/DFF_OUT
	604	Matrix Input 28	CNT7 output
	605	Matrix Input 29	MF7_LUT3/DFF_OUT
	606	Matrix Input 30	LUT3_16/Ripple CNT/Pipe Delay_out0
	607	Matrix Input 31	Ripple CNT/Pipe Delay_out1
4C	608	Matrix Input 32	GPIO0 digital input or I2C_virtual_0 Input
	609	Matrix Input 33	GPIO1 digital input or I2C_virtual_1 Input
	610	Matrix Input 34	I2C_virtual_2 Input
	611	Matrix Input 35	I2C_virtual_3 Input
	612	Matrix Input 36	I2C_virtual_4 Input
	613	Matrix Input 37	I2C_virtual_5 Input
	614	Matrix Input 38	I2C_virtual_6 Input
	615	Matrix Input 39	I2C_virtual_7 Input
4D	616	Matrix Input 40	Ripple CNT_out2
	617	Matrix Input 41	LUT4_0/DFF12 output
	618	Matrix Input 42	Programmable Delay Edge Detect Output
	619	Matrix Input 43	Edge Detect Filter Output
	620	Matrix Input 44	GPI0 Digital Input
	621	Matrix Input 45	GPIO2 Digital Input
	622	Matrix Input 46	Power Switch ON0, GPIO3 Digital Input
	623	Matrix Input 47	GPIO4 Digital Input
4E	624	Matrix Input 48	GPIO5 Digital Input
	625	Matrix Input 49	GPIO6 Digital Input
	626	Matrix Input 50	GPIO7 Digital Input
	627	Matrix Input 51	GPIO8 Digital Input
	628	Matrix Input 52	GPIO9 Digital Input
	629	Matrix Input 53	OSC0 output 0
	630	Matrix Input 54	OSC1 output 0
	631	Matrix Input 55	OSC2 output
4F	632	Matrix Input 56	ACMP0H Output (normal speed)
	633	Matrix Input 57	ACMP1H Output (normal speed)
	634	Matrix Input 58	ACMP2L Output (low speed)
	635	Matrix Input 59	ACMP3L output (low speed)
	636	Matrix Input 60	OSC0 output 1
	637	Matrix Input 61	OSC1 output 1
	638	Matrix Input 62	Matrix nRST
	639	Matrix Input 63	V_{DD}

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
50	640	BG CHOP OFF	0: CHOP enable 1: chopper off
	641	BG Chopper clock test enable	1: enable
	642	Bandgap internal voltage output to IO enable	1: enable
	643	Bandgap power-down control	0: always on 1: power-down if no function enable it (ACMP, Vref, TS)
	644	ACMP1H external Vref0 source selection	0: from GPIO2 1: from GPO0
	645	ACMP2L external Vref1 source selection	0: from GPIO2 1: from GPO0
	646	ACMP3L external Vref1 source selection	0: from GPIO2 1: from GPO0
	647	ACMP3L wake sleep enable	1: enable 0: disable
51	648	VrefO0 register Power-On/Off	1: on 0: off
	649	VrefO0 power-down selection	0: come from register [648] 1: come from matrix out92
	650	VrefO1 register Power-On/Off	1: on 0: off
	651	ACMP0H hysteresis	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	652		
	653	Reserved	
	654	ACMP0_H input buffer enable	1: enable
	655	Reserved	
52	656	ACMP0H input tie to V_{DD} enable	1: enable
	657	ACMP1_H positive input come from AC-MP0_H's input mux output enable; 1:enable	
	658	Reserved	
	659	ACMP1H hysteresis	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	660		
	661	ACMP1H input buffer enable	1: enable
	662	Reserved	
	663	ACMP2L positive input come from ACMP0H's input mux output enable	1: enable
53	664	ACMP2L positive input come from ACMP1H's input mux output enable	1: enable
	665	ACMP2L hysteresis	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	666		
	667	Reserved	
	668	Reserved	
	669	ACMP3_L hysteresis	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	670		
	671	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
54	672	Reserved	
	673	ACMP3_L positive input come from ACMP2L's input mux output enable	1: enable
	674	Temp sensor register pdb control	0: Power-down 1: Power-On
	675	Temp sensor register pdb select	0: come from register 1: come from Matrix
	676	Temp sensor range select	0: range 1 (0.62V ~ 0.99V (TYP)) 1: range 2 (0.75V ~ 1.2V (TYP))
	677	Vref0 output OP	0: disable 1: enable
	678	Vref0 input selection	00: None 01: ACMP0H Vref 10: ACMP1H Vref 11: temp sensor
	679		
55	680	Vref1 output OP	0: disable 1: enable
	681	Vref1 input selection	00: None 01: ACMP2L Vref 10: ACMP3L Vref
	682		
	683	VBG fine tune selection	0000: 1.194, 0001:1.195, 0011:1.196, 0100:1.197, 0101:1.198, 0110:1.199 0111:1.2, 1000:1.201, 1001:1.202, 1010:1.203, 1011:1.204, 1100:1.205, 1101:1.206, 1110:1.207, 1111:1.208
	684		
	685		
	686		
	687	ACMP0H Wake/Sleep enable	
56	688	ACMP1H Wake/Sleep enable	
	689	ACMP Wake/Sleep time selection	0: short time 1: normal w/s
	690	ACMP0H 100 uA current source enable	
	691	Reserve for ACMP	
	692	Reserved	
	693	ACMP3L input come from Temp sensor output enable	
	694	VrefO1 power-down selection	0: come from register [650] 1: come from matrix OUT92
	695	ACMP2L wake sleep enable	0: disable 1: enable
57	696	ACMP0H Gain divider	ACMP gain divider select: 00: 1x 01:0.5x 10:0.33x 11:0.25x
	697		
	698	ACMP0H Vref0	ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/step = 32 mV 111111: External Vref
	699		
	700		
	701		
	702		
	703		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
58	704	ACMP1H Gain divider	ACMP gain divider select: 00: 1x 01:0.5x 10:0.33x 11:0.25x
	705		
	706	ACMP1H Vref0	ACMP Vref select: 000000: 32 mV ~ 1 11110: 2.016V/step = 32mV 111111: External Vref
	707		
	708		
	709		
	710		
	711		
59	712	ACMP2L Gain divider	ACMP gain divider select: 00: 1x 01:0.5x 10:0.33x 11:0.25x
	713		
	714	ACMP2L Vref1	ACMP Vref select: 000000: 32 mV ~ 111110: 2.016V/step = 32mV 111111: External Vref
	715		
	716		
	717		
	718		
	719		
5A	720	ACMP3L Gain divider	ACMP gain divider select: 00: 1x 01:0.5x 10:0.33x 11:0.25x
	721		
	722	ACMP3L Vref1	ACMP Vref select: 000000: 32 mV ~ 111110: 2.016V/step = 32mV 111112: External Vref
	723		
	724		
	725		
	726		
	727		
OSC1			
5B	728	OSC1 turn on by register	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	729	matrix power-down or on select	0: matrix down 1: matrix on
	730	external clock source enable	0: internal OSC1 1: external clock from GPIO2
	731	post divider ratio control OSC1	00: div 1 01: div 2 10: div 4 11: div 8
	732		
	733	matrix divider ratio control OSC1, OUT0	000: /1, 001:/2 , 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64
	734		
	735		
5C	736	matrix out enable OSC1, OUT0	0: disable 1: enable
	737	Reserved	
	738	Reserved	
	739	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
OSC2			
5C	740	OSC2 turn on by register	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	741	matrix power-down or on select	0: matrix down 1: matrix on
	742	external clock source enable	0: internal OSC2 1: external clock from GPIO8
	743	matrix out enable	0: disable 1: enable
5D	744	post divider ratio control OSC2	00: div 1 01: div 2 10: div 4 11: div 8
	745		
	746	matrix divider ratio control OSC2	000: /1, 001:/2 , 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64
	747		
	748		
	749	startup delay with 100 ns	0: enable 1: disable
OSC0			
5D	750	OSC0 turn on by register	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	751	matrix power-down or on select	0: matrix down 1: matrix on
5E	752	external clock source enable	0: internal OSC0 1: external clock from GPIO
	753	matrix out enable OSC0, OUT0	0: disable 1: enable
	754	post divider ratio control OSC0	00: div 1 01: div 2 10: div 4 11: div 8
	755		
	756	matrix divider ratio control OSC0, OUT0	000: /1, 001:/2 , 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64
	757		
	758		
	759	enable OSC0 output gating by wake_sleep signal (note: the wake_sleep clock is separated path, so it is not gated)	0: no gating 1: enable
5F	760	matrix divider ratio control OSC1, OUT1	000: /1, 001:/2 , 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64
	761		
	762		
	763	2nd output to matrix enable OSC1	0: disable 1: enable
	764	matrix divider ratio control OSC0, OUT1	000: /1, 001:/2 , 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64
	765		
	766		
	767	2nd output to matrix enable OSC0, OUT1	0: disable 1: enable

Table 57: Register Map (Continued)

Address Byte	Address Register Bit	Signal Function	Register Bit Definition
60	768	Reserved	
	769		
	770	Reserved	
	771	Reserved	
	772	Reserved	
	773	Reserved	
	774	Reserved	
	775	Reserved	
61	776	Reserved	
	777	Reserved	
	778	IO fast Pull-up/down enable	0: disable 1: enable
GPI0			
61	779	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	780		
	781	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	782		
	783	Pull-up/down selection	0: Pull-down 1: Pull-up
GPIO0			
62	784	input mode configuration	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger (when register [2032] = 1) 10: low voltage digital in 11: Reserved
	785		
	786	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	787		
	788	Pull-up/down selection	0: Pull-down 1: Pull-up
	789	I^2C mode selection	0: I2C fast mode+ (3.2x drivability) 1: I2C standard/fast mode
	790	I/O selection	0: digital input 1: digital output (3.2x Open-Drain NMOS)
GPIO1			
62	791	input mode configuration	00: digital without Schmitt Trigger 01: digital in with Schmitt Trigger (when register [2032] = 1) 10: low voltage digital in 11: Reserved
63	792		
	793	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	794		
	795	Pull-up/down selection	0: Pull-down 1: Pull-up
	796	I/O selection	0: digital input 1: digital output (3.2x Open-Drain NMOS)
	797	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
GPIO2			
63	798	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	799		
64	800	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	801		
	802	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	803		
	804	Pull-up/down selection	0: Pull-down 1: Pull-up
GPIO3			
64	805	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	806		
	807	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
65	808		
65	809	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	810		
	811	Pull-up/down selection	0: Pull-down 1: Pull-up
GPO0			
65	812	Reserved	
	813		
	814	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	815		
66	816	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	817		
	818	Pull-up/down selection	0: Pull-down 1: Pull-up
	819	output enable	0: output disable (input mode) 1: output enable
	820	4x drive	0: disable 1: enable
GPIO4			

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
66	821	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	822		
	823	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
67	824		
	825	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	826		
	827	Pull-up/down selection	0: Pull-down 1: Pull-up
	828	4x drive	0: disable 1: enable
GPIO5			
67	829	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	830		
	831	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
68	832		
	833	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	834		
	835	Pull-up/down selection	0: Pull-down 1: Pull-up
GPIO6			
68	836	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	837		
	838	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	839		
69	840	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	841		
	842	Pull-up/down selection	0: Pull-down 1: Pull-up
GPIO7			

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	**Register Bit**		
69	843	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	844		
	845	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	846		
	847	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
6A	848		
	849	Pull-up/down selection	0: Pull-down 1: Pull-up
GPIO8			
6A	850	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	851		
	852	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	853		
	854	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	855		
6B	856	Pull-up/down selection	0: Pull-down 1: Pull-up
GPIO9			
6B	857	input mode configuration	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	858		
	859	output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	860		
	861	Pull-up/down resistance selection	00: floating 01: 10K 10: 100K 11: 1M
	862		
	863	Pull-up/down selection	0: Pull-down 1: Pull-up
6C	864	Reserved	
	865	Reserved	
	866	Reserved	
	867	Reserved	
	868	Reserved	
	869	Reserved	
	870	Reserved	
	871	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
6D	872	Reserved	
	873	Reserved	
	874	Reserved	
	875	Reserved	
	876	Reserved	
	877	Reserved	
	878	Reserved	
	879	Reserved	
6E	880	Reserved	
	881	Reserved	
	882	Reserved	
	883	Reserved	
	884	Reserved	
	885	Reserved	
	886	Reserved	
	887	Reserved	
6F	888	Reserved	
	889	Reserved	
	890	Reserved	
	891	Reserved	
	892	Reserved	
	893	Reserved	
	894	Reserved	
	895	Reserved	
70	896	Reserved	
	897	Reserved	
	898	Reserved	
	899	Reserved	
	900	Reserved	
	901	Reserved	
	902	Reserved	
	903	Reserved	
71	904	Reserved	
	905	Reserved	
	906	Reserved	
	907	Reserved	
	908	Reserved	
	909	Reserved	
	910	Reserved	
	911	Reserved	
72	912	Reserved	
	913	Reserved	
	914	Reserved	
	915	Reserved	
	916	Reserved	
	917	Reserved	
	918	Reserved	
	919	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
73	920	Reserved	
	921	Reserved	
	922	Reserved	
	923	Reserved	
	924	Reserved	
	925	Reserved	
	926	Reserved	
	927	Reserved	
74	928	Reserved	
	929	Reserved	
	930	Reserved	
	931	Reserved	
	932	Reserved	
	933	Reserved	
	934	Reserved	
	935	Reserved	
75	936	Reserved	
	937	Reserved	
	938	Reserved	
	939	Reserved	
	940	Reserved	
	941	Reserved	
	942	Reserved	
	943	Reserved	
76	944	Reserved	
	945	Reserved	
	946	Reserved	
	947	Reserved	
	948	Reserved	
	949	Reserved	
	950	Reserved	
	951	Reserved	
77	952	Reserved	
	953	Reserved	
	954	Reserved	
	955	Reserved	
	956	Reserved	
	957	Reserved	
	958	Reserved	
	959	Reserved	
78	960	Reserved	
	961	Reserved	
	962	Reserved	
	963	Reserved	
	964	Reserved	
	965	Reserved	
	966	Reserved	
	967	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
79	968	Reserved	
	969	Reserved	
	970	Reserved	
	971	Reserved	
	972	Reserved	
	973	Reserved	
	974	Reserved	
	975	Reserved	
7A	976	Reserved	
	977	Reserved	
	978	Reserved	
	979	Reserved	
	980	Reserved	
	981	Reserved	
	982	Reserved	
	983	Reserved	
7B	984	Reserved	
	985	Reserved	
	986	Reserved	
	987	Reserved	
	988	Reserved	
	989	Reserved	
	990	Reserved	
	991	Reserved	
7C	992	Reserved	
	993	Reserved	
	994	Reserved	
	995	Reserved	
	996	Reserved	
	997	Reserved	
	998	Reserved	
	999	Reserved	
7D	1000	Reserved	
	1001	Reserved	
	1002	Reserved	
	1003	Reserved	
	1004	Reserved	
	1005	Reserved	
	1006	Reserved	
	1007	Reserved	
7E	1008	Reserved	
	1009	Reserved	
	1010	Reserved	
	1011	Reserved	
	1012	Reserved	
	1013	Reserved	
	1014	Reserved	
	1015	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
7F	1016	Reserved	
	1017	Reserved	
	1018	Reserved	
	1019	Reserved	
	1020	Reserved	
	1021	Reserved	
	1022	Reserved	
	1023	Reserved	
80	1030:1024	Single 4-bit LUT	0000000: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	0010000: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DLY_IN - LOW)
		Single CNT/DLY	0000001: Matrix A - UP (CNT); Matrix B - KEEP (CNT); Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (CNT) (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	0000010: Matrix A - DLY_IN; Matrix B - In2; Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In3)
		CNT/DLY → DFF	0010010: Matrix A - DLY_IN; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	0100010: Matrix A - DLY_IN; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In3; In2 - LOW)
		CNT/DLY → DFF	0110010: Matrix A - DLY_IN; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to D; nSET - HIGH)
		CNT/DLY → LUT	1000010: Matrix A - DLY_IN; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - In0 (DLY_OUT connected to In3; In1 - LOW)
		CNT/DLY → DFF	1010010: Matrix A - DLY_IN; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DLY_OUT connected to D; nRST - HIGH)
		CNT/DLY → LUT	0000110: Matrix A - In3; Matrix B - DLY_IN; Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	0010110: Matrix A - D; Matrix B - DLY_IN; Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to nSET)
		CNT/DLY → LUT	1000110: Matrix A - In3; Matrix B - DLY_IN; Matrix C - EXT_CLK (CNT); Matrix D - In0 (DLY_OUT connected to In2; In1 - LOW)

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
80	1030:1024	CNT/DLY → DFF	1010110: Matrix A - D; Matrix B - DLY_IN; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DLY_OUT connected to nSET; nRST - HIGH)
		CNT/DLY → LUT	0001010: Matrix A - In3; Matrix B - In2; Matrix C - DLY_IN; Matrix D - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	0011010: Matrix A - D; Matrix B - nSET; Matrix C - DLY_IN; Matrix D - CLK (DLY_OUT connected to nRST)
		CNT/DLY → LUT	0101010: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - DLY_IN; Matrix D - In0 (DLY_OUT connected to In1; In2 - LOW)
		CNT/DLY → DFF	0111010: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - DLY_IN; Matrix D - CLK (DLY_OUT connected to nRST; nSET - HIGH)
		CNT/DLY → LUT	0001110: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	0011110: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - DLY_IN (DLY_OUT connected to CLK)
		CNT/DLY → LUT	0101110: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - DLY_IN (DLY_OUT connected to In0; In2 - LOW)
		CNT/DLY → DFF	0111110: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - DLY_IN (DLY_OUT connected to CLK; nSET - HIGH)
		CNT/DLY → LUT	1001110: Matrix A - In3; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (DLY_OUT connected to In0; In1 - LOW)
		CNT/DLY → DFF	1011110: Matrix A - D; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (DLY_OUT connected to CLK; nRST - HIGH)
		LUT → CNT/DLY	0000011: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	0010011: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DFF_OUT connected to DLY_IN)
		LUT → CNT/DLY	0100011: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - In0 (LUT_OUT connected to DLY_IN; In2 - LOW)

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
80	1030:1024	DFF → CNT/DLY	0110011: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - CLK (DFF_OUT connected to DLY_IN; nSET - HIGH)
		LUT → CNT/DLY	1000011: Matrix A - In3; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - In0 (LUT_OUT connected to DLY_IN; In1 - LOW)
		DFF → CNT/DLY	1010011: Matrix A - D; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DFF_OUT connected to DLY_IN; nRST - HIGH)
	1031	DLY/CNT0 Mode Selection	00: DLY 01: one shot 10: frequency det 11: CNT register [1040] = 0
81	1032		
	1033	DLY/CNT0 edge Mode Selection	00: both edge 01: falling edge 10: rising edge 11: High Level Reset (only in CNT mode)
	1034		
	1035	DLY/CNT0 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2 K/262144; 1101: CNT7_END; 1110: External; 1111: Not used
	1036		
	1037		
	1038		
	1039	FSM0 SET/RST Selection	0: Reset to 0 1: Set to data
82	1040	CNT0 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers [1032:1031] = 00)
	1041	UP signal SYNC selection	0: bypass 1: after two DFF
	1042	Keep signal SYNC selection	0: bypass 1: after two DFF
	1043	CNT0 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1044		
	1045	Wake sleep power-down state selection	0: low 1: high
	1046	wake sleep mode selection	0: Default Mode 1: Wake Sleep Mode (registers [1032:1031] = 11)
	1047	CNT0 output pol selection	0: Default Output 1: Inverted Output

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
83	1048	CNT0 CNT mode SYNC selection	0: bypass 1: after two DFF
83	1053:1049	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
83	1054	CNT1 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1055		
84	1056		
	1057		
	1058	CNT1 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1059		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
84	1060 1061 1062 1063	DLY/CNT1 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT0_END; 1110: External; 1111: Not used
85	1064	CNT1 output pol selection	0: Default Output 1: Inverted Output
	1065	CNT1 CNT mode SYNC selection	0: bypass 1: after two DFF
	1066	CNT1 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers[1057:1054]=0000/0001/0010)
	1071:1067	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
86	1072	CNT2 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1073		
	1074	CNT2 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1075		
	1076		
	1077		
	1078	DLY/CNT2 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT1_END; 1110: External; 1111: Not used
	1079		
87	1080		
	1081		
	1082	CNT2 output pol selection	0: Default Output, 1: Inverted Output
	1083	CNT2 CNT mode SYNC selection	0: bypass; 1: after two DFF
	1084	CNT2 DLY EDET FUNCTION Selection	0: normal; 1: DLY function edge detection(registers[1077:1074] = 0000/0001/0010)
	1085	CNT3 initial value selection	00:bypass the initial; 01: initial 0; 10: initial 1; 11: initial 1
	1086		
	1087	Multi3 register configure	refer to byte 88
88	1088	CNT3 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1089		
	1090		
	1091		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
88	1087, 1093:1092, 1095:1094	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
89	1096 1097 1098 1099	DLY/CNT3 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT2_END; 1110: External; 1111: Not used
	1100	CNT3 output pol selection	0: Default Output 1: Inverted Output
	1101	CNT3 CNT mode SYNC selection	0: bypass 1: after two DFF
	1102	CNT3 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers[1091:1088]=0000/0001/0010)
	1103	CNT4 CNT mode SYNC selection	0: bypass 1: after two DFF

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
8A	1104 1105	CNT4 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1106	CNT4 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers[1119:1116]=0000/0001/0010)
	1111:1107	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
8B	1112 1113 1114 1115	DLY/CNT4 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT3_END; 1110: External; 1111: Not used

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
8B	1116 1117 1118 1119	CNT4 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
8C	1120	CNT4 output pol selection	0: Default Output 1: Inverted Output
	1121 1122 1123 1124	CNT5 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1125	CNT5 output pol selection	0: Default Output 1: Inverted Output
	1134, 1127:1126, 1133:1132	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
8C	1134, 1127:1126, 1133:1132	CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
8D	1128 1129 1130 1131	DLY/CNT5 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT4_END; 1110: External; 1111: Not used
	1135	CNT5 DLY EDET FUNCTION Selection	0: normal; 1: DLY function edge detection (registers[1124:1121]=0000/0001/0010)
8E	1136	CNT5 CNT mode SYNC selection	0: bypass; 1: after two DFF
	1137 1138	CNT5 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1139 1140 1141 1142	CNT6 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1143	CNT6 output pol selection	0: Default Output 1: Inverted Output

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
8F	1144 1145 1146 1147	DLY/CNT6 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT5_END; 1110: External; 1111: Not used
8F	1152, 1149:1148, 1151:1150	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
8F	1152, 1149:1148, 1151:1150	Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
8F	1152, 1149:1148, 1151:1150	Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
8F	1152, 1149:1148, 1151:1150	CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
8F	1152, 1149:1148, 1151:1150	CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
8F	1152, 1149:1148, 1151:1150	CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
8F	1152, 1149:1148, 1151:1150	CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
8F	1152, 1149:1148, 1151:1150	CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
8F	1152, 1149:1148, 1151:1150	CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
8F	1152, 1149:1148, 1151:1150	LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
90	1152, 1149:1148, 1151:1150	DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
90	1153	CNT6 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers[1142:1139]=0000/ 0001/0010)
90	1154	CNT6 CNT mode SYNC selection	0: bypass 1: after two DFF
90	1155 1156	CNT6 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
90	1157 1158	CNT7 initial value selection	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
90	1159	CNT7 CNT mode SYNC selection	0: bypass 1: after two DFF

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
91	1160	CNT7 DLY EDET FUNCTION Selection	0: normal 1: DLY function edge detection (registers [1174:1171]=0000/0001/0010)
	1161, 1165:1162	Single 3-bit LUT	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
91	1166 1167	DLY/CNT7 Clock Source Select	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT6_END; 1110: External; 1111: Not used
92	1168 1169		
	1170	CNT7 output pol selection	0: Default Output 1: Inverted Output
	1171 1172 1173 1174	CNT7 function and edge mode selection	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1175	Reserved	
93	1176 1177 1178 1179 1180 1181 1182 1183	Multi0_LUT4_DFF setting	[15]:LUT4_1 [15]/DFF20 or LATCH Select 0: DFF function, 1: LATCH function [14]:LUT4_1 [14]/DFF20 Output Select 0: Q output, 1: QB output [13]:LUT4_1 [13]/DFF20 Initial Polarity Select 0: Low, 1: High [12:0]:LUT4_1 [12:0]
94	1184 1185 1186 1187 1188 1189 1190 1191		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
95	1192	REG_CNT0_D[15:0]	Data[15:0]
	1193		
	1194		
	1195		
	1196		
	1197		
	1198		
	1199		
96	1200		
	1201		
	1202		
	1203		
	1204		
	1205		
	1206		
	1207		
97	1208	Multi1_LUT3_DFF setting	[7]:LUT3_9 [7]/DFF13 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_9 [6]/DFF13 Output Select 0: Q output, 1: QB output [5]:LUT3_9 [5]/DFF13 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_9 [4]/DFF13 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_9 [3:0]
	1209		
	1210		
	1211		
	1212		
	1213		
	1214		
	1215		
98	1216	REG_CNT1_D[7:0]	Data[7:0]
	1217		
	1218		
	1219		
	1220		
	1221		
	1222		
	1223		
99	1224	Multi2_LUT3_DFF setting	[7]:LUT3_10 [7]/DFF14 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_10[6]/DFF14 Output Select 0: Q output, 1: QB output [5]:LUT3_10 [5]/DFF14 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_10 [4]/DFF14 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_10 [3:0]
	1225		
	1226		
	1227		
	1228		
	1229		
	1230		
	1231		
9A	1232	REG_CNT2_D[7:0]	Data[7:0]
	1233		
	1234		
	1235		
	1236		
	1237		
	1238		
	1239		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
9B	1240	Multi3_LUT3_DFF setting	[7]:LUT3_11 [7]/DFF15 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_11[6]/DFF15 Output Select 0: Q output, 1: QB output [5]:LUT3_11 [5]/DFF15 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_11 [4]/DFF15 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_11 [3:0]
	1241		
	1242		
	1243		
	1244		
	1245		
	1246		
	1247		
9C	1248	REG_CNT3_D[7:0]	Data[7:0]
	1249		
	1250		
	1251		
	1252		
	1253		
	1254		
	1255		
9D	1256	Multi4_LUT3_DFF setting	[7]:LUT3_12 [7]/DFF16 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_12[6]/DFF16 Output Select 0: Q output, 1: QB output [5]:LUT3_12 [5]/DFF16 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_12 [4]/DFF16 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_12 [3:0]
	1257		
	1258		
	1259		
	1260		
	1261		
	1262		
	1263		
9E	1264	REG_CNT4_D[7:0]	Data[7:0]
	1265		
	1266		
	1267		
	1268		
	1269		
	1270		
	1271		
9F	1272	Multi5_LUT3_DFF setting	[7]:LUT3_13 [7]/DFF17 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_13[6]/DFF17 Output Select 0: Q output, 1: QB output [5]:LUT3_13 [5]/DFF17 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_13 [4]/DFF17 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_13 [3:0]
	1273		
	1274		
	1275		
	1276		
	1277		
	1278		
	1279		
A0	1280	REG_CNT5_D[7:0]	Data[7:0]
	1281		
	1282		
	1283		
	1284		
	1285		
	1286		
	1287		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
A1	1288 1289 1290 1291 1292 1293 1294 1295	Multi6_LUT3_DFF setting	[7]:LUT3_14 [7]/DFF18 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_14[6]/DFF18 Output Select 0: Q output, 1: QB output [5]:LUT3_14 [5]/DFF18 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_14 [4]/DFF18 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_14 [3:0]
A2	1296 1297 1298 1299 1300 1301 1302 1303	REG_CNT6_D[7:0]	Data[7:0]
A3	1304 1305 1306 1307 1308 1309 1310 1311	Multi7_LUT3_DFF setting	[7]:LUT3_15 [7]/DFF19 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_15[6]/DFF19 Output Select 0: Q output, 1: QB output [5]:LUT3_15 [5]/DFF19 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_15 [4]/DFF19 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_15 [3:0]
A4	1312 1313 1314 1315 1316 1317 1318 1319	REG_CNT7_D[7:0]	Data[7:0]
A5	1320 1321 1322 1323 1324 1325 1326 1327	CNT0 (16bits) Counted Value	Virtual Input
A6	1328 1329 1330 1331 1332 1333 1334 1335		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
A7	1336	CNT6 (8bits) Counted Value	Virtual Input
	1337		
	1338		
	1339		
	1340		
	1341		
	1342		
	1343		
A8	1344	CNT7 (8bits) Counted Value	Virtual Input
	1345		
	1346		
	1347		
	1348		
	1349		
	1350		
	1351		
A9	1352	LUT3_1_DFF4 setting	[7]:LUT3_1 [7]/DFF4 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_1 [6]/DFF4 Output Select 0: Q output, 1: QB output [5]:LUT3_1 [5]/DFF4 Initial Polarity Select 0: Low, 1: High [4]:LUT3_1 [4]/DFF4 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_1 [3]/DFF4 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_1 [2:0]
	1353		
	1354		
	1355		
	1356		
	1357		
	1358		
	1359		
AA	1360	LUT3_2_DFF5 setting	[7]:LUT3_2 [7]/DFF5 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_2 [6]/DFF5 Output Select 0: Q output, 1: QB output [5]:LUT3_2 [5]/DFF5 Initial Polarity Select 0: Low, 1: High [4]:LUT3_2 [4]/DFF5 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_2 [3]/DFF5 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_2 [2:0]
	1361		
	1362		
	1363		
	1364		
	1365		
	1366		
	1367		
AB	1368	LUT3_3_DFF6 setting	[7]:LUT3_3 [7]/DFF6 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_3 [6]/DFF6 Output Select 0: Q output, 1: QB output [5]:LUT3_3 [5]/DFF6 Initial Polarity Select 0: Low, 1: High [4]:LUT3_3 [4]/DFF6 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_3 [3]/DFF6 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_3 [2:0]
	1369		
	1370		
	1371		
	1372		
	1373		
	1374		
	1375		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
AC	1376	LUT3_4_DFF7 setting	[7]:LUT3_4 [7]/DFF7 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_4 [6]/DFF7 Output Select 0: Q output, 1: QB output [5]:LUT3_4 [5]/DFF7 Initial Polarity Select 0: Low, 1: High [4]:LUT3_4 [4]/DFF7 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_4 [3]/DFF7 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_4 [2:0]
	1377		
	1378		
	1379		
	1380		
	1381		
	1382		
	1383		
AD	1384	LUT2_3_VAL or PGen_data	LUT2_3[3:0] or PGen 4bit counter data[3:0]
	1385		
	1386		
	1387		
	1388	LUT3_1 or DFF4 Select	0: LUT3_1 1: DFF4
	1389	LUT3_2 or DFF5 Select	0: LUT3_2 1: DFF5
	1390	LUT3_3 or DFF6 Select	0: LUT3_3 1: DFF6
	1391	LUT3_4 or DFF7 Select	0: LUT3_4 1: DFF7
AE	1392	PGen data	PGen Data[15:0]
	1393		
	1394		
	1395		
	1396		
	1397		
	1398		
	1399		
AF	1400		
	1401		
	1402		
	1403		
	1404		
	1405		
	1406		
	1407		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
B0	1408	LUT2_3 or PGen Select	0: LUT2_3 1: PGen
	1409	Active level selection for RST/SET for LUT2_3 or PGen	0: Active low level reset/set 1: Active high level reset/set
	1410	Active level selection for RST/SET for LUT3_16 or Pipe Delay/RIPP CNT	0: Active low level reset/set 1: Active high level reset/set
	1411	Out of LUT3_16 or Out0 of Pipe Delay/RIPP CNT Select	0: LUT3_16 1: OUT0 of Pipe Delay or RIPP CNT
	1412	PIPE_RIPP_CNT_S	0: Pipe delay mode selection 1: Ripple Counter mode selection
	1413	Pipe Delay OUT1 Polarity Select	0: Non-inverted 1: Inverted
	1414	LUT4_0 or DFF12 Select	0: LUT4_0 1: DFF12
	1415	LUT3_0 or DFF3 Select	0: LUT3_0 1: DFF3
B1	1416	LUT value or pipe delay out sel or nSET/END value	[7:4]: LUT3_8 [7:4]/REG_S1[3:0] pipe delay out1 sel [3:0]: LUT3_8 [3:0]/REG_S0[3:0] pipe delay out0 sel at RIPP CNT mode: bit[1418:1416] is the nSET value bit[1421:1419] is the END value bit[1422] is the range control: 0 full cycle, 1 range cycle bit[1423] Not used
	1417		
	1418		
	1419		
	1420		
	1421		
	1422		
	1423		
B2	1424	LUT4_0_DFF12 setting	[15]:LUT4_0 [15]/DFF12 or LATCH Select 0: DFF function, 1: LATCH function [14]:LUT4_0 [14]/DFF12 Output Select 0: Q output, 1: QB output [13]:LUT4_0 [13]/DFF12 Initial Polarity Select 0: Low, 1: High [12]:LUT4_0 [12]/DFF12 stage selection 0: Q of first DFF; 1 Q of second DFF [11]:LUT4_0 [11]/DFF12 0: nRST from Matrix Output, 1: nSET from Matrix Output [10]:LUT4_0 [10]/DFF12 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [9:0]: LUT4_0 [9:0]
	1425		
	1426		
	1427		
	1428		
	1429		
	1430		
	1431		
B3	1432		
	1433		
	1434		
	1435		
	1436		
	1437		
	1438		
	1439		
B4	1440	LUT3_0_DFF3 setting	[7]:LUT3_0 [7]/DFF3 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_0 [6]/DFF3 Output Select 0: Q output, 1: QB output [5]:LUT3_0 [5]/DFF3 Initial Polarity Select 0: Low, 1: High [4]:LUT3_0 [4]/DFF3stage selection 0: Q of first DFF; 1 Q of second DFF [3]:LUT3_0 [3]/DFF3 0: nRST from Matrix Output, 1: nSET from Matrix Output [2]:LUT3_0 [2]/DFF3 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [1:0]: LUT3_0 [1:0]
	1441		
	1442		
	1443		
	1444		
	1445		
	1446		
	1447		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
B5	1448	Filter or Edge Detector selection	0, filter 1, edge det
	1449	Output Polarity Select	0: output non-invert 1: output invert
	1450	Select the edge mode	00: Rising Edge Det 01: Falling Edge Det 10: Both Edge Det 11: Both Edge DLY
	1451		
	1452	Delay Value Select for Programmable Delay & Edge Detector	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns
	1453		
	1454	Select the Edge Mode of Programmable Delay & Edge Detector	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
	1455		
B6	1456	LUT3_5_DFF8 setting	[7]:LUT3_5 [7]/DFF8 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_5 [6]/DFF8 Output Select 0: Q output, 1: QB output [5]:LUT3_5 [5]/DFF8 Initial Polarity Select 0: Low, 1: High [4]:LUT3_5 [4]/DFF8 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_5 [3]/DFF8 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_5 [2:0]
	1457		
	1458		
	1459		
	1460		
	1461		
	1462		
	1463		
B7	1464	LUT3_6_DFF9 setting	[7]:LUT3_6 [7]/DFF9 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_6 [6]/DFF9 Output Select 0: Q output, 1: QB output [5]:LUT3_6 [5]/DFF9 Initial Polarity Select 0: Low, 1: High [4]:LUT3_6 [4]/DFF9 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_6 [3]/DFF9 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_6 [2:0]
	1465		
	1466		
	1467		
	1468		
	1469		
	1470		
	1471		
B8	1472	LUT3_7_DFF10 setting	[7]:LUT3_7 [7]/DFF10 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_7 [6]/DFF10 Output Select 0: Q output, 1: QB output [5]:LUT3_7 [5]/DFF10 Initial Polarity Select 0: Low, 1: High [4]:LUT3_7 [4]/DFF10 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_7 [3]/DFF10 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_7 [2:0]
	1473		
	1474		
	1475		
	1476		
	1477		
	1478		
	1479		
B9	1480	LUT3_8_DFF11 setting	[7]:LUT3_8 [7]/DFF11 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_8 [6]/DFF11 Output Select 0: Q output, 1: QB output [5]:LUT3_8 [5]/DFF11 Initial Polarity Select 0: Low, 1: High [4]:LUT3_8 [4]/DFF11 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_8 [3]/DFF11 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_8 [2:0]
	1481		
	1482		
	1483		
	1484		
	1485		
	1486		
	1487		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
BA	1488	LUT2_0 or DFF0 Select	0: LUT2_0 1: DFF0
	1489	LUT2_1 or DFF1 Select	0: LUT2_1 1: DFF1
	1490	LUT2_2 or DFF2 Select	0: LUT2_2 1: DFF2
	1491	Reserved	
	1492	LUT3_5 or DFF8 Select	0: LUT3_5 1: DFF8
	1493	LUT3_6 or DFF9 Select	0: LUT3_6 1: DFF9
	1494	LUT3_7 or DFF10 Select	0: LUT3_7 1: DFF10
	1495	LUT3_8 or DFF11 Select	0: LUT3_8 1: DFF11
BB	1496 1497 1498 1499	LUT2_0/DFF0 setting	[3]:LUT2_0 [3]/DFF0 or LATCH Select 0: DFF function, 1: LATCH function [2]:LUT2_0 [2]/DFF0 Output Select 0: Q output, 1: QB output [1]:LUT2_0 [1]/DFF0 Initial Polarity Select 0: Low, 1: High [0]:LUT2_0 [0]
	1500 1501 1502 1503	LUT2_1/DFF1 setting	[3]:LUT2_1 [3]/DFF1 or LATCH Select 0: DFF function, 1: LATCH function [2]:LUT2_1 [2]/DFF1 Output Select 0: Q output, 1: QB output [1]:LUT2_1 [1]/DFF1 Initial Polarity Select 0: Low, 1: High [0]:LUT2_1 [0]
BC	1504 1505 1506 1507	LUT2_2/DFF2 setting	[3]:LUT2_2 [3]/DFF2 or LATCH Select 0: DFF function, 1: LATCH function [2]:LUT2_2 [2]/DFF2 Output Select 0: Q output, 1: QB output [1]:LUT2_2 [1]/DFF2 Initial Polarity Select 0: Low, 1: High [0]:LUT2_2 [0]
	1508	Reserved	
	1509		
	1510		
	1511		
BD	1512		
	1513		
	1514		
	1515		
	1516		
	1517		
	1518		
	1519		

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
BE	1520	Reserved	
	1521	Reserved	
	1522	Reserved	
	1523	Reserved	
	1524	Reserved	
	1525		
	1526		
	1527		
BF	1528	Reserved	
	1529	Reserved	
	1530	Reserved	
	1531	Reserved	
	1532	Reserved	
	1533	Reserved	
	1534	Reserved	
	1535	Reserved	
C0	1536	Reserved	
	1537	Reserved	
	1538	Reserved	
	1539	Reserved	
	1540	Reserved	
	1541	Reserved	
	1542	Reserved	
	1543	Reserved	
C1	1544	Reserved	
	1545	Reserved	
	1546	Reserved	
	1547	Reserved	
	1548	Reserved	
	1549	Reserved	
	1550	Reserved	
	1551	Reserved	
C2	1552	Reserved	
	1553	Reserved	
	1554	Reserved	
	1555	Reserved	
	1556	Reserved	
	1557	Reserved	
	1558	Reserved	
	1559	Reserved	
C3	1560	Reserved	
	1561	Reserved	
	1562	Reserved	
	1563	Reserved	
	1564	Reserved	
	1565	Reserved	
	1566	Reserved	
	1567	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
C4	1568	Reserved	
	1569	Reserved	
	1570	Reserved	
	1571	Reserved	
	1572	Reserved	
	1573	Reserved	
	1574	Reserved	
	1575	Reserved	
C5	1576	Reserved	
	1577	Reserved	
	1578	Reserved	
	1579	Reserved	
	1580	Reserved	
	1581	Reserved	
	1582	Reserved	
	1583	Reserved	
C6	1584	Reserved	
	1585	Reserved	
	1586	Reserved	
	1587	Reserved	
	1588	Reserved	
	1589	Reserved	
	1590	Reserved	
	1591	Reserved	
C7	1592	Reserved	
	1593	Reserved	
	1594	Reserved	
	1595	Reserved	
	1596	Reserved	
	1597	Reserved	
	1598	Reserved	
	1599	Reserved	
C8	1600	Reserved	
	1601	Reserved	
	1602	Reserved	
	1603	Reserved	
	1604	Reserved	
	1605	Reserved	
	1606	Reserved	
	1607	Reserved	
C9	1608	Reserved	
	1609	Reserved	
	1610	Reserved	
	1611	Reserved	
	1612	Reserved	
	1613	Reserved	
	1614	Reserved	
	1615	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
CA	1616	Reserved	
	1617	Reserved	
	1618	Reserved	
	1619	Reserved	
	1620	Reserved	
	1621	Reserved	
	1622	Reserved	
	1623	Reserved	
CB	1624	Reserved	
	1625	Reserved	
	1626	Reserved	
	1627	Reserved	
	1628	Reserved	
	1629	Reserved	
	1630	Reserved	
	1631	Reserved	
CC	1632	Reserved	
	1633	Reserved	
	1634	Reserved	
	1635	Reserved	
	1636	Reserved	
	1637	Reserved	
	1638	Reserved	
	1639	Reserved	
CD	1640	Reserved	
	1641	Reserved	
	1642	Reserved	
	1643	Reserved	
	1644	Reserved	
	1645	Reserved	
	1646	Reserved	
	1647	Reserved	
CE	1648	Reserved	
	1649	Reserved	
	1650	Reserved	
	1651	Reserved	
	1652	Reserved	
	1653	Reserved	
	1654	Reserved	
	1655	Reserved	
CF	1656	Reserved	
	1657	Reserved	
	1658	Reserved	
	1659	Reserved	
	1660	Reserved	
	1661	Reserved	
	1662	Reserved	
	1663	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
D0	1664	Reserved	
	1665	Reserved	
	1666	Reserved	
	1667	Reserved	
	1668	Reserved	
	1669	Reserved	
	1670	Reserved	
	1671	Reserved	
D1	1672	Reserved	
	1673	Reserved	
	1674	Reserved	
	1675	Reserved	
	1676	Reserved	
	1677	Reserved	
	1678	Reserved	
	1679	Reserved	
D2	1680	Reserved	
	1681	Reserved	
	1682	Reserved	
	1683	Reserved	
	1684	Reserved	
	1685	Reserved	
	1686	Reserved	
	1687	Reserved	
D3	1688	Reserved	
	1689	Reserved	
	1690	Reserved	
	1691	Reserved	
	1692	Reserved	
	1693	Reserved	
	1694	Reserved	
	1695	Reserved	
D4	1696	Reserved	
	1697	Reserved	
	1698	Reserved	
	1699	Reserved	
	1700	Reserved	
	1701	Reserved	
	1702	Reserved	
	1703	Reserved	
D5	1704	Reserved	
	1705	Reserved	
	1706	Reserved	
	1707	Reserved	
	1708	Reserved	
	1709	Reserved	
	1710	Reserved	
	1711	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
D6	1712	Reserved	
	1713	Reserved	
	1714	Reserved	
	1715	Reserved	
	1716	Reserved	
	1717	Reserved	
	1718	Reserved	
	1719	Reserved	
D7	1720	Reserved	
	1721	Reserved	
	1722	Reserved	
	1723	Reserved	
	1724	Reserved	
	1725	Reserved	
	1726	Reserved	
	1727	Reserved	
D8	1728	Reserved	
	1729	Reserved	
	1730	Reserved	
	1731	Reserved	
	1732	Reserved	
	1733	Reserved	
	1734	Reserved	
	1735	Reserved	
D9	1736	Reserved	
	1737	Reserved	
	1738	Reserved	
	1739	Reserved	
	1740	Reserved	
	1741	Reserved	
	1742	Reserved	
	1743	Reserved	
DA	1744	Reserved	
	1745	Reserved	
	1746	Reserved	
	1747	Reserved	
	1748	Reserved	
	1749	Reserved	
	1750	Reserved	
	1751	Reserved	
DB	1752	Reserved	
	1753	Reserved	
	1754	Reserved	
	1755	Reserved	
	1756	Reserved	
	1757	Reserved	
	1758	Reserved	
	1759	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
DC	1760	Reserved	
	1761	Reserved	
	1762	Reserved	
	1763	Reserved	
	1764	Reserved	
	1765	Reserved	
	1766	Reserved	
	1767	Reserved	
DD	1768	Reserved	
	1769	Reserved	
	1770	Reserved	
	1771	Reserved	
	1772	Reserved	
	1773	Reserved	
	1774	Reserved	
	1775	Reserved	
DE	1776	Reserved	
	1777	Reserved	
	1778	Reserved	
	1779	Reserved	
	1780	Reserved	
	1781	Reserved	
	1782	Reserved	
	1783	Reserved	
DF	1784	Reserved	
	1785	Reserved	
	1786	Reserved	
	1787	Reserved	
	1788	Reserved	
	1789	Reserved	
	1790	Reserved	
	1791	Reserved	
E0	1792	Reserved	
	1793	Reserved	
	1794	Reserved	
	1795	Reserved	
	1796	Reserved	
	1797	Reserved	
	1798	Reserved	
	1799	Reserved	
E1	1800	Reserved	
	1801	Reserved	
	1802	Reserved	
	1803	Reserved	
	1804	Reserved	
	1805	Reserved	
	1806	Reserved	
	1807	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
E2	1808	Reserved	
	1809	Reserved	
	1810	Reserved	
	1811	Reserved	
	1812	Reserved	
	1813	Reserved	
	1814	Reserved	
	1815	Reserved	
E3	1816	Reserved	
	1817	Reserved	
	1818	Reserved	
	1819	Reserved	
	1820	Reserved	
	1821	Reserved	
	1822	Reserved	
	1823	Reserved	
E4	1824	Reserved	
	1825	Reserved	
	1826	Reserved	
	1827	Reserved	
	1828	Reserved	
	1829	Reserved	
	1830	Reserved	
	1831	Reserved	
E5	1832	Reserved	
	1833	Reserved	
	1834	Reserved	
	1835	Reserved	
	1836	Reserved	
	1837	Reserved	
	1838	Reserved	
	1839	Reserved	
E6	1840	Reserved	
	1841	Reserved	
	1842	Reserved	
	1843	Reserved	
	1844	Reserved	
	1845	Reserved	
	1846	Reserved	
	1847	Reserved	
E7	1848	Reserved	
	1849	Reserved	
	1850	Reserved	
	1851	Reserved	
	1852	Reserved	
	1853	Reserved	
	1854	Reserved	
	1855	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
E8	1856	Reserved	
	1857	Reserved	
	1858	Reserved	
	1859	Reserved	
	1860	Reserved	
	1861	Reserved	
	1862	Reserved	
	1863	Reserved	
E9	1864	Reserved	
	1865	Reserved	
	1866	Reserved	
	1867	Reserved	
	1868	Reserved	
	1869	Reserved	
	1870	Reserved	
	1871	Reserved	
EA	1872	Reserved	
	1873	Reserved	
	1874	Reserved	
	1875	Reserved	
	1876	Reserved	
	1877	Reserved	
	1878	Reserved	
	1879	Reserved	
EB	1880	Reserved	
	1881	Reserved	
	1882	Reserved	
	1883	Reserved	
	1884	Reserved	
	1885	Reserved	
	1886	Reserved	
	1887	Reserved	
EC	1888	Reserved	
	1889	Reserved	
	1890	Reserved	
	1891	Reserved	
	1892	Reserved	
	1893	Reserved	
	1894	Reserved	
	1895	Reserved	
ED	1896	Reserved	
	1897	Reserved	
	1898	Reserved	
	1899	Reserved	
	1900	Reserved	
	1901	Reserved	
	1902	Reserved	
	1903	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
EE	1904	Reserved	
	1905	Reserved	
	1906	Reserved	
	1907	Reserved	
	1908	Reserved	
	1909	Reserved	
	1910	Reserved	
	1911	Reserved	
EF	1912	Reserved	
	1913	Reserved	
	1914	Reserved	
	1915	Reserved	
	1916	Reserved	
	1917	Reserved	
	1918	Reserved	
	1919	Reserved	
F0	1920	Reserved	
	1921	Reserved	
	1922	Reserved	
	1923	Reserved	
	1924	Reserved	
	1925	Reserved	
	1926	Reserved	
	1927	Reserved	
F1	1928	Reserved	
	1929	Reserved	
	1930	Reserved	
	1931	Reserved	
	1932	Reserved	
	1933	Reserved	
	1934	Reserved	
	1935	Reserved	
F2	1936	Reserved	
	1937	Reserved	
	1938	Reserved	
	1939	Reserved	
	1940	Reserved	
	1941	Reserved	
	1942	Reserved	
	1943	Reserved	
F3	1944	Reserved	
	1945	Reserved	
	1946	Reserved	
	1947	Reserved	
	1948	Reserved	
	1949	Reserved	
	1950	Reserved	
	1951	Reserved	

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F4	1952	GPO0 I2C output expander data	
	1953	GPO0 I2C output expander select	0: GPO0 output come from matrix 1: GPO0 output is register
	1954	GPIO6 I2C output expander data	
	1955	GPIO6 I2C output expander select	0: GPIO6 output come from matrix 1: GPIO6 output is register
	1956	GPIO7 I2C output expander data	
	1957	GPIO7 I2C output expander select	0: GPIO7 output come from matrix 1: GPIO7 output is register
	1958	GPIO8 I2C output expander data	
	1959	GPIO8 I2C output expander select	0: GPIO8 output come from matrix 1: GPIO8 output is register
F5	1960	I2C reset bit with reloading NVM into Data register (soft reset)	0: Keep existing condition 1: Reset execution
	1961	IO Latching Enable During I2C Write Interface	0: Disable 1: Enable
	1962	Reserved	
	1963	Protect mode enable	0: Disable 1: Enable
	1964	Reserved	
	1965	Register protection mode bit 0	000: all open read/write (mode 0); 001: partly lock read (mode 1); 010: partly lock read2 (mode 2); 011: partly lock read2/write (mode 3); 100: all lock read (mode 4); 101: all lock write (mode 5); 110: all lock read/write (mode 6).
	1966	Register protection mode bit 1	
	1967	Register protection mode bit 2	
F6	1968	I^2C write mask bits	1: mask 0: overwrite
	1969		
	1970		
	1971		
	1972		
	1973		
	1974		
	1975		
F7	1976	Reserved	
	1977		
	1978		
	1979		
	1980		
	1981		
	1982		
	1983		
F8	1984	Reserved	
	1985		
	1986		
	1987		
	1988		
	1989		
	1990		
	1991		

Table 57: Register Map (Continued)

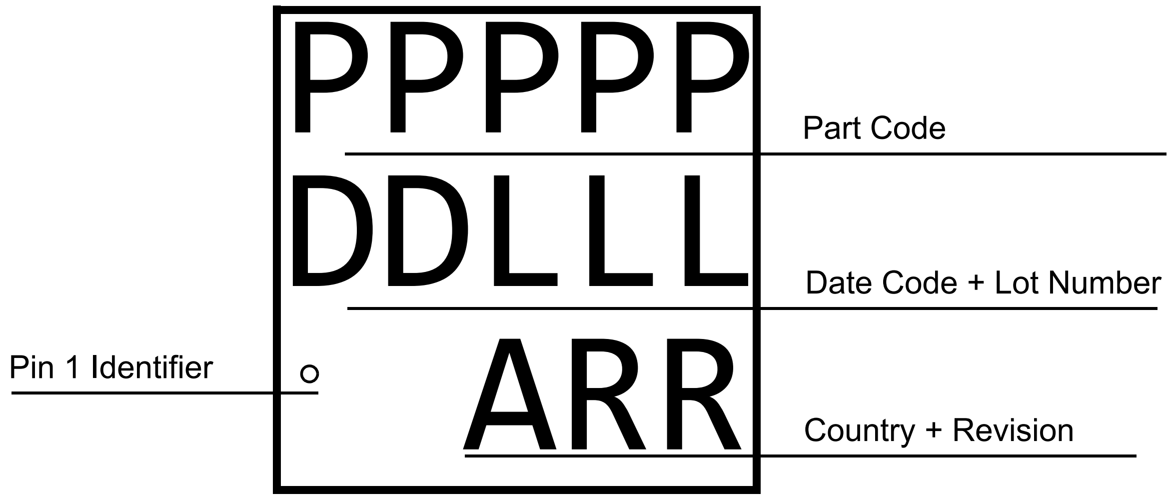
Address		Signal Function	Register Bit Definition
Byte	Register Bit		
F9	1992	Reserved	
	1993	Reserved	
	1994	Reserved	
	1995		
	1996	Reserved	
	1997		
	1998		
	1999		
FA	2000	Reserved	
	2001		
	2002		
	2003		
	2004		
	2005		
	2006		
	2007		
FB	2008	Reserved	
	2009		
	2010		
	2011		
	2012		
	2013		
	2014		
	2015		
FC	2016	Reserved	
	2017		
	2018		
	2019		
	2020		
	2021		
	2022		
	2023		
FD	2024	I^2C slave address	
	2025		
	2026		
	2027		
	2028	Slave address selection bit0	0: from register [2024] 1: from GPI0
	2029	Slave address selection bit1	0: from register [2025] 1: from GPIO2
	2030	Slave address selection bit2	0: from register [2026] 1: from GPIO4
	2031	Slave address selection bit3	0: from register [2027] 1: from GPIO5

Table 57: Register Map (Continued)

Address		Signal Function	Register Bit Definition
Byte	Register Bit		
FE	2032	I2C operation disable bit	0: I2C operation enable; matrix in 32(33) select I2C_virtual_0(1) Input 1: I2C operation disable; matrix in 32(33) select GPIO0(GPIO1) digital input
	2033	Reserved	
	2034	Reserved	
	2035	Reserved	
	2036	Reserved	
	2037	Reserved	
	2038	Reserved	
	2039	Reserved	
FF	2040	Reserved	
	2041		
	2042		
	2043		
	2044		
	2045		
	2046		
	2047		

18 Package Top Marking Definitions

18.1 FCQFN 14L 3MM X 3 MM 0.65P FCD

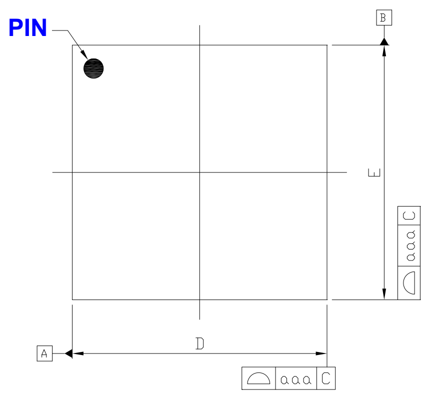


19 Package Information

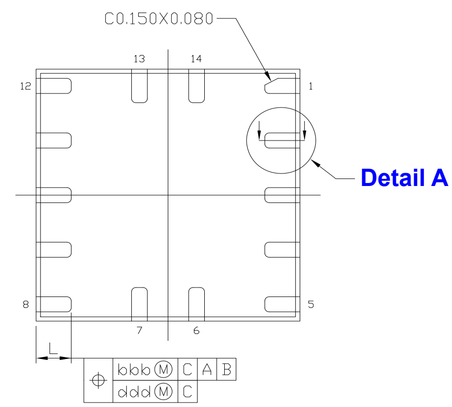
19.1 PACKAGE OUTLINES FOR FCQFN 14L 3.0 MM X 3.0 MM X 0.55 MM 0.65P FC PACKAGE

JEDEC MO-220

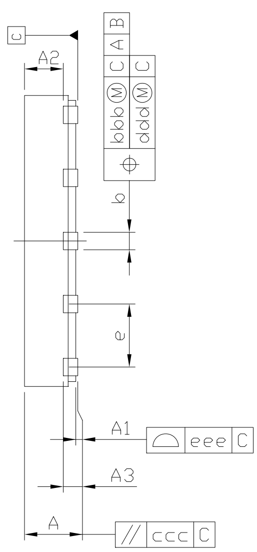
IC Net Weight: 0.0115 g



Top View

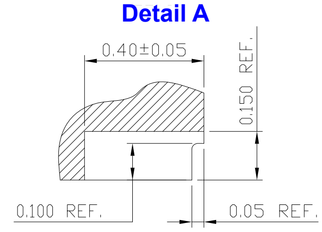


Bottom View



Marking View

Wettable Flank



Terminal Cross Section

Controlling Dimensions: mm

SYMBOLS	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.35	0.40	0.45	0.014	0.016	0.018
A3	0.10	0.15	0.20	0.004	0.006	0.008
b	0.13	0.18	0.23	0.005	0.007	0.009
D	2.95	3.00	3.05	0.116	0.118	0.120
E	2.95	3.00	3.05	0.116	0.118	0.120
e	0.65 BSC			0.026 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

Standard Tolerance: ±0.05

19.2 FCQFN HANDLING

Be sure to handle FCQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle FCQFN package with fingers as this can contaminate the package pins and interface with solder re-flow.

19.3 SOLDERING INFORMATION

Please see IPC/JEDEC J-STD-020: latest revision for re-flow profile based on package volume of 2.64 mm^3 (nominal) for FCQFN 14L Package. More information can be found at www.jedec.org.

20 Ordering Information

Part Number	Type
SLG46855-AP	14-pin FCQFN
SLG46855-APTR	14-pin FCQFN - Tape and Reel (5k units)

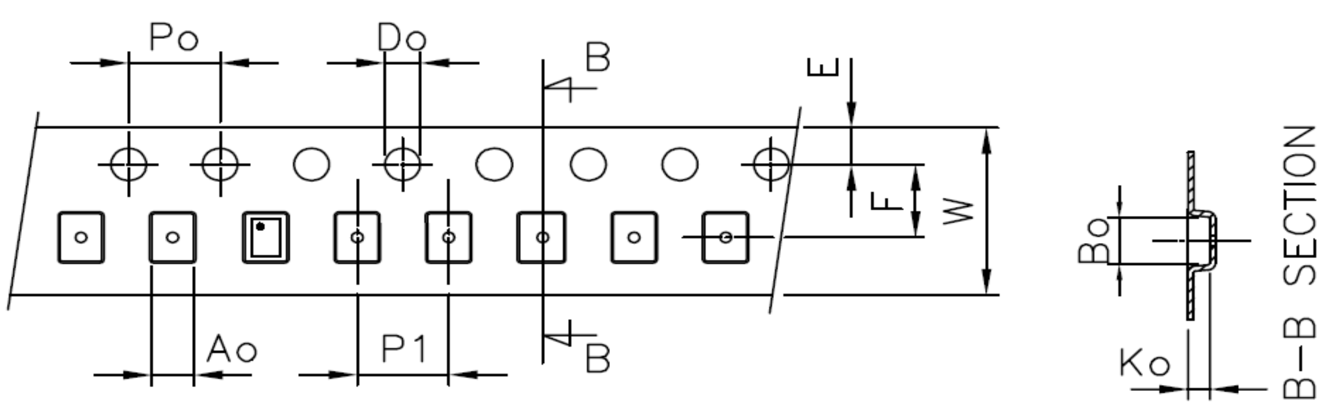
Note 1 Use SLG46855-AP to order. Shipments are automatically in Tape and Reel.
Note 2 “TR” suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

20.1 TAPE AND REEL SPECIFICATIONS

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
FCQFN 14L 3 mm x 3 mm 0.65P FC Green	14	3.0 x 3.0 x0.55	5000	10000	330/102	50	400	50	400	12	8

20.2 CARRIER TAPE DRAWING AND DIMENSIONS

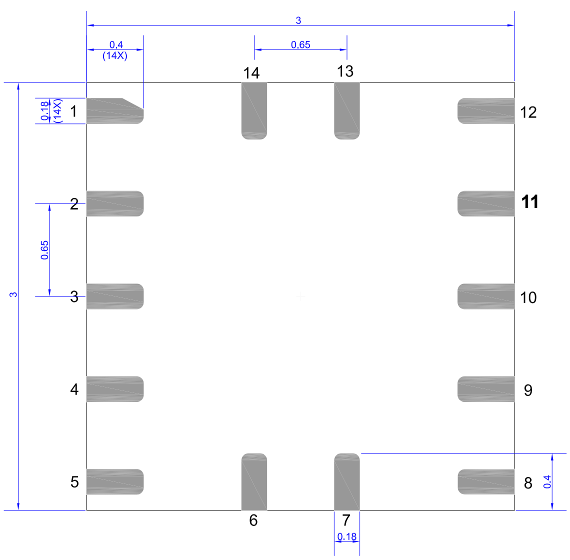
Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
FCQFN 14L 3.0 mm x 3.0mm 0.65P FC Green	3.3	3.3	0.8	4	8	1.5	1.75	5.5	12



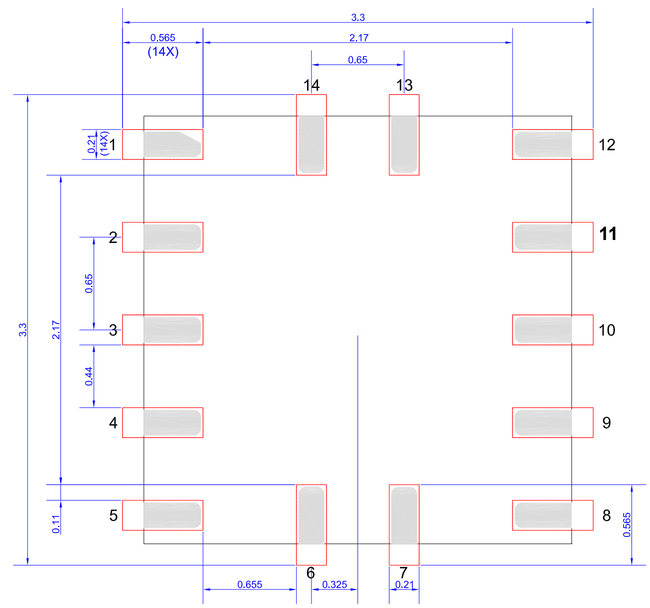
21 Layout Guidelines

21.1 FCQFN 14L 3 MM X 3 MM X 0.5 MM 0.65P FC GREEN

Expose Pad
(Package face down)



Recommended Landing Pattern
(Package face down)



Unit: mm

Glossary

A

ACK	Acknowledge bit
ACMP	Analog Comparator
ACMPH	Analog Comparator High Speed
ACMPL	Analog Comparator Low Power
ADAS	Advanced Driver Assistance Systems

B

BG	Bandgap

C

CLK	Clock
CMO	Connection matrix output
CNT	Counter

D

DFF	D Flip-Flop
DLY	Delay

E

ESD	Electrostatic discharge
EV	End Value

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input
IO	Input/Output

L

LPF	Low Pass Filter
LSB	Least Significant Bit

LUT	Look Up Table
LV	Low Voltage

M

MSB	Most Significant Bit
MUX	Multiplexer

N

NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory

O

OD	Open-Drain
OE	Output Enable
OSC	Oscillator
OTP	one time programmable
OUT	Output

P

PD	Power-down
PGen	Pattern Generator
POR	Power-On Reset
PP	Push-Pull
PWR	Power
P DLY	Programmable Delay

R

R/W	Read/Write

S

SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
SLA	Slave Address
SMT	With Schmitt Trigger
SV	nSET Value

T

TS	Temperature Sensor

V

Vref	Voltage Reference

W

WOSMT	Without Schmitt Trigger
WS	Wake and Sleep Controller

Revision History

Revision	Date	Description
3.5	23-May-2023	Updated tables captions in section Characteristics Updated information in table Recommended Operating Conditions Fixed typos
3.4	28-Feb-2023	Added notes to section Ordering Information
3.3	13-Dec-2022	Added additional information about AEC-Q100
3.2	19-Oct-2022	Fixed typos in sections Layout Guidelines and Characteristics
3.1	7-Mar-2022	Updated R_{PULL} in section Electrical Characteristics Renesas rebranding Added IC Net Weight in Package Information section Updated bytes 5B, 5C, 5D, 5E and 5F in the Register map Added information about SCL and SDA Pins' Schmitt Trigger Updated section GPIO8 Source for Oscillator 2 (25 MHz)
3.0	17-Jun-2021	Final version

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

RoHS Compliance

Renesas Electronics Corporation's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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