LMP92066 Dual Temperature-Controlled DAC with Integrated EEPROM and Output ON/OFF Control

1 Features

- Internal 12-Bit Temperature Sensor
  - Accuracy (–40°C to 120°C), ±3.2°C (maximum)
- Two Independent Transfer Functions Stored in EEPROM
- Dual-Analog Output
  - Two 12-Bit DACs
  - Output Range 0 V to 5 V or 0 V to –5 V
  - High-Capacitive Load Tolerant, up to 10 µF
  - Post-Calibration Accuracy ±2.4 mV (typical)
- Output On/Off Control Switching Time 50 ns (typical)
  - Switching Time 50 ns (typical)
  - RDSON 5 Ω (maximum)
- I^2C Interface: Standard and Fast
  - Nine Selectable Slave Addresses
  - TIMEOUT Function
- VDD Supply Range 4.75 V to 5.25 V
- VIO Range 1.65 V to 3.6 V
- Specified Temperature Range –25°C to 120°C
- Operating Temperature Range –40°C to 125°C

2 Applications

- GaN or LDMOS PA Bias Controller
- Sensor Temperature Compensation
- Timing Circuit Temperature Compensation

3 Description

The LMP92066 is a highly integrated temperature-controlled dual DAC. Both DACs can be programmed by two independent, user-defined, temperature-to-voltage transfer functions stored in the internal EEPROM, allowing any temperature effects to be corrected without additional external circuitry. Once powered up, the device operates autonomously, without intervention from the system controller, to provide a complete solution for setting and compensating bias voltages and currents in control applications.

The LMP92066 has two analog outputs that support two output ranges: zero to plus five volts and zero to minus five volts. Each output can be switched to the load individually through the use of the dedicated control pin. The output switching is designed for rapid response, making the device suitable for the RF Power Amplifier biasing applications.

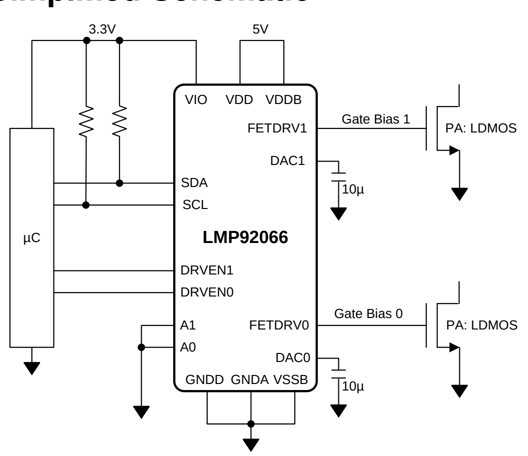
The EEPROM is verified for 100 write operations, enabling repeated field updates. The EEPROM programming is completed upon the user-issued I^2C command.

The LMP92066's digital ports interface to a variety of system controllers, as the dedicated VIO pin sets the digital I/O levels. The device is available in the thermally enhanced PowerPAD™ package, enabling precise PCB temperature measurement.

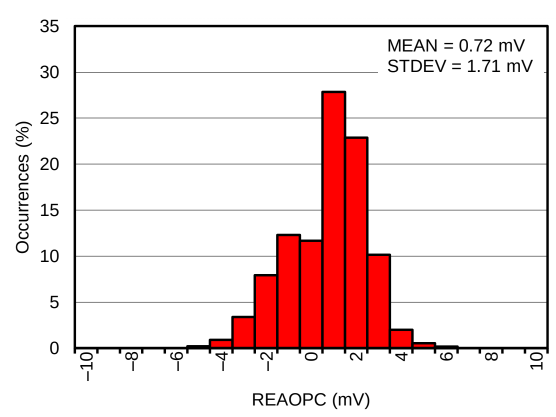
Device Information

PART NUMBER	PACKAGE	BODY SIZE
LMP92066	HTSSOP (16)	5.00 mm x 4.40 mm

4 Simplified Schematic



Residual Error After One Point Calibration



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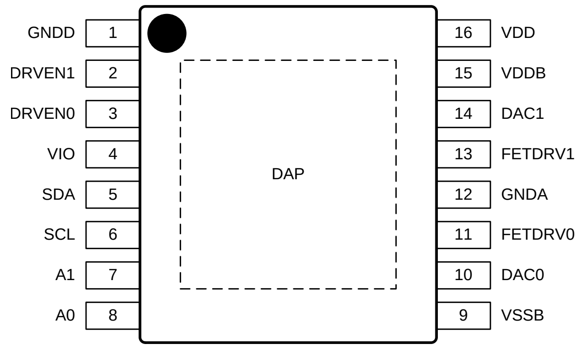
5 Revision History

Changes from Revision A (April 2015) to Revision B	Page
• Added new footnote.	7
• Added VDD Supply Sourcing section.	54

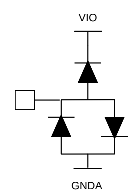
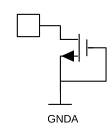
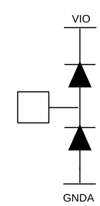
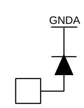
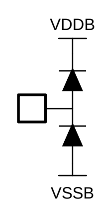
Changes from Original (March 2014) to Revision A	Page
• Changed header row of *Device Information* table; revised "terminal" to "pin" throughout document, changed *Handling Ratings* to *ESD Ratings* table; took out "+" from positive values; italicize section cross references; add titles for tables 3, 4, 5, and 6	1
• Added "Ω" after "k" in EC table	6
• Added "Ω" after "k" in *Output Switching* table	8
• Added "NOTE" to beginning of *Applications and Implementations*	43
• Changed title from *Application Performance Plots* to *Application Curves*; deleted reference to Figure 43 in first sentence of first *Application Curves* section	47
• Added change "5 mA" to "50 mA"	54

6 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP
Top View

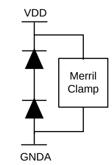
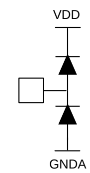
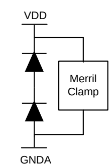
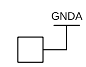


Pin Functions

PIN		TYPE (1)	DESCRIPTION	ESD STRUCTURES
NUMBER	NAME			
1	GNDD	G	Lower power rail of the digital I/O	
2:3	DRVEN[1:0]	I	Asynchronous control of the Changeover Switches	
4	VIO	I	Digital I/O power supply rail	
5	SDA	I/O	I^2C bi-directional data line	
6	SCL	I	I^2C clock input	
7:8	A[1:0]	I	I^2C slave address selector	
9	VSSB	P	Output drive lower supply rail	
10, 14	DAC0 DAC1	O	DAC0 output	
11, 13	FETDRV0 FETDRV1	O	Gate drive of the external FET device	

(1) G = Ground; I = Input; O = Output; P = Power

Pin Functions (continued)

PIN		TYPE [1]	DESCRIPTION	ESD STRUCTURES
NUMBER	NAME			
12	GNDA	G	Analog block lower rail	
15	VDDB	P	Output drive upper supply rail	
16	VDD	P	Analog block upper rail	
---	DAP	G	Die Attach Pad. For best thermal, and noise performance it should be soldered to the local system ground pad.	

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
VDD	Supply voltage with respect to GNDA	–0.3	5.5	V
VDDB		–0.3	5.5	
VIO		–0.3	5.5	
VSSB		–5.5	0.3	
GNDD		–0.3	0.3	
VDDB to VSSB		–0.3	5.5	V
Any other pins to GNDA		–0.3	5.5	
DAC output current			10	mA
Current at all other pins			5	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	Operational temperature	–40	125	°C
	Specification temperature	–25	120	
	DAC output load capacitance	8	12	µF
VDD	Supply voltage range (VDD)	4.75	5.25	V
VIO	Digital I/O supply voltage	1.65	3.3	
VDDB–VSSB	LDMOS mode VSSB = GNDA		5	
	GaN mode VSSB = –5 V		5	

7.4 Thermal Information

THERMAL METRIC (1)		PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	15.1	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	14.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

Unless otherwise noted: VDD = 5 V ±5%, VIO = 1.8 V to 3.3 V, T_A = 25°C. VDDB = 5 V ±5%, VSSB = GNDA, V_{DACx} output range 0 V to 5 V; or VDDB = GNDA, VSSB = –5 V ±5%, V_{DACx} output range 0 V to –5V. DAC input code range 48 to 4047. V_{DACX} load C_L = 10 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SIGNAL PATH CHARACTERISTICS (DAC, Buffer Amplifier, Internal Reference)						
	Resolution	–25°C < T_A < 120°C	12		12	Bits
	Monotonic	–25°C < T_A < 120°C	12			Bits
DNL	Differential non-linearity	R_L = 100 kΩ, –25°C < T_A < 120°C	–0.99		1	LSB
INL	Integral non-linearity	R_L = 100 kΩ, –25°C < T_A < 120°C	–1.93		2.78	LSB
OE	Offset error (1)	LDMOS mode, R_L = 100 kΩ, –25°C < T_A < 120°C	–14		14	mV
		LDMOS mode, R_L = 100 kΩ		±1		mV
		GaN mode, R_L = 100 kΩ, –25°C < T_A < 120°C	–16.5		16.5	mV
OETC	Offset error temperature coefficient (1) (2)	R_L = 100 kΩ, –25°C < T_A < 120°C			43	µV/°C
GE	Gain error (1)	R_L = 100 kΩ, –25°C < T_A < 120°C	–0.72		0.74	%FS
GETC	Gain error temperature coefficient (1) (2)	R_L = 100 kΩ, –25°C < T_A < 120°C			20	ppm/°C
REAOPC	Residual error after one point calibration (1) (2) (3) (4)	BASEx = 1638 (V_{DACX} = 2 V at 24°C) –25°C < T_A < 120°C	–13.3		13.3	mV
		BASEx = 1638 (V_{DACX} = 2 V at 24°C)		±2.4		mV
		BASEx = 819 (V_{DACX} = 1 V at 24°C) –25°C < T_A < 120°C	–11.3		11.3	mV
		BASEx = 819 (V_{DACX} = 1 V at 24°C)		±2.1		mV
ZCO	Zero code output (V_{DACx} – VSSB)	LDMOS mode, R_L = 100 kΩ		0		mV
		LDMOS mode, I_{OUT} = 10 mA		200		mV
FSO	Full-scale output at code 4095 (VDDB – V_{DACx})	LDMOS mode, R_L = 100 kΩ		10		mV
		LDMOS mode, I_{OUT} = –10 mA		150		mV
I_O	Continuous output current per channel allowed (5)	T_A = 125°C			10	mA
C_L	Load capacitance (5)	R_L = 2 kΩ or ∞, –25°C < T_A < 120°C			12	µF
		R_L = 2 kΩ or ∞		10		µF
	DAC output resistance	DACCODEx = 2048		3		Ω
	DAC settling time	C_L = 10 µF		250		µs
OUTPUT SWITCH DC CHARACTERISTICS						
R_{DRV}	On Resistance of the switch between DACx and FETDRVx	–25°C < T_A < 120°C			6	Ω
R_G	On Resistance of the switch between FETDRVx and VSSB			11		Ω
TEMPERATURE SENSOR CHARACTERISTICS						
	Resolution			0.0625		°C/lsb
TE	Temperature sensor error (2)	T_A = –40°C to 120°C	–3.2		3.2	°C
	Conversion time			25		ms

(1) The package mechanical stress-induced parameter shift may cause the parts to manifest behavior beyond the specified limits. Mechanical stresses may also arise as a result of the PCB manufacturing process.
(2) Device specification is verified by characterization and is not tested in production.
(3) The specification is a calculated worst-case value based on the OE, OETC, GE, and GETC limits.
(4) The outcome of the REAOPC characterization of the PCB mounted devices is shown in Figure 4, Figure 5, and Figure 6 of the *Typical Characteristics*. The 97, randomly selected, devices from 3 diffusion lots were installed on the 4-layer RO4003 Laminate using Convection Reflow. The Look-Up-Table was set for maximum gain; for example, all DELx = 0xFF. While powered up, the devices were subjected to 3 thermal cycles, from –40°C to 125°C, during which their REAOPC was recorded.
(5) Parameter based on the process data and circuit simulation.

Electrical Characteristics (continued)

Unless otherwise noted: VDD = 5 V ±5%, VIO = 1.8 V to 3.3 V, T_A = 25°C. VDDB = 5 V ±5%, VSSB = GNDA, V_{DACx} output range 0 V to 5 V; or VDDB = GNDA, VSSB = –5 V ±5%, V_{DACx} output range 0 V to –5V. DAC input code range 48 to 4047. V_{DACX} load C_L = 10 µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EEPROM						
	Maximum EEPROM write cycles				100	
DIGITAL INPUT CHARACTERISTICS (DRVEN0, DRVEN1, SDA, and SCL)						
V_{IH}	Input high voltage	–25°C < T_A < 120°C	0.7 × VIO			V
V_{IL}	Input low voltage	–25°C < T_A < 120°C			0.3 × VIO	V
	Hysteresis			0.2 × VIO		V
C_{IND}	Input capacitance			5		pF
DIGITAL INPUT CHARACTERISTICS (A0, A1)						
V_{IH}	Input high voltage	–25°C < T_A < 120°C	0.7 × VIO			V
V_{IL}	Input low voltage	–25°C < T_A < 120°C			0.3 × VIO	V
R_{UP}	Internal pullup resistance			17		kΩ
R_{DN}	Internal pulldown resistance			17		kΩ
	Max external capacitance(5)				30	pF
DIGITAL OUTPUT CHARACTERISTICS (SDA)						
V_{OL}	Output low voltage	I_{OUT} = 4 mA, –25°C < T_A < 120°C			0.4	V
		I_{OUT} = 4 mA		0.16		V
I_{LEAK}	Open-drain output leakage current with output high(5)	Current from the supply rail through the pullup resistor into the drain of the open-drain output device, –25°C < T_A < 120°C			±1	µA
C_{OUT}	Output capacitance			4		pF
SUPPLY CURRENT SPECIFICATIONS						
I_{DD}		Normal operation(6), (7) –25°C < T_A < 120°C			2.6	mA
		While executing EEPROM BURN(8)		4		mA
		While transferring EEPROM content to operating memory(9)		9		mA
I_{VIO}		I^2C inactive, –25°C < T_A < 120°C			3	µA
		I^2C in fast mode, –25°C < T_A < 120°C			3.1	µA
I_{VDDB}		LDMOS mode, R_L = ∞, –25°C < T_A < 120°C			1.5	mA
I_{VSSB}		GaN mode, R_L = ∞, –25°C < T_A < 120°C	–1.4			mA
PWR (Conv)	Power consumption, conversion mode	All output pins R_L = ∞		20		mW

(6) The normal operation current through the VDD excludes the current supplied to the external load, and excludes the current required by the EPPROM BURNS and TRANSFERS.
(7) The power supply must be capable of sourcing a minimum of 50mA in order to avoid the continuous activation of the LMP92066's power-on-reset (POR) circuit.
(8) During the EEPROM BURN command execution the device activates internal systems that are not active during the Normal operation. This causes a momentary increase in supply current through the VDD pin. The duration of this temporary surge in supply current is typically 125 ms.
(9) During the data transfer from the EEPROM to the Operating memory there will be a momentary surge in supply current through the VDD pin. The duration of this surge is typically 200 µs.

7.6 Timing Requirements

Unless otherwise noted: VDD = 5 V ±5%, VIO = 1.8 V to 3.3 V. VDDB = 5 V ±5%, VSSB = GNDA; or VDDB = GNDA, VSSB = –5V ±5%.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
	I^2C clock frequency		10	400	kHz
t_{LOW}	Clock low time		1.3		µs
t_{HIGH}	Clock high time		0.6		
t_{HD-STA}	Hold time repeated START condition	After this period, the first clock pulse is generated	0.6		
$t_{SU;STA}$	Setup time for a repeated START condition		0.6		
$t_{HD;DAT}$	Data hold time (Note x and y)		0	900	ns
$t_{SU;DAT}$	Data setup time		100		
t_f	SDA fall time	$I_L \le 3$ mA and $C_L \le 400$ pF		250	
$t_{SU;STO}$	Setup time for STOP condition		0.6		µs
t_{BUF}	Bus free time between a STOP and START condition		1.3		
C_b	SDA capacitive load			400	pF
t_{SP}	Pulse width of spikes that must be suppressed by the input filter			50	ns
	SCL and SDA timeout		25	35	ms

7.7 Output Switching Characteristics

Unless otherwise noted: VDD = 5 V ±5%, VIO = 1.8 V to 3.3 V. VDDB = 5 V ±5%, VSSB = GNDA; or VDDB = GNDA, VSSB = –5V ±5%.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	On time	DACCODEx = 4095, R_L = 100 kΩ		50		ns
t_{OFF}	Off time			50		
t_{BBM}	Break-before-make time			15		
C_{FETDRV}	FETDRV output capacitance			10		pF

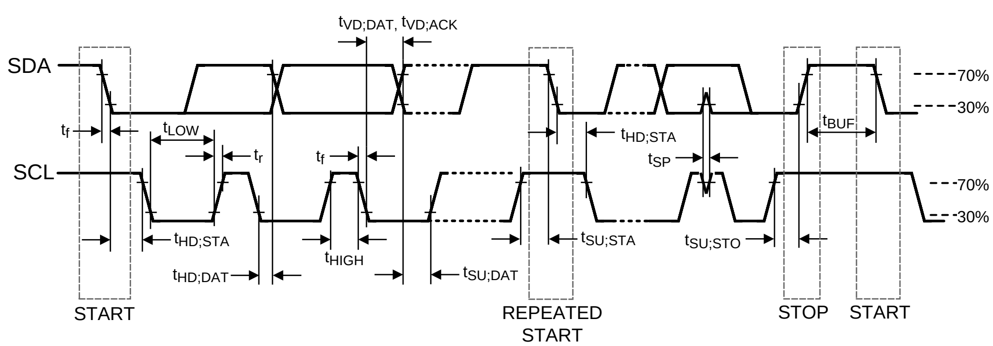


Figure 1. I^2C Timing

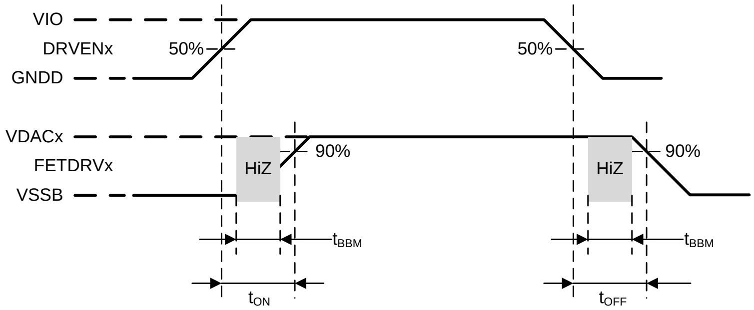


Figure 2. Switching

7.8 Typical Characteristics

Unless otherwise stated the plot data was collected under these conditions: VDD = 5 V, VDDB = 5 V, VSSB = GNDA, VIO = 3.3 V, Temperature = 24°C, R_L = 100 kΩ.

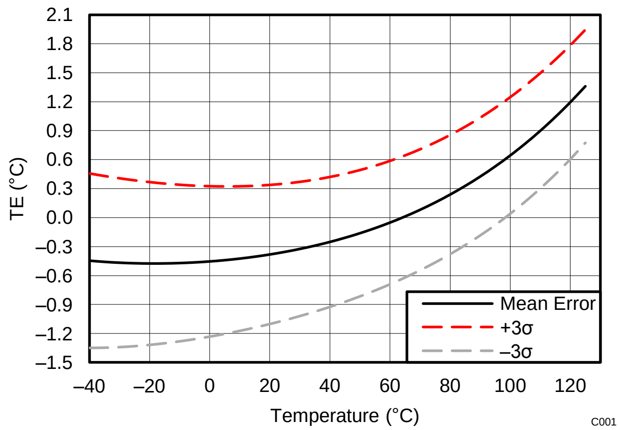
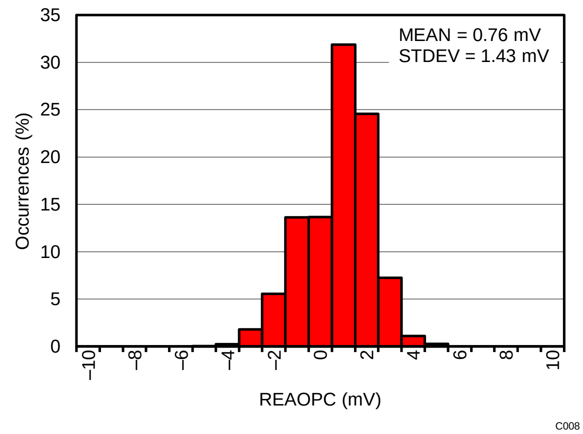
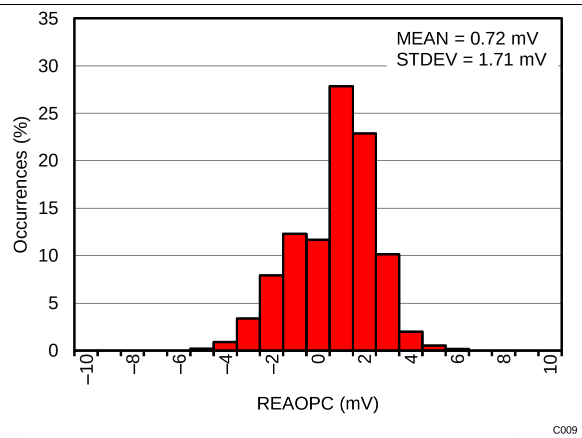


Figure 3. Temperature Sensor Error



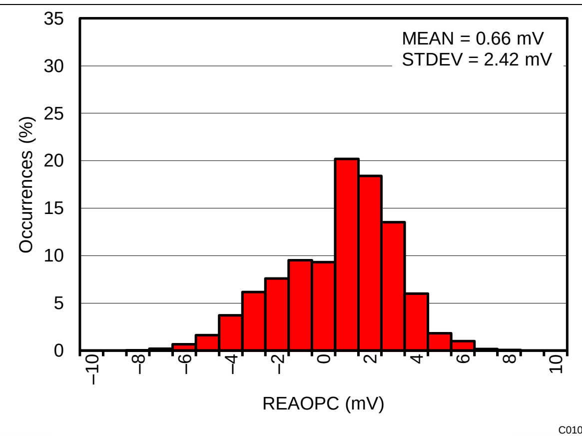
BASE = 819 PCB Mounted
97 devices 3 Cycles: –40°C to 125°C

Figure 4. REAOPC



BASE = 1638 PCB Mounted
97 devices 3 Cycles: –40°C to 125°C

Figure 5. REAOPC



BASE = 3277 PCB Mounted
97 devices 3 Cycles: –40°C to 125°C

Figure 6. REAOPC

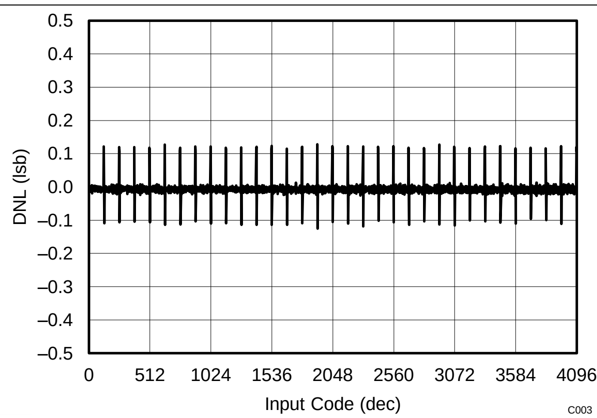


Figure 7. DAC DNL

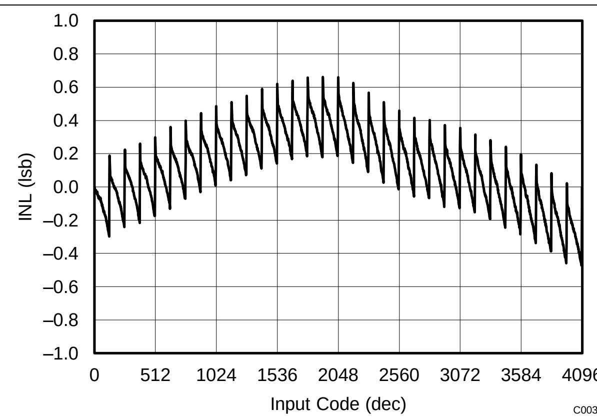


Figure 8. DAC INL

Typical Characteristics (continued)

Unless otherwise stated the plot data was collected under these conditions: VDD = 5 V, VDDB = 5 V, VSSB = GNDA, VIO = 3.3 V, Temperature = 24°C, R_L = 100 kΩ.

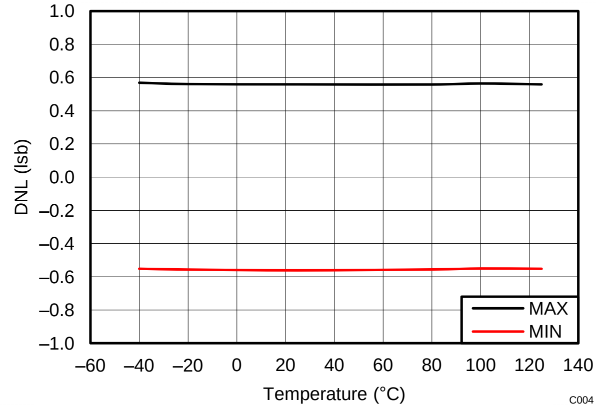


Figure 9. DAC MIN/MAX DNL vs Temperature

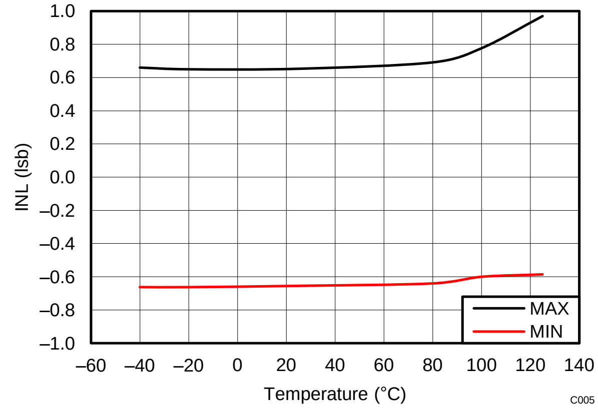
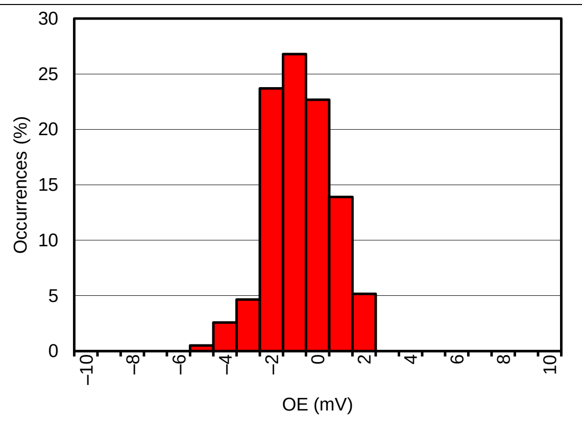
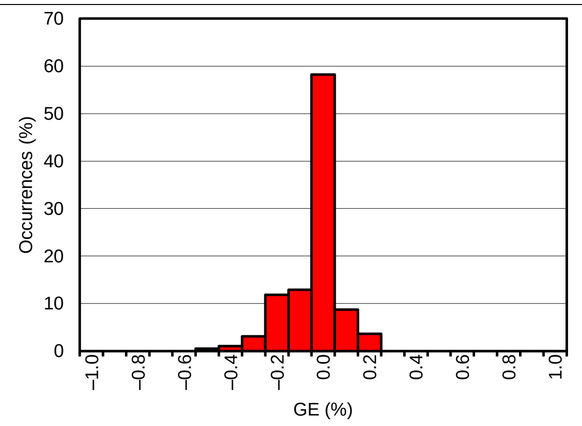


Figure 10. DAC MIN/MAX INL vs Temperature



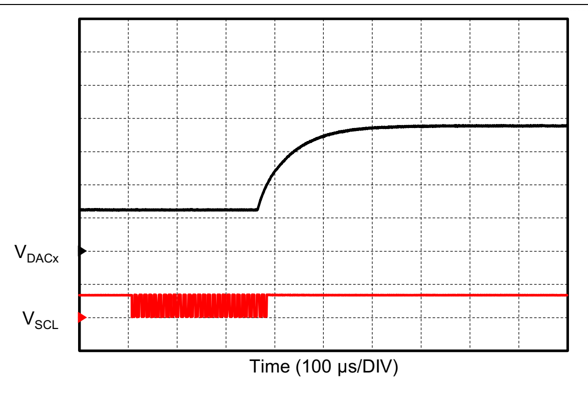
TEMP = –40°C to 120°C

Figure 11. DAC Offset Error



TEMP = –40°C to 120°C

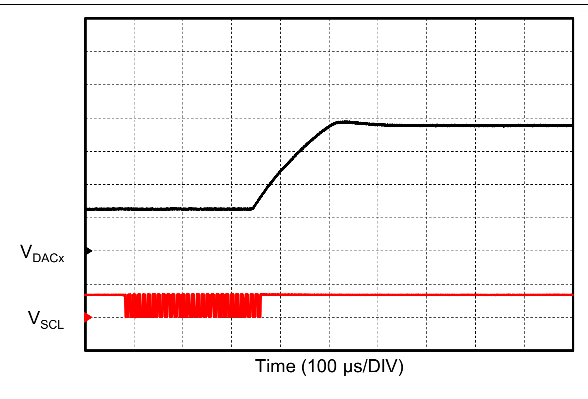
Figure 12. DAC Gain Error



DAC OVERRIDE MODE
C_L = 10 µF

I^2C command triggers DAC step
Step size: 1/4 to 3/4 FS

Figure 13. DAC Step Response



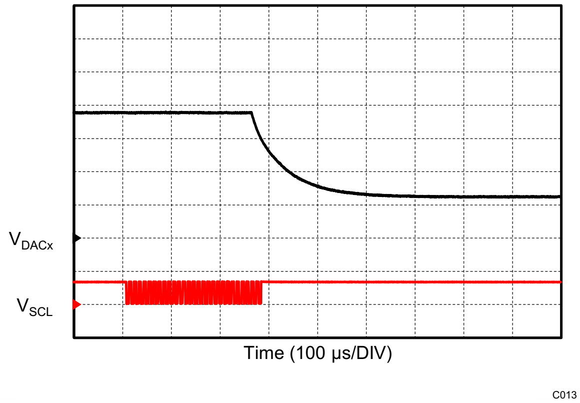
DAC OVERRIDE MODE
C_L = 10 pF

I^2C command triggers DAC step
Step size: 1/4 to 3/4 FS

Figure 14. DAC Step Response

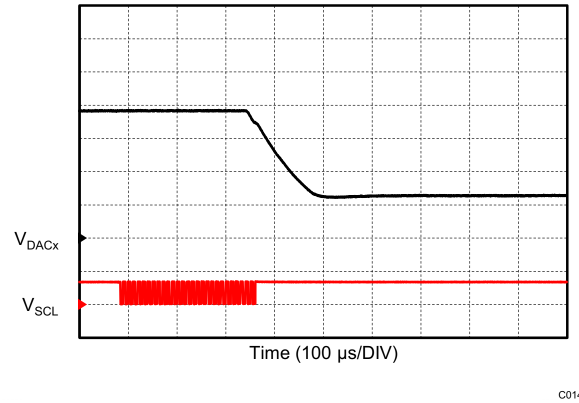
Typical Characteristics (continued)

Unless otherwise stated the plot data was collected under these conditions: VDD = 5 V, VDDB = 5 V, VSSB = GNDA, VIO = 3.3 V, Temperature = 24°C, R_L = 100 kΩ.



DAC OVERRIDE MODE C_L = 10 µF I²C command triggers DAC step Step size: 3/4 to 1/4 FS

Figure 15. DAC Step Response



DAC OVERRIDE MODE C_L = 10 pF I²C command triggers DAC step Step size: 3/4 to 1/4 FS

Figure 16. DAC Step Response

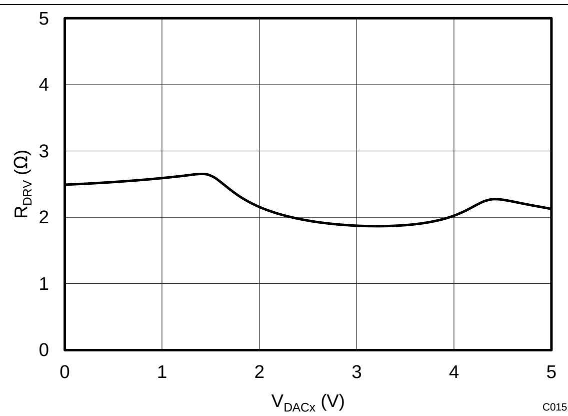


Figure 17. R_{DRV} Resistance vs DAC Output Level

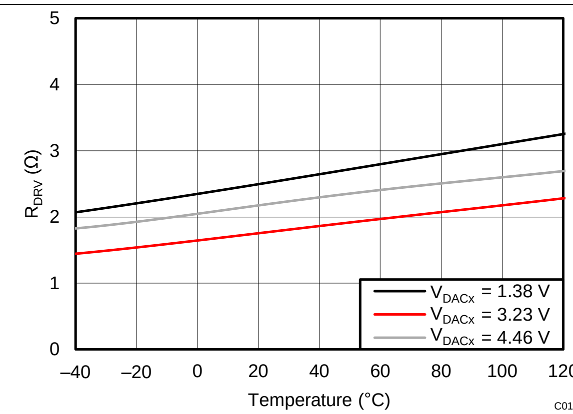


Figure 18. R_{DRV} vs Temperature

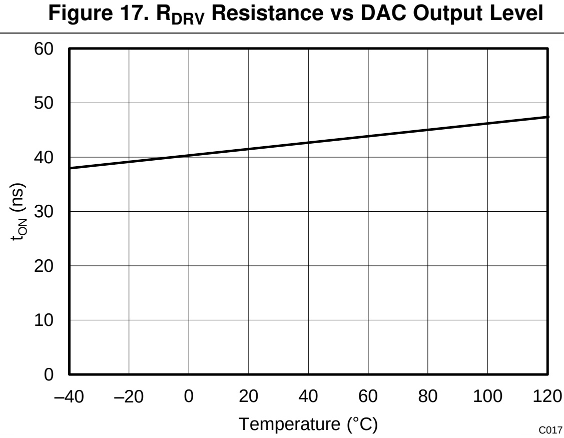


Figure 19. Output Switch ON Time vs Temperature

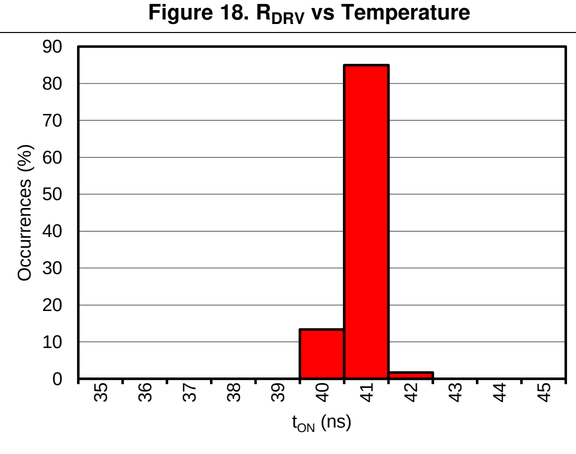


Figure 20. Output Switch ON Time

Typical Characteristics (continued)

Unless otherwise stated the plot data was collected under these conditions: VDD = 5 V, VDDB = 5 V, VSSB = GNDA, VIO = 3.3 V, Temperature = 24°C, R_L = 100 kΩ.

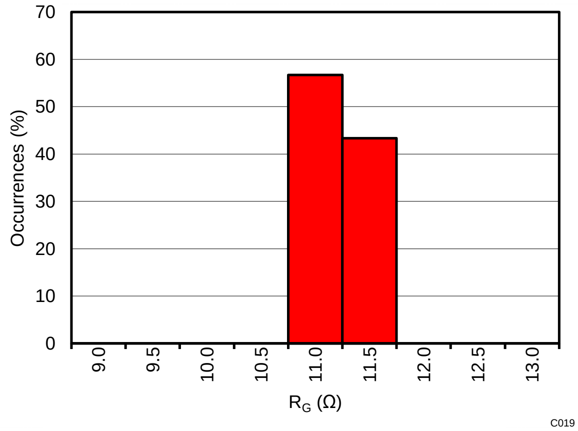


Figure 21. Ground Switch Resistance When Closed

8 Detailed Description

8.1 Overview

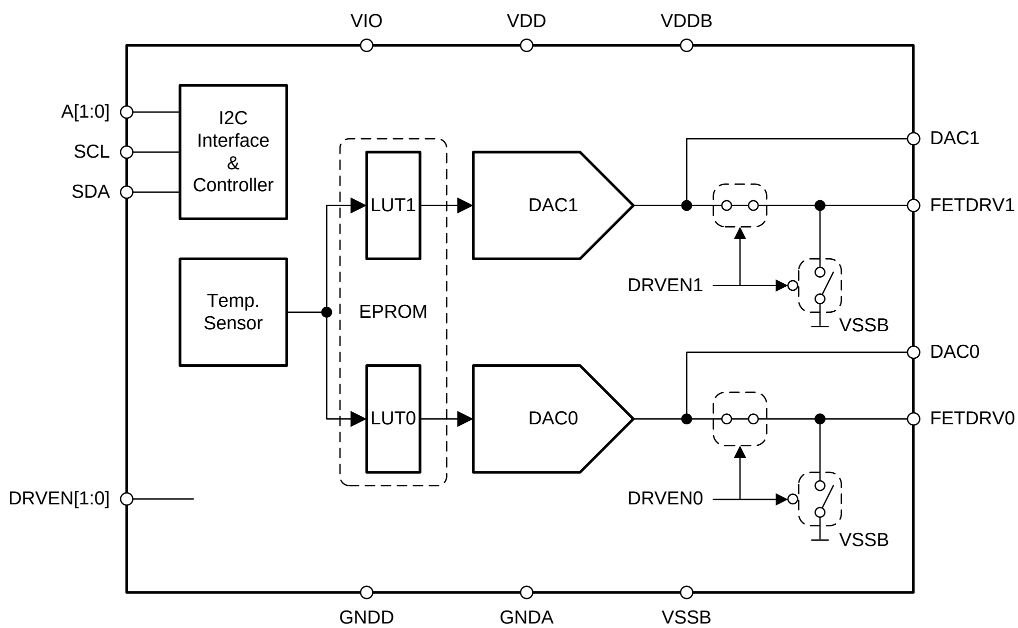
The LMP92066 is a dual temperature-dependent bias generator whose temperature-to-voltage transfer functions are user defined. The device contains a digital temperature sensor that addresses two independently programmable Look-Up-Tables (LUTs). The outputs of LUTs are sent on to their respective 12-bit DACs to produce two independent output voltages. For added flexibility the device can be configured to provide bias potential above or below GNDA.

In applications requiring rapid ON/OFF switching of the bias voltage, the LMP92066 provides asynchronous control over its outputs. Dedicated digital input pins control analog output switching.

All aspects of the device functionality are controlled through internal registers. These registers, and the LUTs, are accessible through the I^{2}C-compatible interface.

The LMP92066 can operate autonomously of the system controller, once LUT coefficients have been committed to its non-volatile memory, EEPROM. Upon power up the EEPROM content is automatically transferred to the operating memory, and the device begins to produce required bias voltage.

8.2 Functional Block Diagram



8.3 Features Description

8.3.1 Temperature Sensor

The onboard digital temperature sensor produces 12-bit, twos complement output, where the LSB represents +0.0625°C, and MSB represents –128°C. The output of the temperature sensor is stored in the TEMPM and TEMPL registers. These registers are updated automatically once the temperature sensor completes a new conversion, approximately every 25 ms. The temperature sensor begins operation immediately after the supply voltage at VDD has reached its minimum operating level. Initially, right after power up, TEMPM and TEMPL registers contain 0s. The first measurement result is loaded into TEMPM and TEMPL registers 25 ms after power up.

Table 1. Temperature Sensor Output

TEMPERATURE SENSOR OUTPUT {TEMPM[3:0], TEMPL[7:0]}	TEMPERATURE (°C)
100000000000	–128.0000
111001000000	–28.0000
111111111111	–0.0625
000000000001	0.0625
000110000000	24.0000
011111111111	127.9375

NOTE

The maximum output of the temperature sensor stored in the TEMPM and TEMPL registers is 127.9375°C.

8.3.2 Look-Up-Table (LUT) and Arithmetic-Logic Unit (ALU)

The LUT is used to create an arbitrary transfer function which maps the temperature to the analog output of the device. In concept, the temperature readout is used as a pointer to a table of discrete values that are representative of the samples of the desired temperature-dependent function.

In order to minimize the storage requirements, the LMP92066 LUTs are indexed in 4°C increments. Also, the stored values are only the increments, or first derivatives (Δs) of the modeled transfer function. The internal ALU reconstructs the original transfer function by integrating the coefficients stored in the LUTs. The errors due to the coarseness of the temperature quantization are significantly reduced through the use of linear interpolation, which is also implemented in the ALU.

Consider the example shown in Figure 22. The target output vs temperature is shown in the top graph. V_{DACx} is a smooth, monotonic function with, ideally, infinite precision. The LUT stores only the increments, or the rise, within each 4°C interval.

In order to recreate the original transfer function, the series of increments must be summed together and added to the constant BASE value. BASE represents the constant offset which is lost due to the differentiation - storage of the increments only. This process must also be referenced to the common temperature point. This reference temperature is called BASELINE in this document, and is fixed at 24°C.

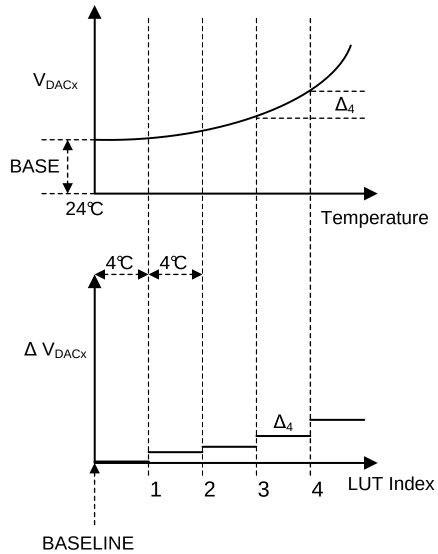


Figure 22. Original Transfer Function

The *LUT and ALU Organization*, *LUT Coefficient to Register Mapping*, and *The LUT Input and Output Ranges* sections below detail the operation of the LUTs and the ALUs.

8.3.2.1 LUT and ALU Organization

In Figure 23 TEMP represents the 12-bit input value to the LUT. This value is produced by the local temperature sensor, or it can be provided by the user through the use of the OVERRIDE registers. The OVERRIDE modes are described in the later sections.

TEMP is truncated, and TEMP[11:6] is used to index the LUT. The truncation is equivalent to reducing the TEMP resolution from 0.0625°C/LSB to 4°C/LSB.

The overall transfer function is stored in the LUT as a set of unsigned 4-bit increments from the BASE value, that is, LUT location (+1) stores the value of the increment Δ_1. This is shown in Figure 23. The BASELINE is 24°C temperature reference point, and BASE is the numeric representation of the required output at 24°C

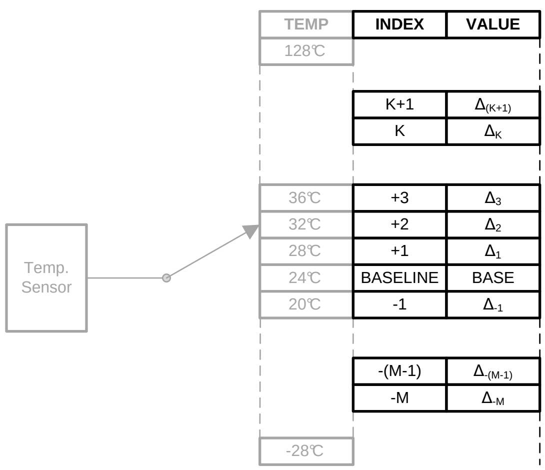


Figure 23. LUT Organization

When TEMP is above 24°C, the LUT is addressed above the BASELINE address, all increments are added to the BASE value to produce numeric equivalent of the analog output. When TEMP is below 24°C, LUT is addressed below the BASELINE, all increments are subtracted from the BASE value to produce DACIN.

Interpolation function is implemented in the ALU that follows the LUT. The truncated lower bits of the TEMP value, REM = TEMP[5:0], are used to interpolate between data points stored in the LUT. A portion of increment, $\alpha\Delta i$, is added to form the final numeric output - the input data to the DAC. The factor α is a fraction of 4°C temperature span, or equivalently it is a fraction of the 64-code temperature span.

$$\alpha = \frac{REM}{64} \quad (1)$$

The process of calculating the DACIN, including the interpolation, is depicted in Figure 24. The DACIN is the final 12-bit value produced by the ALU and the LUT, and forwarded to the DAC for conversion to analog domain.

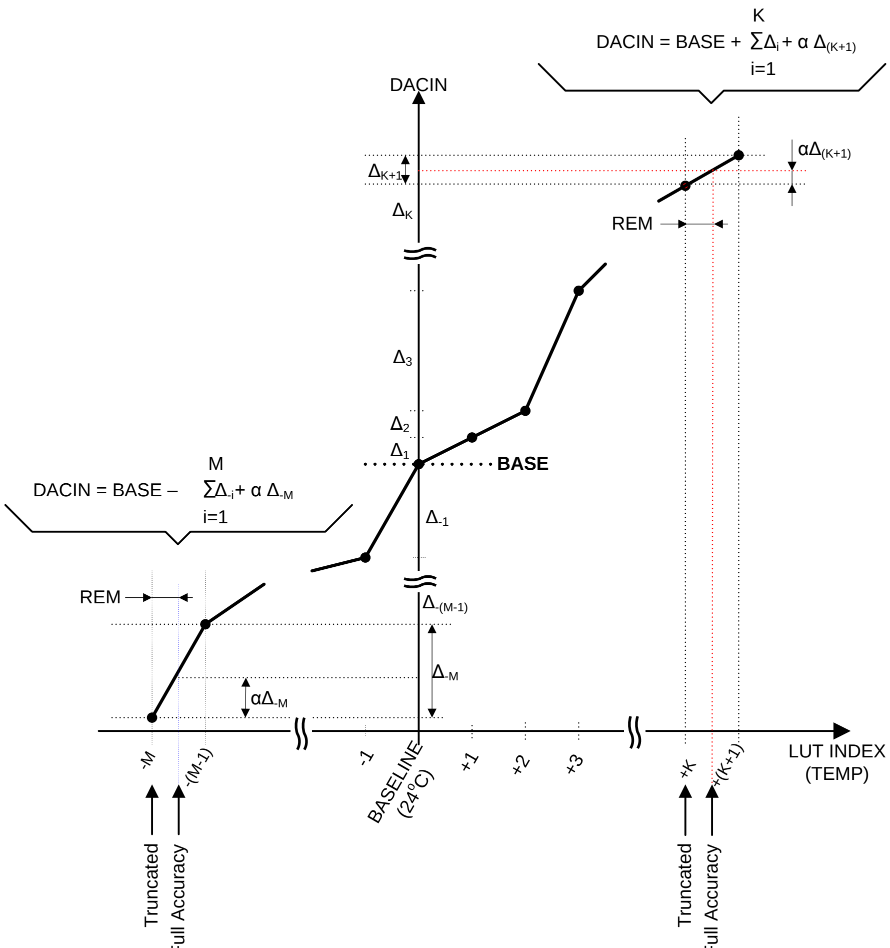


Figure 24. DACIN Calculation

Up to this point the algorithm description concerned only the generation of the monotonically increasing transfer function. The device can also produce monotonically decreasing transfer function by setting the DACx_BASEM.POL bit.

The effect of polarity reversal (POL = 1) on the overall transfer function is shown in Figure 25. The LUT content is unchanged from the original example above. Note that now the LUT values stored at locations above BASELINE address are subtracted from BASE value, and the LUT values stored at locations below BASELINE address are added to the BASE value.

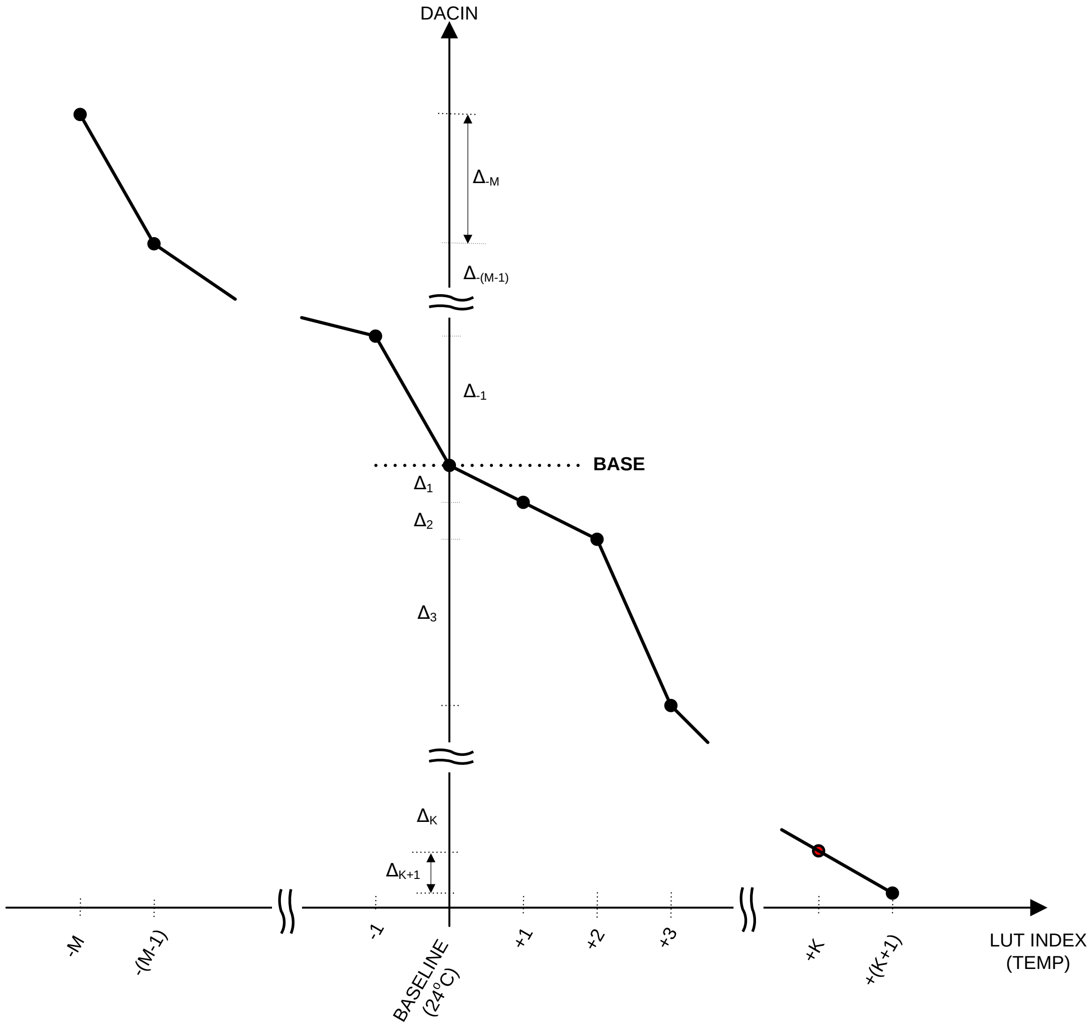


Figure 25. Monotonically Decreasing Transfer Function

The expressions used in the calculation of the transfer function are summarized below:

LUT index > BASELINE:

$$DACIN = BASE + (-1)^{POL}\left(\sum_{i=1}^{K}\Delta_i + \alpha\Delta_{(K+1)}\right) \tag{2}$$

LUT index < BASELINE:

$$DACIN = BASE - (-1)^{POL}\left(\sum_{i=1}^{M}\Delta_{-i} - \alpha\Delta_{-M}\right) \tag{3}$$

8.3.2.2 LUT Coefficient to Register Mapping

For the sake of convenience the preceding sections referred to LUT coefficients as Δ_K. These are stored in the operating memory in the registers DELx. This is reflected in the Register Map section of this document. The example of the Δ_K to DELx register mapping is shown in Table 2 section below.

Table 2. ΔK to DELx Register Mapping

TEMPERATURE	FUNCTION INCREMENT	REGISTER ASSIGNMENT
–28°C	Δ_{-13}	DEL0
↓	↓	↓
20°C	Δ_{-1}	DEL12
28°C	Δ_{+1}	DEL13
↓	↓	↓
124°C		
128°C	Δ_{+26}	DEL38

8.3.2.3 The LUT Input and Output Ranges

The programmable LUT input range spans temperatures –28°C to 128°C. For the temperatures below –28°C the LUT output is linearly extrapolated; that is, the increment Δ_{-13} (register DEL0) stored at the location corresponding to –28°C is used as the slope down to –40°C.

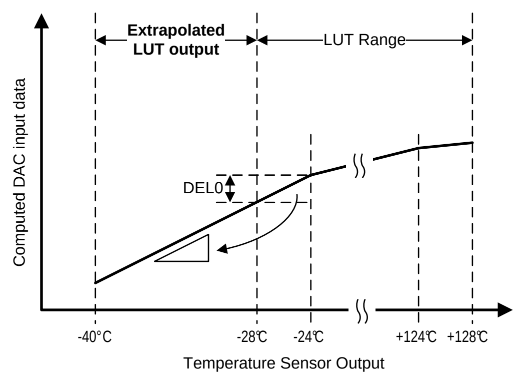


Figure 26. Temperature Sensor Output

Although the maximum output of the temperature sensor is 127.9375°C, the LUT index corresponding to 128°C (DEL38) is required for proper interpolation when the temperature is above 124°C.

The increments stored in the LUT are 4-bit unsigned values. This limits the maximum slope of the transfer function stored in the LUT to:

$$SLOPE_{MAX} = \frac{16LSB}{4°C} = \frac{4LSB}{°C} \tag{4}$$

Given this slope limit imposed by the LUT structure, and the fact that the LUT input range is 156°C (from –28°C to 128°C), the maximum output range of the LUT due to the temperature sensor input is 624 LSBs, for the given BASE value.

NOTE

The maximum span of 624 codes can reside anywhere within the 0 to 4095 code space of the 12-bit DAC input. The total input code to the DAC is the sum of the increments (Δs) and the 12-bit BASE value.

8.3.3 Analog Signal Path

The simplified schematic of one analog channel of the device is shown in Figure 27. The LMP92066 contains 2 such channels. The following sub-sections describe each of the individual blocks within a channel.

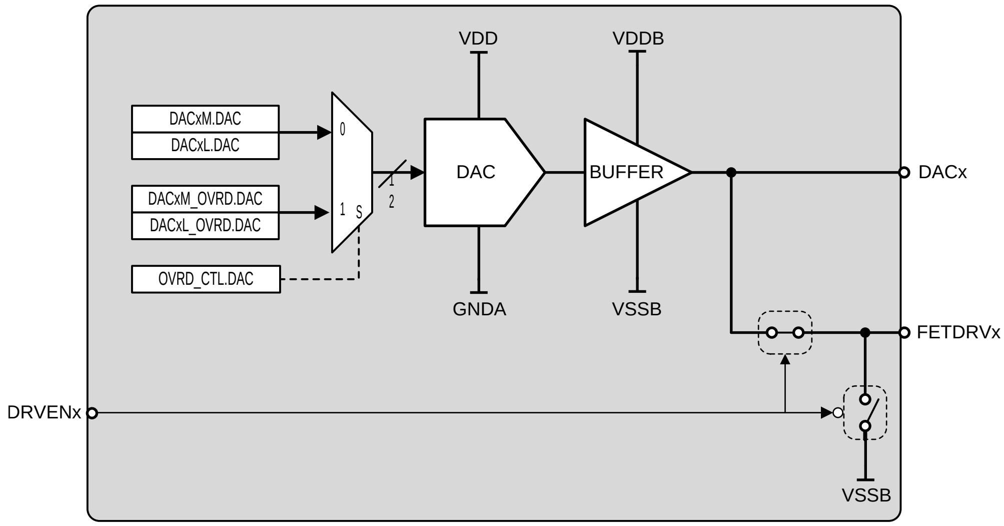


Figure 27. One Analog Channel Simplified Schematic

8.3.3.1 DAC

The DAC produces unipolar output voltage proportional to the 12-bit input code. The input code format is offset binary, where 0x000 represents minimum and the 0xFFF full-scale input. The input code is produced by the LUT/ALU and stored in the DACxM and DACxL read-only registers. The user can also insert the DAC input code via the DACxM_OVRD and DACxL_OVRD registers, and by setting the OVRD_CTL.DAC bit. The DAC is referenced to the internally generated 5 V.

The DAC transfer functions:

$$V_{DACx} = 5A\frac{DACIN}{4096}(V) \quad (5)$$

Where A is the Buffer Amplifier gain (see *Buffer Amplifier*) and DACIN is the 12-bit input code stored in either:

{ DACxM[3:0], DACxL[7:0] }
or
{ DACxM_OVRD[3:0], DACxL_OVRD[7:0] }

The LUT Input and Output Ranges describes the maximum output code span of the LUT, for the given base value. This also implies that when DACxM and DACxL registers are selected as the DAC inputs, the maximum V_{DACx} output excursion over temperature is:

$$dV_{DACx} = SLOPE_{MAX}\ x\ T_{RANGE}\ x\ V_{LSB} = \frac{4LSB}{°C} x 156°C\ x\ \frac{5V}{4096} = 762mV \quad (6)$$

However, this limitation is lifted when using DACxM_OVRD and DACxL_OVRD registers as the DAC inputs. In this case the DAC input range is full 4096 codes, and the output spans 0 V to 5 V.

8.3.3.2 Buffer Amplifier

The buffer amplifier provides the low impedance drive for the potential generated by the DAC. The output of the amplifier is always available at the DACx output pin of the device. The buffer is designed to drive large capacitive loads, as high as 10 µF.

The structure of the Buffer is such that it can produce output voltages above or below GNDA potential. Both Buffer Amplifiers are biased from dedicated supply rails: VDDB and VSSB. The difference between the VDDB and VSSB is nominally 5 V, but the span can be above or below GNDA. The gain A of the Buffer Amplifier depends on the state of supply rails VDDB and VSSB.

When the span is above GNDA, or VDDB = 5 V and VSSB = 0 V, then the output buffer gain is A = 1. The net effect on the output of the analog processing chain is shown in Figure 28. The DAC input codes in the range of 0x000 to 0xFFF are mapped to the output voltage in the range of 0 V to 5 V.

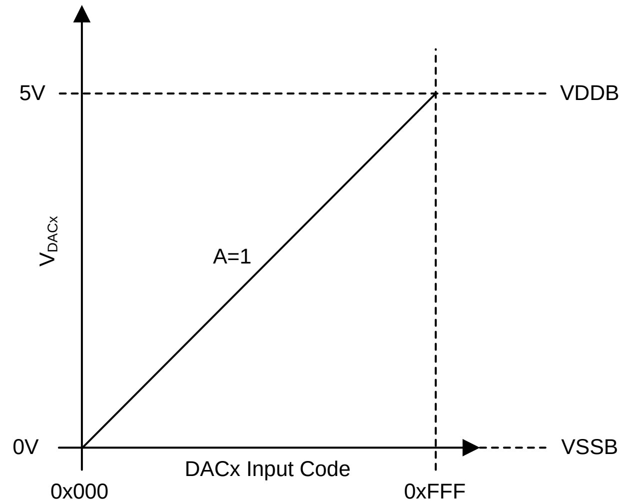


Figure 28. Output of Analog Processing Chain: Net Effect

If the span is below GNDA, or VDDB = 0 V and VSSB = –5 V, then the output buffer gain is A = –1. This configuration is depicted Figure 29. This results in effective mapping of the DAC input codes in the range of 0x000 to 0xFFF, to the output voltage range of 0 V to –5 V.

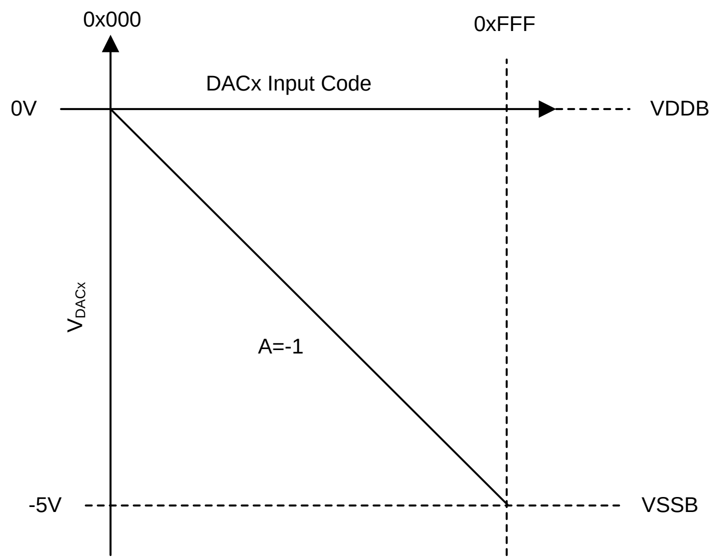


Figure 29. Common Mode Voltage Below GNDA, or VDDB = 0 V and VSSB = –5 V

NOTE

Both Buffer Amplifiers share the VDDB and VSSB rails. Therefore, both Buffers produce gain of A = 1, or both produce gain of A = –1.

The state of the VDDB and VSSB supplies, whether their span is above or below GNDA is indicated by the state of the DRV_STATUS.GAN bit, and can be read by the controller via the I^2C interface.

8.3.3.3 Output On and Off Control

The LMP92066 facilitates rapid turnon and shutdown of the downstream devices. The FETDRVx outputs can be switched ON or OFF by the DRVENx input, independently of the I²C bus transactions. The FETDRVx pin is driven by the Buffer amplifier when the corresponding DRVENx input pin is asserted HIGH. Otherwise, the FETDRVx pin is connected to VSSB.

The control and switch design was optimized for minimum delay between the DRVENx input and the FETDRVx switching. The design also ensures that during the state transition there exists an instance when both switches at FETDRVx are open; that is, no possibility for the crow-bar current to flow from the Buffer output to VSSB.

The switches are assured to default to the state where FETDRVx output is connected to VSSB at power up, as long as logic 0 is present at the DRVENx input.

8.3.4 Memory

The internal memory of the device consists of 2 distinct areas: the user register set or operating memory and the EEPROM (non-volatile storage).

The operating memory registers provide the control over device functionality, report internal status of the device, and store the signal path data (LUT, temperature sensor output, etc). A section of operating memory, designated as a SCRATCH PAD, is available for arbitrary data storage. *All operating memory locations are directly accessible to the user via the I²C bus.*

The EEPROM is not directly accessible via the I²C bus. The EEPROM acquires its data via the transfer from the operating memory, upon user issued command.

Sections *READ and WRITE Access*, *Access Control*, *LUT, NOTEPAD Storage, and EEPROM*, and *Figure 30* detail the internal memory functionality.

8.3.4.1 READ and WRITE Access

The operating memory consists of individually addressable bytes whose content can be accessed via a single I²C transaction. For 8-bit data, as soon as the I²C transfer is complete the transferred value takes effect.

The device also uses values longer that 8 bits — for example, with Temperature Sensor output, Temperature Sensor Override input, and the DAC input and Override registers are 12-bit values which require storage in 2 adjacent registers. For these values any access should start with the register containing the upper 4 bits, immediately followed by the access to the lower byte.

NOTE

It is the WRITE of the lower byte that results in the update of the 12-bit value. See Table 3.

Table 3. Block Writing

I²C OPERATION	REGISTER	DATA	DESCRIPTION
WRITE	BLK_CNTL	0x8F	Enable the BLOCK access and set the block length to 15. This transfer results in the **immediate update** of the BLK_CNTL register and immediate change of behavior of the I²C interface.
WRITE	TEMPM_OVRD	0x08	Write the upper nibble of the Temperature Sensor override value. This transaction **does not result in the update** of the TEMPM_OVRD register. The transferred value is placed on a queue awaiting the transfer of the lower byte. The output of the device is not affected.
WRITE	TEMPL_OVRD	0x00	Write the lower byte of the Temperature Sensor override value. This transaction **results in the update of both** the TEMPM_OVRD and TEMPL_OVRD registers. The output of the device changes accordingly with the new setting.

8.3.4.2 Access Control

By default, all operating memory locations are open to READ access. The WRITE access is controlled by the Access Level setting. Increasing the Access Level, broadens the scope of the WRITE access. There are 3 access levels available to the user; see *Access Control*.

User can change the current Access Level by writing a "password" sequence to the ACC_CNTL register. The "password" sequences are 2 consecutive I^{2}C byte transfers to the ACC_CNTL register. The data content of each 2 byte transfer is unique for each access level.

For example, to enter access level L2 perform the following 2 transfers:

Table 4. Memory Access Control

I^{2}C OPERATION	REGISTER	DATA	DESCRIPTION
WRITE	ACC_CNTL	0xCD	First byte of the "password".
WRITE	ACC_CNTL	0xF0	Second byte of the "password". After this transfer is completed the access level is changed to L2.
READ	ACC_CNTL	0x03	Optional: Reading the ACC_CNTL serves as status report. The possible returned values are: 0x00 – access level L0 0x01 – access level L1 is activated 0x03 – access level L2 is activated (and due to nesting, L1 is also indicated)

Table 5. EEPROM Access Levels

ACCESS LEVEL	SCOPE
L0	Default. User has READ access only to all locations in the operating memory.
L1	User has READ access to all locations, and WRITE access to ADR_LK and BLK_CNTL registers.
L2	User has READ and WRITE access to all operating memory locations.

NOTE

The access levels are nested. This means that L1 access level also gives all L0 level functionality. L2 access level provides L1 and L0 functionality.

8.3.4.3 LUT, NOTEPAD Storage, and EEPROM

The LUT (its coefficients, BASE value, ALU control bits) and the NOTEPAD are stored in the operating memory block spanning addresses 0x40 through 0x7F. This space is directly accessible (READ and WIRITE) via the I^{2}C bus.

There is an option to store the LUT and the NOTEPAD in the non-volatile memory, EEPROM. The move of data from the operating memory to the EEPROM (BURN) is initiated by WRITING a command byte to the EEPROM_CNTL register.

Upon power up the device automatically executes the TRANSFER of the EEPROM data to the operating memory. The user can also issue a command via the I^{2}C bus to force the TRANSFER of data from the EEPROM to the operating memory.

Table 6. EEPROM Control

TRANSFER/BURN	I^{2}C OPERATION	REGISTER	DATA	COMMENT
TRANSFER	WRITE	EEPROM_CNTL	0x4E	Transfer of data from the EEPROM to the operating memory.
BURN	WRITE	EEPROM_CNTL	0xE4	Transfer of data from the operating memory to the EEPROM.

The READ of the EEPROM_CNTL register returns the status of the BURN or TRANSFER.

Table 7. Status of BURN or TRANSFER

EEPROM_CNTL BIT FIELD	DESCRIPTION
RDYB	0 - The TRANSFER or BURN has completed 1 – The TRANSFER or BURN is in progress
COR	1 – A bit error was detected during the transfer from EEPROM to the operating memory. The error has been corrected and the data is valid.
UCOR	1 – A bit error was detected during the transfer from EEPROM to operating memory. The error was not corrected. LUT data is compromised.

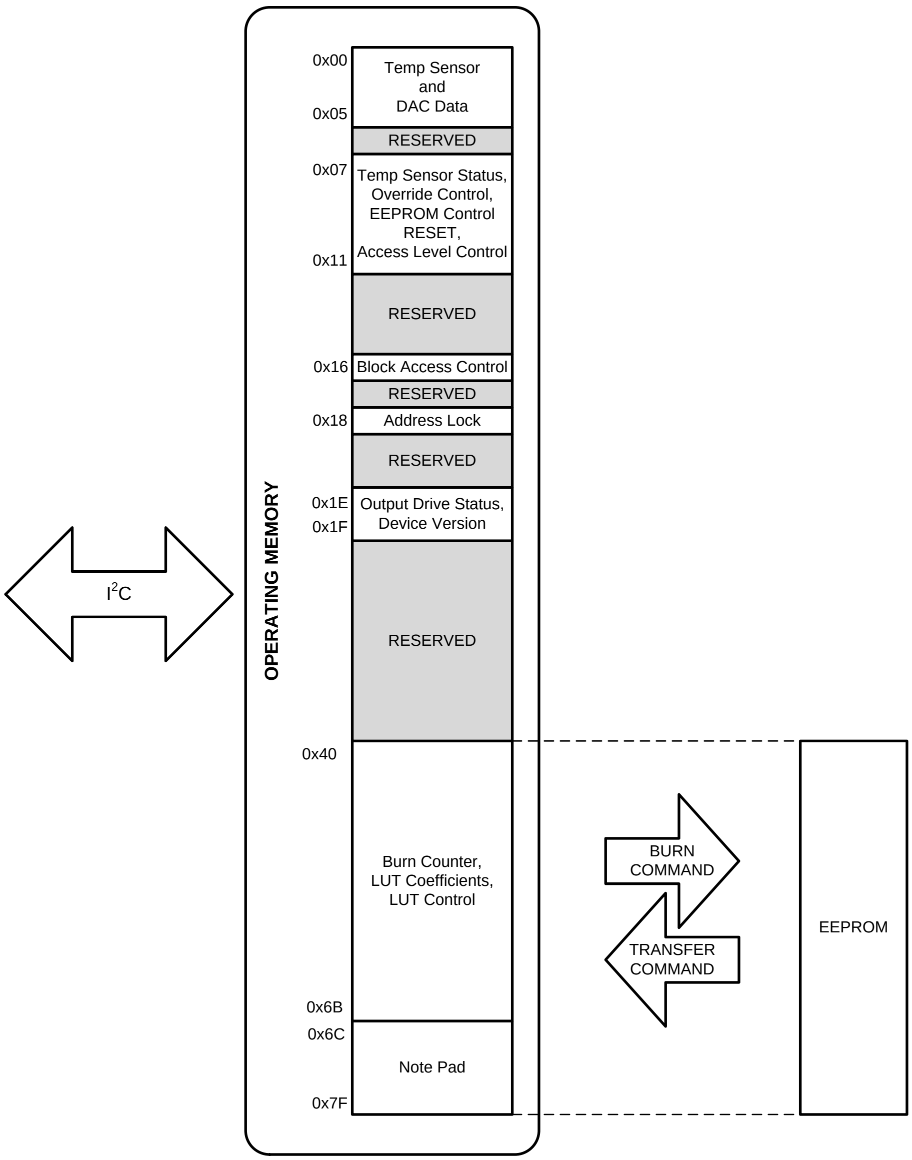


Figure 30. Memory-to-EEPROM Mapping

8.3.5 I²C Interface

I²C bus is used for communication between the Master (the digital supervisor; for example, the microcontroller) and the Slave (LMP92066). This interface provides the user full access to all Data, Status, and Control registers of the device.

LMP92066 supports Standard-mode and Fast-mode, 100 kbit/s and 400 kbit/s, respectively.

All transactions follow the format:

- Master begins all transactions by generating START condition.
- All transfers comprise 8-bit bytes.
- First byte following START must contain 7-bit Slave address.
- First byte is followed by a READ/WRITE bit.
- All subsequent bytes contain 8-bit data.
- By default, the device assumes 1-byte data transfers. Block access can be enabled via BLK_CNTL register, resulting in multi-byte transfers.
- Bit order within a byte is always MSB first
- ACK/NAK condition follows every byte transfer – this can be generated by either Master or the Slave depending on direction of data transfer.
- STOP condition generated by the MASTER terminates all transactions, and resets the I²C bus. LMP92066 resets its internal address pointer to 0x00.

8.3.5.1 Supported Data Transfer Formats

Table 8 lists all conditions defined by the I²C specification and supported by this device. All following bus descriptions refer to the symbols listed in Table 8.

Table 8. I²C Symbol Set

CONDITION	SYMBOL	SOURCE	DESCRIPTION
START	S	Master	Begins all bus transactions
STOP	P	Master	Terminates all transations and resets bus
ACK (Acknowledge)	A	Master/Slave	Handshaking bit (LOW)
NAK (Not Acknowledge)	$\overline{A}$	Master/Slave	Handshaking bit (HIGH)
READ	R	Master	Active HIGH bit that follows immediately after the slave address sequence. Indicates that the master is initiating the slave-to-master data transfer.
WRITE	$\overline{W}$	Master	Active LOW bit that follows immediately after the slave address sequence. Indicates that the master is initiating the master-to-slave data transfer.
REPEATED START	Sr	Master	Generated by master, same function as the START condition (highlights the fact that STOP condition is not strictly necessary.)

The single data byte transfers are shown in Figure 31 and Figure 32:

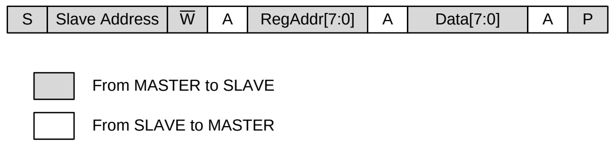


Figure 31. Single-Byte WRITE Access Protocol

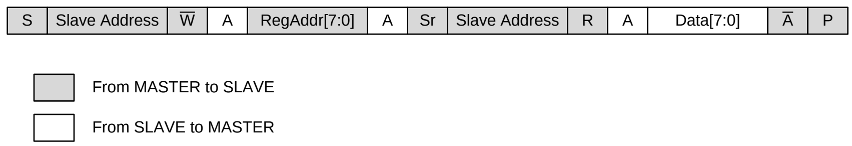


Figure 32. Single-Byte READ Access Protocol

Block Access functionality is provided to minimize the transfer overhead of large data sets. By default the LMP92066 is ready to accept multi-byte transfers. Until the transaction is terminated by the STOP condition, the device will READ (WRITE) the subsequent memory locations.

The size of the contiguous block can be limited by the user. This functionality can be enabled by setting BLK_CNTL.EN bit. The 7-bit value of BLK_CNTL.SIZE=N sets the size of the contiguous memory block that can be accessed via the block transfer.

If the Master generates a block transfer that is larger than (BLK_CNTL.SIZE + 1), the internal register pointer wraps around to the First Register address and the access continue to subsequent memory locations. The examples of the block WRITE and READ transactions are shown below in Figure 33 and Figure 34:

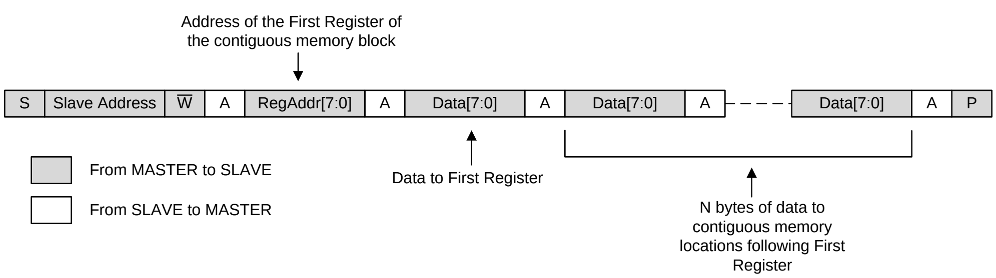


Figure 33. Block WRITE Access — BLK_CNTL.EN = 1, BLK_CNTL.SIZE = N

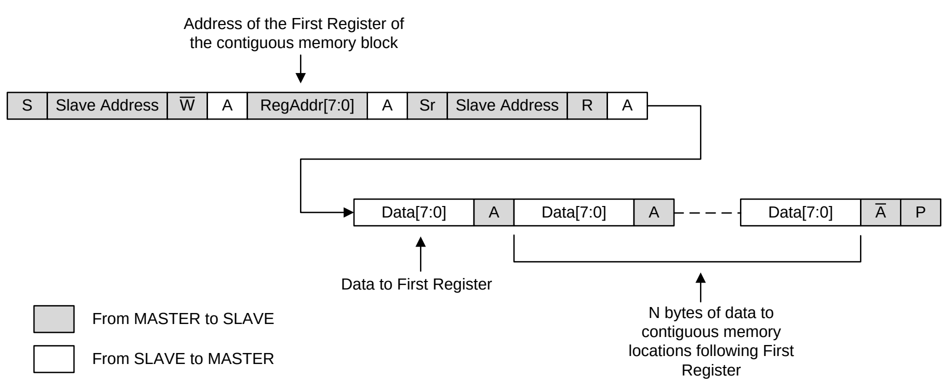


Figure 34. Block READ Access — BLK_CNTL.EN = 1, BLK_CNTL.SIZE = N

8.3.5.2 Slave Address Selection

The I^{2}C bus slave address is selected by installing shunts from A0 and A1 pins of the device to the VIO or GNDD rails. The device discerns between 3 possible options for each pin: shunt to VIO, shunt to GNDD, or left not connected (floating), for the total of 9 possible slave addresses.

The state of the A0 and A1 pins is tested after every occurrence of START condition on the I^{2}C bus. However, the user has an option to LOCK the acquired address by setting the ADR_LK.EN bit. Once the address is locked, the device stores its Slave address internally and does not attempt to decode the address during subsequent I^{2}C transactions. The address lock can be disabled by resetting ADR_LK.EN bit. The device resets the ADR_LK.EN upon power up.

Figure 35 and Figure 36 illustrate the operation of the address decoder circuit. The device internally attempts to pull up, and then pull down, the Ax pin while monitoring the voltage at that pin. If the shunts are installed, the weak pull-ups or pull-downs does not affect the voltage at the Ax pin; that is. the state is fixed by the shunt. If the Ax pin floats, then pull-up and pull-down change the voltage at that pin.

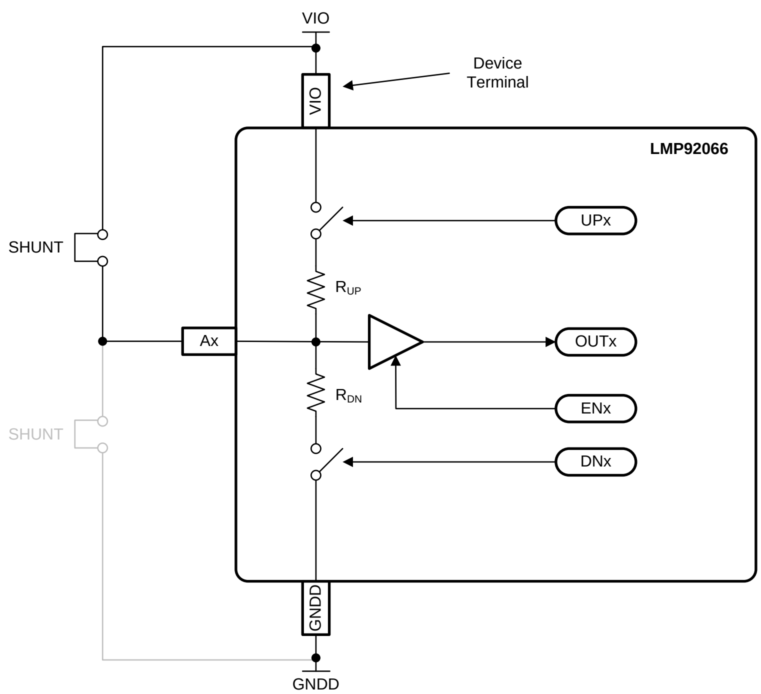


Figure 35. I^{2}C Address Decoder - Simplified Diagram

The address decoder operates during 2nd through 4th cycles of the SCL. The decoding of the state of Ax pins is performed serially; that is, A0 is decoded first then A1. The functional diagram of the address decoder is shown in Figure 36.

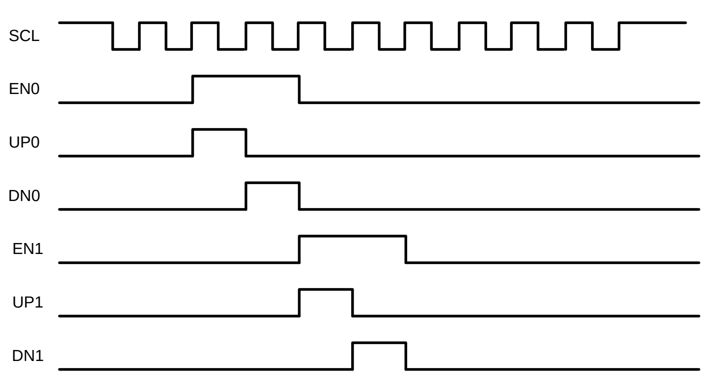


Figure 36. I^{2}C Address Decoder - Functional Diagram

The interpretation of the OUTx values produced from the test phases is summarized in the following table. For example: if a shunt is present between Ax and VIO (first case in the table), both UPx phase and DNx phase result in OUTx being decoded as logical 1, unambiguously indicating the presence of the shunt to VIO, or HI state of Ax.

Table 9. Address Decoder Output

	TEST PHASE		DECODED Ax ↓
	UPx	DNx	
SHUNT to VIO: OUTx →	1	1	HI
SHUNT to GNDD: OUTx →	0	0	LO
NO SHUNT: OUTx →	1	0	N.C.

The mapping from the decoded Ax states to the I^{2}C Slave address is shown in Table 10.

Table 10. Slave Address Space

DEVICE PINS		I^{2}C SLAVE ADDRESS
A1	A0	[A6:A0]
LO	LO	0111111
LO	N.C.	1000000
LO	HI	1000001
N.C.	LO	1000010
N.C.	N.C.	1000011
N.C.	HI	1000100
HI	LO	1000101
HI	N.C.	1000110
HI	HI	1000111

The Slave Address alignment within the first byte following the START condition is shown in Figure 37:

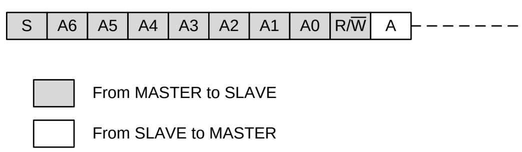


Figure 37. Slave Address Alignment

8.4 Device Functional Modes

The numeric signal path is shown in Figure 38. The signal flow is generally from left to right: the system input is the temperature sensor, signal processing is done by the LUT/ALU, and the output is driven by the DACs - DAC detail is omitted as DACs provide a conversion from numeric domain to voltage domain only, and they do not affect the signal flow.

There are a number of multiplexers in the signal path which alter the data flow when their respective control bits are set. The multiplexer states, and thus modes of device operation, are described in further detail below.

Device Functional Modes (continued)

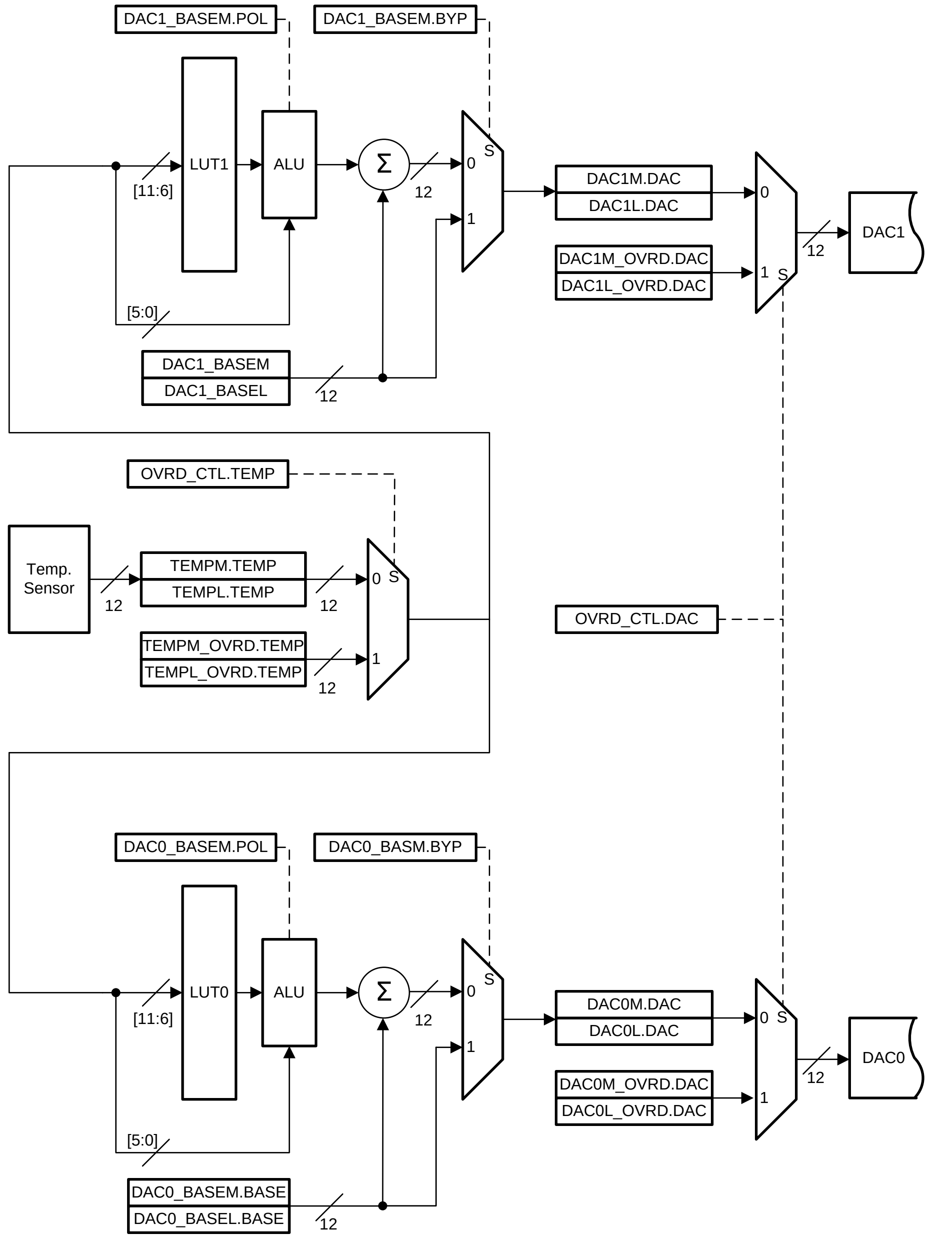


Figure 38. Modes of Operation

8.4.1 Default Operating Mode

This mode of operation is active upon power up. By default the OVRD_CTL.TEMP and OVRD_CTL.DAC are cleared. The temperature sensor continuously updates readings every 25 ms (registers: TEMPM, TEMPL). Each temperature sensor update triggers the ALU to re-calculate its output using the user defined coefficients stored in the LUT. The ALU output is passed on to the DACs (registers: DACxM, DACxL) which ultimately drive the V_{DACx} outputs. All of the functionality described here occurs automatically, without intervention from the system controller, as long as the power is applied to the device supply pins: VDD, VIO, and VDDB.

Device Functional Modes (continued)

8.4.2 Temperature Sensor Override

The temperature sensor output can be overridden by the externally supplied data. This capability may be used to verify the validity of the function stored in the LUT. The externally supplied data can act as the temperature sweep input and the output response due to temperature may be readily observed, without actually altering the temperature of the test setup.

This functionality is facilitated by the multiplexer that follows the temperature sensor, and user writable data registers TEMPM_OVRD and TEMPL_OVRD. TEMPM_OVRD[3:0] is the upper nibble of the temperature data. TEMPL_OVRD[7:0] is the lower byte of the temperature data. The multiplexer control signal is the OVRD_CTL.TEMP bit.

Table 11 shows an example of the I²C bus transfer sequence which results in externally supplied data indexing the LUT.

Table 11. I²C Bus Transfer Sequence: Externally Supplied Data Indexing LUT

I²C OPERATION	REGISTER	DATA	DESCRIPTION
WRITE	ACC_CNTL	0xCD	First byte of the “password”
WRITE	ACC_CNTL	0xF0	Second byte of the “password”. After this transfer is completed the access level is changed to L2
READ	ACC_CNTL	0x03	Optional: Reading the ACC_CNTL serves as status report. 0x03 – access level L2 is activated (and due to nesting, L1 is also indicated)
WRITE	TEMPM_OVRD	0x01	Writes 0x1 as the value of the top nibble of the 12-bit, twos complement, temperature value. After this transaction the TEMPM_OVRD register is not updated, yet. The update takes place only after the TEMPL_OVRD register is written.
WRITE	TEMPL_OVRD	0x01	Writes 0x01 into the lower byte of temperature value. After this transaction completes both TEMPM_OVRD and TEMPL_OVRD registers are updated. The 12-bit value in this example is 0x101 which corresponds to 16.0625°C
WRITE	OVRD_CTL	0x01	Sets the OVRD_CTL.TEMP bit. This causes the temperature stored in the TEMPM_OVRD and TEMPL_OVRD to index the LUT.
READ READ	TEMPM TEMPL	0x** 0x**	Optional: Read the actual temperature reported by the temperature sensor.

The temperature sensor override is cancelled by clearing the OVRD_CTL.TEMP bit.

NOTE

TEMPM_OVRD, TEMPL_OVRD and OVRD_CTL registers are in the volatile section of memory and are not backed by EEPROM. Upon power up these registers are cleared.

8.4.3 ALU Bypass

It may be desirable that the device produces a predetermined constant output level as soon as it is powered up. The ALU bypass mode does that. This mode is enabled by setting DACx_BASEM.BYP bit. Since DACx_BASEM.BYP is stored in the EEPROM, its value is automatically loaded into the operating memory at power up. If the stored value for DACx_BASEM.BYP is 1, upon power up the corresponding DAC output immediately produces an analog output equivalent of the BASE.

In this mode of operation the ALU is bypassed, and the BASE value of the LUT is presented at the input of the DAC. This is the result of DACx_BASEM.BYP, which controls the mux that follows the ALU in the signal path, being set. Therefore, the output of the device is constant over the operating temperature range of the device.

NOTE
Each channel has its own BYP bit, and its own BASE value.

8.4.4 DAC Input Override

The DAC inputs words can be directly written via the I²C interface. In this mode the LMP92066 is a dual 12-bit DAC. This functionality is facilitated by the multiplexers that precede the DACs, and user writable data registers DACxM_OVRD and DACxL_OVRD. DACxM_OVRD[3:0] is the upper nibble of the DAC input word. DACxL_OVRD[7:0] is the lower byte of the DAC input data.

The multiplexer control signal is the OVRD_CTL.DAC bit. This bit is shared by both channels; that is, both channels are either in the DAC input override mode, or both are in the default mode.

Table 12 shows the example of the I²C bus transfer sequence which results in externally supplied data being the source of input to the DACs.

Table 12. I²C Bus Transfer Sequence: Externally Supplied Data Sourcing Input to DACs

I²C OPERATION	REGISTER	DATA	DESCRIPTION
WRITE	ACC_CNTL	0xCD	First byte of the "password"
WRITE	ACC_CNTL	0xF0	Second byte of the "password". After this transfer is completed the access level is changed to L2
READ	ACC_CNTL	0x03	Optional: Reading the ACC_CNTL serves as status report. 0x03 – access level L2 is activated (and due to nesting, L1 is also indicated)
WRITE	DAC0M_OVRD	0x08	Writes 0x8 as the value of the top nibble of the 12-bit, offset binary, DAC0 input value. After this transaction the DAC0M_OVRD register is not updated, yet. The update takes place only after the DAC0L_OVRD register is written.
WRITE	DAC0L_OVRD	0x00	Writes 0x00 into the lower byte of the DAC0 input value. After this transaction completes both DAC0M_OVRD and DAC0L_OVRD registers are updated. The 12-bit value in this example is 0x800.
WRITE	DAC1M_OVRD	0x04	Writes 0x4 as the value of the top nibble of the 12-bit, offset binary, DAC1 input value. After this transaction the DAC1M_OVRD register is not updated, yet. The update takes place only after the DAC1L_OVRD register is written.
WRITE	DAC1L_OVRD	0x00	Writes 0x00 into the lower byte of the DAC1 input value. After this transaction completes both DAC1M_OVRD and DAC1L_OVRD registers are updated. The 12-bit value in this example is 0x400.
WRITE	OVRD_CTL	0x02	Sets the OVRD_CTL.TEMP bit. This causes both multiplexers that precede the DACs to start routing the DACx_OVRD values to the inputs of their respective DACs. As a result the outputs of the device are: VDAC0 = 2.5 V, and VDAC1 = 1.25 V
READ READ	DAC0M DAC0L	0x** 0x**	Optional: Read the values computed by the ALU.

NOTE
The DAC Input Override and Temperature Sensor Override modes are mutually exclusive. The allowed values for OVRD_CTRL register are 0x00, 0x01 or 0x02.

NOTE
DACxM_OVRD, DACxL_OVRD and OVRD_CTL registers are in the volatile section of memory and are not backed by EEPROM. Upon power up these registers are cleared.

8.4.5 LDMOS and GaN Drives

The LDMOS mode and the GaN mode result from 2 possible biasing methods of the DAC output buffers – these were described in earlier sections of this data sheet.

The LDMOS mode is in effect when the VDDB and VSSB common mode is above GNDA. This mode is suitable for biasing of the LDMOS Power Amplifiers, since the output produced by the LMP92066 is in the 0 V to 5 V range. The GaN mode is in effect when the VDDB and VSSB common mode is below GNDA. This mode is suitable for biasing of the GaN type Power Amplifiers, as the output produced by the LMP92066 is in the 0V to –5V range.

8.5 Programming

8.5.1 Temperature Sensor Output Data Access Registers

The temperature sensor produces a 12-bit output value, TEMP[11:0], which is stored in 2 adjacent registers: TEMPM and TEMPL.

The temperature sensor updates its output every 25 ms, nominally, but the exact instance of the update is unknown to the user. It is possible that the temperature sensor produces a new value between READ operations of TEMPM and TEMPL. Therefore, a synchronization mechanism was implemented, to assure that TEMPM and TEMPL values correspond to the same temperature sample. The coherence of the temperature sensor data is maintained if the READ sequence is: read TEMPM first, then TEMPL.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x00	TEMPM	R	L0	7	RES	Reserved bit. The value may be reported as 0 or 1
				6:5	*	Reserved bit. Always reported as 0.
				4	RES	Reserved bit. The value may be reported as 0 or 1.
				3:0	TEMP[11:8]	4-bit MSB nibble of the 12-bit Temperature Sensor output word.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x01	TEMPL	R	L0	7:0	TEMP[7:0]	8-bit LSB byte of the 12-bit Temperature Sensor output word.

8.5.2 DAC Input Data Registers

The 12-bit data produced by the LUT and ALU is stored in the DAC0M and DAC0L, and DAC1M and DAC1L pairs of registers. Unless overridden (see *Override Control Register*), the contents of these registers are presented at each DAC inputs.

In cases where the user wants to read the temperature sensor output and resulting DACxM or DACxL data, the following read order has to be maintained to assure the coherency of data: TEMPM, TEMPL, DAC0M, DAC0L, DAC1M, DAC1L.

Coherency of the TEMPM is still maintained, and TEMPL read is omitted in the sequence above.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x02	DAC0M	R	L0	7:4	*	Reserved bit. Always report as 0.
				3:0	DAC[11:8]	4-bit MSB nibble of the 12-bit DAC0 input word.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x03	DAC0L	R	L0	7:0	DAC[7:0]	8-bit LSB byte of the 12-bit Temperature Sensor output word.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x04	DAC1M	R	L0	7:4	*	Reserved bit. Always report as 0.
				3:0	DAC[11:8]	4-bit MSB nibble of the 12-bit DAC1 input word.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x05	DAC1L	R	L0	7:0	TEMP[7:0]	8-bit LSB byte of the 12-bit DAC1 input word.

8.5.3 Temperature Sensor Status Register

This register may contain non-zero values immediately after the device power up. Within 100 ms of the power up the TEMP_STATUS register clears, indicating the temperature sensor's output is valid.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x07	TEMP_STATUS	R	L0	7:0	RBYB	If RDYB=0x00, the Temperature Sensor is initialized and producing valid output.

8.5.4 Override Control Register

Override functionality allows the user to insert external data into the signal path of the device. When TEMP override is enabled, the temperature sensor's data is ignored, and the user-supplied data is used to index the LUT (TEMPM_OVRD and TEMPL_OVRD, below). When DAC override is enabled the LUT and ALU produced output is ignored, and both DAC0 and DAC1 use external data as their inputs (DAC0M_OVRD, DAC0L_OVRD and DAC1M_OVRD and DAC1L_OVRD described below).

NOTE

Only 3 OVRD_CNTL[2:0] settings are allowed: 0x0, 0x1, 0x2; simultaneous DAC and TEMP override is not allowed.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x08	OVRD_CNTL	R/W	L2	7:4	*	Reserved bit. Always WRITE 0
				3	RES	Reserved bit. Always WRITE 0
				2	RES	Reserved bit. Always WRITE 0
				1	DAC	DAC override enable bit: 0: DAC input generated by LUT 1: DAC input is supplied from user accessible registers DACxy_OVRD.
				0	TEMP	DAC override enable bit: 0: DAC input generated by LUT 1: DAC input is supplied from user accesible registers TEMPy_OVRD.

8.5.5 Override Data Registers

These registers hold the externally supplied data to be inserted into the signal path of the device (see OVRD_CNTL).

NOTE

Since override data are 12-bit words stored in 2 adjacent registers, it is the writing of the lower byte that makes the new value take effect.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x09	TEMPM_OVRD	R/W	L2	7:4	*	Reserved bit. Always report as 0.
				3:0	TEMP[11:8]	4-bit MSB nibble of the 12-bit Temperature Sensor override input word.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x0A	TEMPL_OVRD	R/W	L2	7:0	TEMP[7:0]	8-bit LSB byte of the 12-bit Temperature Sensor output word.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x0B	DAC0M_OVRD	R/W	L2	7:4	*	Reserved bit. Always report as 0.
				3:0	DAC[11:8]	4-bit MSB nibble of the 12-bit DAC0 input override word.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x0C	DAC0L_OVRD	R/W	L2	7:0	DAC[7:0]	8-bit LSB byte of the 12-bit DAC0 input override word.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x0D	DAC1M_OVRD	R/W	L2	7:4	*	Reserved bit. Always report as 0.
				3:0	DAC[11:8]	4-bit MSB nibble of the 12-bit DAC1 input override word.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x0E	DAC1L_OVRD	R/W	L2	7:0	DAC[7:0]	8-bit LSB byte of the 12-bit DAC1 input override word.

8.5.6 EEPROM Control Register

Writing a command byte results in either the EEPROM BURN (the commitment of a section of operating memory to non-volatile storage), or the TRANSFER (recall of the data in the non-volatile storage to the operating memory.

Reading this register yields status information.

NOTE
UCOR and COR bits are updated only by the TRANSFER command.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x0F	EEPROM_CNTL	W	L2	7:0	*	Instruction to BURN EEPROM or TRANSFER EEPROM content to operating memory: 0xE4: BURN EEPROM. 0x4E: TRANSFER data from EEPROM to operating memory.
		R	L0	7:3	*	Reserved bit.
				2	UCOR	1: More than one bit error was detected during the TRANSFER, and correction was not possible. 0: No uncorrected errors were detected during the TRANSFER.
				1	COR	1: A bit error was detected and corrected during the TRANSFER. 0: No errors detected during the TRANSFER.
				0	RDYB	1: BURN or TRANSFER in progress. 0: BURN or TRANSFER completed.

8.5.7 Software RESET Register

Has the same effect as the power-on reset.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x10	RESET	W	L2	7:0	DAC[7:0]	WRITE 0xC3 to reset the deice to the power-up default state.

8.5.8 Access Control Register

Changing the Access Level requires writing the 2-byte password sequence. Reading this register yields status information.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x11	ACC_CNTL	W	L0	7:0	PSWD	WRITE 2-byte password to change access level: 0xCD, 0xEF: Access Level L1. 0xCD, 0xF0: Access Level L2.
		R	L0	7:2	*	*
				1	*	1: Access Level L2 is enabled. 0: L2 not enabled.
				0	RES	1: Access Level L1 is enabled. 0: L1 not enabled.

8.5.9 Block I²C Access Control Register

The I²C master may request a continuous transfer of data from or to the slave. By default, the slave continues advancing its internal register pointer to the end of the internal register space, and then wrap back to address 0x00 and continue on.

BLK_CNTL allows to limit the size of the contiguous memory accessed continuously.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x16	BLK_CNTL	R/W	L1	7	EN	Enable the control of the I²C access block size: 1: Enabled. 0: Block size control is disabled.
				6:0	*	7-bit SIZE of the I²C access block. The continuous I²C transaction accesses SIZE+1 memory locations, and then wrap back to the starting address.

8.5.10 I²C Address LOCK Register

Allows the device to LOCK its own I²C slave address. Once the slave address is locked, the device does not attempt to decode the state of A0 and A1 address setting pins on subsequent transactions.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x18	ADR_LK	R/W	L1	7:3	*	Always set to 0
				2	RES	Reserved bit. Always write 0.
				1	RES	Reserved bit. Always write 0.
				0	EN	1: Lock the slave address 0: Slave address is not locked. Device decodes state of A1 and A0 after every START condition of the I²C bus.

NOTE

The locked address is the one present at the A[1:0] pins during the I²C transaction that follows the ADR_LK command.

8.5.11 Output Drive Supply Status Register

The device output stage can operate in either LDMOS or GaN modes. The mode is determined by the potential applied to the VDDB and VSSB supply pins.

The device monitors the VDDB and VSSB supplies, and reports the mode of operation via the GaN status bit.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x1E	DRV-STATUS	R	L0	7:1	*	Reserved. Always reports 0
				0	GAN	1: GaN mode supply rails detected; that is, VDDB = GNDA, VSSB = –5V. 0: LDMOS mode supply rails detected; that is, VDDB = +5V, VSSB = GNDA.

8.5.12 Device Version Register

Factory set value.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x1F	VERSION	R	L0	7:0	VERSION	8-bit device revision number.

8.5.13 EEPROM Burn Counter

The value is incremented automatically at the start of BURN sequence.

This data is transferred automatically from the EEPROM to operating memory upon power up.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x40	BURN_CT	R	L0	7:0	COUNT	8-bit EEPROM BURN counter.

8.5.14 LUT Coefficient Registers

This data is transferred to the EEPROM when a BURN command sequence is issued.

This data is transferred automatically from the EEPROM to operating memory upon power up or after a software reset.

NOTE

The LUT values are stored at locations corresponding to 4°C increments from –28°C to 128°C. There is no increment corresponding to 24°C because this temperature is a BASELINE, and the corresponding LUT value is 12-bit BASE (see *Look-Up-Table (LUT) and Arithmetic-Logic Unit (ALU)*).

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x41 ↓ 0x4D 0x4E ↓ 0x67	DEL0 ↓ DEL12 (20°C) DEL13 (28°C) ↓ DEL38 (128°C)	R/W	L2	7:4	DAC1[3:0]	4-bit LUT1 entry
				3:0	DAC0[3:0]	4-bit LUT0 entry

8.5.15 LUT Control Registers

This data is transferred to the EEPROM when a BURN command sequence is issued.

This data is transferred automatically from the EEPROM to operating memory upon power up.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x68	DAC0_BASEM	R/W	L2	7	RES	Reserved bit. Always write 0.
				6	RES	Reserved bit. Always reported as 0.
				5	BYP	ALU bypass control: 1: Bypass ALU. Send BASE value to DAC0. 0: ALU output sent to DAC0.
				4	POL	LUT increment polarity control: 1: All LUT values are treated as negatives. This realizes a monotonically decreasing LUT0 transfer function. 0: All LUT values are treated as positive numbers. This realizes a monotonically increasing LUT0 transfer function.
				3:0	BASE[11:8]	4-bit MSB nibble of the 12-bit LUT0 BASE value (LUT0 output at +24°C).

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x69	DAC0_BASEL	R	L2	7:0	BASE[7:0]	8-bit LSB byte of the 12-bit BASE value (LUT0 output at +24°C).

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x6A	DAC1_BASEM	R/W	L2	7	RES	Reserved bit. Always write 0.
				6	RES	Reserved bit. Always reported as 0.
				5	BYP	ALU bypass control: 1: Bypass ALU. Send BASE value to DAC1. 0: ALU output sent to DAC1.
				4	POL	LUT increment polarity control: 1: All LUT values are treated as negatives. This realizes a monotonically decreasing LUT1 transfer function. 0: All LUT values are treated as positive numbers. This realizes a monotonically increasing LUT1 transfer function.
				3:0	BASE[11:8]	4-bit MSB nibble of the 12-bit LUT1 BASE value (LUT0 output at +24°C).

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x6B	DAC1_BASEL	R	L2	7:0	BASE[7:0]	8-bit LSB byte of the 12-bit BASE value (LUT1 output at +24°C).

8.5.16 Notepad Registers

20 bytes of memory for arbitrary data storage. This data does not affect the operation of the device. This data is transferred to the EEPROM when BURN command sequence is issued.

This data is transferred automatically from the EEPROM to operating memory upon power up.

ADDRESS	NAME	ACCESS TYPE	ACCESS LEVEL	BIT	FUNCTION	DESCRIPTION
0x6C ↓ 0x7F	PAD0 ↓ PAD19	R/W	L2	7:0	*	20 bytes of memory for arbitrary data storage. This data does not affect the operation of the device. This data is transferred to the EEPROM when BURN command sequence is issued via I^2C transaction.

8.6 Register Map

ADDRESS	TYPE	ACC. LVL	NAME	BIT FIELDS 7	6	5	4	3	2	1	0	NOTES	POR
8'h00	R	L0	TEMPM	RES	0		RES	TEMP[11:8]					
8'h01	R	L0	TEMPL	TEMP[7:0]									
8'h02	R	L0	DAC0M	0				DAC[11:8]					
8'h03	R	L0	DAC0L	DAC[7:0]									
8'h04	R	L0	DAC1M	0				DAC[11:8]					
8'h05	R	L0	DAC1L	DAC[7:0]									
8'h06	R	L0	RES	RES									
8'h07	R	L0	TEMP_STATUS	RDYB	RDYB	RDYB	RDYB	RDYB	RDYB	RDYB	RDYB		8'hFF
8'h08	R/W	L2	OVRD_CNTL					RES	RES	DAC	TEMP		
8'h09	R/W	L2	TEMPM_OVRD	0				TEMP[11:8]					8'h01
8'h0A	R/W	L2	TEMPL_OVRD	TEMP[7:0]									8'h80
8'h0B	R/W	L2	DAC0M_OVRD	0				DAC[11:8]					8'h80
8'h0C	R/W	L2	DAC0L_OVRD	DAC[7:0]									8'h00
8'h0D	R/W	L2	DAC1M_OVRD	0				DAC[11:8]					8'h80
8'h0E	R/W	L2	DAC1L_OVRD	DAC[7:0]									8'h00
8'h0F	W	L2	EEPROM_CNTL	BURN or TRNASFER command								For BURN write: 8'hE4 For TRANSFER write: 8'h4E	
8'h0F	R	L0	EEPROM_CNTL						UCOR	COR	RDYB		
8'h10	W	L2	RESET	SYSTEM RESET – EQUIVALENT TO POWER-UP								write: 8'hC3	
8'h11	W	L0	ACC_CNTL	ACCESS LEVEL PASSWORD								For L1 write: 8'hCD,8'hEF For L2 write: 8'hCD,8'hF0	
8'h11	R	L0	ACC_CNTL							L2	L1		8'h00
8'h12	R/W	L1	RES	0							RES		8'h00
8'h13	W	L1	RES	0							RES		8'h00
8'h13	R	L0	RES	0							RES		8'h00
8'h14	R/W	L1	RES	RES									8'h00
8'h15	R/W	L1	RES	RES									8'h00
8'h16	R/W	L1	BLK_CNTL	EN	SIZE								8'h00
8'h17	R/W	L1	RES	0					RES	RES	RES		8'h00
8'h18	R/W	L1	ADR_LK	0					RES	RES	EN		8'h00
8'h19	R/W	L1	RES	0						RES	RES		8'h00
8'h1A	R/W	L1	RES	0						RES	RES		8'h00
8'h1E	R	L0	DRV_STATUS	0							GAN		
8'h1F	R	L0	VERSION	VERSION=8'hA0									

Register Map (continued)

ADDRESS	TYPE	ACC. LVL	NAME	BIT FIELDS 7	6	5	4	3	2	1	0	NOTES	POR
8'h40	R	L0	BURN_CT										
8'h41	R/W	L2	DEL0	DAC1[3:0]				DAC0[3:0]				-28℃	
8'h42	R/W	L2	DEL1	DAC1[3:0]				DAC0[3:0]				-24℃	
8'h43	R/W	L2	DEL2	DAC1[3:0]				DAC0[3:0]				-20℃	
8'h44	R/W	L2	DEL3	DAC1[3:0]				DAC0[3:0]				-16℃	
8'h45	R/W	L2	DEL4	DAC1[3:0]				DAC0[3:0]				-12℃	
8'h46	R/W	L2	DEL5	DAC1[3:0]				DAC0[3:0]				-8℃	
8'h47	R/W	L2	DEL6	DAC1[3:0]				DAC0[3:0]				-4℃	
8'h48	R/W	L2	DEL7	DAC1[3:0]				DAC0[3:0]				0℃	
8'h49	R/W	L2	DEL8	DAC1[3:0]				DAC0[3:0]				4℃	
8'h4A	R/W	L2	DEL9	DAC1[3:0]				DAC0[3:0]				6℃	
8'h4B	R/W	L2	DEL10	DAC1[3:0]				DAC0[3:0]				12℃	
8'h4C	R/W	L2	DEL11	DAC1[3:0]				DAC0[3:0]				16℃	
8'h4D	R/W	L2	DEL12	DAC1[3:0]				DAC0[3:0]				20℃	
8'h4E	R/W	L2	DEL13	DAC1[3:0]				DAC0[3:0]				28℃	
8'h4F	R/W	L2	DEL14	DAC1[3:0]				DAC0[3:0]				32℃	
8'h50	R/W	L2	DEL15	DAC1[3:0]				DAC0[3:0]				36℃	
8'h51	R/W	L2	DEL16	DAC1[3:0]				DAC0[3:0]				40℃	
8'h52	R/W	L2	DEL17	DAC1[3:0]				DAC0[3:0]				44℃	
8'h53	R/W	L2	DEL18	DAC1[3:0]				DAC0[3:0]				48℃	
8'h54	R/W	L2	DEL19	DAC1[3:0]				DAC0[3:0]				52℃	
8'h55	R/W	L2	DEL20	DAC1[3:0]				DAC0[3:0]				56℃	

Register Map (continued)

ADDRESS	TYPE	ACC. LVL	NAME	BIT FIELDS								NOTES	POR
				7	6	5	4	3	2	1	0		
8'h56	R/W	L2	DEL21	DAC1[3:0]				DAC0[3:0]				60℃	
8'h57	R/W	L2	DEL22	DAC1[3:0]				DAC0[3:0]				64℃	
8'h58	R/W	L2	DEL23	DAC1[3:0]				DAC0[3:0]				68℃	
8'h59	R/W	L2	DEL24	DAC1[3:0]				DAC0[3:0]				72℃	
8'h5A	R/W	L2	DEL25	DAC1[3:0]				DAC0[3:0]				76℃	
8'h5B	R/W	L2	DEL26	DAC1[3:0]				DAC0[3:0]				80℃	
8'h5C	R/W	L2	DEL27	DAC1[3:0]				DAC0[3:0]				84℃	
8'h5D	R/W	L2	DEL28	DAC1[3:0]				DAC0[3:0]				88℃	
8'h5E	R/W	L2	DEL29	DAC1[3:0]				DAC0[3:0]				92℃	
8'h5F	R/W	L2	DEL30	DAC1[3:0]				DAC0[3:0]				96℃	
8'h60	R/W	L2	DEL31	DAC1[3:0]				DAC0[3:0]				100℃	
8'h61	R/W	L2	DEL32	DAC1[3:0]				DAC0[3:0]				104℃	
8'h62	R/W	L2	DEL33	DAC1[3:0]				DAC0[3:0]				108℃	
8'h63	R/W	L2	DEL34	DAC1[3:0]				DAC0[3:0]				112℃	
8'h64	R/W	L2	DEL35	DAC1[3:0]				DAC0[3:0]				116℃	
8'h65	R/W	L2	DEL36	DAC1[3:0]				DAC0[3:0]				120℃	
8'h66	R/W	L2	DEL37	DAC1[3:0]				DAC0[3:0]				124℃	
8'h67	R/W	L2	DEL38	DAC1[3:0]				DAC0[3:0]				128℃	
8'h68	R/W	L2	DAC0_BASEM	RES	RES	BYP	POL	BASE[11:8]				24℃	
8'h69	R/W	L2	DAC0_BASEL	BASE[7:0]								24℃	
8'h6A	R/W	L2	DAC1_BASEM	RES	RES	BYP	POL	BASE[11:8]				24℃	
8'h6B	R/W	L2	DAC1_BASEL	BASE[7:0]								24℃	

Register Map (continued)

ADDRESS	TYPE	ACC. LVL	NAME	BIT FIELDS 7 6 5 4 3 2 1 0	NOTES	POR
8'h6C	R/W	L2	PAD0			
8'h6D	R/W	L2	PAD1			
8'h6E	R/W	L2	PAD2			
8'h6F	R/W	L2	PAD3			
8'h70	R/W	L2	PAD4			
8'h71	R/W	L2	PAD5			
8'h72	R/W	L2	PAD6			
8'h73	R/W	L2	PAD7			
8'h74	R/W	L2	PAD8			
8'h75	R/W	L2	PAD9			
8'h76	R/W	L2	PAD10			
8'h77	R/W	L2	PAD11			
8'h78	R/W	L2	PAD12			
8'h79	R/W	L2	PAD13			
8'h7A	R/W	L2	PAD14			
8'h7B	R/W	L2	PAD15			
8'h7C	R/W	L2	PAD16			
8'h7D	R/W	L2	PAD17			
8'h7E	R/W	L2	PAD18			
8'h7F	R/W	L2	PAD19			

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMP92066 was designed for ease of use. The device requires minimum external components to realize its full functionality. In the typical application the bulk of the design effort is spent on characterization of the target transfer function, and then developing a set of coefficients that the LMP92066 to accurately reproduce the target function.

NOTE

The LMP92066 can approximate temperature dependent functions, $V_{DAC0,1}(T)$, only if the following requirements are met:

1. Each $V_{DAC0,1}(T)$ must be unipolar. The range of the function must be either wholly positive, or wholly negative. This is dictated by the structure of the Buffer Amplifier that drives the FETDRVx. See the *Buffer Amplifier* section.
2. Both functions $V_{DAC0,1}(T)$ must be of the same polarity. See the *Buffer Amplifier* section.
3. Each $V_{DAC0,1}(T)$ must be monotonic. This is dictated by the structure of the LUTs. See the *LUT and ALU Organization* section.
4. The maximum slope of each $V_{DAC0,1}(T)$ is no greater than 4.88 mV/°C. This also limits the maximum range, the minimum to maximum span, for the $V_{DAC0,1}(T)$ to 761 mV. This is due to the fact that the LUT stores the slope of the $V_{DAC0,1}(T)$ as 4-bit values. See the *The LUT Input and Output Ranges* section.

9.2 Typical Applications

9.2.1 Temperature Compensated Bias Generator for LDMOS Power Amplifer (PA)

The typical application for the LMP92066 is the biasing of the power amplifiers in an RF system. What is required in such applications is for the PA drain current to remain constant over a wide range of operating temperatures. The LMP92066 senses the PA temperature and adjust the bias potential at the gate of the PA in accordance with the known $V_{GS}(T)$, at I_D = constant, characteristic of the PA.

The typical application circuit for LDMOS applications is shown in Figure 39. A thermal path has to be provided between the LMP92066 and the PA. This is typically accomplished through the close proximity of the 2 devices, and the common metal layer. See also the *Layout Example*.

Typical Applications (continued)

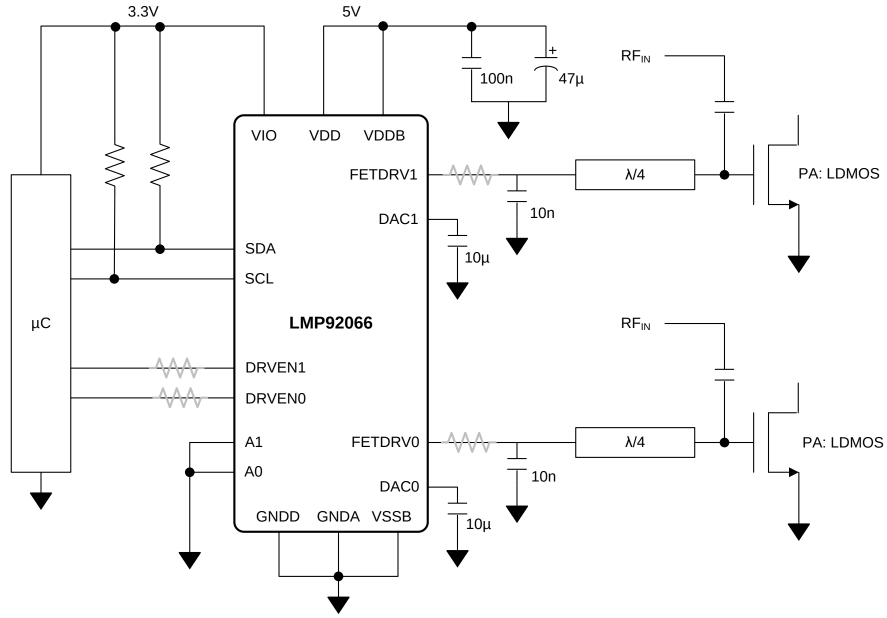


Figure 39. Temperature-Compensated Bias Generator for LDMOS Power Amplifier (PA)

9.2.1.1 Design Requirements

The thermal characteristic of a hypothetical LDMOS PA is plotted in Figure 40. This characteristic was obtained from the temperature sweep of the LDMOS gate-source voltage, V_{GS}, while keeping the drain current, I_D = 750 mA. The goal is to have the LMP92066 produce that same V_{GS} vs T characteristic which, when applied to the gate of the PA device ensures constant I_D throughout the operating temperature range.

In the following sections the curve V_{GS} vs T are referred to as the Target Function, V_{DAC} (T).

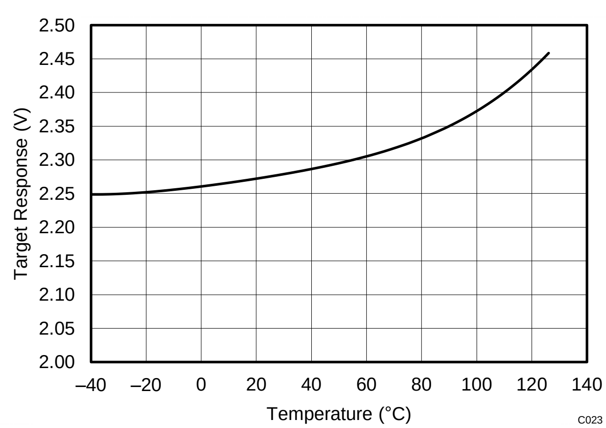


Figure 40. Target Function to be Reproduced by the LMP92066: V_{GS} vs T Characteristic of an LDMOS PA

The target function is approximated by the following polynomial (T unit is °C):

$$V_{DAC}(T) = 5.1 \times 10^{-10}(T)^4 - 2.63 \times 10^{-8}(T)^3 + 3.58 \times 10^{-6}(T)^2 + 5.14 \times 10^{-4}(T) + 2.26 \quad (7)$$

In the *Detailed Design Requirements* section the above expression is used to obtain the LUT coefficient values.

Typical Applications (continued)

9.2.1.2 Detailed Design Requirements

Figure 41 outlines the LUT design procedure. The procedure is for one channel only – repeat for the second available channel, as needed. In principle, the procedure follows the signal path backwards from the output, which is ideally the target function $V_{DAC}(T)$, back to the LUT coefficients, and each block's processing has to be "reversed". Additional comments for each design step are listed below Figure 41.

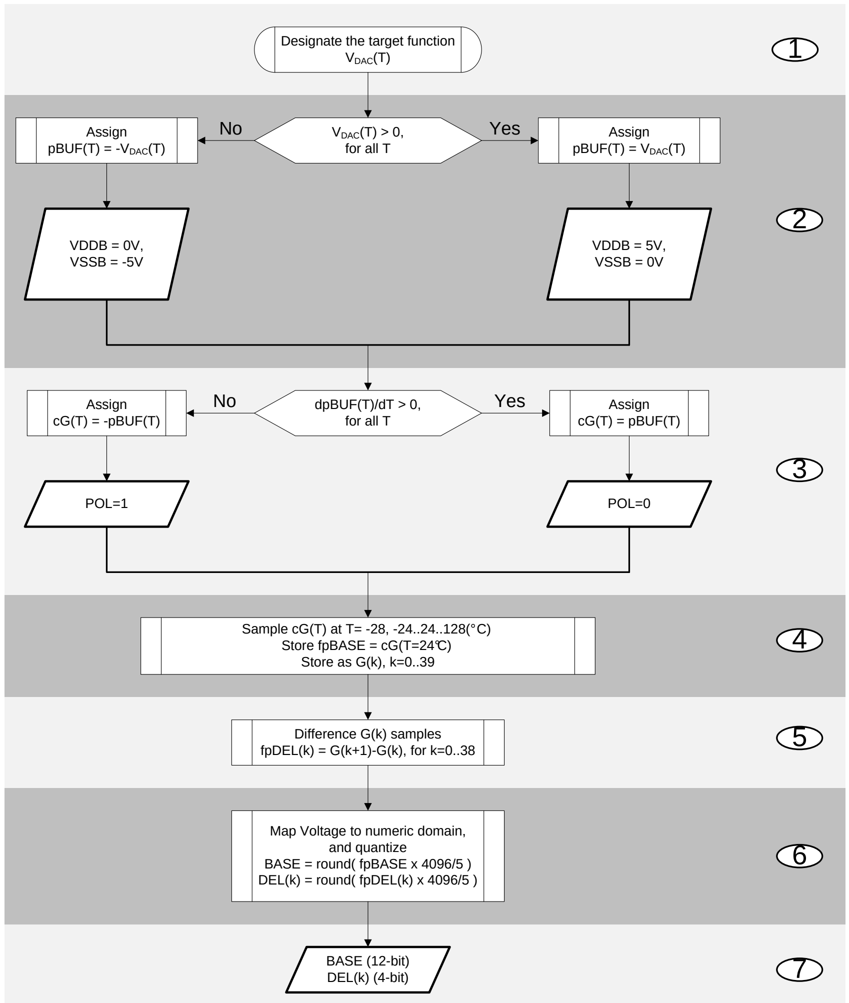


Figure 41. Flowchart of the Generalized LUT Design Procedure

1. Before attempting to calculate the LUT coefficients for the given target function $V_{DAC}(T)$, verify the requirements listed in the *Application Information* section are met.
2. Test if the function is wholly positive, or negative. If necessary "undo" the action of the Buffer Amplifier. (See the *Buffer Amplifier* section.) From now on consider the pre-buffer signal pBUFF(T). The design variable set in this step is the state of the VDDB and VSSB supplies. $V_{DAC}(T)$ is a strictly positive valued function, therefore:

$$VDDB = 5\ V$$
$$VSSB = GNDA$$
$$pBUFF(T) = V_{DAC}(T) \quad (8)$$

Typical Applications (continued)

3. Check the slope of the pBUF(T). Record the sign of the slope, and from here on consider a positive slope function cG(T). The design variable set in this step is the POL bit. pBUFF(T) is a monotonically increasing function, therefore:

$$\text{POL} = 0$$
$$\text{cG(T)} = \text{pBUFF(T)} \quad (9)$$

4. Discretize the continuous cG(T) along its temperature domain, thus creating the sequence G(k). Maintain the full precision of the G(k) values. Note the full precision cG(T) at T = 24°C — this is the full precision BASE value, fpBASE, still in voltage domain.

$$G(0) = cG(-28°C) = 2.2499$$
$$G(1) = cG(-24°C) = 2.2508$$
$$G(2) = cG(-20°C) = 2.2508$$
$$\downarrow$$
$$G(13) = cG(24°C) = 2.2747 = fpBASE$$
$$\downarrow$$
$$G(39) = cG(128°C) = 2.4667$$

5. Apply difference operation to the G(k) sequence, and obtain new sequence fpDEL(k). These are now the full precision increments of the target function with each 4°C interval.

$$fpDEL(0) = G(1) - G(0) = 0.9528 \times 10^{-3}$$
$$fpDEL(1) = G(2) - G(1) = 1.1846 \times 10^{-3}$$
$$fpDEL(2) = G(3) - G(2) = 1.3891 \times 10^{-3}$$
$$\downarrow$$
$$fpDEL(38) = G(39) - G(38) = 16.9789 \times 10^{-3}$$

6. Convert the full precision voltages of fpDEL(k) and fpBASE to a numeric, quantized domain. This reverses the DAC action.

$$BASE = round\left(\frac{fpBASE \times 4096}{5}\right) = 1863_{10} = 747_{16} = 011101000111_2$$
$$DEL(0) = round\left(\frac{fpDEL(0) \times 4096}{5}\right) = 1_{10} = 1_{16} = 0001_2$$
$$\downarrow$$
$$DEL(38) = round\left(\frac{fpDEL(38) \times 4096}{5}\right) = 14_{10} = E_{16} = 1110_2$$

7. Usually BYP bit is reset, BYP=0. However, in cases where it is desirable to bypass the LUT and ALU, and have the DACx output produce voltage equivalent of the BASE value, set BYP = 1.
8. Repeat steps 1 to 6 to obtain POL, BYP, BASE, DELx values for the second channel.
9. Now have BYP, POL, BASE, and DEL(0..38) values ready to be programmed into the LUT.

NOTE

The device has to be in the L2 Access Level before commencing the WRITE access of BYP, POL, BASE, DELx values. The register WRITE operation immediately affects the operation of the device. However, operating memory is volatile, and BURN operation is required to commit the LUT coefficients to non-volatile memory, EEPROM.

Typical Applications (continued)

9.2.1.3 Application Curves

The output of the LMP92066 due to the coefficients calculated in the above procedure is shown in Figure 42.

Figure 43 shows the absolute difference between the target function and the measured response of the LMP92066.

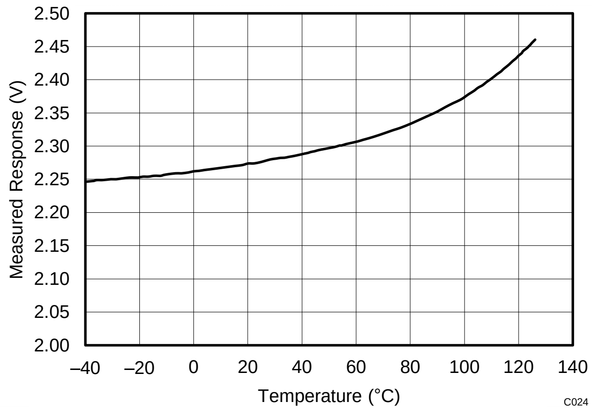


Figure 42. Measured Response of the LMP92066 Resulting from the LUT Coefficients (see *Detailed Design Requirements*)

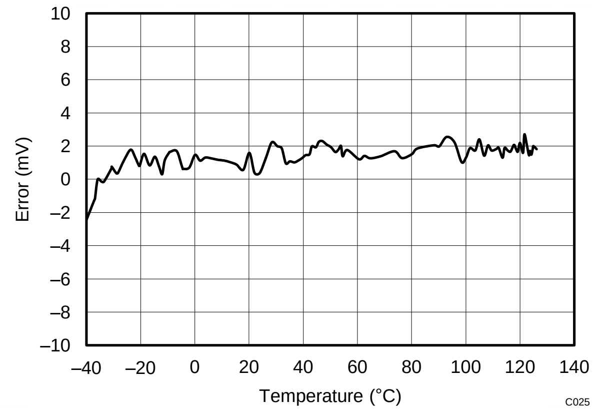


Figure 43. Difference Between the Target Response shown in Figure 40 and Measured Response in Figure 42

9.2.2 Temperature Compensated Bias Generator for GaN Power Amplifer (PA)

The typical application for the LMP92066 is the biasing of the power amplifiers in an RF system. What is required in such applications is for the PA drain current to stay constant over a wide range of operating temperatures. The LMP92066 senses the PA temperature and adjust the bias potential at the gate of PA in accordance with the known $V_{GS}(T)$, at I_D = constant, characteristic of the PA.

Typical Applications (continued)

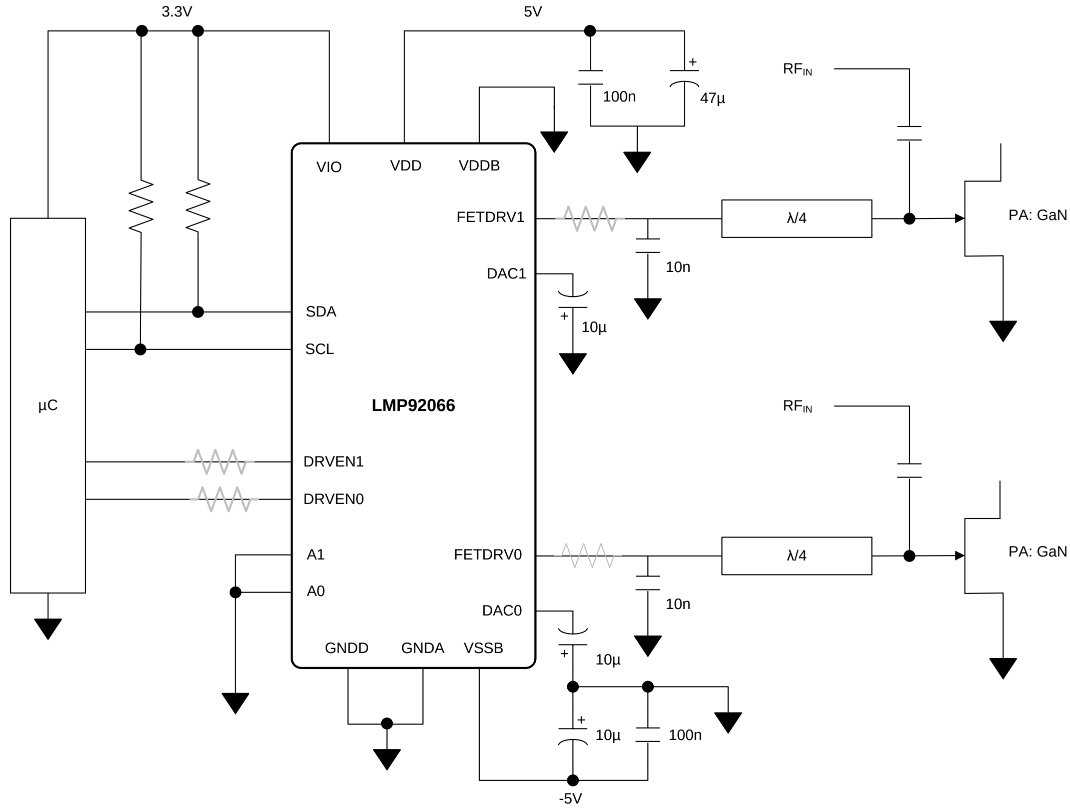


Figure 44. Temperature-Compensated Bias Generator for GaN Power Amplifier (PA)

9.2.2.1 Design Requirements

The thermal characteristic of a hypothetical GaN PA is plotted in Figure 45. This characteristic was obtained from the temperature sweep of the GaN gate-source voltage, V_{GS}, while keeping the drain current, I_D = 750 mA. The goal is to have the LMP92066 produce that same V_{GS} vs T characteristic which, when applied to the gate of the PA device ensures constant ID throughout the operating temperature range.

In the following sections the curve V_{GS} vs T is referred to as the Target Function, V_{DAC} (T).

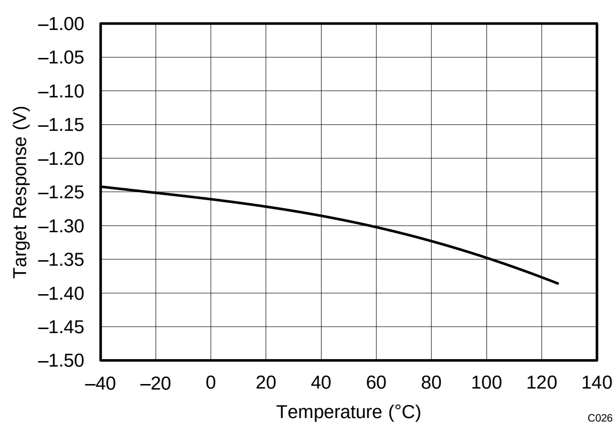


Figure 45. The Target Function to be Reproduced by the LMP92066: V_{GS} vs T Characteristic of an GaN PA

Typical Applications (continued)

The target function is approximated by the following polynomial (T unit is °C):

$$V_{DAC}(T) = 6.33 \times 10^{-11}(T)^4 - 2.34 \times 10^{-8}(T)^3 - 1.95 \times 10^{-6}(T)^2 - 5.04 \times 10^{-4}(T) - 1.26$$

9.2.2.2 Detailed Design Procedure

Figure 46 outlines the LUT design procedure. The procedure is for one channel only – repeat for the second available channel, as needed.

In principle, the procedure follows the signal path backwards from the output, which is ideally the target function $V_{DAC}(T)$, back to the LUT coefficients, reversing the processing of each block. Additional comments for each design step are listed below Figure 46.

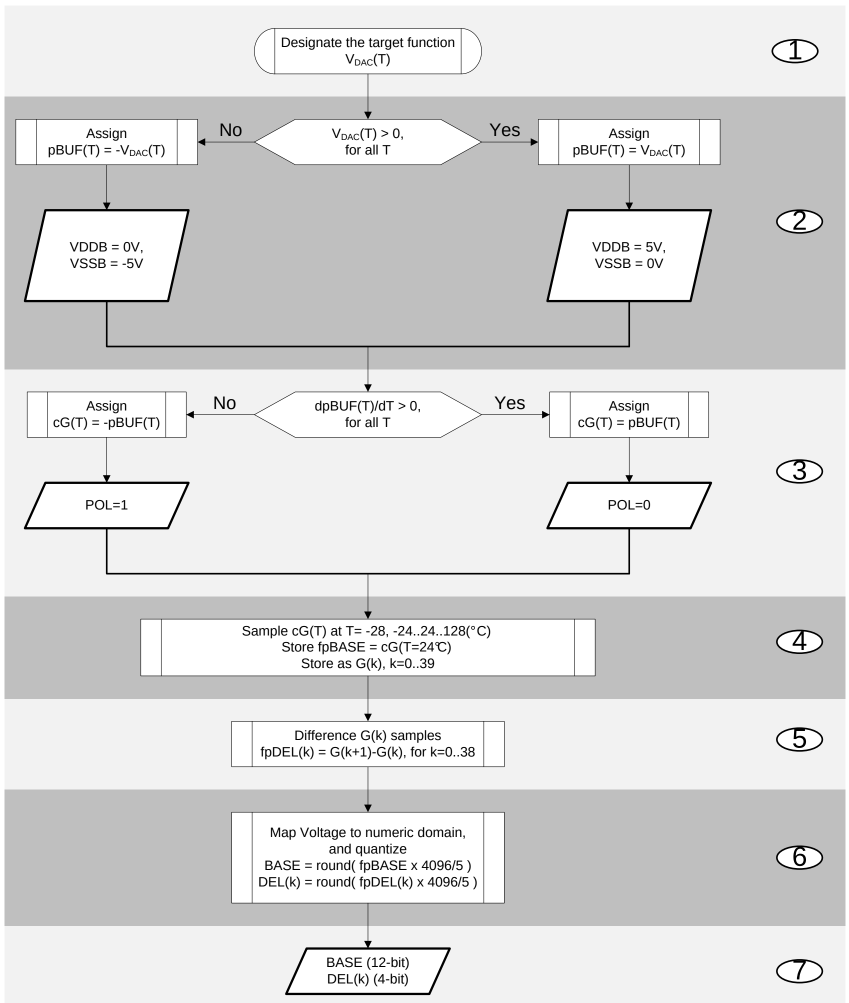


Figure 46. Flowchart of the Generalized LUT Design Procedure

1. Before attempting to calculate the LUT coefficients for the given target function $V_{DAC}(T)$, verify the requirements listed in the *Application Information* section are met.
2. Test if the function is wholly positive, or negative. If necessary "undo" the action of the Buffer Amplifier. (See the *Buffer Amplifier* section.) From now on consider the pre-buffer signal pBUFF(T). The design variable set in this step is the state of the VDDB, VSSB supplies. $V_{DAC}(T)$ is a strictly positive valued function, therefore:

Typical Applications (continued)

$$VDDB = GNDA$$
$$VSSB = -5\ V$$
$$pBUFF(T) = -V_{DAC}(T) \tag{10}$$

3. Check the slope of the pBUF(T). Record the sign of the slope, and from here on consider a positive slope function cG(T). The design variable set in this step is the POL bit. pBUFF(T) is a monotonically increasing function, therefore:

$$POL = 0$$
$$cG(T) = pBUFF(T) \tag{11}$$

4. Discretize the continuous cG(T) along its temperature domain, thus creating the sequence G(k). Maintain the full precision of the G(k) values. Note the full precision cG(T) at T = 24°C — this is the full precision BASE value, fpBASE, still in voltage domain.

$$G(0) = cG(-28°C) = 1.2477$$
$$G(1) = cG(-24°C) = 1.2495$$
$$G(2) = cG(-20°C) = 1.2513$$
$$\downarrow$$
$$G(13) = cG(24°C) = 1.2743 = fpBASE$$
$$\downarrow$$
$$G(39) = cG(128°C) = 1.3893 \tag{12}$$

5. Apply difference operation to the G(k) sequence, and obtain new sequence fpDEL(k). These are now the full precision increments of the target function with each 4°C interval.

$$fpDEL(0) = G(1) - G(0) = 1.8174 \times 10^{-3}$$
$$fpDEL(1) = G(2) - G(1) = 1.8189 \times 10^{-3}$$
$$fpDEL(2) = G(3) - G(2) = 1.8316 \times 10^{-3}$$
$$\downarrow$$
$$fpDEL(38) = G(39) - G(38) = 6.4124 \times 10^{-3}$$

6. Convert the full precision voltages of fpDEL(k) and fpBASE to a numeric, quantized domain. This reverses the DAC action.

$$BASE = round\left(\frac{fpBASE \times 4096}{5}\right) = 1044_{10} = 414_{16} = 010000010100_2$$
$$\downarrow$$
$$DEL(0) = round\left(\frac{fpDEL(0) \times 4096}{5}\right) = 1_{10} = 1_{16} = 0001_2$$
$$\downarrow$$
$$DEL(38) = round\left(\frac{fpDEL(38) \times 4096}{5}\right) = 5_{10} = 5_{16} = 0101_2$$

7. Usually BYP bit is reset, BYP=0. However, in cases where it is desirable to bypass the LUT and ALU, and have the DACx output produce voltage equivalent of the BASE value, set BYP = 1.
8. Repeat steps 1 to 6 to obtain POL, BYP, BASE, DELx values for the second channel.
9. Now have BYP, POL, BASE, and DEL(0..38) values ready to be programmed into the LUT.

Typical Applications (continued)

NOTE

The device has to be in the L2 Access Level before commencing the WRITE access of BYP, POL, BASE, DELx values. The register WRITE operation immediately affects the operation of the device. However, operating memory is volatile, and BURN operation is required to commit the LUT coefficients to non-volatile memory, EEPROM.

9.2.2.3 Application Curves

The output of the LMP92066 due to the coefficients calculated in the above procedure is shown in Figure 47.

Figure 48 shows the absolute difference between the target function and the measured response of the LMP92066.

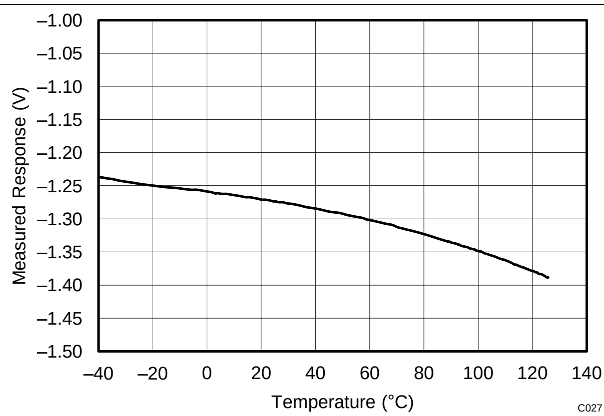


Figure 47. Measured Response of the LMP92066 Resulting from the LUT Coefficients (see *Detailed Design Procedure*)

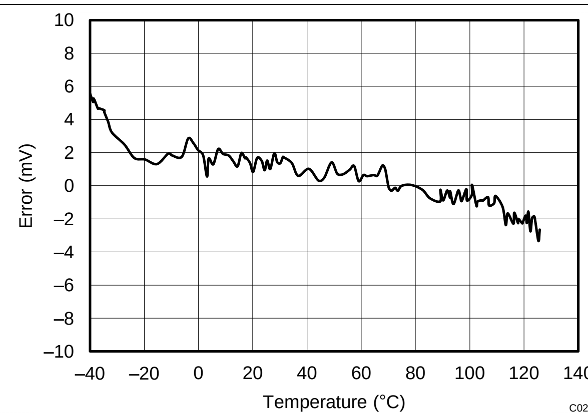


Figure 48. Difference Between the Target Response shown in Figure 45 and Measured Response in Figure 47

9.3 Do's and Don'ts

9.3.1 Output Drive Switching

Some applications may require that the FETDRVx output reaches the level set by the DACx as fast as possible after the assertion of DRVENx.

There are parameters which determine the delay between the assertion of DRVENx, and the FETDRVx output achieving its final level as set by the DACx:

- The delay between the DRVENx input the output switch.
- The charge up time of the FETDRVx node once the output switch is closed.

The delay of the switch response to the DRVENx input, t_{ON}, is specified in the *Electrical Characteristics* table.

The charge up time of the FETDRVx node is dependent on the selection of the external components. Rapid rise time of the FETDRVx output, is made possible through the use of the external capacitor C1. C1 is always charged to the potential generated by the DACx, and used to provide instantaneous charge to the load present at the FETDRVx when the output switch closes – the switch between DACx and FETDRVx pin.

C1 is chosen to be several orders of magnitude larger than the total capacitance present at the FETDRVx pin, CEXT. In the typical application C1 is 10 µF, and CEXT is limited to 10 nF. See Figure 49. When the output switch closes, a current flows from the C1, acting as a reservoir, to CEXT. This charge-up current is limited only by the resistance of the output switch RDRV, resulting in very rapid slewing at the FETDRVx pin. RDRV is specified in the *Electrical Characteristics* table.

For example, given the following parameters.

- t_{ON} = 50 ns

Do's and Don'ts (continued)

- R_{DRV} = 5 Ω
- C_{EXT} = 10 nF

The total delay time between activation of DRVENx and FETDRVx achieving 95% of its final value is:

$$T_{DELAY} = t_{ON} + 5\tau = t_{ON} + 5R_{DRV}C_{EXT} = 300\text{ ns} \quad (13)$$

NOTE

The charge current flowing into the C_{EXT} at the instant the output switch closes is relatively large and of very short duration, which makes the parasitic inductance in the charge path significant. This parasitic inductance is due to the bond wire and package pin between the device die and the C_{EXT}, and is shown as LP in Figure 49. In some applications it may be beneficial to insert a small resistance in the charge path, see R_{EXT} in Figure 49, to dampen the resonance of the LP and C_{EXT}. Choice of R_{EXT} is highly application dependent, but 5 Ω is a good initial selection.

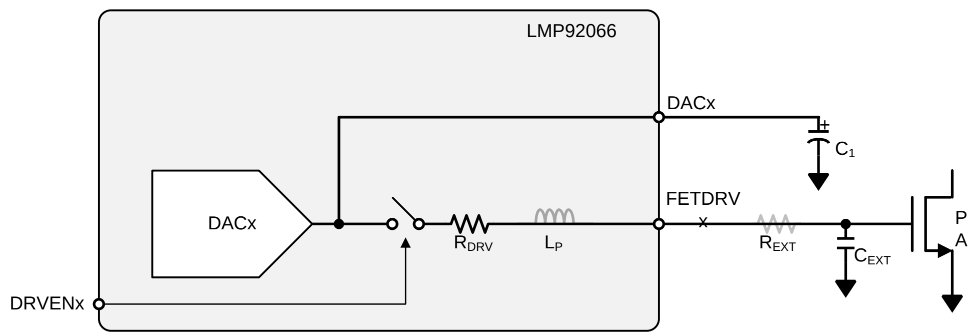


Figure 49. Flow of Charge Current

9.4 Initialization Setup

9.4.1 Factory Default

At the factory the EEPROM is initialized such that all LUT increment values (Δ) are set to 0, BASE value is set to 0x00, and BYP and POL bits are set to 0. This results in the device producing constant output of 0V at DACx pins upon power up, regardless of the temperature or mode or state at the DRVENx inputs.

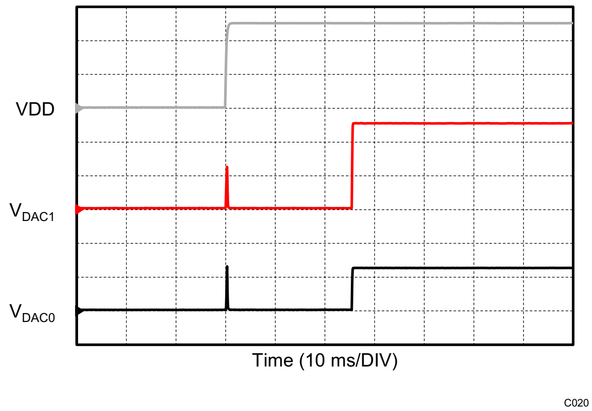
9.4.2 At Power Up

The device is capable of autonomous operation upon power up, without intervention form the system controller. When the power is applied and reaches the minimum level (approximately 4.1 V) the temperature sensor begins operating, and the internal sequencer begins the transfer of LUT values from the EEPROM to the operating memory. Once the transfer is complete, and the Temperature Sensor has completed the first conversion, the ALU computes the DACs input values, and the DACs start producing output voltages representative of the transfer functions implemented in the LUTs.

The control signal applied to the DRVENx input determines whether the DAC output voltage is present at the FETDRVx output, or that output is driven to VSSB potential.

Figure 50 shows the typical power-up transient behavior at the DACx outputs. While VDD voltage is ramping up from 0 to 5 V the DACx outputs initially follow the VDD. This is due to the fact that initially the device is in the undefined state. When VDD reaches 4.1 V the internal reset occurs and clears the internal data path, resulting in V_{DACx} = 0 V. The Temperature Sensor begins operation at the moment of reset, and 25 ms later produces its first temperature measurement. This, in turn, causes the ALU to update DAC input data, resulting in new V_{DACx} output.

Initialization Setup (continued)



VDD = 2V/div V_{DAC1} = 1V/div V_{DAC0} = 1V/div

Figure 50. Power-Up Transient Behavior

See also the *Default Operating Mode* section.

10 Power Supply Recommendations

The device rails VIO, VDD, and VDDB (VSSB in GaN mode) should be supplied from a well-regulated power supply capable of sourcing at least 50 mA. The required supply levels are shown in the *Specifications* tables of this document. Along with ceramic bypass capacitors, additional bulk capacitance is recommended on the VDD node. The function of this bulk capacitance is to provide the momentary increases in the supply current requirements due to the EEPROM activity. An electrolytic capacitor with a value of 10 µF to 47 µF is a typical choice.

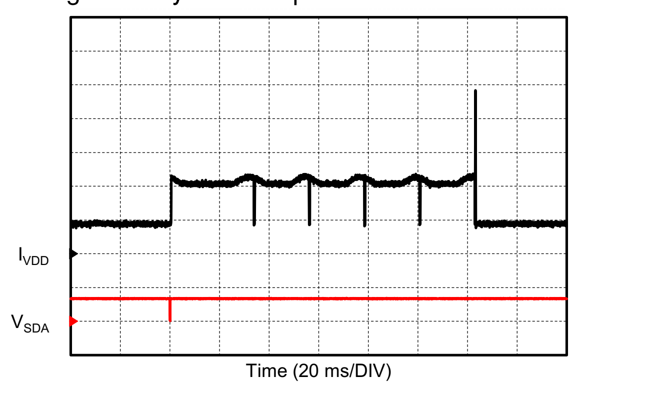
10.1 VDD Supply Sourcing

The power supply powering the VDD pin must be capable of sourcing a minimum of 50mA. This is required in order to avoid the continuous activation of the LMP92066's power-on-reset (POR) circuit. When the VDD supply rail passes through the POR voltage of approximately 4.2V (either rising or falling edge), an increase in supply current occurs. If the power supply is not capable of sourcing the 50mA that is required under worst case conditions, the voltage supplied to VDD will not increase beyond the POR voltage level and the LMP92066's POR circuitry remains active and continues to draw excess current. This excess current draw is approximately 20mA under nominal conditions.

Since the LMP92066's POR circuitry also responds to the discharge (falling edge) of the supply line, an increase in supply current occurs when the VDD supply is turned off as well. Similar to the condition described above, if the VDD supply is not capable of sourcing a minimum of 50mA, an increase in VDD supply current can be experienced if the VDD supply is immediately ramped back up after being discharged. Under this circumstance, the increase in VDD supply current will persist until the voltage surpasses 4.2V. This is a result of the POR circuitry never turning off. The POR circuit will only turn off once the VDD supply has passed through the POR voltage level of 4.2V.

10.2 I_{VDD} During EEPROM BURN

Figure 51 shows the transient behavior of I_{VDD} due to the EEPROM BURN operation. VSDA trace activity is used as the trigger. The triggering event is the BURN command sent via the I^2C interface. During the BURN the I_{VDD} increases to almost 4 mA for 125 ms. The 10-mA peaking in I_{VDD} is due to the TRANSFER of newly stored data from EEPROM back to the operating memory – this is part of the internal error detection and correction process.



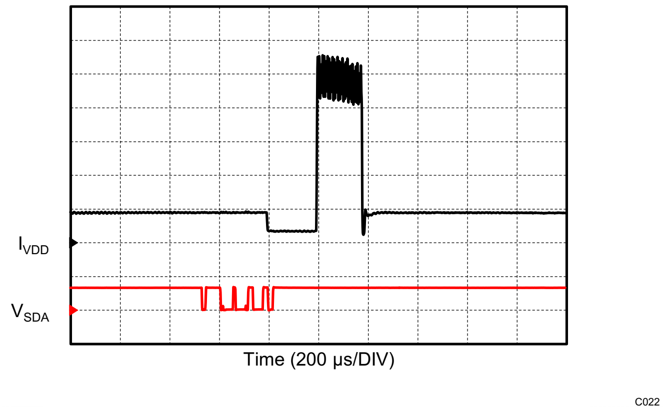
I_{VDD} = 2mA/div V_{SDA} = 5V/div

Figure 51. I_{VDD} Transient During EEPROM BURN

10.3 I_{VDD} During EEPROM TRANSFER

The transfer of data, from the EEPROM to the operating memory, results in the temporary increase in supply current I_{VDD}. The total I_{VDD} increases to about 10 mA for the duration of the TRANFER operation, typically 200 µs. Given the infrequent occurrence, and the short duration, the increased I_{VDD} can be easily supplied by the external bulk capacitors; that is, this does not represent an additional burden to the system power supply. The typical I_{VDD} transient during TRANSFER is shown in Figure 52. The triggering event is the TRANSFER command issued via the I^2C interface.

I_{VDD} During EEPROM TRANSFER (continued)



I_{VDD} = 2mA/div V_{SDA} = 5V/div

Figure 52. I_{VDD} Transient During EEPROM Transfer

The TRANSFER operation occurs due to the following:

1. Power-On RESET
2. Software RESET
3. EEPROM TRANSFER command issued via the I^2C interface
4. Upon completion of the EEPROM BURN operation, as a data verification step.

11 Layout

11.1 Layout Guidelines

The LMP92066 is a device for which the input signal is temperature. The primary path of heat conduction is through the exposed PowerPAD on the underside of the package. The layout should provide direct, high thermal conductivity path between the LMP92066 and the devices controlled by its output:

- Use heavy copper layer as the thermal conduction path. This layer must be also a GND node.
- If the heavy copper layer is not a top layer, use a dense array of vias to connect to both the LMP92066 and the heat sources to maintain high thermal conductivity.
- Place the LMP92066 in the geometric center between the multiple heat sources in order to minimize the “thermal offsets” due to the temperature gradients.

11.2 Layout Example

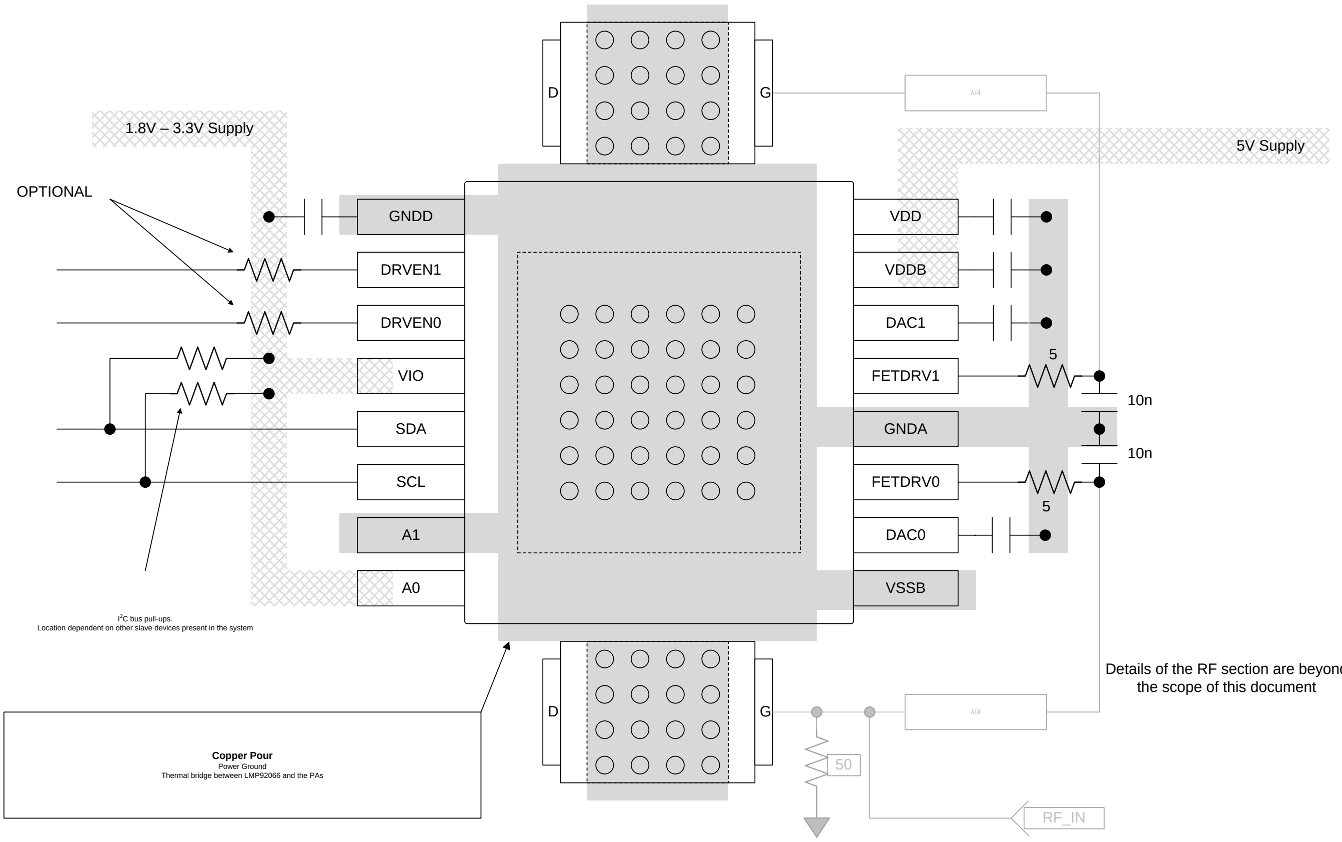


Figure 53. LMP92066 Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

REAOPC Residual Error After One Point Calibration is the error acquired in the Analog Signal Path due to the inaccuracies of the constituent signal processing blocks: DAC, Buffer Amplifier, internal Reference. REAOPC is dominated by the Offset and Gain temperature drifts, since the significant portion of the initial error is eliminated through the One Point Calibration process. The small contribution from the DAC linearity error (INL) is omitted, since it is numerically insignificant. REAOPC can be predicted through the following formulation:

$$REAOPC(T) = A[x(T) - x(T_O)]GE(T) + A[GE(T) - GE(T_O)]x(T_O) + \Delta$$

$$A = \frac{5}{4096}\ (V)$$

$$GE(T) = \text{Gain Error at temperature } T$$

$$\Delta = OE(T) - OE(T_O)$$

$$OE(T) = \text{Offset error at temperature } T$$

$$x(T) = \text{DAC input code at temperature } T$$

$$T_O = \text{temperature at which One Point Calibration is performed}$$

One Point Calibration One Point Calibration is the process where the output of the LMP92066 is adjusted in the target system to achieve the desired response, at temperature T_0. Typically this involves measurement of the overall system output variable; for example, I_D of the PA, and modification of the BASE value in the LUT to achieve the desired PA bias current.

12.2 Trademarks

PowerPAD is a trademark of Texas Instruments Incorporated.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated device(s). This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP92066PWP	ACTIVE	HTSSOP	PWP	16	92	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	LMP920 66PWP	Samples
LMP92066PWPR	ACTIVE	HTSSOP	PWP	16	2500	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	LMP920 66PWP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

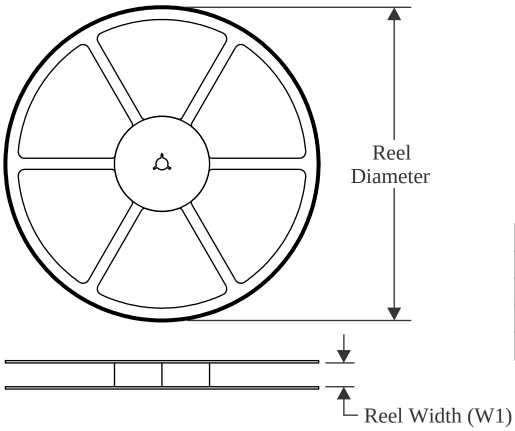
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

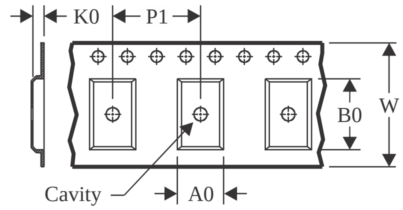
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

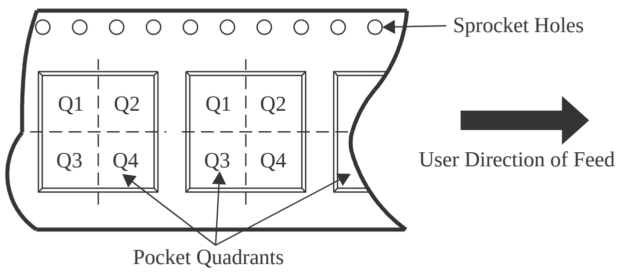


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

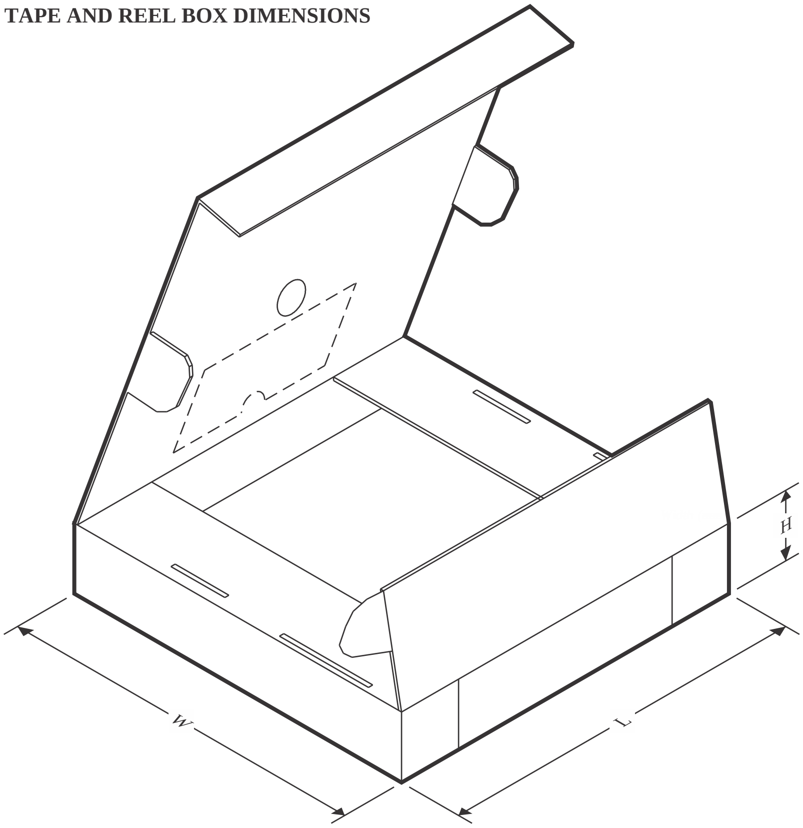
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP92066PWPR	HTSSOP	PWP	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

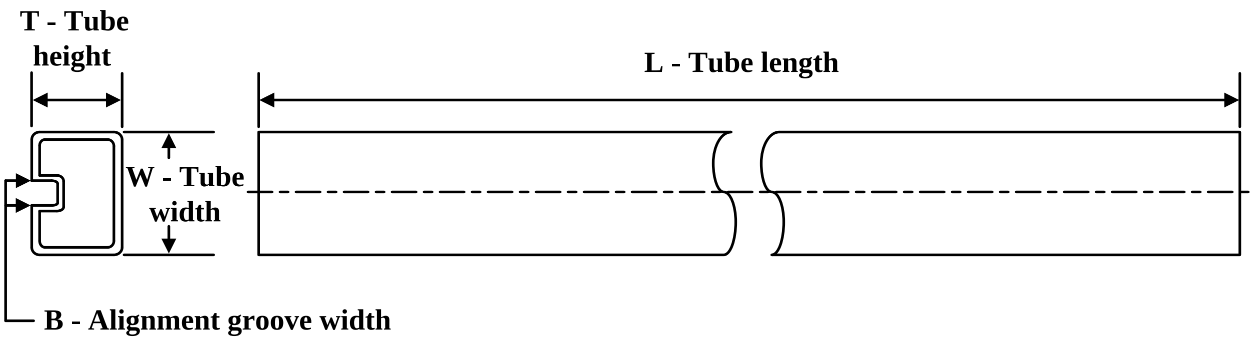
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

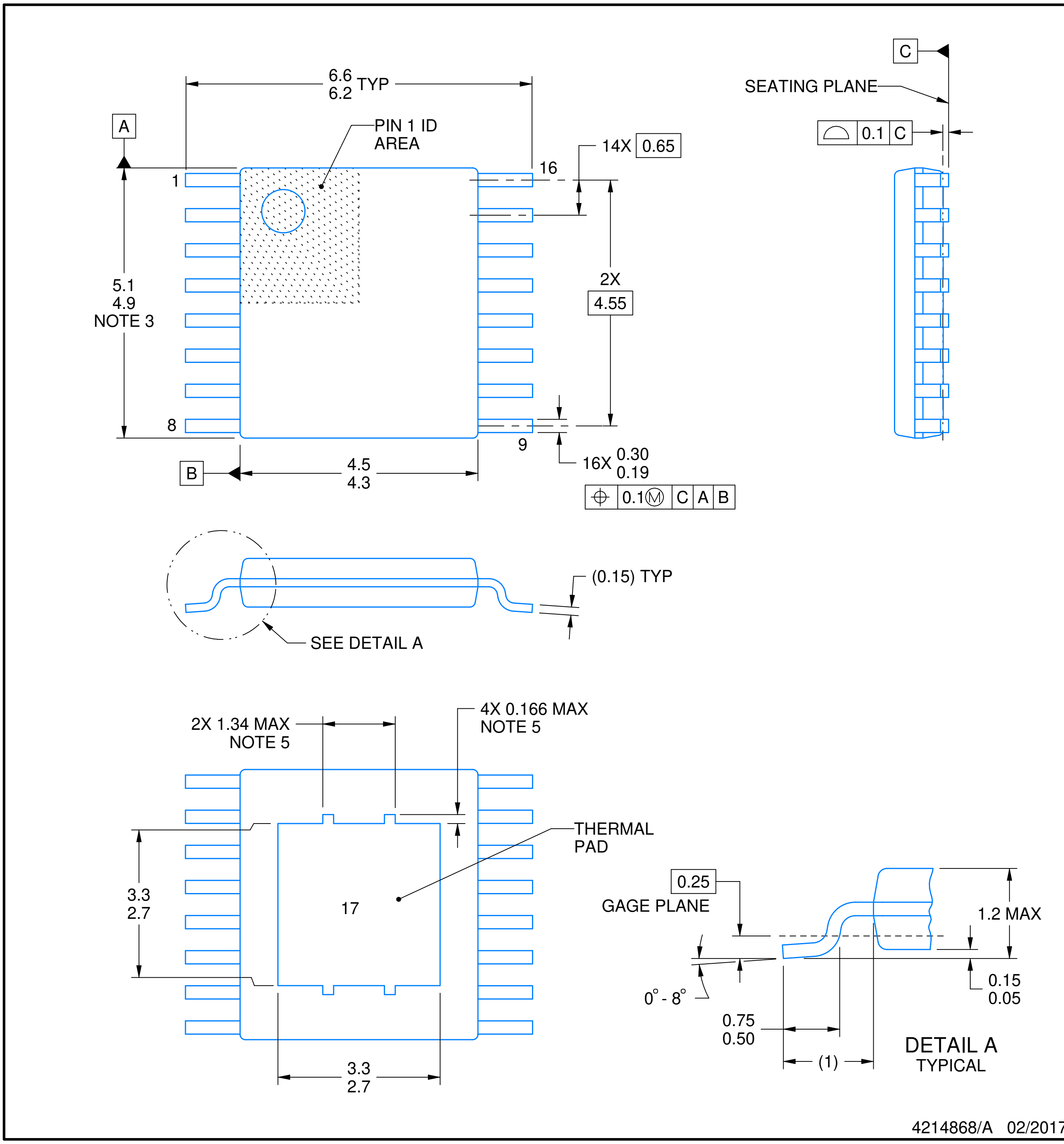
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP92066PWPR	HTSSOP	PWP	16	2500	356.0	356.0	35.0

TUBE



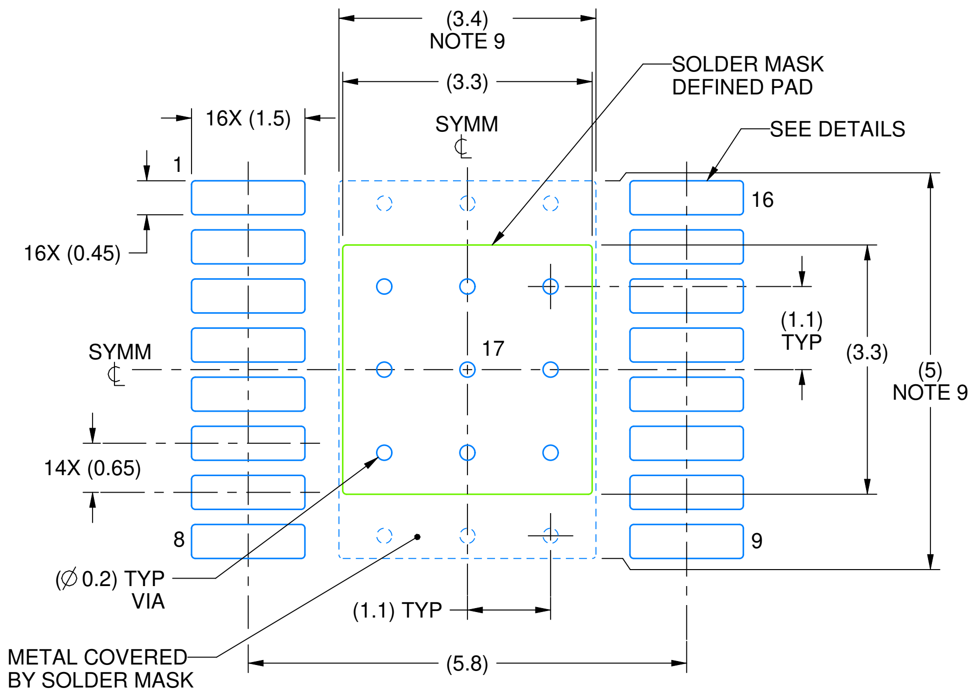
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMP92066PWP	PWP	HTSSOP	16	92	495	8	2514.6	4.06

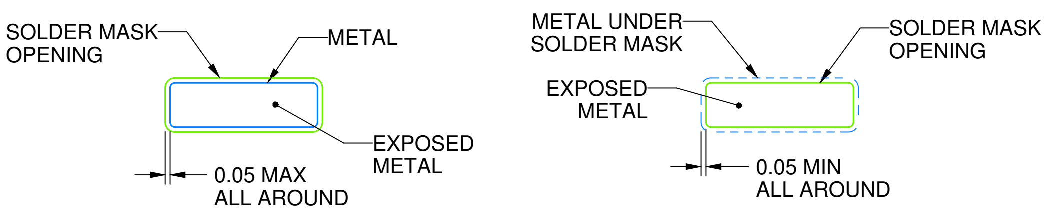


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
PADS 1-16

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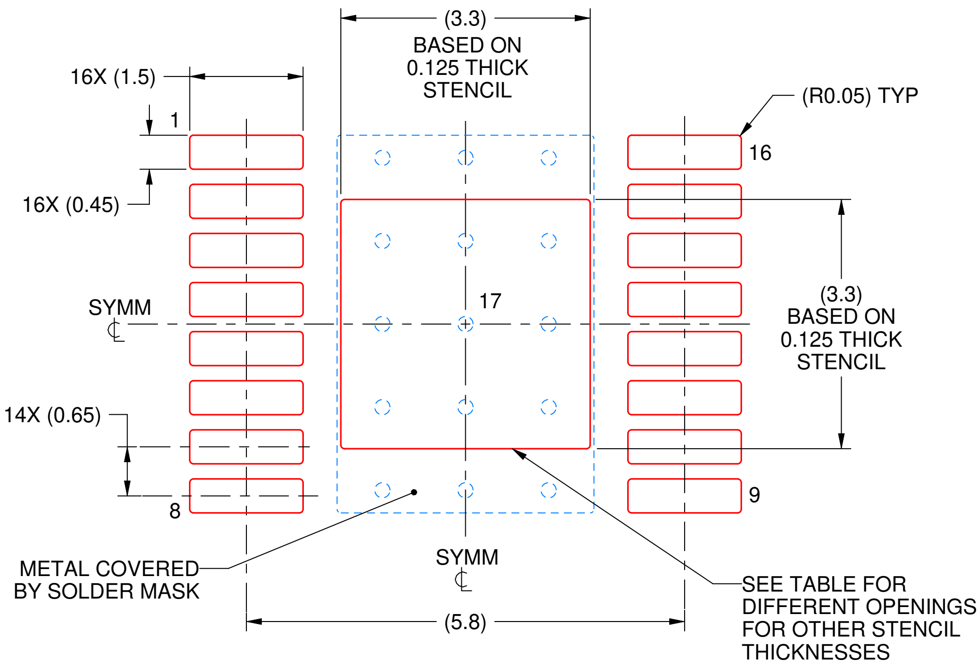
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.69 X 3.69
0.125	3.3 X 3.3 (SHOWN)
0.15	3.01 X 3.01
0.175	2.79 X 2.79

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.