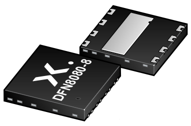

GAN080-650EBE

650 V, 80 mOhm Gallium Nitride (GaN) FET in a DFN 8 mm x 8 mm package

5 May 2023 Product data sheet

1. General description

The GAN080-650EBE is a general purpose 650 V, 80 mΩ Gallium Nitride (GaN) FET in a DFN 8 mm x 8 mm surface mount package. It is a normally-off e-mode device offering superior performance.

2. Features and benefits

- Enhancement mode - normally-off power switch
- Ultra high frequency switching capability
- No body diode
- Low gate charge, low output charge
- Qualified for standard applications
- ESD protection
- RoHS, Pb-free, REACH-compliant
- High efficiency and high power density
- Low package inductance and low package resistance

3. Applications

- High power density and high efficiency power conversion
- AC-to-DC converters, totem pole PFC
- DC-to-DC converters
- Fast battery charging, mobile phone, laptop, tablet and USB type-C chargers
- Datacom and telecom (AC-to-DC and DC-to-DC) converters
- Motor drives
- Solar (PV) inverters
- Class D audio amplifiers, TV PSU and LED drivers

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	-	650	V
V_{TDS}	transient drain to source voltage	pulsed; t_p = 1 µs; δ_{factor} = 0.01		-	-	800	V
I_D	drain current	V_{GS} = 6 V; T_{mb} = 25 °C	[1]	-	-	29	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	240	W
T_j	junction temperature			-55	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 6 V; I_D = 8 A; T_j = 25 °C; Fig. 11; Fig. 12; Fig. 13		-	60	80	mΩ
		V_{GS} = 6 V; I_D = 8 A; T_j = 150 °C; Fig. 11; Fig. 14		-	135	-	mΩ

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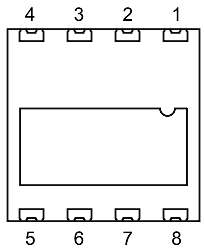
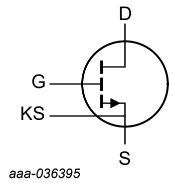
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_G	gate resistance	f = 5 MHz; T_j = 25 °C; open drain		-	3	-	Ω
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 8 A; V_{DS} = 400 V; V_{GS} = 6 V; T_j = 25 °C; Fig. 15; Fig. 16		-	2.2	-	nC
$Q_{G(tot)}$	total gate charge			-	6.2	-	nC
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 400 V; T_j = 25 °C	[2]	-	60	-	nC

[1] Limited by device saturation

[2] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since $Q_r = Q_{oss} + Q_D$, and Q_D = 0. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 Transparent top view **DFN8080-8 (SOT8074-1)**	
2	D	drain		
3	D	drain		
4	D	drain		
5	S	source		
6	S	source		
7	KS	kelvin source		
8	G	gate		
mb	S	mounting base; connected to source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
GAN080-650EBE	DFN8080-8	plastic thermal enhanced small outline package; no leads; 8 terminals; body: 8 x 8 x 0.9 mm	SOT8074-1

7. Marking

Table 4. Marking codes

Type number	Marking code
GAN080-650EBE	`080IEBE`

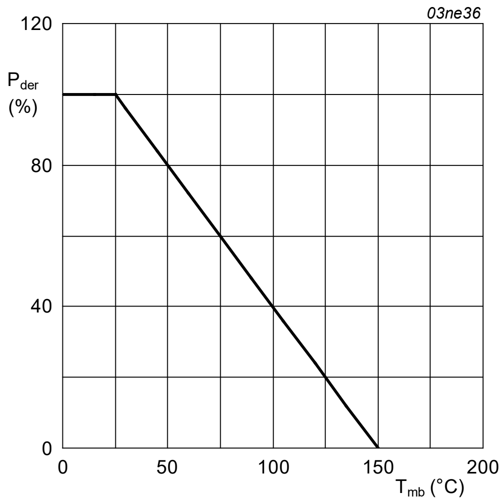
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).Tj = 25 °C unless otherwise stated.

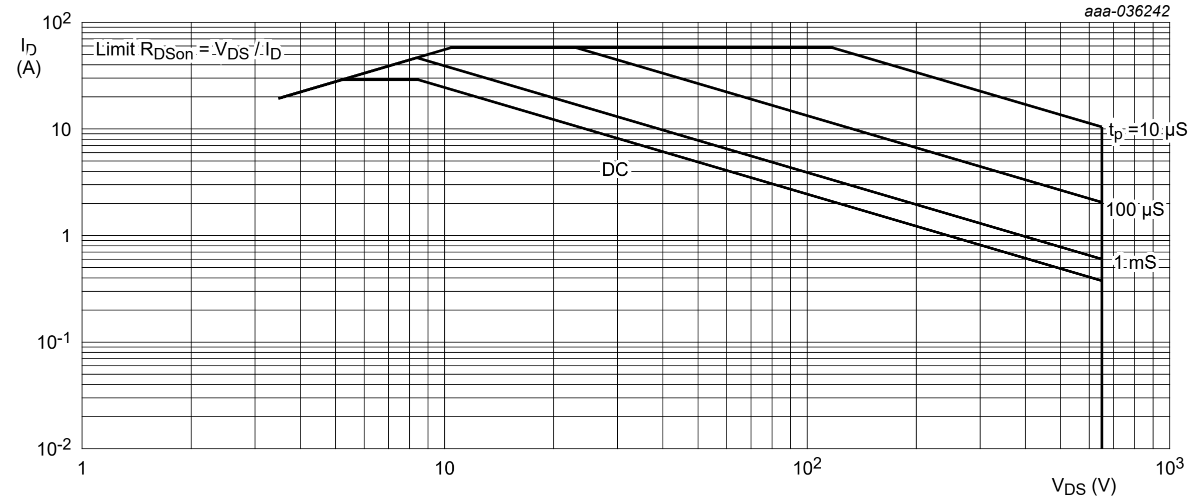
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	-55 °C ≤ T_j ≤ 150 °C		-	650	V
V_{TDS}	transient drain to source voltage	pulsed; t_p = 1 µs; δ_{factor} = 0.01		-	800	V
V_{GS}	gate-source voltage			-6	7	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	240	W
I_D	drain current	V_{GS} = 6 V; T_{mb} = 25 °C	[1]	-	29	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 2	[1]	-	58	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C

[1] Limited by device saturation



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	Fig. 3		-	-	0.52	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient			-	-	33.6	K/W

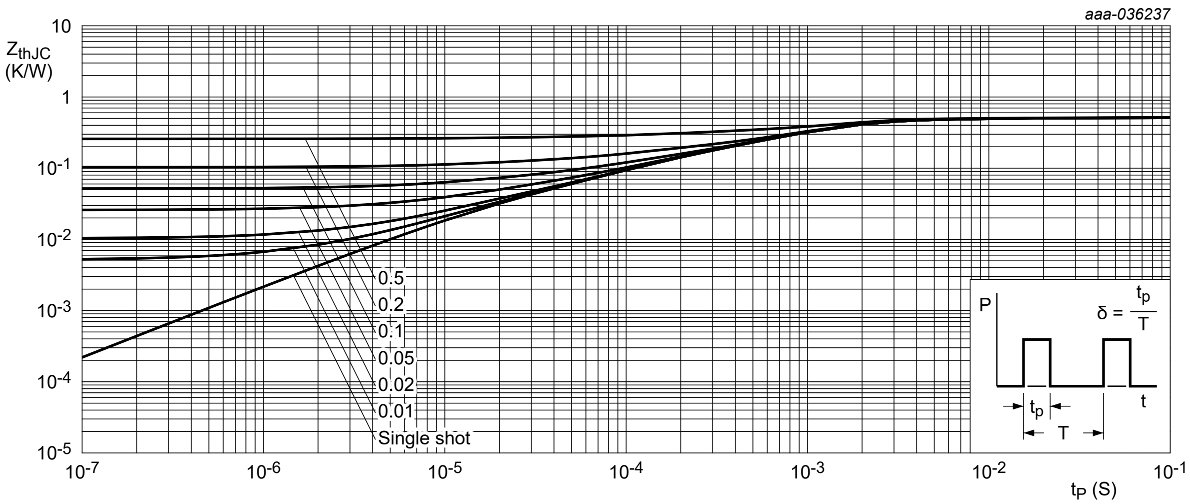


Fig. 3. Transient thermal impedance from junction to case as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{GS(th)}$	gate-source threshold voltage	I_D = 30.7 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 8		1.2	1.7	2.5	V
		I_D = 30.7 mA; V_{DS} = V_{GS}; T_j = 150 °C; Fig. 8		-	1.6	-	V
I_{DSS}	drain leakage current	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C; Fig. 9		-	1	65	µA
		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C; Fig. 9		-	13	390	µA
I_{GSS}	gate leakage current	V_{GS} = 6 V; V_{DS} = 0 V; T_j = 25 °C; Fig. 10		-	163	-	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = 6 V; I_D = 8 A; T_j = 25 °C; Fig. 11; Fig. 12; Fig. 13		-	60	80	mΩ
		V_{GS} = 6 V; I_D = 8 A; T_j = 150 °C; Fig. 11; Fig. 14		-	135	-	mΩ
R_G	gate resistance	f = 5 MHz; T_j = 25 °C; open drain		-	3	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 8 A; V_{DS} = 400 V; V_{GS} = 6 V; T_j = 25 °C; Fig. 15; Fig. 16		-	6.2	-	nC
Q_{GS}	gate-source charge			-	0.5	-	nC
Q_{GD}	gate-drain charge			-	2.2	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 8 A; V_{DS} = 400 V; T_j = 25 °C; Fig. 15		-	2.2	-	V
C_{iss}	input capacitance	V_{DS} = 400 V; V_{GS} = 0 V; f = 100 kHz; T_j = 25 °C; Fig. 17		-	225	-	pF
C_{oss}	output capacitance			-	70	-	pF
C_{rss}	reverse transfer capacitance			-	0.5	-	pF
$C_{o(er)}$	effective output capacitance, energy related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C; Fig. 18	[1]	-	105	-	pF
$C_{o(tr)}$	effective output capacitance, time related	0 V ≤ V_{DS} ≤ 400 V; V_{GS} = 0 V; T_j = 25 °C	[2]	-	150	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 400 V; V_{GS} = 6 V; T_j = 25 °C; I_D = 16 A; L = 318 µH; R_{on} = 10 Ω; R_{off} = 2 Ω; Fig. 19; Fig. 20		-	3	-	ns
t_r	rise time			-	4	-	ns
$t_{d(off)}$	turn-off delay time			-	5	-	ns
t_f	fall time			-	4	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 400 V; T_j = 25 °C	[3]	-	60	-	nC
Source-drain characteristics							
V_{SD}	source-drain voltage	I_S = 8 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 21; Fig. 22; Fig. 23; Fig. 24		-	2.3	-	V

[1] $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V
[2] $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V
[3] Q_r is not specified separately from Q_{oss} for e-mode GaN FETs, since Q_r = Q_{oss} + Q_D, and Q_D = 0. (Q_D is charge associated with diffusion of minority carriers. Since there is no body diode, no minority carriers in excess of Q_{oss} have to be transferred for e-mode GaN FETs.)

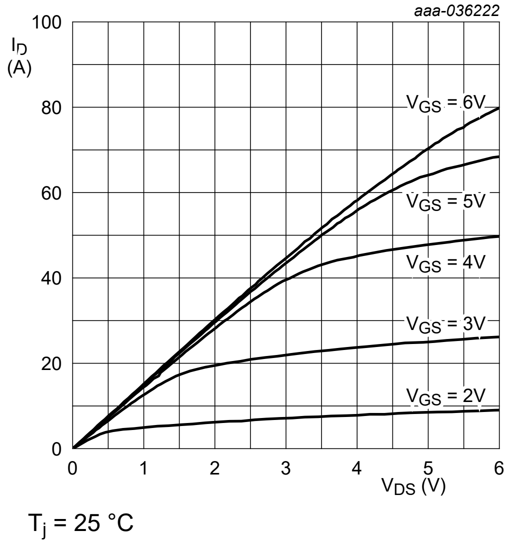


Fig. 4. Output characteristics: drain current as a function of drain-source voltage; typical values

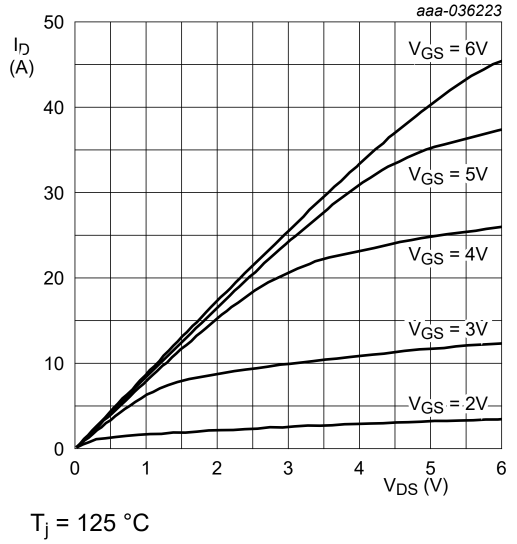


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

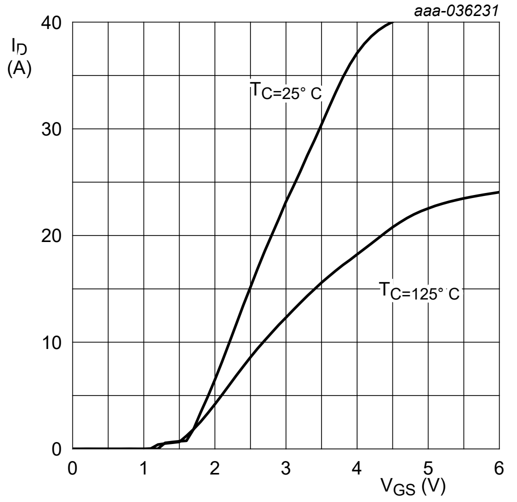


Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values

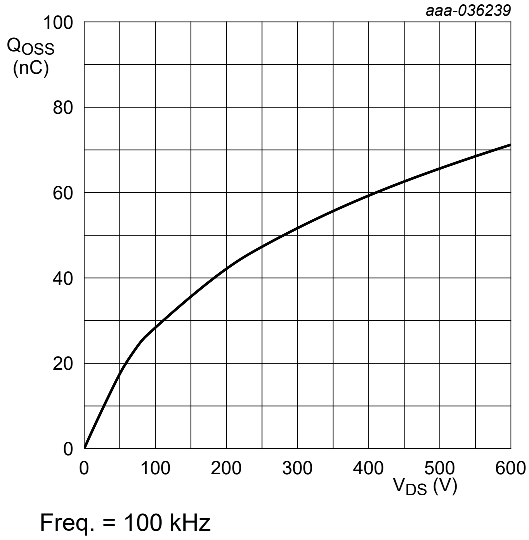
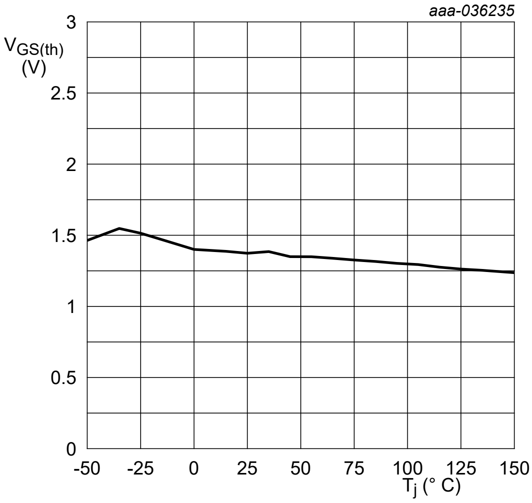
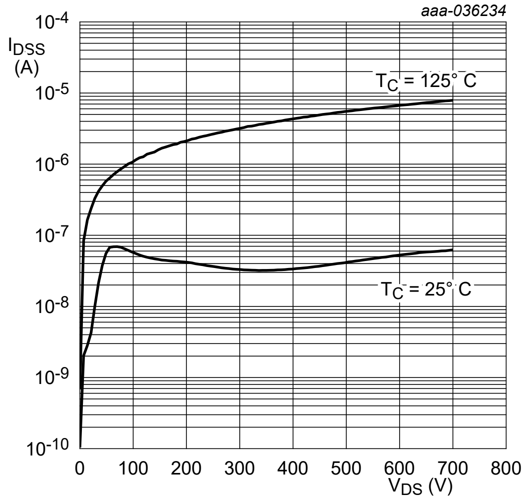


Fig. 7. Output charge as a function of drain-source voltage; typical values



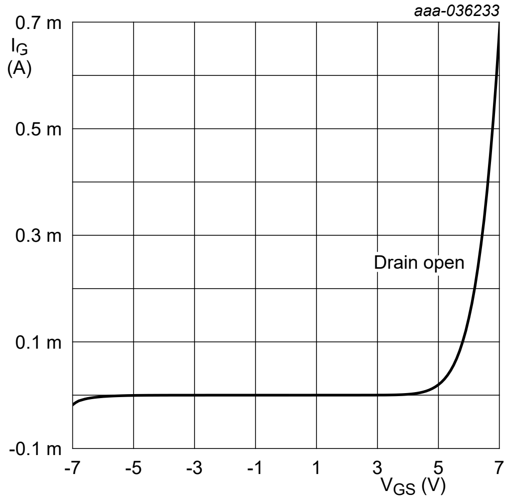
$V_{GS} = V_{DS}$; I_D = 30.7 mA

Fig. 8. Gate-source threshold voltage as a function of junction temperature



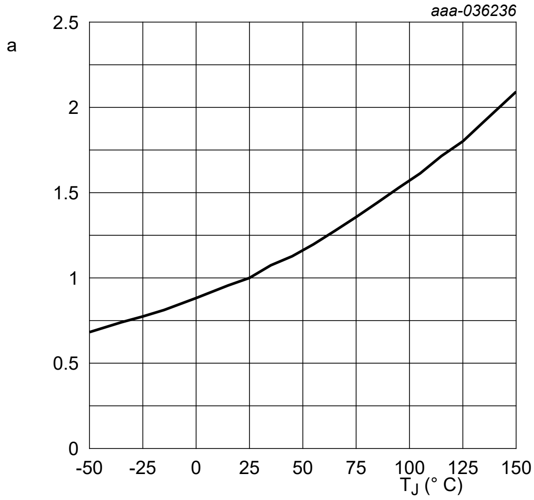
V_{GS} = 0 V

Fig. 9. Drain-source current as a function of drain-source voltage; typical values



Ig reverse turn on by ESD unit

Fig. 10. Gate-source current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

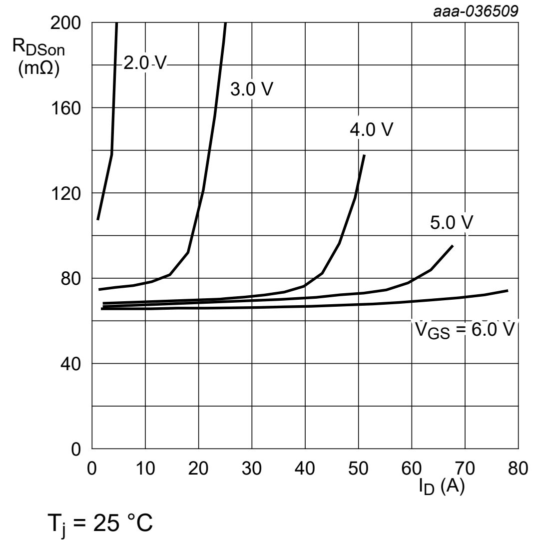


Fig. 12. Drain-source on-state resistance as a function of drain current ; typical values

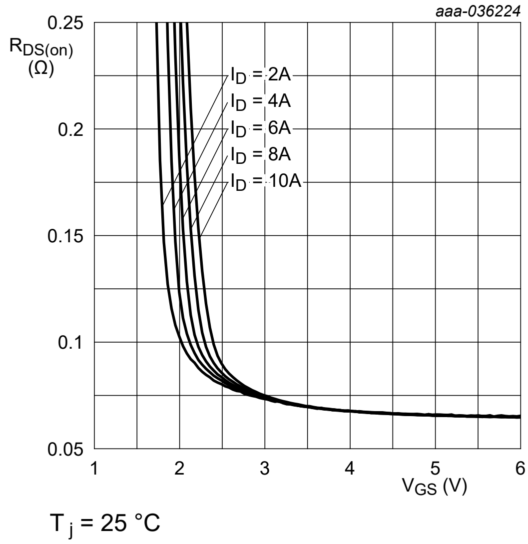


Fig. 13. Drain-source on-state resistance as a function of gate-source voltage; typical values

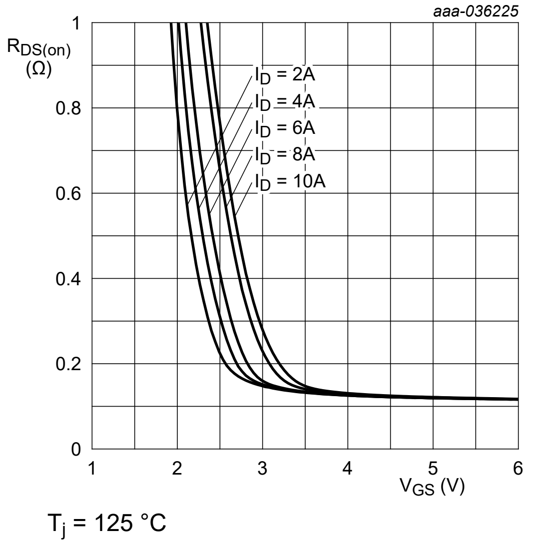


Fig. 14. Drain-source on-state resistance as a function of gate-source voltage; typical values

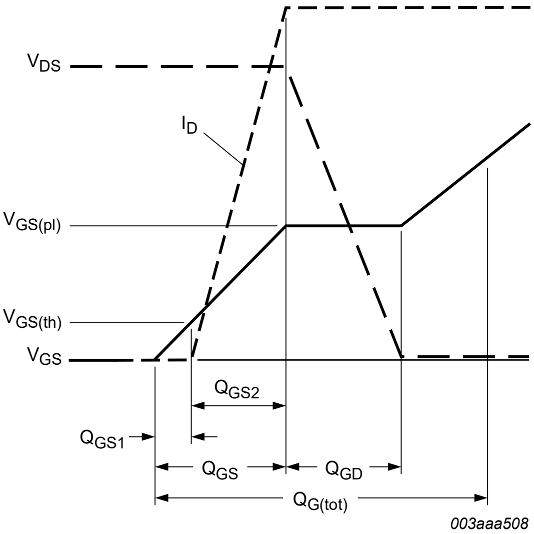
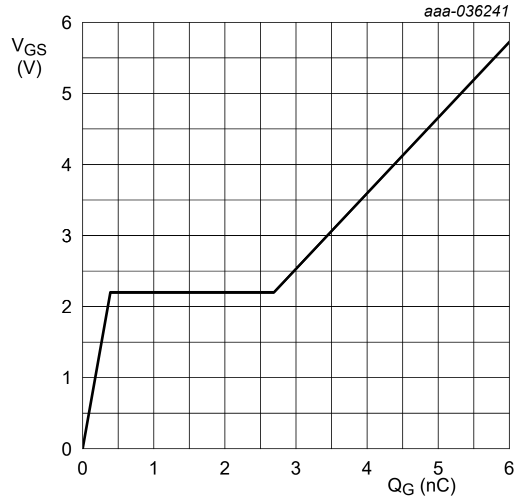


Fig. 15. Gate charge waveform definitions



T_J = 25 °C ; I_D = 8 A

Fig. 16. Gate-source voltage as a function of gate charge; typical values

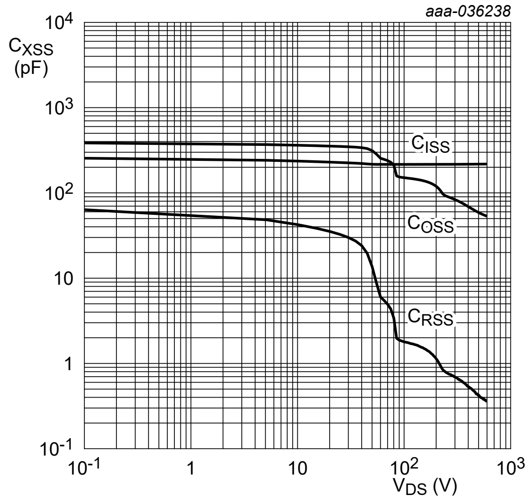
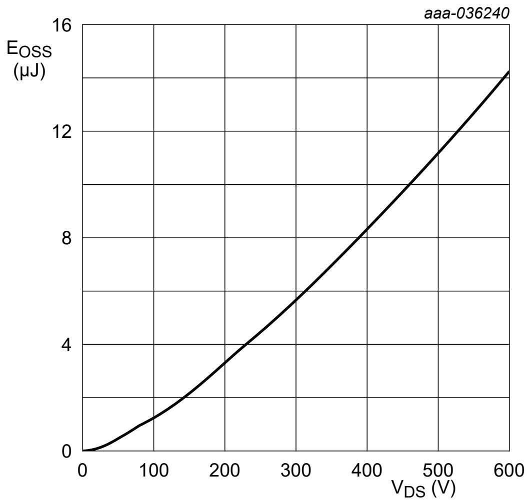
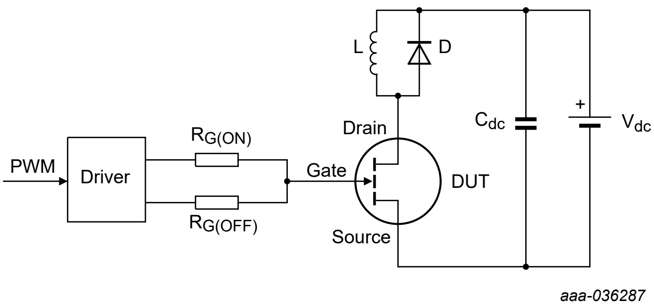


Fig. 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



Freq. = 100 kHz

Fig. 18. COSS stored energy as a function of drain-source voltage; typical values



V_{DS} = 400 V; I_D = 10 A; L = 318 µH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 2 Ω

Fig. 19. Typical switching times with inductive load

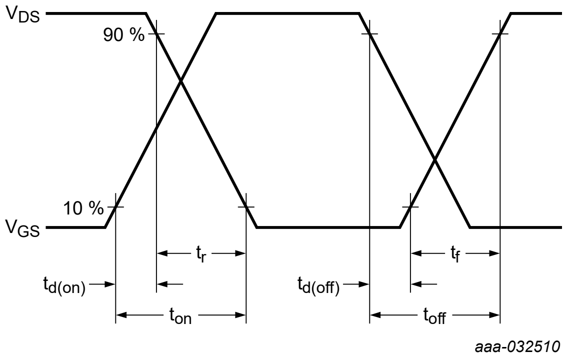
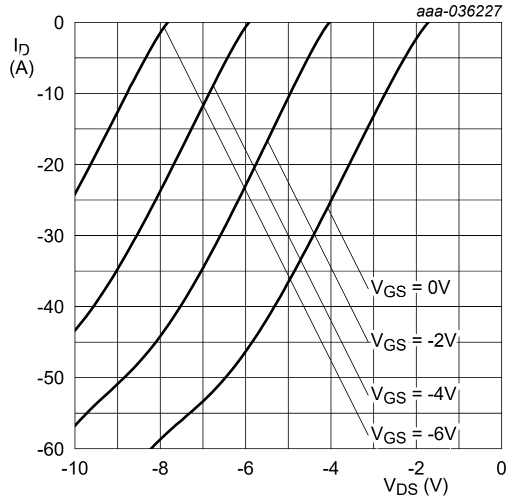
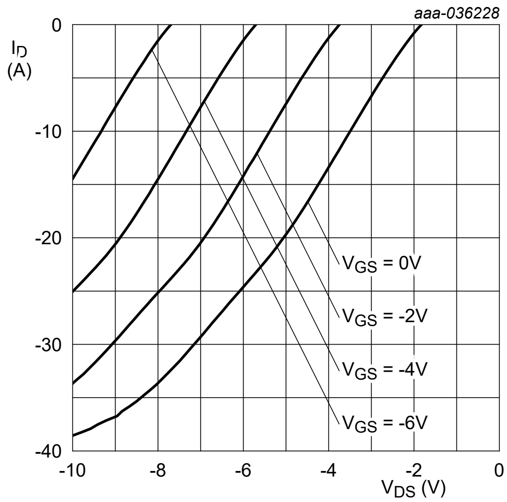


Fig. 20. Switching time waveform



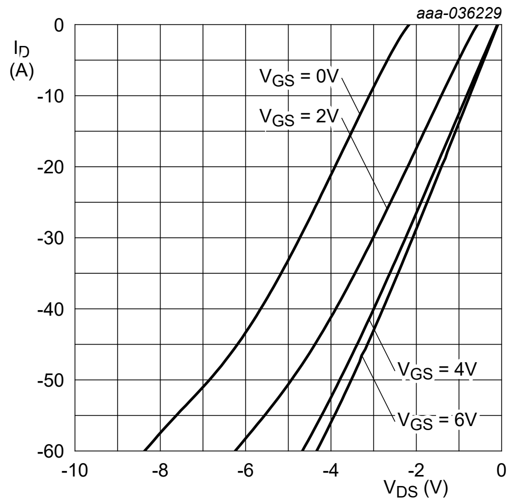
T_j = 25 °C

Fig. 21. Source current as a function of source-drain voltage; typical values



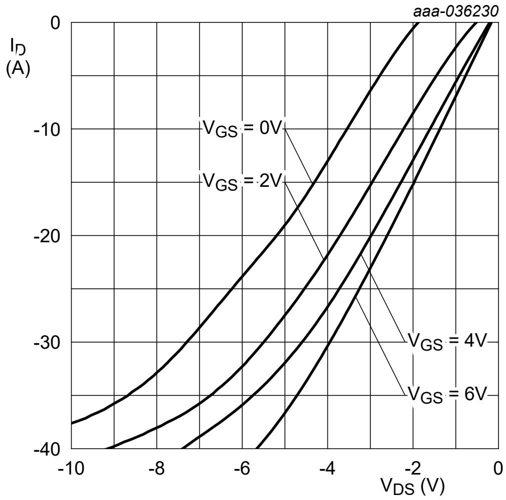
T_j = 125 °C

Fig. 22. Source current as a function of source-drain voltage; typical values



T_j = 25 °C

Fig. 23. Source current as a function of source-drain voltage; typical values

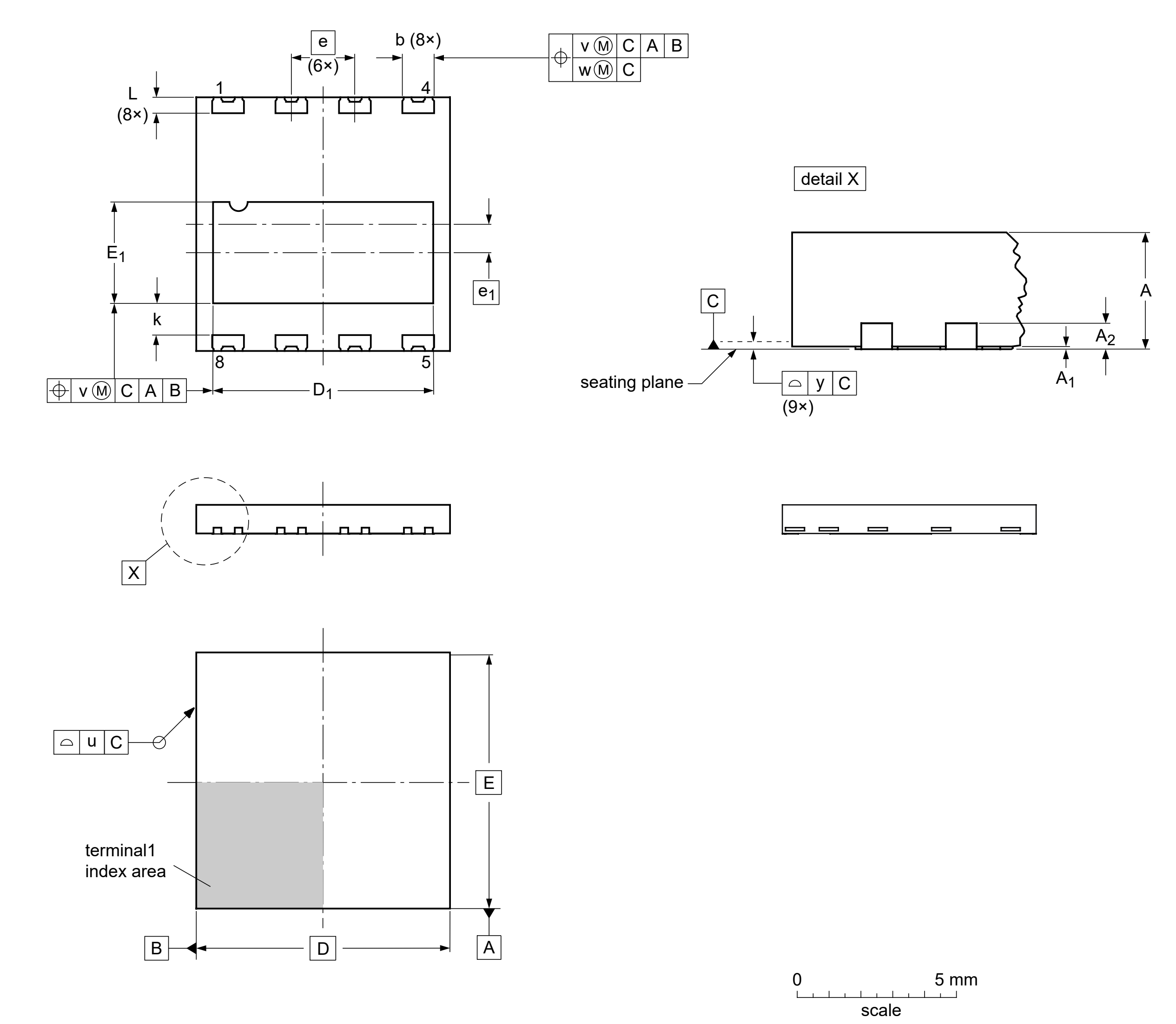


T_j = 125 °C

Fig. 24. Source current as a function of source-drain voltage; typical values

11. Package outline

DFN8080-8: plastic thermal enhanced small outline package; no leads; 8 terminals; body: 8 × 8 × 0.9 mm **SOT8074-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	D_1	E	E_1	e	e_1	k	L	y	u	v	w
mm	max	1.0	0.05	0.203 REF	1.05	8 BSC	7.04	8 BSC	3.3	2 BSC	0.9 BSC	1 REF	0.6	0.1	0.1	0.1	0.05
	nom	0.9	0.02		1.00		6.94		3.2				0.5				
	min	0.8	0.00		0.92		6.84		3.1				0.4				

sot8074-1_po

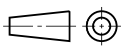
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8074-1		MO-229 compatible				23-03-03

Fig. 25. Package outline DFN8080-8 (SOT8074-1)

12. Soldering

Footprint information for reflow soldering of DFN8080-8 package **SOT8074-1**

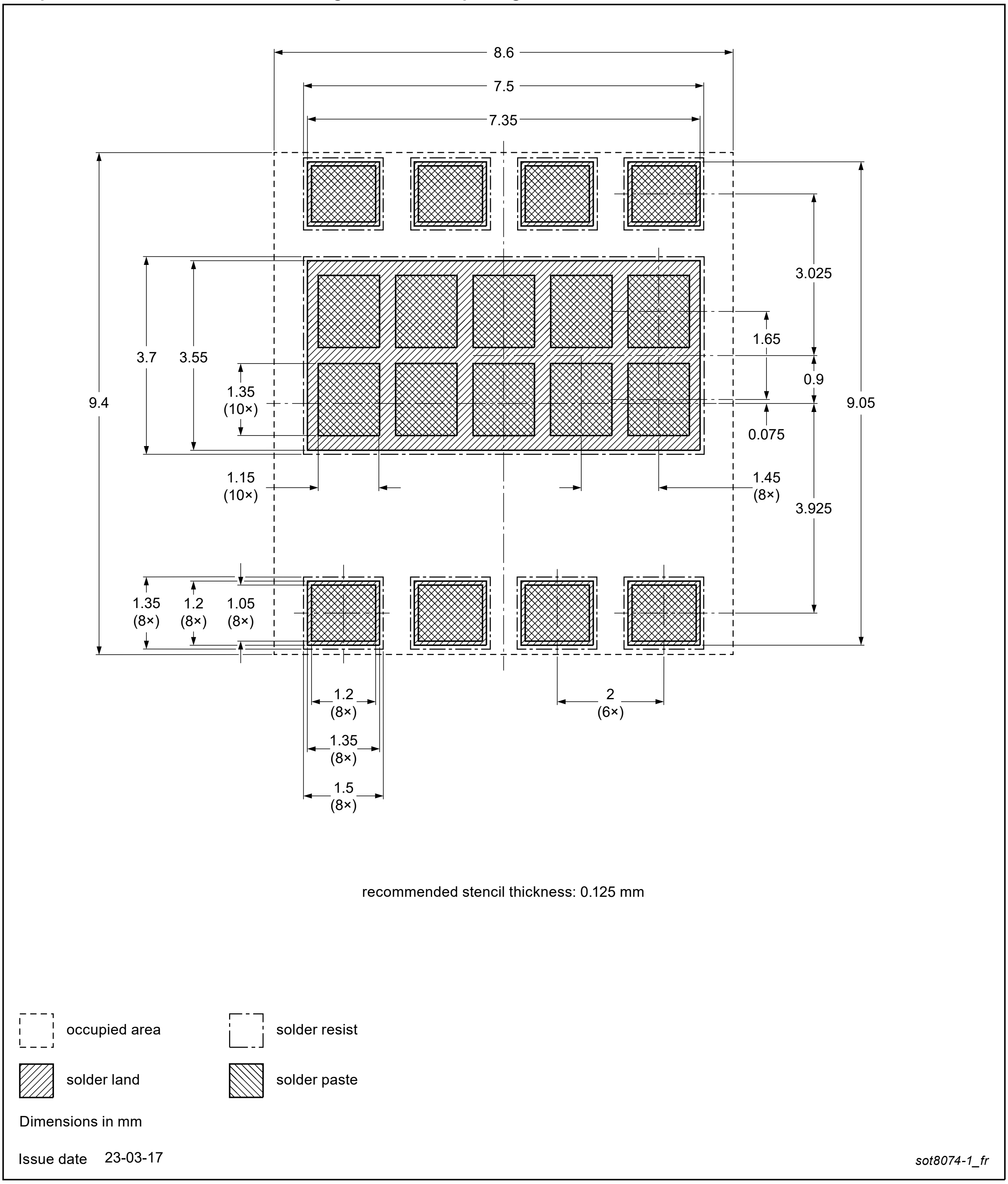


Fig. 26. Reflow soldering footprint for DFN8080-8 (SOT8074-1)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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