Instruction manual for Evaluation Board - TC78B016FTG -

April 3, 2018

Rev.1.0

【Outline】

The TC78B016FTG is a three-phase brushless DC motor driver incorporating our original technology, Intelligent Phase Control (InPAC) that is an automatic phase adjustment function. Elimination of adjustment burden and high-efficiency motor drive are possible by using this technology.
Using BiCD process and realizing the rating of 40 V and 3.0 A per one phase.
This evaluation board equipped with motor evaluation function can control a motor by connecting the motor to the external hall element.
Please sense excellent controllability of three-phase brushless DC motor by applying the TC78B016FTG.

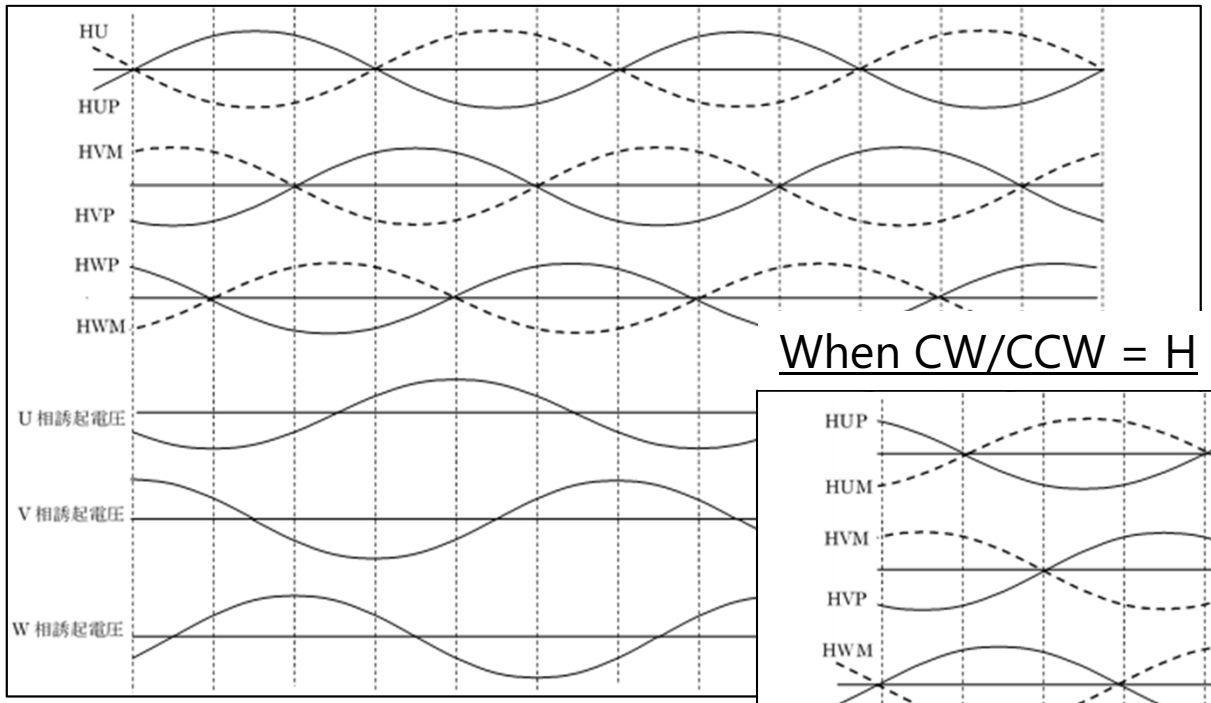
【Note】

In using, please be careful about the thermal condition sufficiently.
As for each control signal, please refer to the IC specification by accessing to the below URL.
http://toshiba.semicon-storage.com/jp/product/linear/motordriver/detail.TC78B016FTG.html
Further, the application of this evaluation board is limited to the purpose of evaluating and learning the motor control. Please do not ship them to a market.

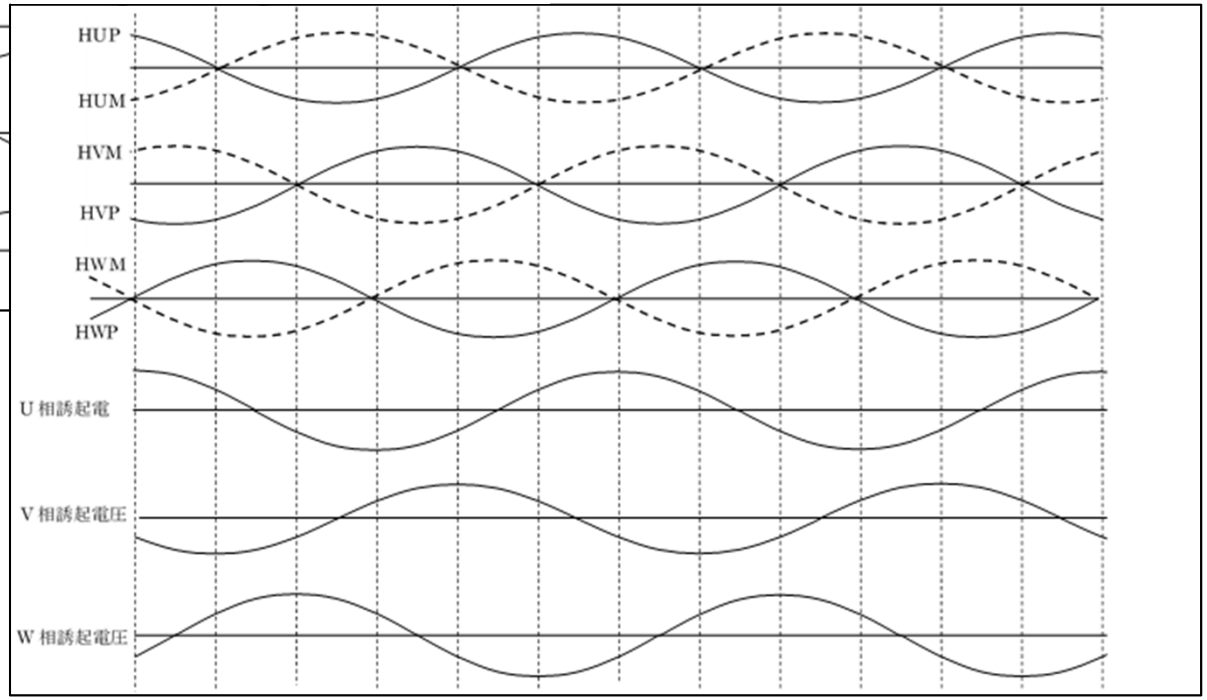
Note in Using a Motor

Use the motor whose phase relation of the hall element and the induced voltage is shown in the below timing charts.

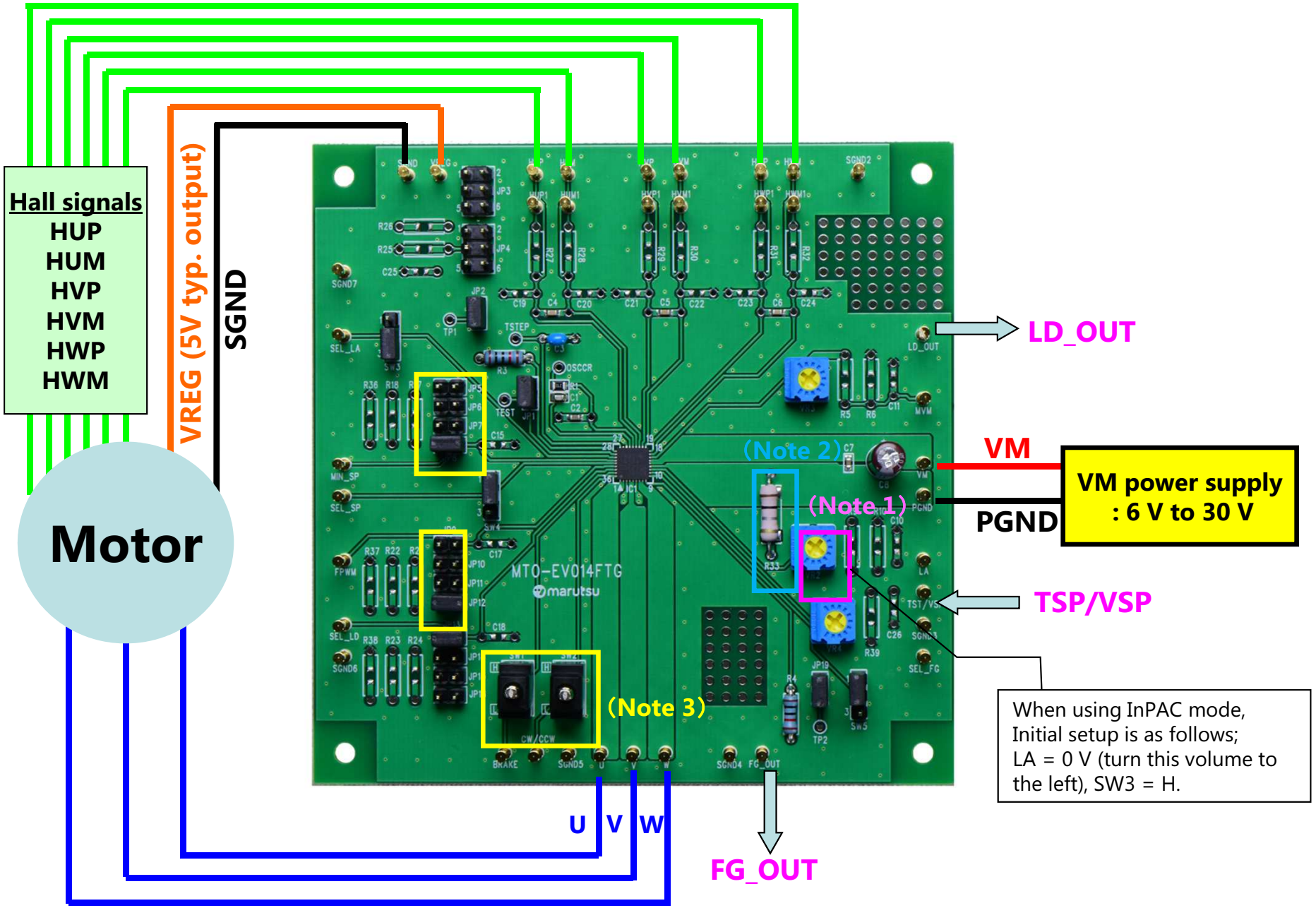
When CW/CCW= L



When CW/CCW = H



Connection Example of Evaluation Board and Motor (In case of using Hall element)



Startup and Shutdown Sequence / Notes

-Startup sequence

1. Confirm the conditions: SW4 = H (pin 2 and pin 3 are short-circuited), TSP/VSP = GND (VR4 = 0 Ω, volume is turned in downward direction)
2. Apply VM: 6 to 30 V
3. Change the volume of VR4 gradually to raise the voltage of TSP/VSP pins. (Motor rotates when their voltage reaches 0.625 V (typ.).)

- Shutdown sequence

1. Change the volume of VR4 gradually to set TSP/VSP pins GND. (VR4 = 0 Ω, turn the volume in downward direction)
2. VM = OFF

Note 1:
When using InPAC mode, please initially set as follows; LA = 0 V (VR2 = 0 Ω, turn downward this volume), SW3 = H (Short-circuit pin 2 and pin 3).

Note 2:
Use the shunt resistor (R33) for current limit.
(Current limit setup) When 0.1 Ω is applied for the resistor R33, the current is limited as follows; Iout (max) = 0.25 V / R33 = 2.5 A

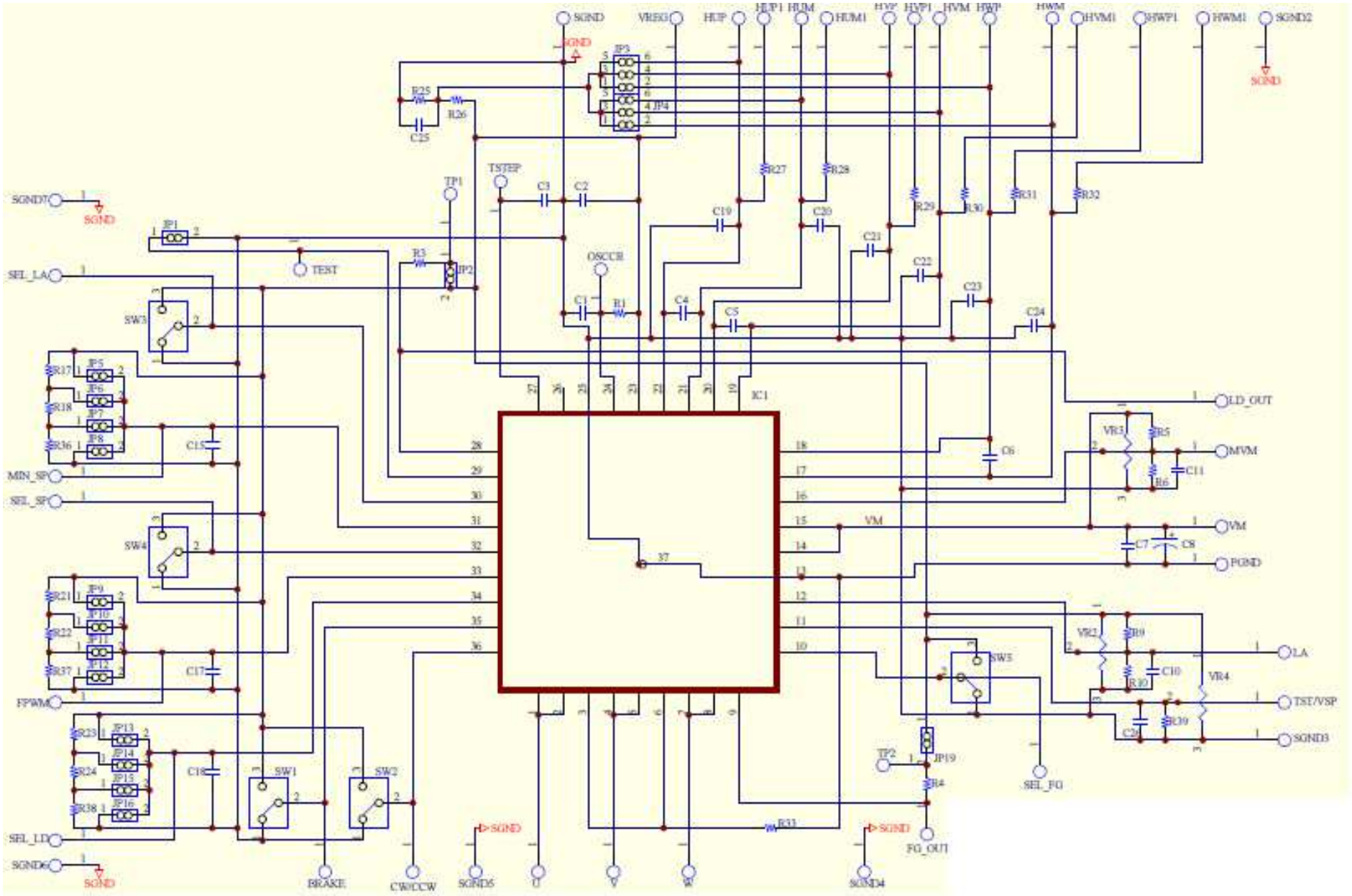
Note 3:
Switches for setting BRAKE pin, CW/CCW pin, SEL_LA pin, and SEL_SP pin

SW name	Pin name	H/L	Description
SW1	BRAKE	H	Brake function
		L	Normal function
SW2	CW/CCW	H	Reverse
		L	Forward
SW3	SEL_LA	H	Auto lead angle mode: InPAC
		Open	Auto lead angle mode: Proportion to frequency
		L	LA external input mode
SW4	SEL_SP	H	Analog voltage input (0.625 V (typ.) to 3.125 V (typ.))
		Open	Pulse duty signal input (Input signal: 0 to 100 %, 0/5V, 1 kHz to 100 kHz)

Using JP (Jumper)

JP name	Relative pin	Initial state	Description
JP1	TEST-SGND	JP1: Short	Be sure to short-circuit.
JP2	VREG,(OSCCR)	JP2: Short	Be sure to short-circuit.
JP3, JP4	For Hall IC	$JP3_{(1-2)}$: Open $JP3_{(3-4)}$: Open $JP3_{(5-6)}$: Open $JP4_{(1-2)}$: Open $JP4_{(3-4)}$: Open $JP4_{(5-6)}$: Open	・When using Hall IC, following setup is necessary. Open capacitors of C4, C5, and C6. Connect resistors of R25 and R26. And short-circuit $JP3_{(1-2)}$, $JP3_{(3-4)}$, and $JP3_{(5-6)}$, or $JP4_{(1-2)}$, $JP4_{(3-4)}$, and $JP4_{(5-6)}$. (Example: R25 = 20 kΩ, R26 = 20 kΩ) ・Also refer to “Notes in using Hall IC" in the application note.
JP5 to 8	MIN_SP	JP5: Open JP6: Open JP7: Open JP8: Short	・MIN_SP pin is set SGND by short-circuiting JP8, and it is set VREG by short-circuiting JP5. ・JP6 and JP7 can be selected by connecting resistors to R17, R18, and R36. (Example: R17 = 20 kΩ, R18 = 8.2 kΩ, and R36 = 12 kΩ) ・Refer to the technical datasheets for more information on the functions.
JP9 to 12	FPWM	JP9: Open JP10: Open JP11: Open JP12: Short	・FPWM pin is set SGND by short-circuiting JP12, and it is set VREG by short-circuiting JP9. ・JP6 and JP7 can be selected by connecting resistors to R21, R22, and R37. (Example: R21 = 20 kΩ, R22 = 8.2 kΩ, and R37 = 12 kΩ) ・Refer to the technical datasheets for more information on the functions.
JP13 to 16	SEL_LD	JP13: Short JP14: Open JP15: Open JP16: Open	・SEL_LD pin is set SGND by short-circuiting JP12, and FPWM pin is set VREG by short-circuiting JP5. ・JP6 and JP7 can be selected by connecting resistors to R23, R24, and R38. (Example: R23 = 20 kΩ, R24 = 8.2 kΩ, and R38 = 12 kΩ) ・Refer to the technical datasheets for more information on the functions.
JP19	FG_OUT-VREG	JP19: Short	High level voltage of FG_OUT pin is set 5 V by short-circuiting JP19.

Circuit Diagram



External Components

No.	Parts
R1	27 kΩ
R3	10 kΩ
R4	10 kΩ
R5	-
R6	-
R9	-
R10	-
R17	-
R18	-
R21	-
R22	-
R23	-
R24	-
R25	-
R26	-
R27	-
R28	-
R29	-
R30	-
R31	-
R32	-
R33	0.1 Ω
R36	-
R37	-
R38	-
R39	-

No.	Parts
C1	360 pF
C2	0.1 µF
C3	0.01 µF
C4	0.01 µF
C5	0.01 µF
C6	0.01 µF
C7	0.1 µF
C8	10 µF/50 V
C10	-
C11	-
C15	-
C17	-
C18	-
C21	-
C22	-
C23	-
C24	-
C25	-
C26	-

No.	Parts
JP1	Short
JP2	Short
JP3	-
JP4	-
JP5	-
JP6	-
JP7	-
JP8	Short
JP9	-
JP10	-
JP11	-
JP12	Short
JP13	Short
JP14	-
JP15	-
JP16	-
JP19	Short

No.	Parts
SW1	SW
SW2	SW
SW3	SW
SW4	SW
SW5	SW

No.	Parts
VR2	VR (50 kΩ)
VR3	VR (50 kΩ)
VR4	VR (50 kΩ)