High Linearity Differential RF/IF Amplifier/ADC Driver

FEATURES

- **50.0dBm OIP3 at 240MHz into a 100Ω Diff Load**
- **NF = 3.0dB at 240MHz**
- **20MHz to 2000MHz Bandwidth**
- **15.2dB Gain**
- **A-Grade 100% OIP3 Tested at 240MHz**
- 1.0nV/√Hz Total Input Noise
- S11 < –15dB Up to 1.2GHz
- S22 < –15dB Up to 1.2GHz
- >2.75V_{P-P} Linear Output Swing
- P1dB = 24.0dBm
- Insensitive to V_{CC} Variation
- 100Ω Differential Gain-Block Operation
- Input/Output Internally Matched to 100Ω Diff
- Single 5V Supply
- DC Power = 800mW
- Unconditionally Stable
- 4mm × 4mm, 24-Lead QFN Package

APPLICATIONS

- Differential ADC Driver
- Differential IF Amplifier
- OFDM Signal Chain Amplifier
- 50Ω Balanced IF Amplifier
- 75Ω CATV Amplifier
- 700MHz to 800MHz LTE Amplifier

DESCRIPTION

The LTC®6430-15 is a differential gain block amplifier designed to drive high resolution, high speed ADCs with excellent linearity beyond 1000MHz and with low associated output noise. The LTC6430-15 operates from a single 5V power supply and consumes only 800mW.

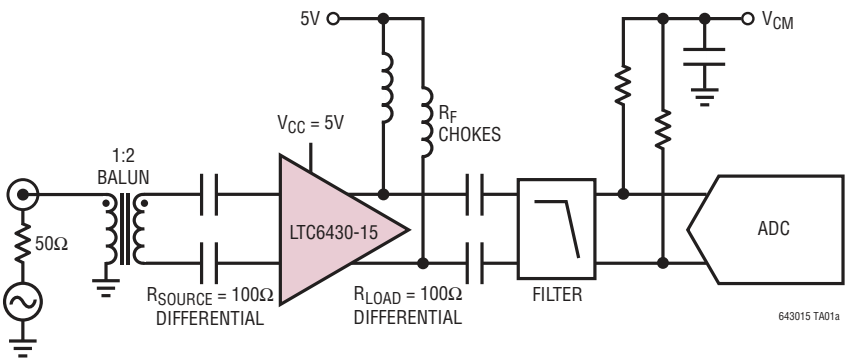
In its differential configuration, the LTC6430-15 can directly drive the differential inputs of an ADC. Using 1:2 baluns, the device makes an excellent 50Ω wideband balanced amplifier. While using 1:1.33 baluns, the device makes a high fidelity 50MHz to 1000MHz 75Ω CATV amplifier.

The LTC6430-15 is designed for ease of use, requiring a minimum of support components. The device is internally matched to 100Ω differential source/load impedance. On-chip bias and temperature compensation ensure consistent performance over environmental changes.

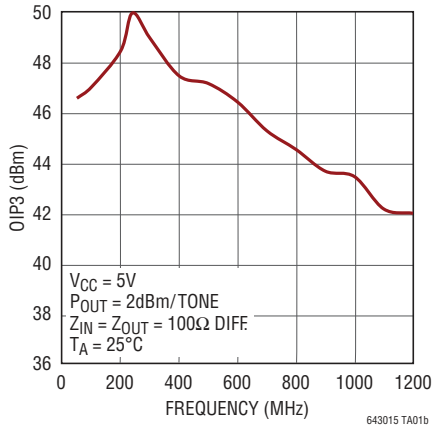
The LTC6430-15 uses a high performance SiGe BiCMOS process for excellent repeatability compared with similar GaAs amplifiers. All A-grade LTC6430-15 devices are tested and guaranteed for OIP3 at 240MHz. The LTC6430-15 is housed in a 4mm × 4mm, 24-lead, QFN package with an exposed pad for thermal management and low inductance. For a single-ended 50Ω IF gain block with similar performance, see the related LTC6431-15.

TYPICAL APPLICATION

Differential 16-Bit ADC Driver



OIP3 vs Frequency

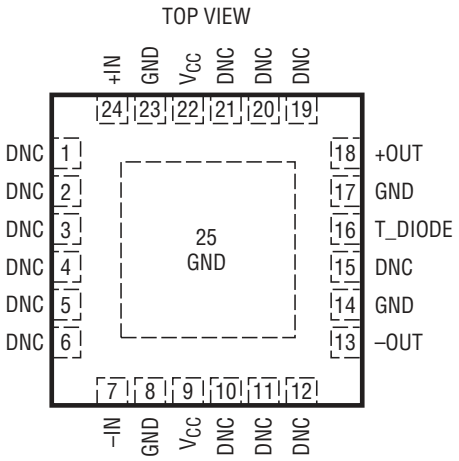


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V_{CC} to GND).....5.5V
Amplifier Output Current (+OUT) 105mA
Amplifier Output Current (–OUT) 105mA
RF Input Power, Continuous, 50Ω (Note 2)..... +15dBm
RF Input Power, 100µs Pulse, 50Ω (Note 2) .....+20dBm
Operating Temperature Range (T_{CASE}) ...–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C
Junction Temperature (T_J) ..... 150°C
Lead Temperature (Soldering, 10 sec).....300°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JC} = 40°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

The LTC6430-15 is available in two grades. The A-grade guarantees a minimum OIP3 at 240MHz while the B-grade does not.

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6430AIUF-15#PBF	LTC6430AIUF-15#TRPBF	43015	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC6430BIUF-15#PBF	LTC6430BIUF-15#TRPBF	43015	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 100Ω. Typical measured DC electrical performance using Test Circuit A (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_S	Operating Supply Range			4.75	5.0	5.25	V
$I_{S,TOT}$	Total Supply Current	All V_{CC} Pins Plus +OUT and –OUT	 ●	126 93	160	190 216	mA mA
$I_{S,OUT}$	Total Supply Current to OUT Pins	Current to +OUT and –OUT	 ●	112 79	146	176 202	mA mA
I_{VCC}	Current to V_{CC} Pin	Either V_{CC} Pin May Be Used	 ●	12 11	14	22 26	mA mA

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 100Ω, unless otherwise noted (Note 3). Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Small Signal							
BW	–3dB Bandwidth	De-Embedded to Package (Low Frequency Cut-Off, 20MHz)			2000		MHz
S11	Differential Input Match, 25MHz to 2000MHz	De-Embedded to Package			–10		dB
S21	Forward Differential Power Gain, 100MHz to 400MHz	De-Embedded to Package			15.1		dB
S12	Reverse Differential Isolation, 25MHz to 4000MHz	De-Embedded to Package			–19		dB
S22	Differential Output Match, 25MHz to 1600MHz	De-Embedded to Package			–10		dB
Frequency = 50MHz							
S21	Differential Power Gain	De-Embedded to Package			15.2		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			46.6 45.6		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			–89.2 –87.2		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–82.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–95.3		dBc
P1dB	Output 1dB Compression Point				23.8		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.0		dB
Frequency = 140MHz							
S21	Differential Power Gain	De-Embedded to Package			15.1		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			47.2 46.2		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			–90.4 –88.4		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–82.6		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–94.7		dBc
P1dB	Output 1dB Compression Point				23.8		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.0		dB
Frequency = 240MHz							
S21	Differential Power Gain	De-Embedded to Package	 ●	14.5 14.3	15.1	16.5 16.5	dB dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 8MHz, Z_O = 100Ω A-Grade B-Grade		47.0	50.0 47.0		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 8MHz, Z_O = 100Ω A-Grade B-Grade		–90.0	–96.0 –90.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–80.5		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–87.0		dBc
P1dB	Output 1dB Compression Point				24.1		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.0		dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 100Ω, unless otherwise noted (Note 3). Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Frequency = 300MHz							
S21	Differential Power Gain	De-Embedded to Package			15.1		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			48.5 47.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			–93.0 –91.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–76.9		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–84.4		dBc
P1dB	Output 1dB Compression Point				23.7		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.2		dB
Frequency = 380MHz							
S21	Differential Power Gain	De-Embedded to Package			15.1		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			47.5 46.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			–91.0 –89.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–81.9		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–88.0		dBc
P1dB	Output 1dB Compression Point				23.2		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.2		dB
Frequency = 500MHz							
S21	Differential Power Gain	De-Embedded to Package			15.0		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			47.2 46.2		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			–90.4 –88.4		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–79.0		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–90.0		dBc
P1dB	Output 1dB Compression Point				23.4		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.5		dB
Frequency = 600MHz							
S21	Differential Power Gain	De-Embedded to Package			15.0		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			46.5 45.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω A-Grade B-Grade			–89.0 –87.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–72.7		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–81.4		dBc
P1dB	Output 1dB Compression Point				23.1		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.5		dB
Frequency = 700MHz							
S21	Differential Power Gain	De-Embedded to Package			14.9		dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 100Ω, unless otherwise noted (Note 3). Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	A-Grade B-Grade		45.3 44.3		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	A-Grade B-Grade		–86.6 –84.6		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–71.4		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–79.5		dBc
P1dB	Output 1dB Compression Point				23.0		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			3.8		dB
Frequency = 800MHz							
S21	Differential Power Gain	De-Embedded to Package			14.8		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	A-Grade B-Grade		44.5 43.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	A-Grade B-Grade		–85.0 –83.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–71.2		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–76.7		dBc
P1dB	Output 1dB Compression Point				22.6		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			4.0		dB
Frequency = 900MHz							
S21	Differential Power Gain	De-Embedded to Package			14.8		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	A-Grade B-Grade		43.7 42.7		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	A-Grade B-Grade		–83.4 –81.4		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–71.7		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–76.5		dBc
P1dB	Output 1dB Compression Point				22.3		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			4.2		dB
Frequency = 1000MHz							
S21	Differential Power Gain	De-Embedded to Package			14.7		dB
OIP3	Output Third-Order Intercept Point	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	A-Grade B-Grade		43.5 42.5		dBm dBm
IM3	Third-Order Intermodulation	P_{OUT} = 2dBm/Tone, Δf = 1MHz, Z_O = 100Ω	A-Grade B-Grade		–83.0 –81.0		dBc dBc
HD2	Second Harmonic Distortion	P_{OUT} = 8dBm			–74.2		dBc
HD3	Third Harmonic Distortion	P_{OUT} = 8dBm			–86.0		dBc
P1dB	Output 1dB Compression Point				22.3		dBm
NF	Noise Figure	De-Embedded to Package for Balun Input Loss			4.2		dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and characterization. This parameter is not tested.

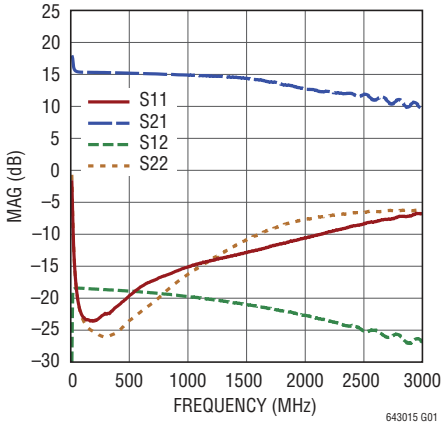
Note 3: The LTC6430-15 is guaranteed functional over the case operating temperature range of –40°C to 85°C.

Note 4: Small signal parameters S and noise are de-embedded to the package pins, while large signal parameters are measured directly from the test circuit.

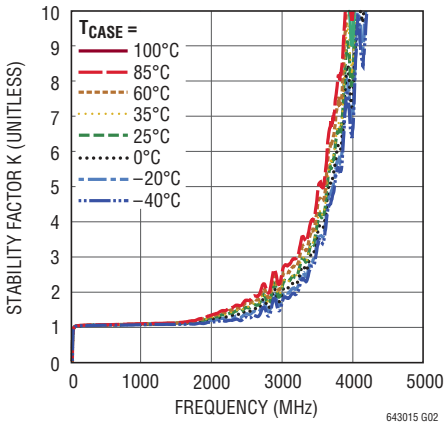
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 100Ω, unless otherwise noted (Note 3). Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

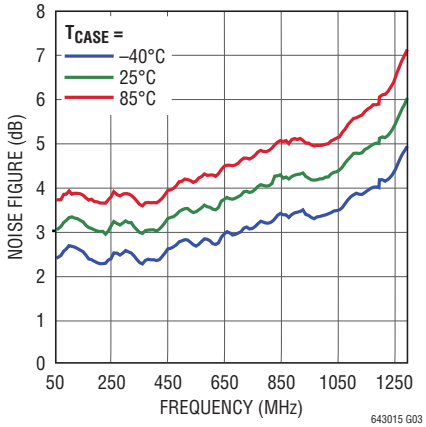
Differential S Parameters vs Frequency



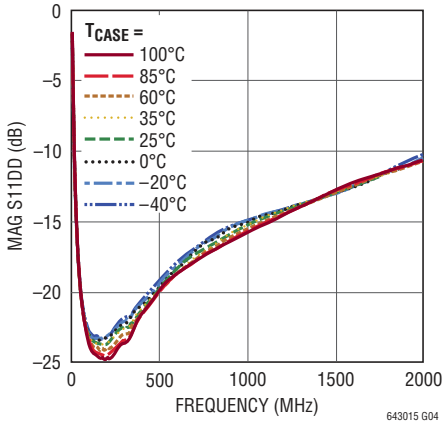
Differential Stability Factor K vs Frequency Over Temperature



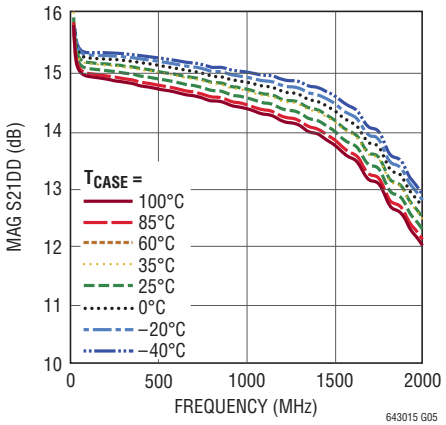
Noise Figure vs Frequency Over Temperature



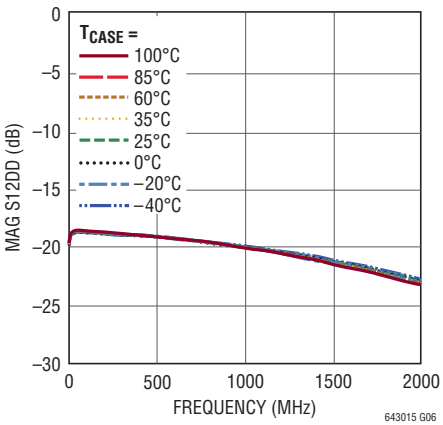
Differential Input Match ($S11_{DD}$) vs Frequency Over Temperature



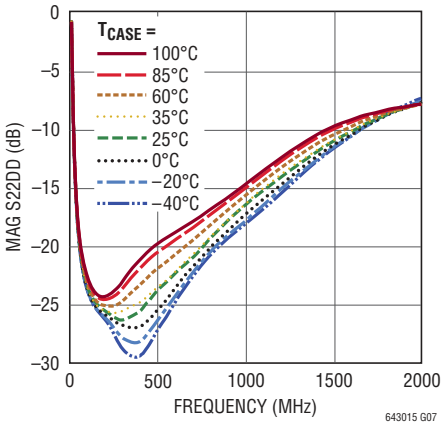
Differential Gain ($S21_{DD}$) vs Frequency Over Temperature



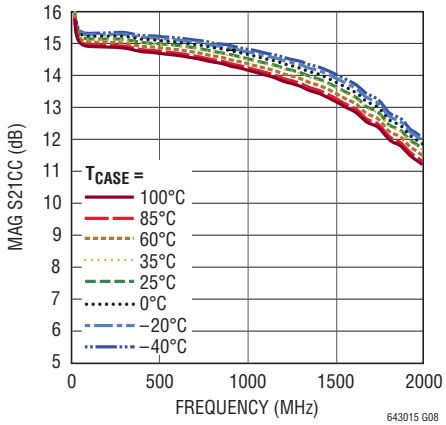
Differential Reverse Isolation ($S12_{DD}$) vs Frequency Over Temperature



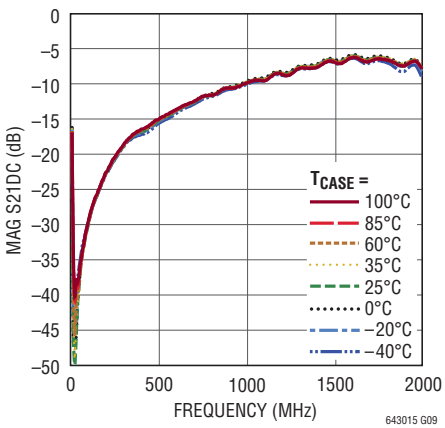
Differential Output Match ($S22_{DD}$) vs Frequency Over Temperature



Common Mode Gain ($S21_{CC}$) vs Frequency Over Temperature



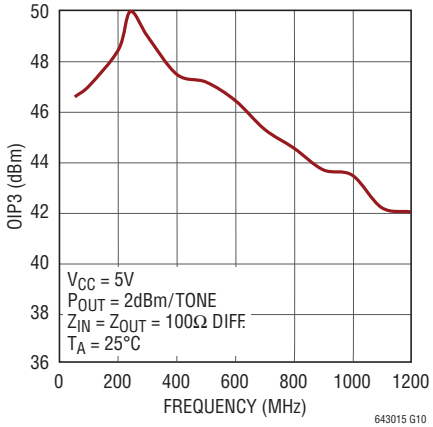
CM-DM Gain ($S21_{DC}$) vs Frequency Over Temperature



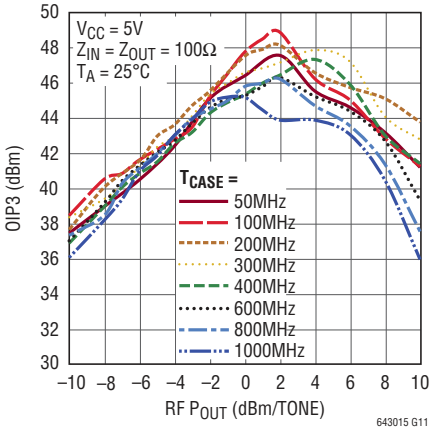
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 100Ω, unless otherwise noted (Note 3). Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

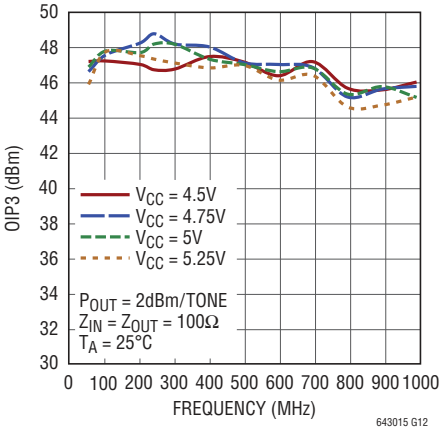
OIP3 vs Frequency



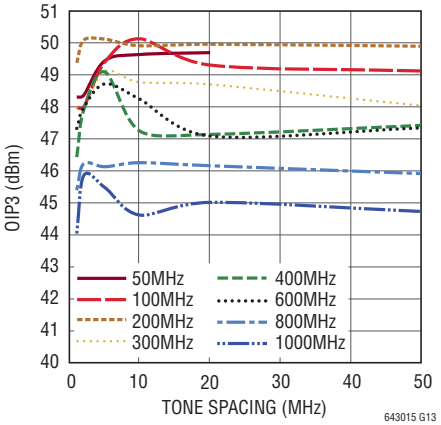
OIP3 vs RF Power Out/Tone Over Frequency



OIP3 vs Frequency Over V_{CC} Voltage

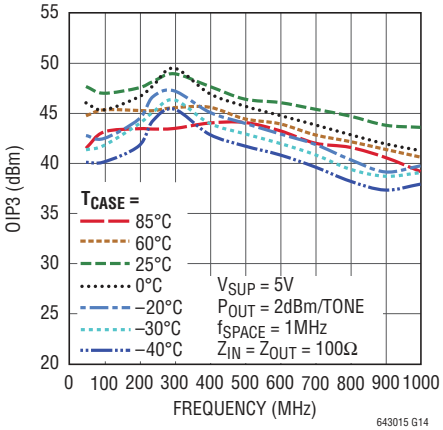


OIP3 vs Tone Spacing Over Frequency

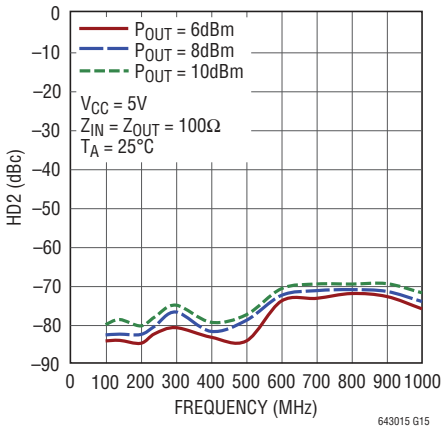


VCC = 5V, POUT = 2dBm/TONE, ZIN = ZOUT = 100Ω, TA = 25°C

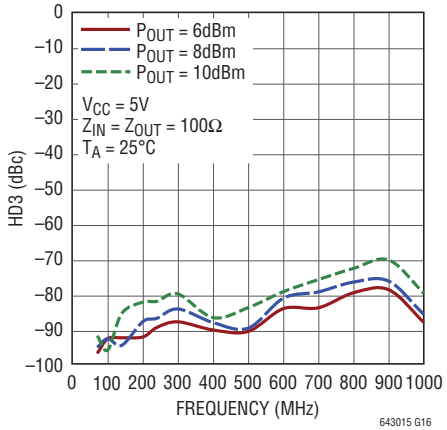
OIP3 vs Frequency Over Temperature



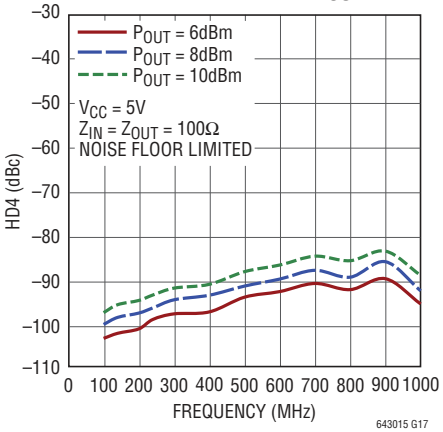
HD2 vs Frequency Over P_{OUT}



HD3 vs Frequency Over P_{OUT}



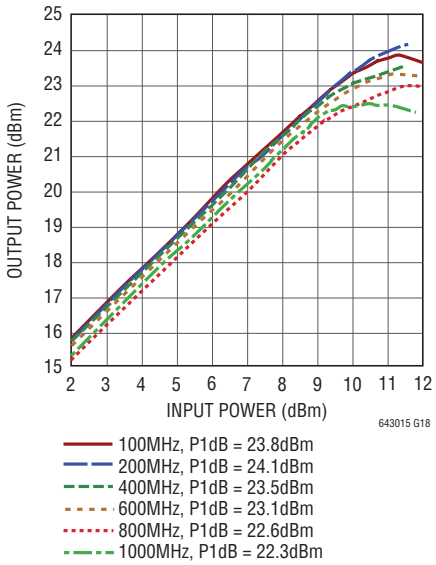
HD4 vs Frequency Over P_{OUT}



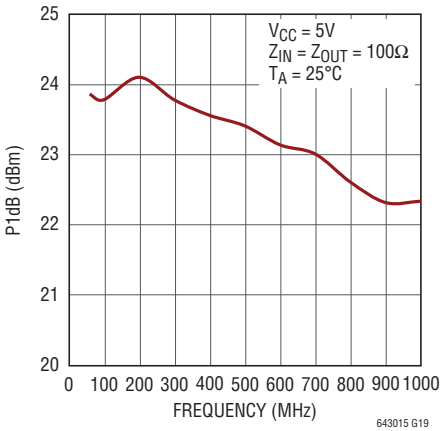
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V, Z_{SOURCE} = Z_{LOAD} = 100Ω, unless otherwise noted (Note 3). Measurements are performed using Test Circuit A, measuring from 50Ω SMA to 50Ω SMA without de-embedding (Note 4).

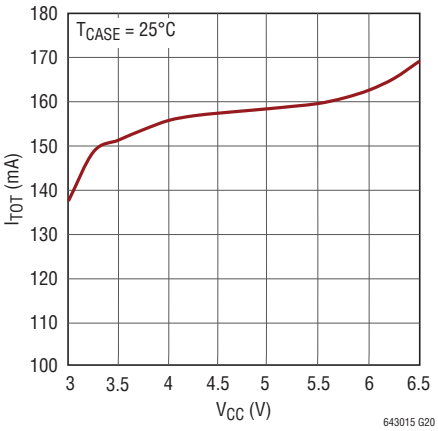
Output Power vs Input Power Over Frequency



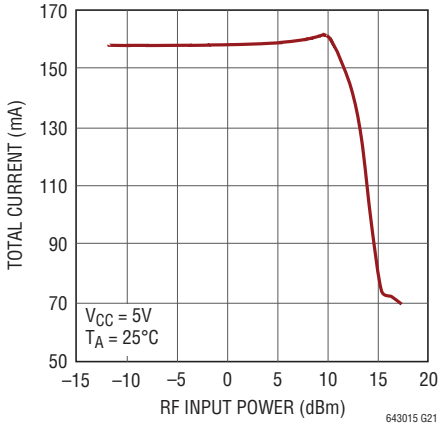
P1dB vs Frequency



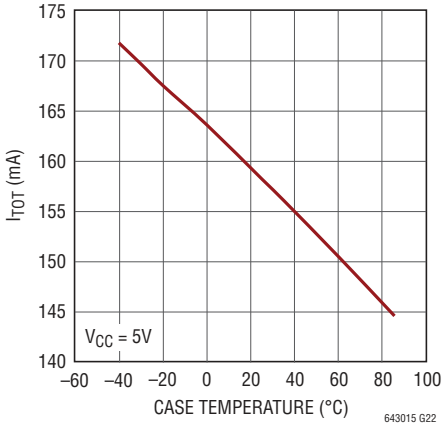
Total Current (I_{TOT}) vs V_{CC}



Total Current vs RF Input Power



Total Current (I_{TOT}) vs Case Temperature



PIN FUNCTIONS

GND (Pins 8, 14, 17, 23, Exposed Pad Pin 25): Ground. For best RF performance, all ground pins should be connected to the printed circuit board ground plane. The exposed pad (Pin 25) should have multiple via holes to an underlying ground plane for low inductance and good thermal dissipation.

+IN (Pin 24): Positive Signal Input Pin. This pin has an internally generated 2V DC bias. A DC-blocking capacitor is required. See the Applications Information section for specific recommendations.

–IN (Pin 7): Negative Signal Input Pin. This pin has an internally generated 2V DC bias. A DC-blocking capacitor is required. See the Applications Information section for specific recommendations.

V_{CC} (Pins 9, 22): Positive Power Supply. Either or both V_{CC} pins should be connected to the 5V supply. Bypass the V_{CC} pin with 1000pF and 0.1µF capacitors. The 1000pF capacitor should be physically close to a V_{CC} pin.

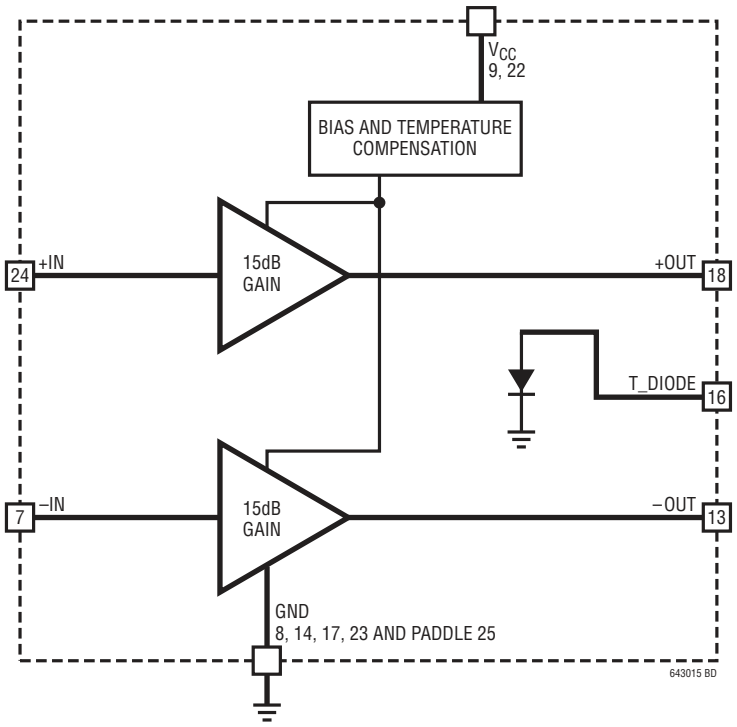
+OUT (Pin 18): Positive Amplifier Output Pin. A transformer with a center tap tied to V_{CC} or a choke inductor tied to 5V supply is required to provide DC current and RF isolation. For best performance select a choke with low loss and high self resonant frequency (SRF). See the Applications Information section for more information.

–OUT (Pin 13): Negative Amplifier Output Pin. A transformer with a center tap tied to V_{CC} or a choke inductor is required to provide DC current and RF isolation. For best performance select a choke with low loss and high SRF.

DNC (Pins 1 to 6, 10 to 12, 15, 19 to 21): Do Not Connect. Do not connect these pins, allow them to **float. Failure to float these pins may impair the performance of the LTC6430-15.**

T_DIODE (Pin 16): Optional. A diode which can be forward biased to ground with up to 1mA of current. The measured voltage will be an indicator of the chip temperature.

BLOCK DIAGRAM



TEST CIRCUIT A

Differential Application Test Circuit A (Balanced Amp)

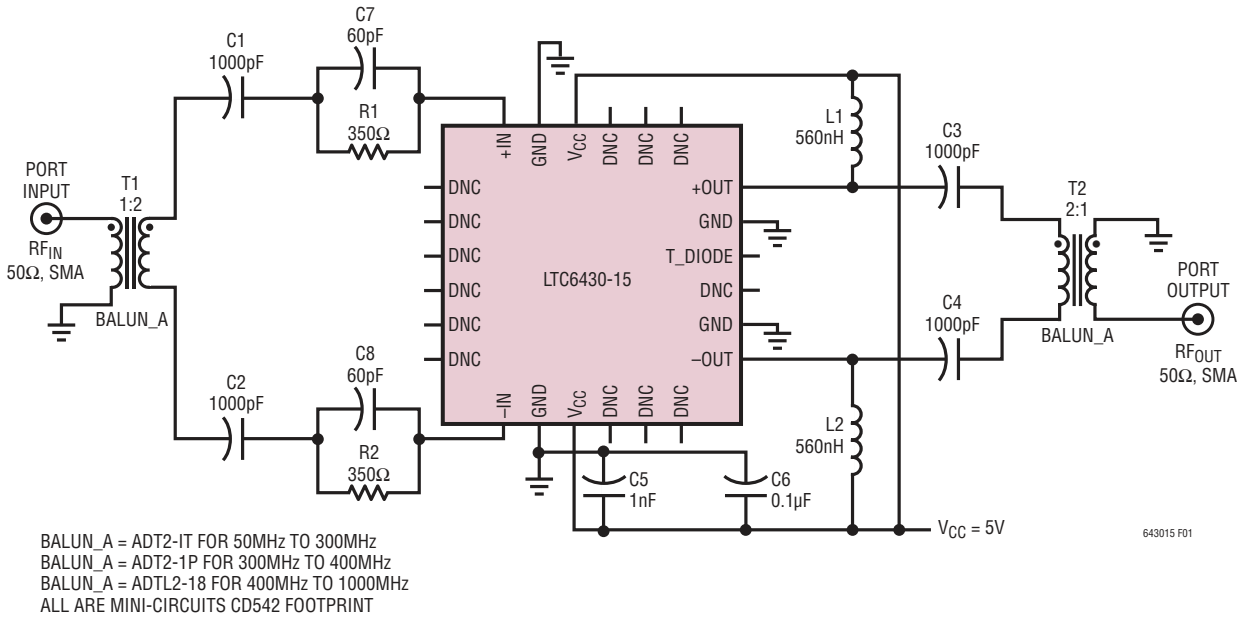


Figure 1. Test Circuit A

OPERATION

The LTC6430-15 is a highly linear, fixed-gain amplifier for differential signals. It can be considered a pair of 50Ω single-ended devices operating 180 degrees apart. Its core signal path consists of a single amplifier stage minimizing stability issues. The input is a Darlington pair for high input impedance and high current gain. Additional circuit enhancements increase the output impedance commensurate with the input impedance and minimize the effects of internal Miller capacitance.

The LTC6430-15 uses a classic RF gain block topology, with enhancements to achieve excellent linearity. Shunt and series feedback elements are added to lower the input/output impedance and match them simultaneously to the source and load. An internal bias controller optimizes the bias point for peak linearity over environmental changes. This circuit architecture provides low noise, good RF power handling capability and wide bandwidth; characteristics that are desirable for IF signal-chain applications.

APPLICATIONS INFORMATION

The LTC6430-15 is a highly linear fixed-gain amplifier which is designed for ease of use. Both the input and output are internally matched to 100Ω differential source and load impedance from 20MHz to 1700MHz. Biasing and temperature compensation are also handled internally to deliver optimized performance. The designer need only supply input/output blocking capacitors, RF chokes and decoupling capacitors for the 5V supply. However, because the device is capable of such wideband operation, a single application circuit will probably not result in optimized performance across the full frequency band.

Differential circuits minimize the common mode noise and 2nd harmonic distortion issues that plague many designs. Additionally, the LTC6430's differential topology matches well with the differential inputs of an ADC. However, evaluation of these differential circuits is difficult, as high resolution, high frequency, differential test equipment is lacking.

Our test circuit is designed for evaluation with standard single ended 50Ω test equipment. Therefore, 1:2 balun transformers have been added to the input and output to transform the LTC6430-15's 100Ω differential source/load impedance to 50Ω single-ended impedance compatible with most test equipment.

Other than the balun, the evaluation circuit requires a minimum of external components. Input and output DC-blocking capacitors are required as this device is internally biased for optimal operation. A frequency appropriate choke and de-coupling capacitors provide DC bias to the RF ±OUT nodes. Only a single 5V supply is necessary to either of the V_{CC} pins on the device. Both V_{CC} pins are connected inside the package. Two V_{CC} pins are provided for the convenience of supply routing on the PCB. An optional parallel 60pF, 350Ω input network has been added to ensure low frequency stability.

The particular element values shown in Test Circuit A are chosen for wide bandwidth operation. Depending on the desired frequency, performance may be improved by custom selection of these supporting components.

Choosing the Right RF Choke

Not all choke inductors are created equal. It is always important to select an inductor with low R_{LOSS} as resistance will drop the available voltage to the device. Also look for an inductor with high self resonant frequency (SRF) as this will limit the upper frequency where the choke is useful. Above the SRF, the parasitic capacitance dominates and the choke's impedance will drop. For these reasons, wirewound inductors are preferred, while multilayer ceramic chip inductors should be avoided for an RF choke if possible. Since the LTC6430-15 is capable of such wideband operation, a single choke value will not result in optimized performance across its full frequency band. Table 1 lists common frequency bands and suggested corresponding inductor values.

Table 1. Target Frequency and Suggested Inductor Value

FREQUENCY BAND (MHz)	INDUCTOR VALUE (nH)	SRF (MHz)	MODEL NUMBER	MANUFACTURER
20 to 100	1500nH	100	0603LS	Coilcraft www.coilcraft.com
100 to 500	560nH	525	0603LS	
500 t o 1000	100nH	1150	0603LS	
1000 to 2000	51nH	1400	0603LS	

DC-Blocking Capacitor

The role of a DC-blocking capacitor is straightforward: block the path of DC current and allow a low series impedance path for the AC signal. Lower frequencies require a higher value of DC-blocking capacitance. Generally, 1000pF to 10,000pF will suffice for operation down to 20MHz. The LTC6430-15 linearity is insensitive to the choice of blocking capacitor.

RF Bypass Capacitor

RF bypass capacitors act to shunt the AC signals to ground with a low impedance path. They prevent the AC signal from getting into the DC bias supply. It is best to place the bypass capacitor as close as possible to the DC supply pins of the amplifier. Any extra distance translates into additional series inductance which lowers the effectiveness of the bypass capacitor network. The suggested bypass capacitor network consists of two capacitors: a low value 1000pF capacitor to shunt high frequencies

APPLICATIONS INFORMATION

and a larger 0.1µF capacitor to handle lower frequencies. Use ceramic capacitors of appropriate physical size for each capacitance value (e.g., 0402 for the 1000pF, 0805 for the 0.1µF) to minimize the equivalent series resistance (ESR) of the capacitor.

Low Frequency Stability

Most RF gain blocks suffer from low frequency instability. To avoid stability issues, the LTC6430-15, contains an internal feedback network that lowers the gain and matches the input and output impedance of the intrinsic amplifier. This feedback network contains a series capacitor, whose value is limited by physical size. So, at some low frequencies, this feedback capacitor looks like an open circuit; the feedback fails, gain increases and gross impedance mismatches occur which can create instability. This situation is easily resolved with a parallel capacitor and a resistor network on the input. This is shown in Figure 1. This network provides resistive loss at low frequencies and is bypassed by the capacitor at the desired band of operation. However, if the LTC6430-15 is preceded by a low frequency termination, such as a choke or balun transformer, the input stability network is not required. A choke at the output can also terminate low frequencies out-of-band and stabilize the device.

Exposed Pad and Ground Plane Considerations

As with any RF device, minimizing the ground inductance is critical. Care should be taken with PC board layouts using exposed pad packages, as the exposed pad provides the lowest inductive path to ground. The maximum allowable number of minimum diameter via holes should be placed underneath the exposed pad and connected to as many ground plane layers as possible. This will provide good RF ground and low thermal impedance. Maximizing the copper ground plane at the signal and microstrip ground will also improve the heat spreading and lower inductance. It is a good idea to cover the via holes with solder mask on the backside of the PCB to prevent the solder from wicking away from the critical PCB to exposed pad interface. One to two ounces of copper plating is suggested to improve heat spreading from the device.

Frequency Limitations

The LTC6430-15 is a wide bandwidth amplifier but it is not intended for operation down to DC. The lower frequency cutoff is limited by on-chip matching elements. The cutoff may be arbitrarily pushed lower with off chip elements; however, the translation between the low fixed DC common mode input voltage and the higher open collector DC common mode output bias point make DC-coupled operation impractical.

Test Circuit A

Test Circuit A, shown in Figure 1, is designed to allow for the evaluation of the LTC6430-15 with standard single-ended 50Ω test equipment. This allows the designer to verify the performance when the device is operated differentially. This evaluation circuit requires a minimum of external components. Since the LTC6430-15 operates over a very wide band, the evaluation test circuit is optimized for wideband operation. Obviously, for narrowband operation, the circuit can be further optimized.

Input and output DC-blocking capacitors are required, as this device is internally DC biased for optimal performance. A frequency appropriate choke and decoupling capacitors are required to provide DC bias to the RF output nodes (+OUT and –OUT). A 5V supply should also be applied to one of the V_{CC} pins on the device.

Components for a suggested parallel 60pF, 350Ω stability network have been added to ensure low frequency stability. The 60pF capacitance can be increased to improve low frequency (<150 MHz) performance, however the designer needs to be sure that the impedance presented at low frequency will not create an instability.

APPLICATIONS INFORMATION

Balanced Amplifier Circuit, 50Ω Input and 50Ω Output

This balanced amplifier circuit is a replica of the Test Circuit A. It is useful for single-ended 50Ω amplifier requirements and is surprisingly wideband. Using this balanced arrangement and the frequency appropriate baluns, one can achieve the intermodulation and harmonic performance listed in the AC Electrical Characteristics specifications of this data sheet. Besides its impressive intermodulation performance, the LTC6430-15 has impressive 2nd harmonic suppression as well. This makes it particularly well suited for multioctave applications where the 2nd harmonic cannot be filtered.

This balanced circuit example uses two Mini-Circuits 1:2 baluns. The baluns were chosen for their bandwidth and frequency options that utilize the same package footprint (see Table 2). A pair of these baluns, back-to-back has less than 1.5dB of loss, so the penalty for this level of performance is minimal. Any suitable 1:2 balun may be used to create a balanced amplifier with the LTC6430-15.

The optional stability network is only required when the balun's bandwidth reaches below 20MHz. It is included in the circuit as a comprehensive protection for any passive element placed at the LTC6430-15 input. Its performance degradation at low frequencies can be mitigated by increasing the 60pF capacitor's value.

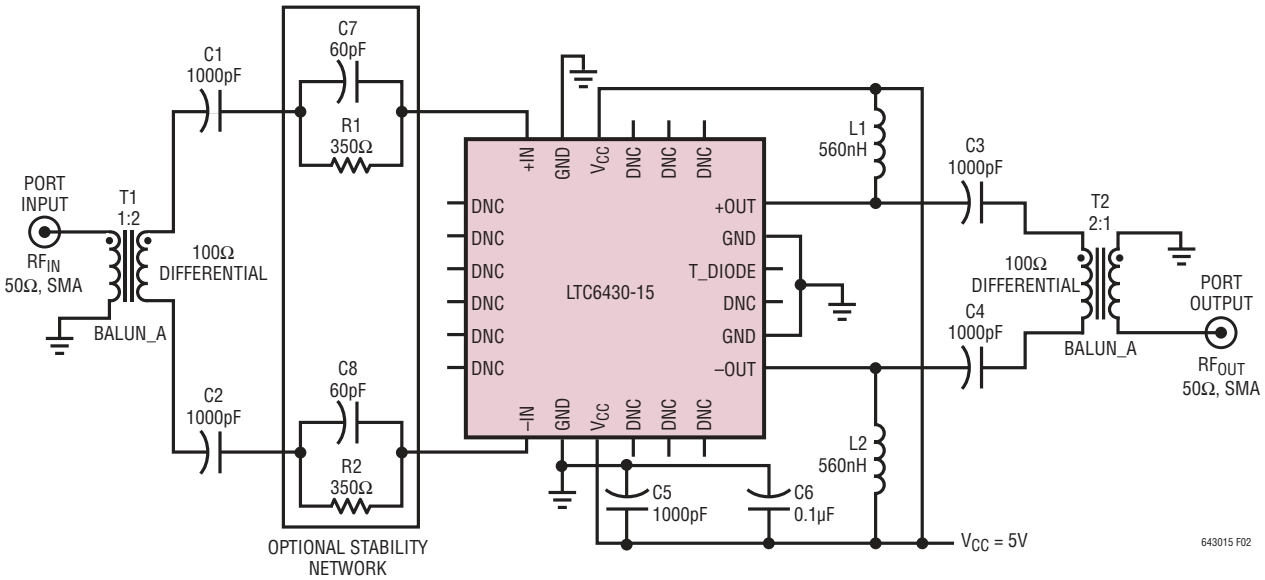
Demo Boards 1774A-A and 1774A-B implement this balanced amplifier circuit. It is shown in Figure 18 and Figure 19.

Please note that a number of DNC pins are connected on the evaluation board. These connections are not necessary for normal circuit operation.

The evaluation board also includes an optional back to back pair of baluns so that their losses may be measured. This allows the designer to de-embed the balun losses and more accurately predict the LTC6430-15 performance in a differential circuit.

Table 2. Target Frequency and Suggested 2:1 Balun

FREQUENCY BAND (MHz)	MODEL NUMBER	MANUFACTURER
50 to 300	ADT2-1T	Mini-Circuits www.minicircuits.com
300 to 400	ADT2-1P	
400 to 1300	ADTL2-18	



BALUN_A = ADT2-1T FOR 50MHz TO 300MHz
BALUN_A = ADT2-1P FOR 300MHz TO 400MHz
BALUN_A = ADTL2-18 FOR 400MHz TO 1300MHz
ALL ARE MINI-CIRCUITS CD542 FOOTPRINT

Figure 2. Balanced Amplifier Circuit, 50Ω Input and 50Ω Output

APPLICATIONS INFORMATION

Driving the LTC2158, 14-Bit, 310Msps ADC with 1.25GHz of Bandwidth

Boasting high linearity, low associated noise and wide bandwidth, the LTC6430-15 is well suited to drive high speed, high resolution ADCs with over a GHz of input bandwidth. To demonstrate its performance, the LTC6430-15 was used to drive an LTC2158 14-bit, 310Msps ADC with 1.25GHz of input bandwidth in an undersampling application. Typically, a filter is used between the ADC driver amplifier and ADC input to minimize the noise contribution from the amplifier. However, with the typical SNR of higher sample rate ADCs, the LTC6430-15 can drive them without any intervening filter, and with very little penalty in SNR. This system approach has the added benefit of allowing over two octaves of usable frequency range. The LTC6430-15 driving the LTC2158, as shown in the circuit in Figure 3, with band limiting provided only by the 1.25GHz input BW of the ADC, still produces 64.4dB SNR, and offers IM performance that varies little from 300MHz to 1GHz. At the lower end of this frequency range, the IM contribution of the ADC and amplifier are comparable, and the third-order IM products may be additive, or may see cancelation. At 1GHz input, the ADC is dominant in terms of IM and noise contribution, limited by internal clock jitter and high input signal amplitude. Table 3 shows noise and linearity performance. Example outputs at 380MHz and 1000MHz are shown in Figure 5, Figure 6, Figure 7, Figure 8 and Figure 9.

As a final display of the utility of this LTC6430-15/LTC2158 combination with real world signals, Figure 9 shows a wideband code division multiple access (WCDMA) signal was introduced to the LTC6430-15/LTC2158 combination at 830MHz. The output indicates an ACPR near 60dB calculated from the adjacent power on the upper side where the filter stop band suppresses the contribution from the generator. Please note that the adjacent channels on the lower side are not suppressed as they are within the passband of the filter.

The LTC6430-15 can directly drive the high speed ADC inputs and settles quickly. Most feedback amplifiers require protection from the sampling disturbances, the mixing products that result from direct sampling. This is in part due to the fact that unless the ADC input driving circuitry offers settling in less than one-half clock cycle, the ADC may not exhibit the expected linearity. If the ADC samples the recovery process of an amplifier it will be seen as distortion. If an amplifier exhibits envelope detection in

Table 3. LTC6430-15 and LTC2158 Combined Performance

Frequency (MHz)	Sample Rate (Msps)	IM3 (Low, Hi) (dBFS)	HD3 (3rd Harmonic) (dBc)	SFDR (dB)	SNR (dB)
380	310	(–98, –105)	–80.2	68.7	61.8
533	307.2		–82.2	79.3	59.4
656	291.8	(–94, –92)			
690	307.2	(–93, –92)	–80.8	70.5	58.2
842	307.2		–78	66.7	57.1
1000	307.2	(–83,–83)	–89.7	69.3	56.0

APPLICATIONS INFORMATION

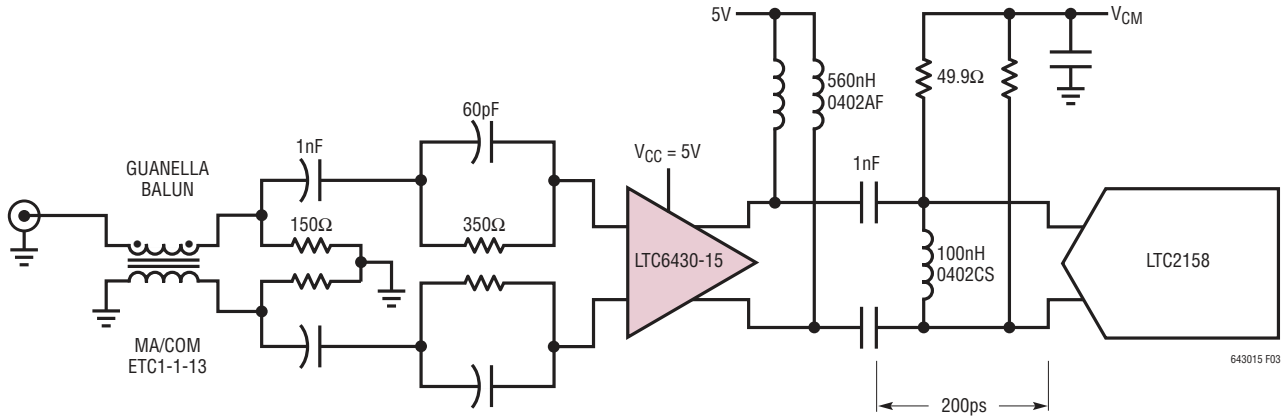


Figure 3. Wideband ADC Driver, LTC6430-15 Directly Driving the LTC2158 ADC

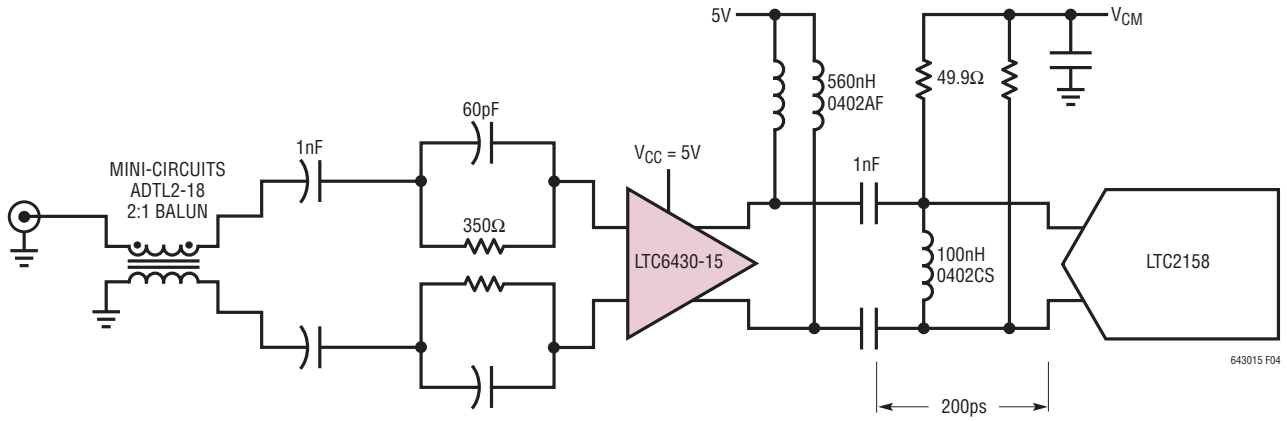


Figure 4. Wideband ADC Driver, LTC6430-15 Directly Driving the LTC2158 ADC—Alternative Using Mini Circuits 2:1 Balun

the presence of multi GHz mixing products, it will distort. A band limiting filter would provide suppression from those products beyond the capability of the amplifier, as well as limit the noise bandwidth, however the settling of the filter can be an issue. The LTC2158, at 310Msps only allows 1.5ns settling time for any driver that is disturbed by these transients.

This approach of removing the filter between the ADC and driver amplifier offers many advantages. It opens the opportunity to precede the amplifier with switchable bandpass filters, without any need to change the critical network between the drive amplifier and ADC. The transmission line distances shown in the schematic are part of the design, and are devised such that there are no impedance discontinuities, and therefore no reflections, in the distances between 75ps to 200ps from the ADC. End termination can be immediately prior to, or preferably after the ADC, and the amplifier should either be within the 75ps inner boundary, or outside the 200ps distance. Similarly, any shunt capacitor or resonator, including the large pads required by some inductors with more than a small fraction of 1pF, incorporated into a filter, should not be in this range of distances from the ADC where reflections will impair performance. Transformers with large

APPLICATIONS INFORMATION

pads should be avoided within these distances.

A 100nH shunt inductor at the ADC input approximates the complex conjugate of the ADC sampling circuit, and in doing so, improves power transfer and suppresses the low frequency difference products produced by direct sampling ADCs. If the entire frequency range from 300MHz to 1GHz were of interest, a 100nH inductor at the input is acceptable, but if interest is only in higher frequencies, performance would be better if the input inductor is reduced in value. If lower frequencies are of interest, a higher value up to some 200nH may be practical, but beyond that range the SRF of the inductor becomes an issue. As this inductor is placed at different distances either before or after the ADC inputs, the optimal value may change. In all cases, it should be within 50ps of the ADC inputs. End termination may be more than 200ps distant if after the ADC. If the end termination were perfect, it could be at any distance after the ADC. To terminate the input path after the ADC, place the termination resistors on the back of the PCB. If the input signal path is buried or on the back of the PCB, termination resistors should be placed on the top of the PCB to properly terminate after the ADC.

Although the ADC is isolated by a driver amplifier, care must be taken when filtering at the amplifier input. Much like MESFETs, high frequency mixing products are handled well by the LTC6430. However, if there is no band limiting after the LTC6430, these mixing products, reduced by reverse isolation but subsequently reflected from a filter prior to the LTC6430 and reamplified, can cause distortion. In such cases, the network will then be sensitive to transmission line lengths and impedance characteristics of the filter prior to the LTC6430. Diplexers or absorptive filters can produce more robust results. An absorptive filter or diplexer-like structure after the amplifier reduces the sensitivity to the network prior to the amplifier, but the same constraints previously outlined apply to the filter.

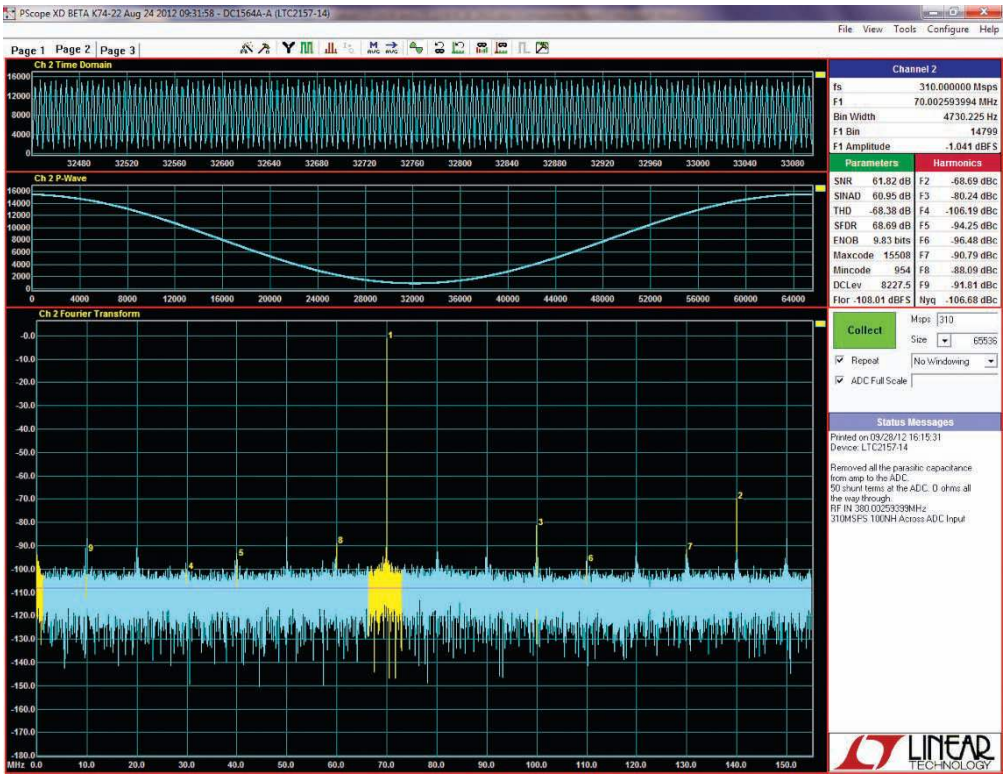


Figure 5. ADC Output: 1-Tone Test at 380MHz with 310Msps Sampling Rate Undersampled in the Third Nyquist Zone

APPLICATIONS INFORMATION

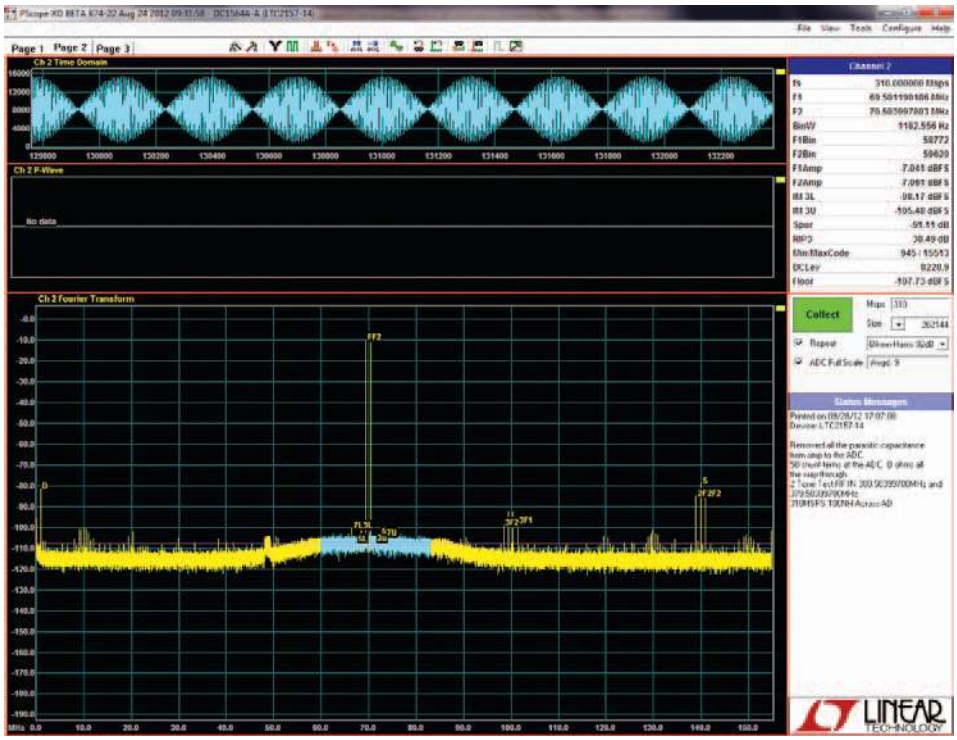


Figure 6. ADC Output: 2-Tone Test at 380MHz with 310Msps Sampling Rate Undersampled in the Third Nyquist Zone

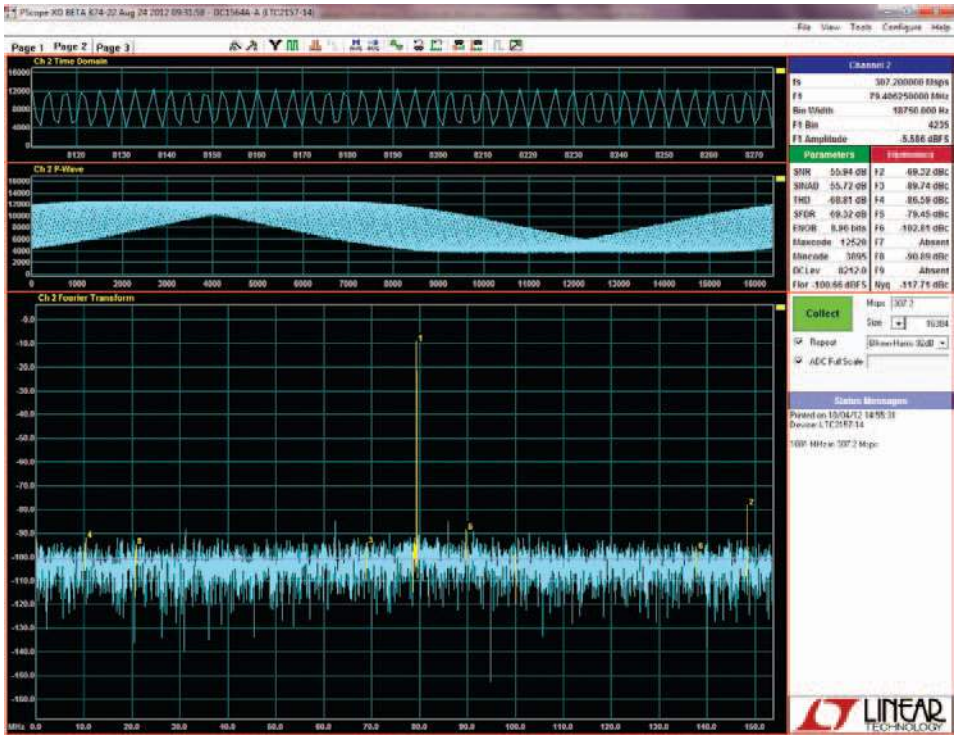


Figure 7. ADC Output: 1-Tone Test at 1000MHz with 307.2Msps Sampling Rate Undersampled in the Seventh Nyquist Zone

APPLICATIONS INFORMATION

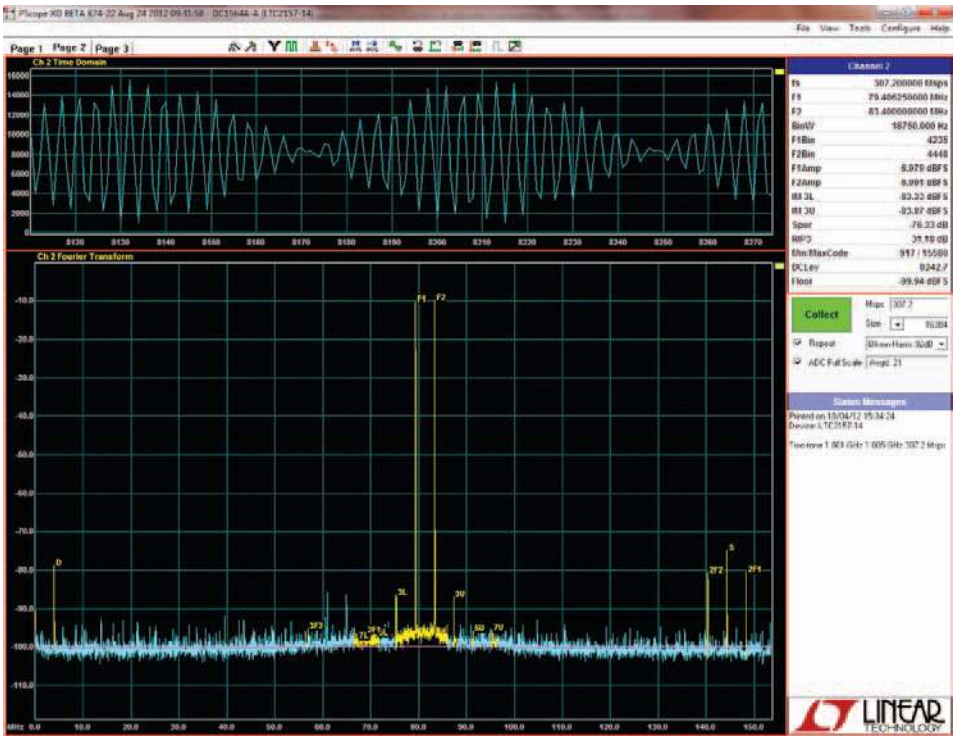


Figure 8. ADC Output: 2-Tone Test at 1000MHz with 307.2Msps Sampling Rate Undersampled in the Seventh Nyquist Zone

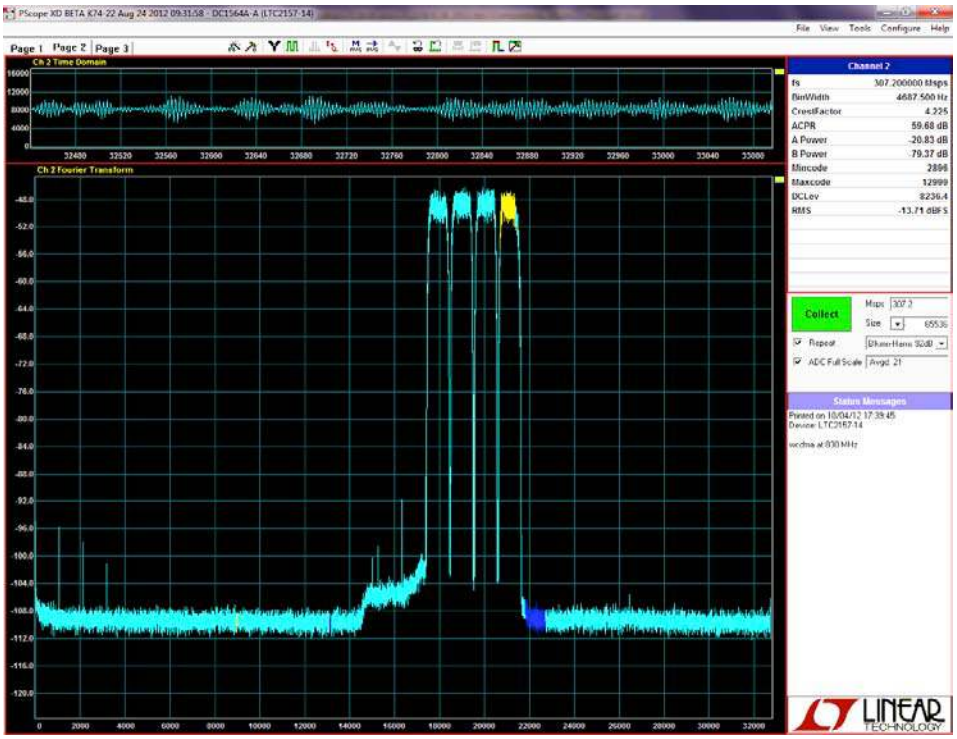


Figure 9. ADC Output: WCDMA Test at 830MHz IF Using 30MHz Wide Diplexer Prior to the LTC6430-15

APPLICATIONS INFORMATION

50MHz to 1000MHz CATV Push-Pull Amplifier: 75Ω Input and 75Ω Output

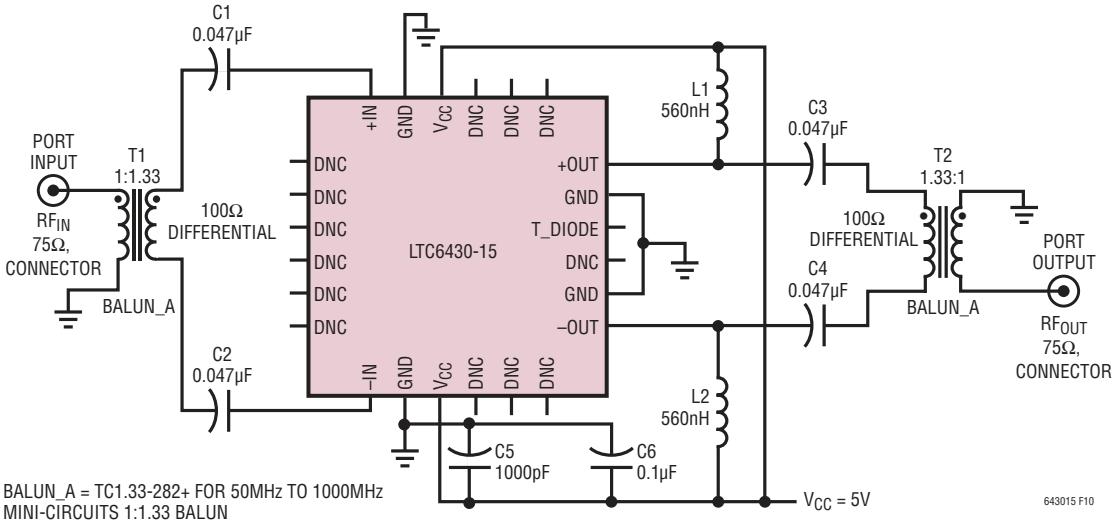


Figure 10. CATV Amplifier: 75Ω Input and 75Ω Output

Wide bandwidth, excellent linearity and low output noise makes the LTC6430-15 an exceptional candidate for CATV amplifier applications.

As expected, the LTC6430-15 works well in a push-pull circuit to cover the entire 40MHz to 1000MHz CATV band. Using readily available SMT baluns, the LTC6430-15 offers high linearity and low noise across the whole CATV band. Remarkably, this performance is achieved with only 800mW of power at 5V. Its low power dissipation greatly reduces the heat sinking requirements relative to traditional "block" CATV amplifiers.

The native LTC6430-15 device is well matched to 100Ω differential impedance at both the input and the output. Therefore, we can employ 1:1.33 surface mount (SMT) baluns to transform its native 100Ω impedance to the standard 75Ω CATV impedance, while retaining all the exceptional characteristics of the LTC6430-15. In addition, the balun's excellent phase balance and the 2nd order linearity of the LTC6430-15 combine to further suppress 2nd order products across the entire CATV band. As with any wide bandwidth application, care must be taken when selecting a choke. An SMT wire wound ferrite core inductor was chosen for its low series resistance, high self resonant frequency (SRF) and compact size. An input stability network is not required for this application as the balun presents a low impedance to the LTC6430-15's input at low frequencies. Our resulting push-pull CATV amplifier circuit is simple, compact, completely SMT and extremely power efficient.

The LTC6430-15 push-pull circuit has 14.1dB of gain with ±0.4dB of flatness across the entire 50MHz to 1000MHz band. It sports an OIP3 of 46dBm and a noise figure of only 4.5dB. The CTB and CSO measurements have not been taken as of this writing.

These characteristics make the LTC6430-15 an ideal amplifier for head-end cable modem applications or CATV distribution amplifiers. The circuit is shown in Figure 10, with 75Ω "F" connectors at both input and output. The evaluation board may be loaded with either 75Ω "F" connectors, or 75Ω BNC connectors, depending on the users preference. Please note that the use of substandard connectors can limit usable bandwidth of the circuit.

APPLICATIONS INFORMATION

50MHz to 1000MHz CATV Push-Pull Amplifier: 75Ω Input and 75Ω Output

Figure 11. CATV Circuit, Input and Output Return Loss vs Frequency

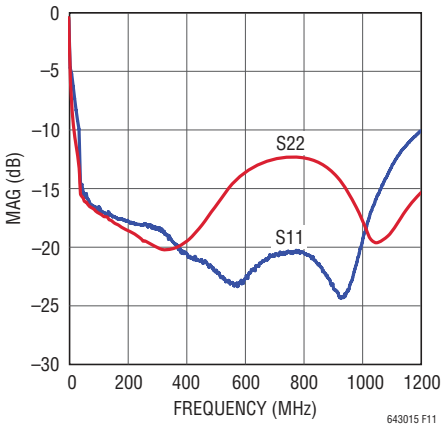


Figure 12. CATV Amplifier Circuit, Gain (S21) vs Frequency

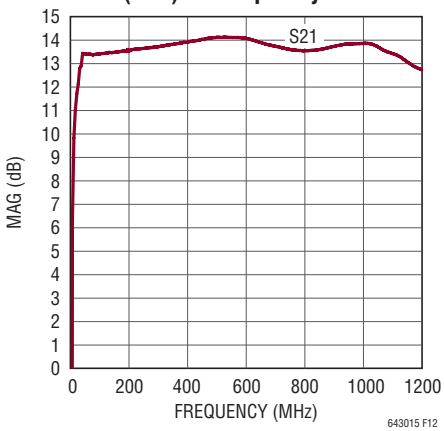


Figure 13. CATV Amplifier Circuit, Noise Figure vs Frequency

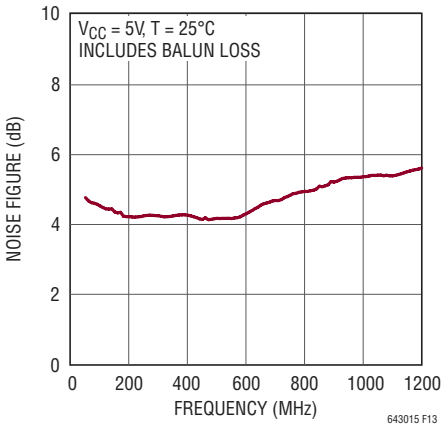


Figure 14. CATV Amplifier Circuit, OIP3 vs Frequency

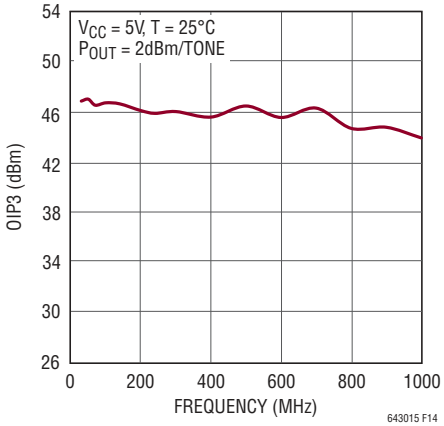
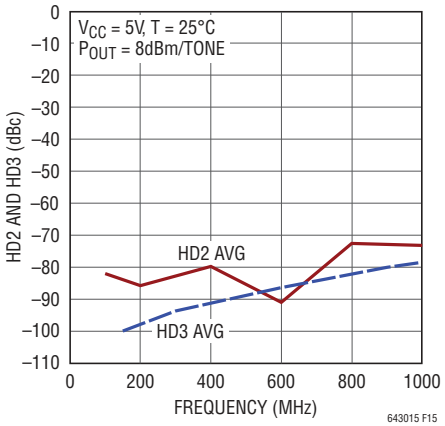


Figure 15. HD2 and HD3 Products vs Frequency



APPLICATIONS INFORMATION

50MHz to 1000MHz CATV Push-Pull Amplifier: 75Ω Input and 75Ω Output

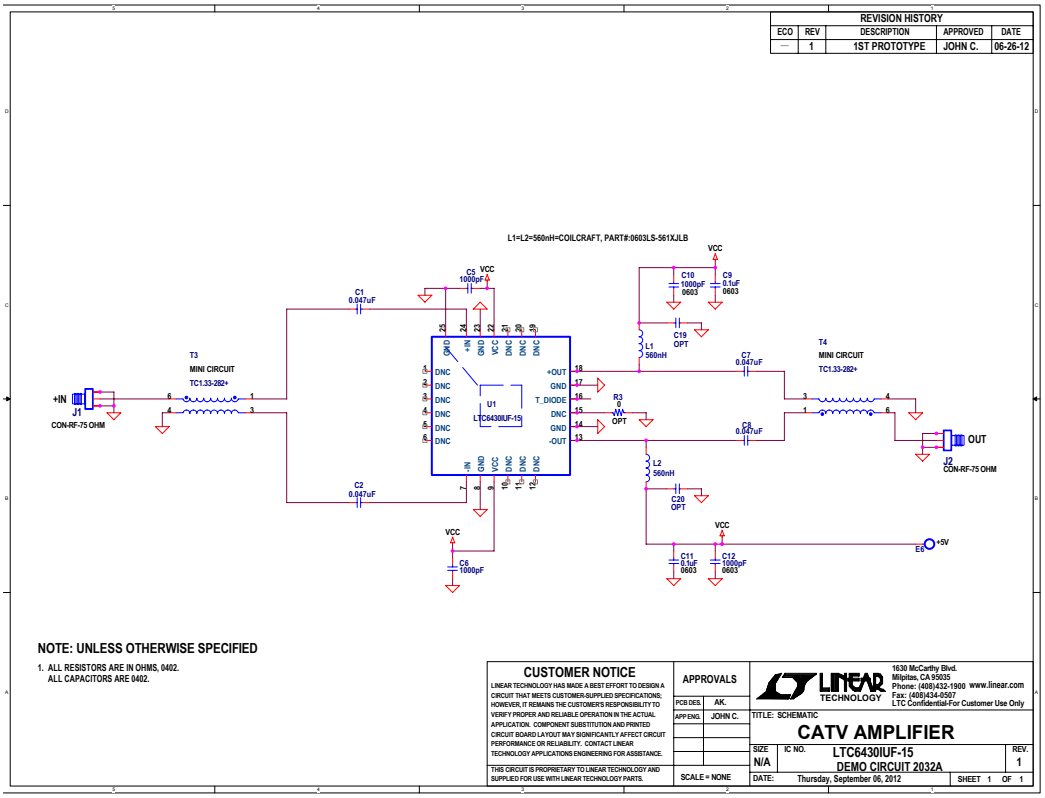


Figure 16. LTC6430-15 CATV Circuit Schematic

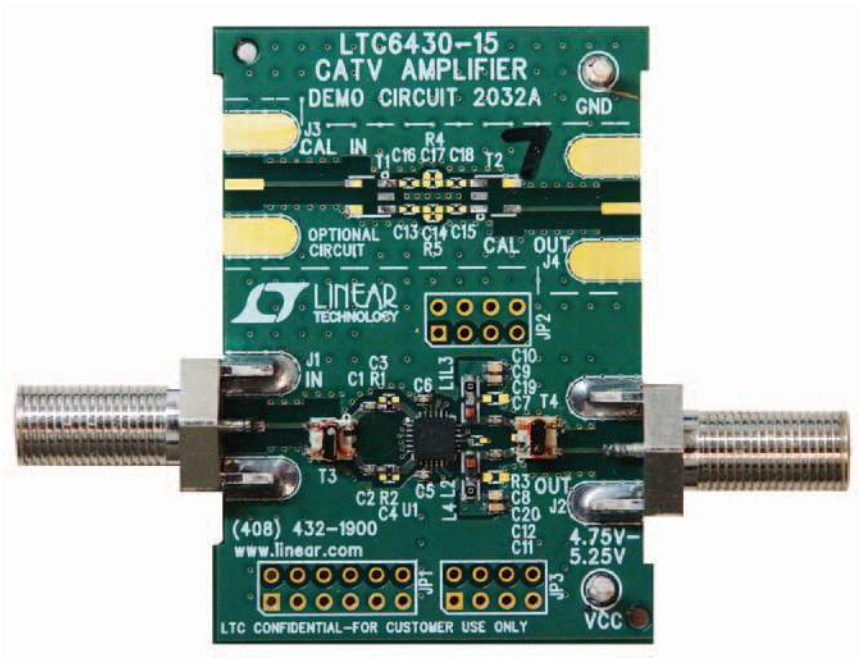
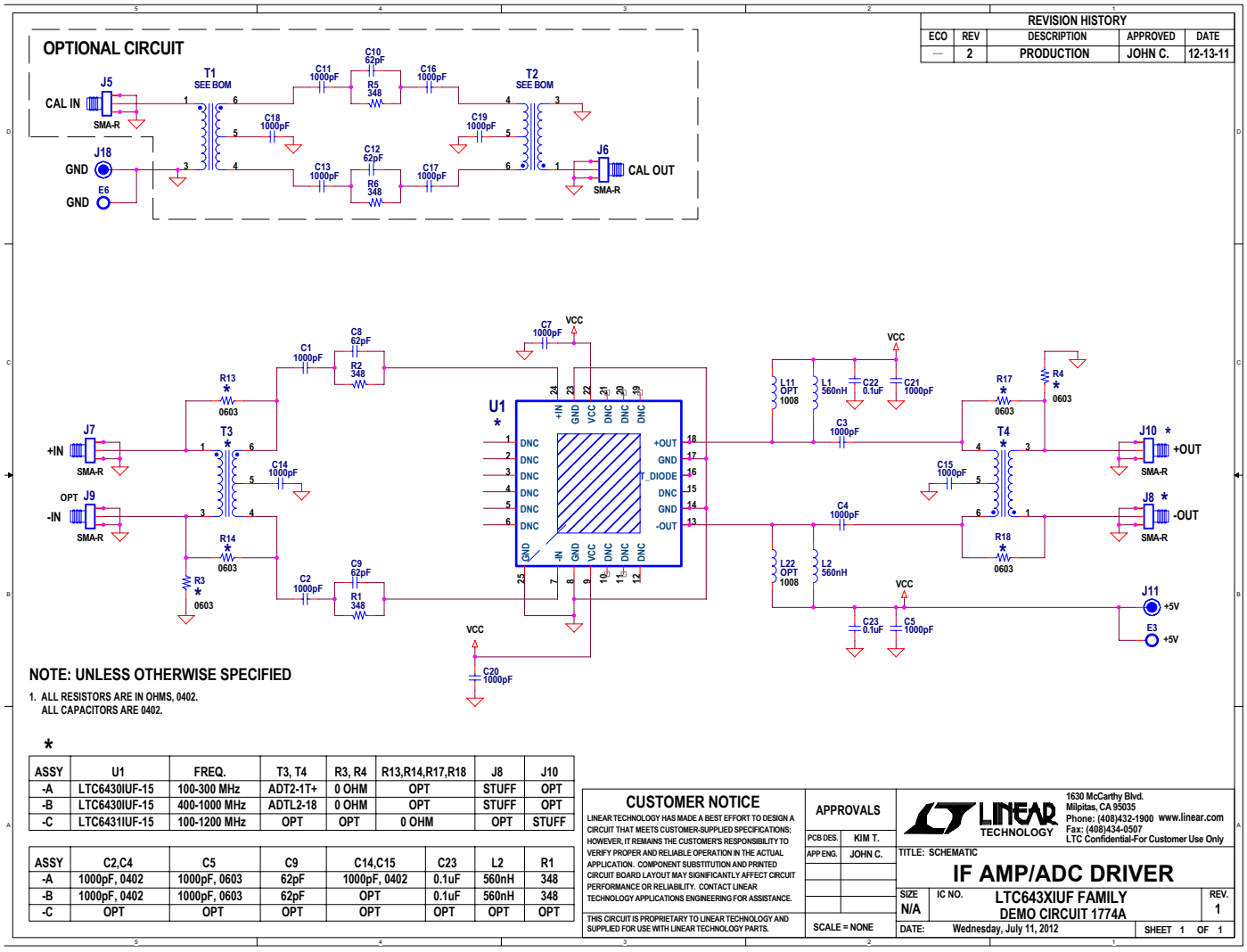


Figure 17. LTC6430-15 CATV Evaluation Board

APPLICATIONS INFORMATION



ASSY	U1	FREQ.	T3, T4	R3, R4	R13,R14,R17,R18	J8	J10
-A	LTC6430IUF-15	100-300 MHz	ADT2-1T+	0 OHM	OPT	STUFF	OPT
-B	LTC6430IUF-15	400-1000 MHz	ADTL2-18	0 OHM	OPT	STUFF	OPT
-C	LTC6431IUF-15	100-1200 MHz	OPT	OPT	0 OHM	OPT	STUFF

ASSY	C2,C4	C5	C9	C14,C15	C23	L2	R1
-A	1000pF, 0402	1000pF, 0603	62pF	1000pF, 0402	0.1uF	560nH	348
-B	1000pF, 0402	1000pF, 0603	62pF	OPT	0.1uF	560nH	348
-C	OPT	OPT	OPT	OPT	OPT	OPT	OPT

Figure 18. Demo Board 1774A Schematic

APPLICATIONS INFORMATION

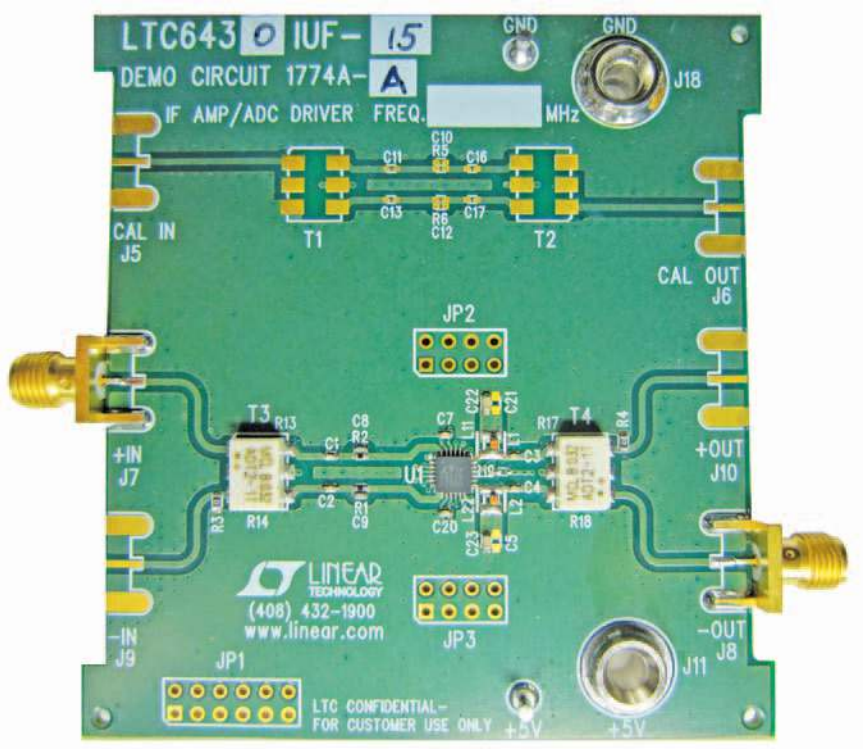


Figure 19. Demo Board 1774A PCB

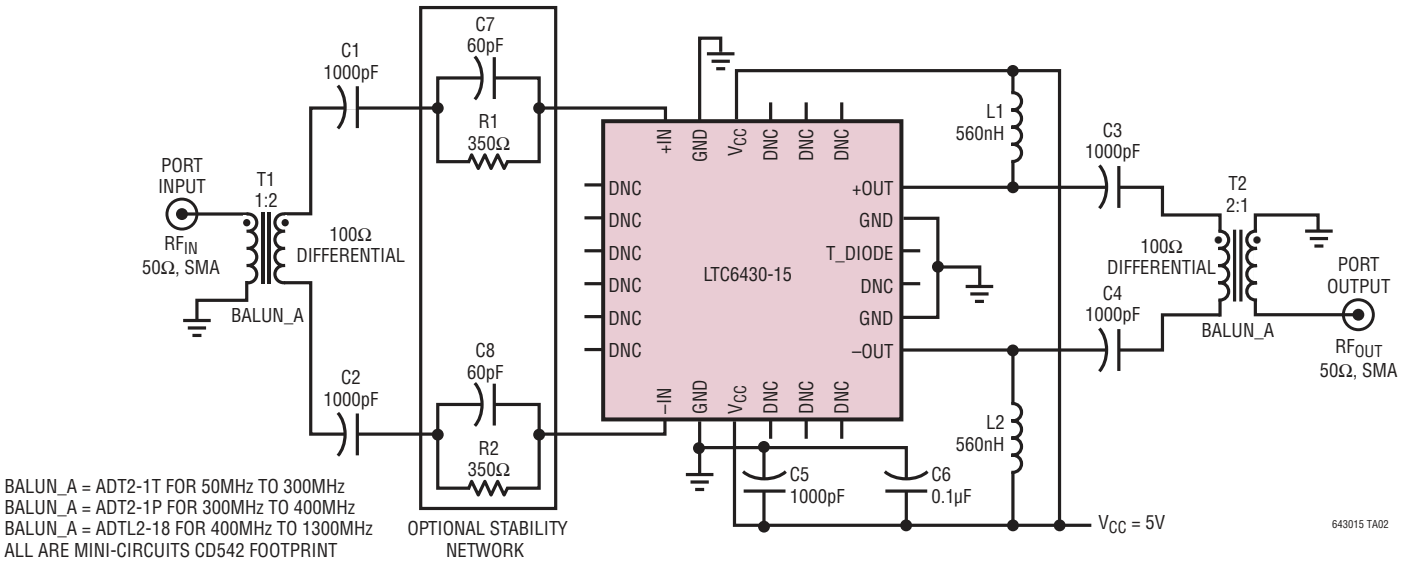
DIFFERENTIAL S PARAMETERS

5V, Z_{DIFF} = 100Ω, T = 25°C, De-Embedded to Package Pins,
DD: Differential In to Differential Out

FREQUENCY (MHz)	$S11_{DD}$ (Mag)	$S11_{DD}$ (Ph)	$S21_{DD}$ (Mag)	$S21_{DD}$ (Ph)	$S12_{DD}$ (Mag)	$S12_{DD}$ (Ph)	$S22_{DD}$ (Mag)	$S22_{DD}$ (Ph)	GTU (Max)	STABILITY (K)
23.5	–14.79	–83.75	15.59	166.68	–18.75	9.35	–14.74	–66.63	15.88	0.99
83.5	–22.74	–107.27	15.16	170.23	–18.67	–3.01	–22.99	–48.57	15.21	1.07
143	–23.62	–121.45	15.14	167.23	–18.74	–8.44	–24.91	–37.10	15.18	1.08
203	–23.66	–133.07	15.13	163.30	–18.81	–12.91	–25.64	–33.28	15.16	1.08
263	–22.92	–142.28	15.11	159.19	–18.85	–17.06	–26.20	–29.50	15.15	1.08
323	–22.64	–151.62	15.09	154.85	–18.93	–21.05	–26.12	–31.14	15.13	1.09
383	–21.56	–157.35	15.06	150.64	–18.97	–25.11	–25.59	–33.23	15.11	1.09
443	–20.69	–162.14	15.04	146.31	–19.05	–29.05	–24.66	–32.63	15.09	1.09
503	–19.70	–166.01	15.00	142.01	–19.12	–32.90	–23.61	–32.94	15.07	1.10
563	–18.85	–170.61	14.98	137.67	–19.21	–36.89	–22.75	–33.85	15.06	1.10
623	–18.10	–175.10	14.94	133.32	–19.28	–40.59	–21.89	–36.24	15.04	1.10
683	–17.59	–179.62	14.91	128.98	–19.37	–44.51	–21.10	–40.64	15.02	1.10
743	–17.07	176.30	14.88	124.59	–19.46	–48.37	–20.20	–45.87	15.01	1.10
803	–16.67	171.92	14.82	120.28	–19.57	–52.05	–19.19	–50.45	14.97	1.11
863	–16.24	168.04	14.80	115.83	–19.67	–56.02	–18.27	–55.85	14.97	1.11
923	–15.80	163.82	14.75	111.55	–19.82	–59.92	–17.40	–60.20	14.94	1.11
983	–15.42	160.15	14.72	107.07	–19.95	–63.56	–16.63	–65.14	14.94	1.12
1040	–15.03	156.56	14.67	102.65	–20.06	–67.32	–15.88	–70.73	14.92	1.12
1100	–14.74	153.02	14.62	98.25	–20.21	–71.16	–15.22	–76.33	14.91	1.12
1160	–14.47	149.97	14.59	93.56	–20.36	–74.78	–14.53	–82.33	14.90	1.13
1220	–14.22	147.29	14.52	89.20	–20.49	–78.43	–13.84	–88.47	14.87	1.13
1280	–13.96	144.60	14.50	84.43	–20.64	–82.16	–13.21	–94.61	14.89	1.13
1340	–13.71	142.54	14.40	79.82	–20.82	–85.95	–12.56	–100.71	14.84	1.14
1400	–13.46	140.50	14.36	75.06	–20.97	–89.58	–11.95	–106.83	14.84	1.14
1460	–13.21	138.25	14.25	70.23	–21.14	–93.14	–11.38	–113.18	14.79	1.14
1520	–12.93	136.52	14.12	65.45	–21.31	–96.91	–10.84	–119.34	14.72	1.15
1580	–12.69	134.85	14.00	60.83	–21.46	–100.58	–10.38	–125.57	14.65	1.16
1640	–12.44	132.91	13.83	55.62	–21.67	–104.18	–9.88	–131.85	14.56	1.17
1700	–12.08	130.90	13.61	51.75	–21.85	–107.65	–9.44	–138.66	14.41	1.18
1760	–11.83	128.75	13.48	46.46	–22.08	–111.59	–9.05	–145.10	14.35	1.20
1820	–11.59	126.05	13.15	42.83	–22.27	–114.99	–8.66	–151.89	14.10	1.23
1880	–11.26	123.96	13.04	38.17	–22.43	–118.70	–8.39	–158.77	14.05	1.23
1940	–11.04	121.35	12.74	34.51	–22.77	–122.54	–8.09	–165.44	13.83	1.28
2000	–10.77	118.82	12.52	30.70	–22.94	–125.55	–7.86	–172.29	13.67	1.31
2060	–10.50	116.06	12.44	27.13	–23.20	–129.50	–7.71	–178.95	13.66	1.33
2120	–10.25	113.21	12.13	23.32	–23.47	–132.67	–7.50	174.30	13.41	1.38
2180	–9.95	110.44	12.17	20.08	–23.67	–136.37	–7.38	167.79	13.51	1.38
2240	–9.66	107.44	11.95	15.44	–23.98	–139.65	–7.21	161.17	13.37	1.42
2300	–9.43	103.84	11.86	11.58	–24.24	–143.03	–7.10	154.86	13.33	1.45

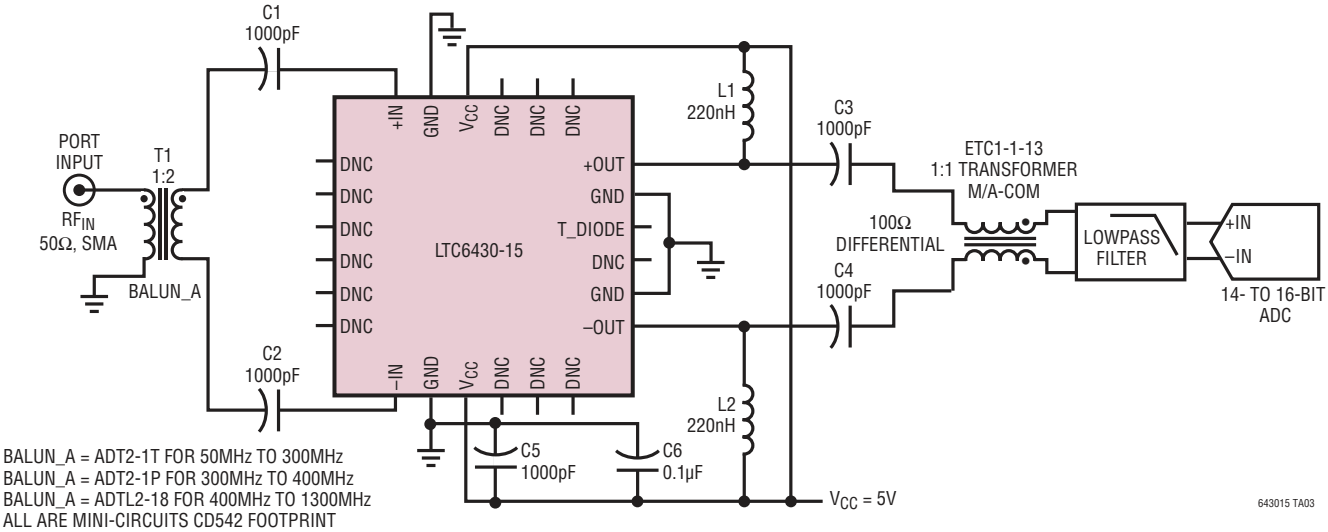
TYPICAL APPLICATIONS

50Ω Input/Output Balanced Amplifier



BALUN_A = ADT2-1T FOR 50MHz TO 300MHz
BALUN_A = ADT2-1P FOR 300MHz TO 400MHz
BALUN_A = ADTL2-18 FOR 400MHz TO 1300MHz
ALL ARE MINI-CIRCUITS CD542 FOOTPRINT

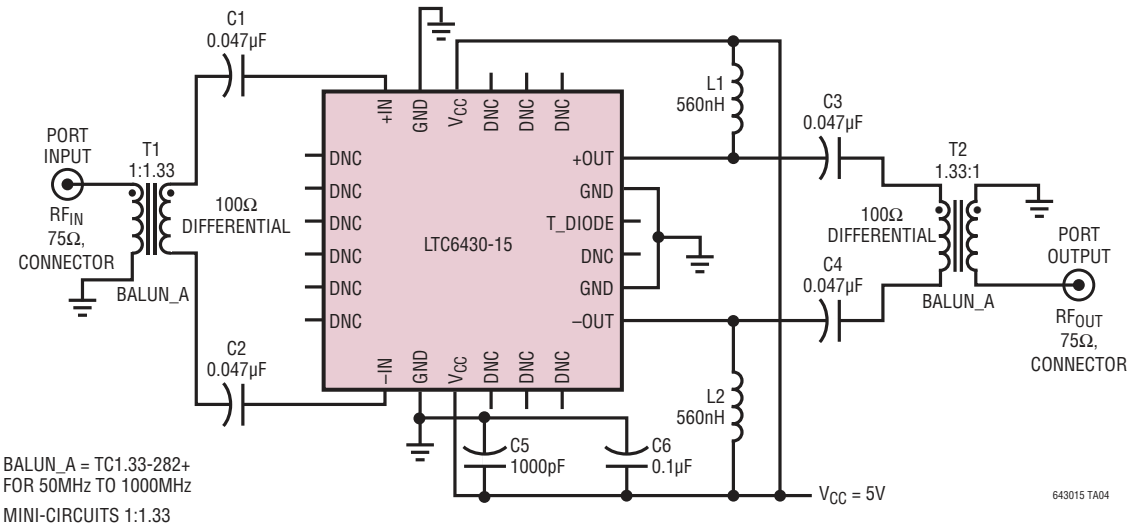
16-Bit ADC Driver



BALUN_A = ADT2-1T FOR 50MHz TO 300MHz
BALUN_A = ADT2-1P FOR 300MHz TO 400MHz
BALUN_A = ADTL2-18 FOR 400MHz TO 1300MHz
ALL ARE MINI-CIRCUITS CD542 FOOTPRINT

TYPICAL APPLICATIONS

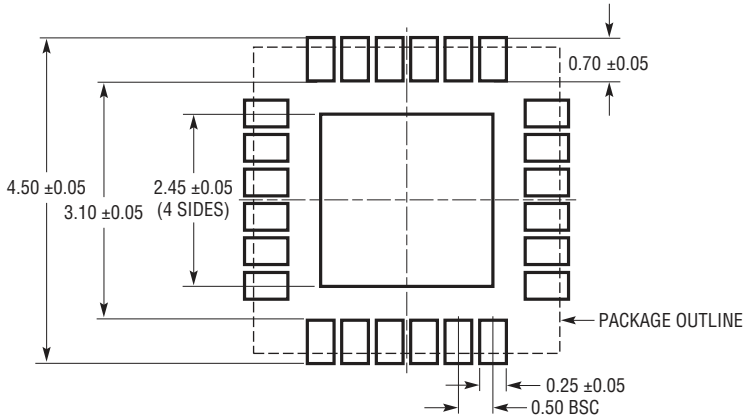
75Ω 50MHz to 1000MHz CATV Amplifier



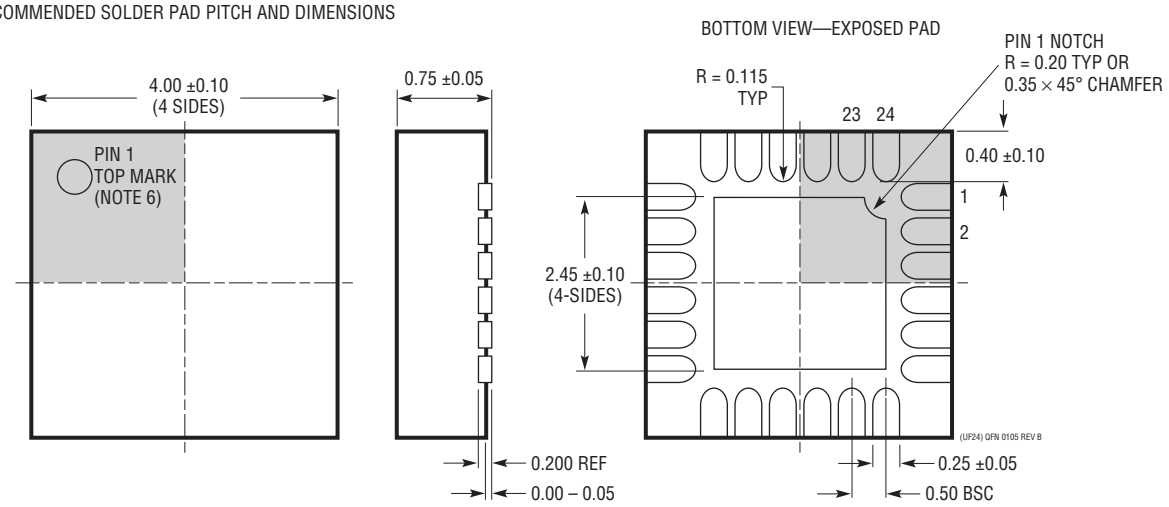
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



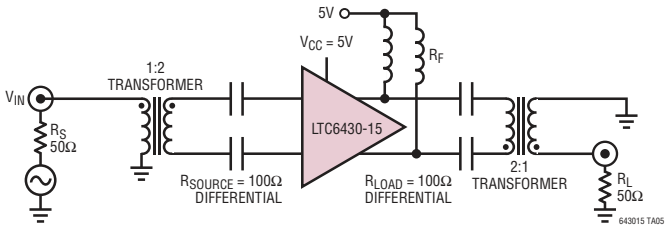
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Wideband Balanced Amplifier



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Fixed Gain IF Amplifiers/ADC Drivers		
LTC6431-15	50Ω Gain Block IF Amplifier	Single-Ended Version of LTC6431-15, 15.5dB Gain, 47dBm OIP3 at 240MHz into a 50Ω Load
LTC6417	1.6GHz Low Noise High Linearity Differential Buffer/ ADC Driver	OIP3 = 41dBm at 300MHz, Can Drive 50W Differential Output High Speed Voltage Clamping Protects Subsequent Circuitry
LTC6400-8/LTC6400-14/ LTC6400-20/LTC6400-26	1.8GHz Low Noise, Low Distortion Differential ADC Drivers	–71dBc IM3 at 240MHz $2V_{P-P}$ Composite, I_S = 90mA, A_V = 8dB, 14dB, 20dB, 26dB
LTC6401-8/LTC6401-14/ LTC6401-20/LTC6401-26	1.3GHz Low Noise, Low Distortion Differential ADC Drivers	–74dBc IM3 at 140MHz $2V_{P-P}$ Composite, I_S = 50mA, A_V = 8dB, 14dB, 20dB, 26dB
LT6402-6/LT6402-12/ LT6402-20	300MHz Differential Amplifier/ADC Drivers	–71dBc IM3 at 20MHz $2V_{P-P}$ Composite, A_V = 6dB, 12dB, 20dB
LTC6410-6	1.4GHz Differential IF Amplifier with Configurable Input Impedance	OIP3 = 36dBm at 70MHz, Flexible Interface to Mixer IF Port
LTC6416	2GHz, 16-Bit Differential ADC Buffer	–72dBc IM2 at 300MHz $2V_{P-P}$ Composite, I_S = 42mA, eN = 2.8nV/$\sqrt{Hz}$, A_V = 0dB, 300MHz } 0.1dB Bandwidth
LTC6420-20	Dual 1.8GHz Low Noise, Low Distortion Differential ADC Drivers	Dual Version of the LTC6400-20, A_V = 20dB
Variable Gain IF Amplifiers/ADC Drivers		
LT6412	800MHz, 31dB Range Analog-Controlled VGA	OIP3 = 35dBm at 240MHz, Continuously Adjustable Gain Control
Baseband Differential Amplifiers		
LTC6409	1.1nV/$\sqrt{Hz}$ Single Supply Differential Amplifier/ADC Driver	88dB SFDR at 100MHz, AC- or DC-Coupled Inputs
LTC6406	3GHz Rail-to-Rail Input Differential Amplifier/ ADC Driver	–65dBc IM3 at 50MHz $2V_{P-P}$ Composite, Rail-to-Rail Inputs, eN = 1.6nV/$\sqrt{Hz}$, 18mA
LTC6404-1/LTC6404-2	Low Noise Rail-to-Rail Output Differential Amplifier/ ADC Driver	16-Bit SNR, SFDR at 10MHz, Rail-to-Rail Outputs, eN = 1.5nV/$\sqrt{Hz}$, LTC6404-1 Is Unity-Gain Stable, LTC6404-2 Is Gain-of-Two Stable
LTC6403-1	Low Noise Rail-to-Rail Output Differential Amplifier/ ADC Driver	16-Bit SNR, SFDR at 3MHz, Rail-to-Rail Outputs, eN = 2.8nV/$\sqrt{Hz}$
High Speed ADCs		
LTC2208/LTC2209	16-Bit, 13Msps/160Msps ADC	74dBFS Noise Floor, SFDR > 89dB at 140MHz, $2.25V_{P-P}$ Input
LTC2259-16	16-Bit, 80Msps ADC, Ultralow Power	72dBFS Noise Floor, SFDR > 82dB at 140MHz, $2.00V_{P-P}$ Input
LTC2160-14/LTC2161-14/ LTC2162-14	14-bit, 25Msps/40Msps/60Msps ADC Low Power	76.2 dBFS Noise Floor, SFDR > 84dB at 140MHz, $2.00V_{P-P}$ Input
LTC2155-14/LTC2156-14/ LTC2157-14/LTC2158-14	14-bit, 170Msps/210Msps/250Msps/310Msps ADC 2-Channel	69dBFS Noise Floor, SFDR > 80dB at 140MHz, $1.50V_{P-P}$ Input, >1GHz Input BW
LTC2216	16-Bit, 80Msps ADC	79dBFS Noise Floor, SFDR > 91dB at 140MHz, $75V_{P-P}$ Input

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