

## Automotive 2.5 A Peak High Output Current SiC MOSFET and IGBT Gate Drive Optocoupler with Rail-to-Rail Output Voltage in Stretched SO-8

### Data Sheet

#### Description

Avago Technologies' 2.5 Amp Automotive R2Coupler® Gate Drive Optocoupler contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. The ACPL-K33T features fast propagation delay and tight timing skew, is ideally designed for driving SiC MOSFET and IGBTs used in AC-DC and DC-DC converters. The high operating voltage range of the output stage provides the drive voltages required by gate-controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving SiC MOSFET and IGBTs at high frequency for high efficiency conversion.

Avago R2Coupler isolation products provide reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high-temperature industrial applications.

**CAUTION** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

#### Features

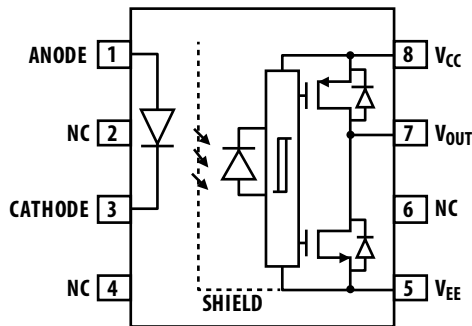
- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: -40 °C to +125 °C
- Peak output current: 2.0 A min.
- Rail-to-rail output voltage
- Propagation delay: 120 ns max.
- Dead time distortion: +50 ns/-40 ns
- LED input threshold current hysteresis
- Common Mode Rejection (CMR): 50 kV/μs min. at VCM = 1500 V
- Low supply current allow bootstrap half-bridge topology: ICC = 4.2 mA max.
- Under Voltage Lock-Out (UVLO) protection with hysteresis for SiC MOSFET and IGBT
- Wide operating VCC range: 15 V to 30 V
- Safety Approvals:
  - UL Recognized 5000 VRMS for 1 min
  - CSA
  - IEC/EN/DIN EN 60747-5-5 VIORM = 1140 Vpeak

#### Applications

- Hybrid Power Train DC/DC Converter
- EV/PHEV Charger
- Automotive Isolated IGBT Gate Drive
- AC and Brushless DC Motor Drives

## Functional Diagram

Figure 1 ACPL-K33T Functional Diagram



**NOTE** Minimum 1  $\mu\text{F}$  bypass capacitor must be connected between pins  $V_{CC}$  and  $V_{EE}$ .

## Truth Table

LED	$V_{CC} - V_{EE}$	$V_{OUT}$
OFF	0 – 30 V	LOW
ON	$< V_{UVLO-}$	LOW
ON	$> V_{UVLO+}$	HIGH

## Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	UL 5000 Vrms/1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-K33T	-000E	Stretched SO-8	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

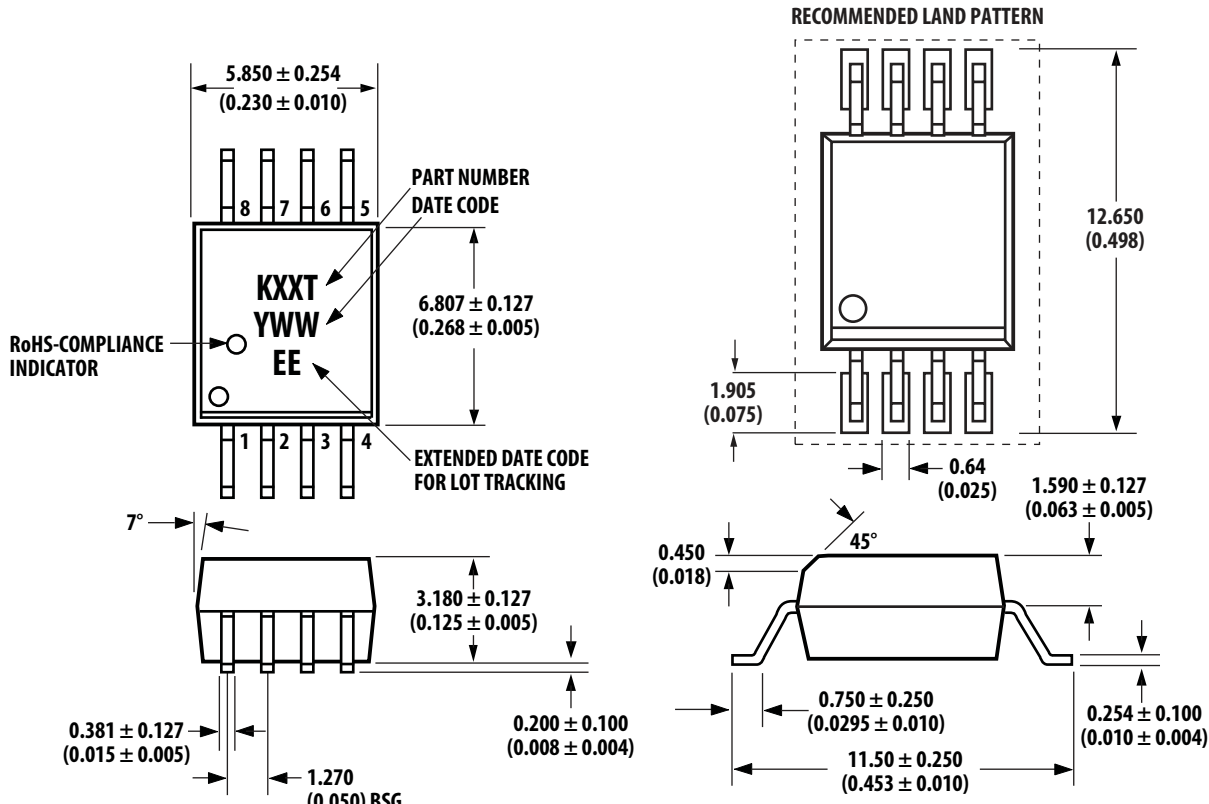
To order, choose a part number from the Part Number column and combine it with the desired option from the Option column to form an order entry.

Example 1:

ACPL-K33T-560E to order product of SSO-8 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and is RoHS compliant.

Option data sheets are available. Contact your Avago sales representative or authorized distributor for information.

## Package Outline Drawings (Stretched SO-8)



Dimensions in millimeters (inches).

- Notes:
1. Lead coplanarity = 0.1 mm (0.004 inches).
  2. Floating lead protrusion = 0.25 mm (10 mils) max.

### Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

**NOTE** Non-halide flux should be used.

### Regulatory Information

The ACPL-K33T is approved by the following organizations:

UL	UL 1577, component recognition program up to $V_{ISO} = 5 \text{ kV}_{RMS}$
CSA	CSA Component Acceptance Notice #5
IEC/EN/DIN EN 60747-5-5	IEC/EN/DIN EN 60747-5-5

## IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristic (Option 060 and 560 only)

Description	Symbol	Option 060 and 560	Units
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage < 600 V <sub>RMS</sub> for rated mains voltage < 1000 V <sub>RMS</sub>		I - IV I - III	
Climatic Classification <sup>a</sup>		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V <sub>IORM</sub>	1140	V <sub>peak</sub>
Input to Output Test Voltage, Method b V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with t <sub>m</sub> =1 sec, Partial discharge < 5 pC	V <sub>PR</sub>	2137	V <sub>peak</sub>
Input to Output Test Voltage, Method a V <sub>IORM</sub> × 1.6 = V <sub>PR</sub> , Type and Sample Test with t <sub>m</sub> =10 sec, Partial discharge < 5 pC	V <sub>PR</sub>	1824	V <sub>peak</sub>
Highest Allowable Overvoltage (Transient Overvoltage t <sub>ini</sub> = 60 sec)	V <sub>IOTM</sub>	8000	V <sub>peak</sub>
Safety-limiting values – maximum values allowed in the event of a failure Case Temperature Input Current Output Power	T <sub>s</sub> I <sub>s, INPut</sub> P <sub>s, OUTPUT</sub>	175 230 600	°C mA mW
Insulation Resistance at T <sub>y</sub> , V <sub>IO</sub> =500 V	R <sub>s</sub>	> 10 <sup>9</sup>	Ω

- a. Climatic classification denotes <Minimum ambient temperature of operation>/<Maximum ambient temperature of operation>/<Number of days of the damp heat, steady state test>.

## Insulation and Safety-Related Specifications

Parameter	Symbol	ACPL-K33T	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (DIN VDE0109)		IIIa		Material Group (DIN VDE 0109)

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	$T_S$	-55	150	°C
Operating Temperature	$T_A$	-40	125	°C
IC Junction Temperature <sup>a</sup>	$T_J$		150	°C
Average Input Current	$I_{F(AVG)}$		20	mA
Peak Input Current (50% duty cycle, < 1 ms pulse width)	$I_{F(PEAK)}$		40	mA
Peak Transient Input Current (<1 $\mu$ s pulse width, 300 pps)	$I_{F(TRAN)}$		1	A
Reverse Input Voltage	$V_R$		6	V
“High” Peak Output Current <sup>b</sup>	$I_{OH(PEAK)}$		2.5	A
“Low” Peak Output Current <sup>b</sup>	$I_{OL(PEAK)}$		2.5	A
Total Output Supply Voltage	$(V_{CC} - V_{EE})$	0	35	V
Output Voltage	$V_{O(PEAK)}$	-0.5	$V_{CC}$	V
Output IC Power Dissipation <sup>c</sup>	$P_O$		500	mW
Total Power Dissipation <sup>a</sup>	$P_T$		550	mW

- a. Total power dissipation is derated linearly above 110 °C free-air temperature at a rate of 13 mW/°C. The maximum LED and IC junction temperature should not exceed 150 °C.
- b. Maximum pulse width = 100 ns, Duty cycle = 2%.
- c. Derate linearly above 110 °C free-air temperature at a rate of 13 mW/°C. Refer to Figure 2 from Output IC Power Dissipation Derating Chart.

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Operating Temperature	$T_A$	-40	125	°C
Output Supply Voltage	$(V_{CC} - V_{EE})$	15	30	V
Input Current (ON)	$I_{F(ON)}$	7	13	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-5.5	0.8	V

## Electrical Specifications (DC)

Unless otherwise noted, all Minimum/Maximum specifications are at Recommended Operating Conditions. All typical values are at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 15\text{ V}$ ,  $V_{EE} = \text{Ground}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.
High Level Peak Output Current	$I_{OH}$		-3.5	-2.0	A	$V_{CC} - V_O = 15\text{ V}$	3
Low Level Peak Output Current	$I_{OL}$	2.0	4		A	$V_O - V_{EE} = 15\text{ V}$	4
High Output Transistor RDS(ON) <sup>a</sup>	$R_{DS,OH}$		2.2	4.0	$\Omega$	$I_{OH} = -2.0\text{ A}$	
Low Output Transistor RDS(ON) <sup>a</sup>	$R_{DS,OL}$		1.0	2.0	$\Omega$	$I_{OL} = 2.0\text{ A}$	
High Level Output Voltage <sup>b, c</sup>	$V_{OH}$	$V_{CC} - 0.45$	$V_{CC} - .2$		V	$I_F = 10\text{ mA}$ , $I_O = -100\text{ mA}$	
Low Level Output Voltage	$V_{OL}$		0.1	0.25	V	$I_O = 100\text{ mA}$	
High Level Supply Current	$I_{CCH}$		2.65	4.2	mA	$I_F = 10\text{ mA}$	5
Low Level Supply Current	$I_{CCL}$		2.55	4.2	mA	$V_F = 0\text{ V}$	6
Threshold Input Current Low to High	$I_{FLH}$		2.6	5.5	mA	$V_O > 5\text{ V}$	7
Threshold Input Voltage High to Low	$V_{FHL}$	0.8			V		
Input Forward Voltage	$V_F$	1.25	1.5	1.85	V	$I_F = 10\text{ mA}$	7
Temperature Coefficient of Input Forward Voltage	$\Delta V_F / \Delta T_A$		-1.5		mV/°C		
Input Reverse Breakdown Voltage	$BV_R$	6			V	$I_R = 100\text{ }\mu\text{A}$	
Input Capacitance	$C_{IN}$		90		pF	$f = 1\text{ MHz}$ , $V_F = 0\text{ V}$	
UVLO Threshold	$V_{UVLO+}$	12.1	13	13.9	V	$V_O > 5\text{ V}$	8
	$V_{UVLO-}$	11.1	12	12.9		$I_F = 10\text{ mA}$	8
UVLO Hysteresis	$UVLO_{HYS}$	0.5	1.0		V		

- Output is source at  $-2.0\text{ A}$  or  $2.0\text{ A}$  with a maximum pulse width of  $10\text{ }\mu\text{s}$ .
- In this test,  $V_{OH}$  is measured with a DC load current. When driving capacitive loads  $V_{OH}$  will approach  $V_{CC}$  as  $I_{OH}$  approaches zero amperes.
- Maximum pulse width =  $1\text{ ms}$ .

## Switching Specifications (AC)

Unless otherwise noted, all Minimum/Maximum specifications are at Recommended Operating Conditions. All typical values are at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{CC} - V_{EE} = 15\text{ V}$ ,  $V_{EE} = \text{Ground}$ .

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.
Propagation Delay Time to High Output Level <sup>a</sup>	$t_{PLH}$	30	65	120	ns	$V_{CC} = 15\text{ V}$ $R_G = 7.5\ \Omega$	9,12,14
Propagation Delay Time to Low Output Level	$t_{PHL}$	30	65	120	ns	$C_L = 10\text{ nF}$ $f = 20\text{ kHz}$	10,12,14
Pulse Width Distortion ( $t_{PHL} - t_{PLH}$ ) <sup>b</sup>	PWD	-40	0	40	ns	Duty Cycle = 50% $V_{in} = 4.5\text{ V to }5.5\text{ V}$	11
Dead Time Distortion Caused by Any Two Parts ( $t_{PLH} - t_{PHL}$ ) <sup>c</sup>	DTD	-40		50	ns	$R_{in} = 350\ \Omega$	
Rise Time	$t_R$		15		ns	$V_{CC} = 15\text{ V}$ $C_L = 1\text{ nF}$	13,14
Fall Time	$t_F$		15		ns	$f = 20\text{ kHz}$ Duty Cycle = 50% $V_{in} = 4.5\text{ V to }5.5\text{ V}$ $R_{in} = 350\ \Omega$	
Output High Level Common Mode Transient Immunity <sup>d, e</sup>	$ CM_H $	50	>75		kV/ $\mu\text{s}$	$T_A = 25\text{ }^\circ\text{C}$ $V_{CC} = 30\text{ V}$ ,	15
Output Low Level Common Mode Transient Immunity <sup>d, f</sup>	$ CM_L $	50	>75		kV/ $\mu\text{s}$	$V_{CM} = 1500\text{ V}$ , with split resistors	

- This load condition approximates the gate load of a 600 V/50 A power devices.
- Pulse Width Distortion (PWD) is defined as  $t_{PHL} - t_{PLH}$  for any given device.
- Dead Time Distortion (DTD) is defined as  $t_{PLH} - t_{PHL}$  between any two parts under the same test condition. A negative DTD reduces original system dead time; while a positive DTD increases original system dead time.
- Pin 2 and Pin 4 need to be connected to LED common.
- Common mode transient immunity in the high state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse, VCM, to ensure that the output will remain in the high state, (i.e.,  $V_O > 15\text{ V}$ ).
- Common mode transient immunity in a low state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse, VCM, to ensure that the output will remain in a low state (i.e.,  $V_O < 1.0\text{ V}$ ).

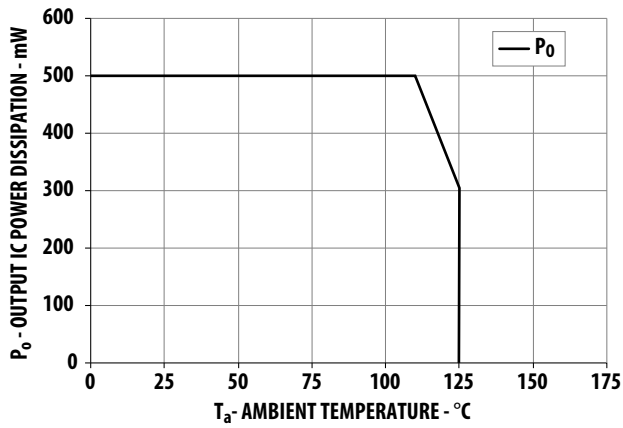
## Package Characteristics

Unless otherwise noted, all Minimum/Maximum specifications are at Recommended Operating Conditions. All typical values are at  $T_A = 25\text{ }^\circ\text{C}$ . The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage <sup>a, b, c</sup>	$V_{ISO}$	5000			VRMS	$RH < 50\%$ , $t = 1\text{ min}$ $T_A = 25\text{ }^\circ\text{C}$
Input-Output Resistance <sup>c</sup>	$R_{I-O}$	109	1014		$\Omega$	$V_{I-O} = 500\text{ V}_{DC}$
Input-Output Capacitance	$C_{I-O}$		0.6		pF	$f = 1\text{ MHz}$

- The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Avago Technologies Application Note 1074 "Optocoupler Input-Output Endurance Voltage."
- In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 6000\text{ V}_{RMS}$  for 1 second.
- Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Figure 2 Output IC Power Dissipation Derating Chart



## Typical Performance Plots

Figure 3 I<sub>OH</sub> vs. (V<sub>CC</sub> - V<sub>OH</sub>)

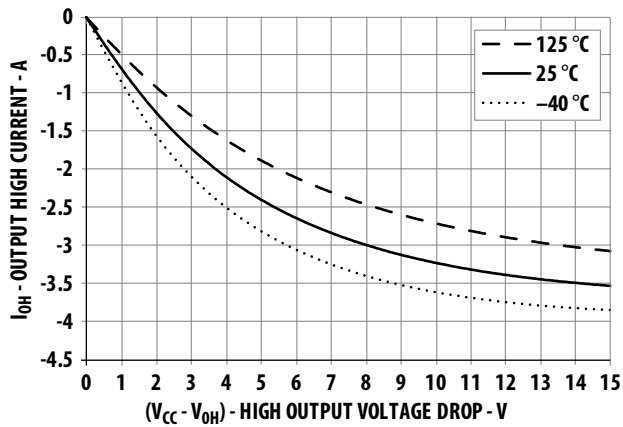


Figure 4 I<sub>OL</sub> vs. V<sub>OL</sub>

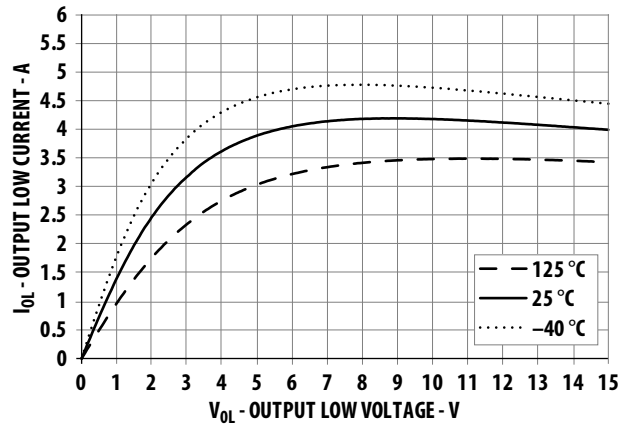


Figure 5 I<sub>CCH</sub> vs. Temperature

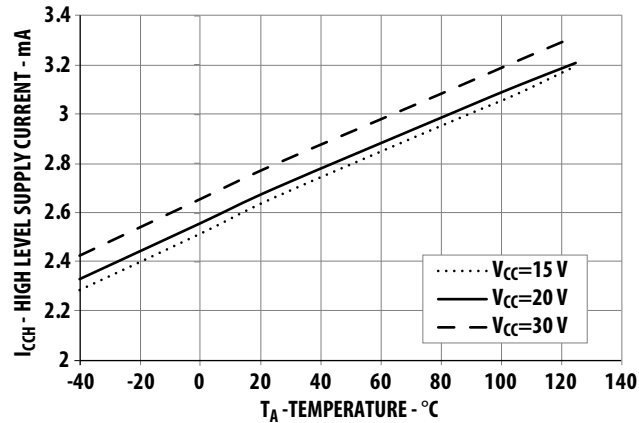


Figure 6 I<sub>CCL</sub> vs. Temperature

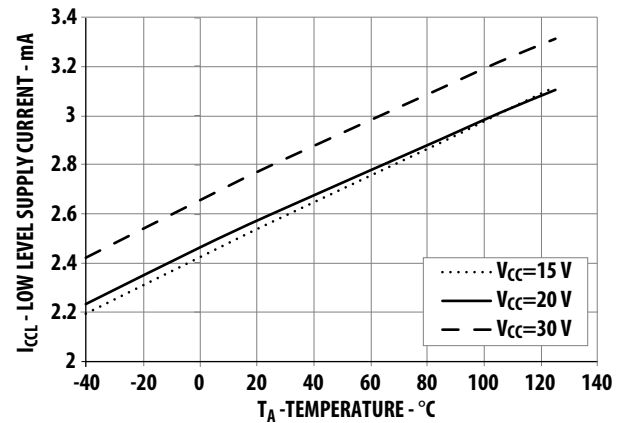




Figure 7  $V_F$  vs. Temperature

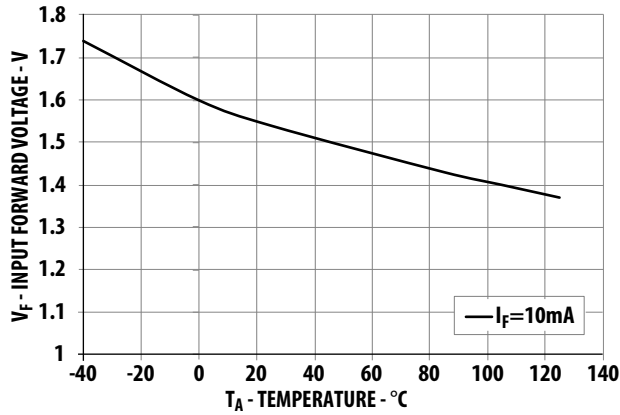


Figure 8  $I_F$  vs.  $V_F$

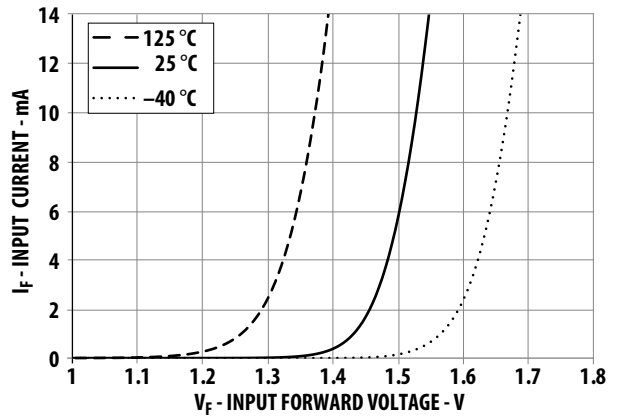


Figure 9  $t_{PLH}$  vs. Temperature

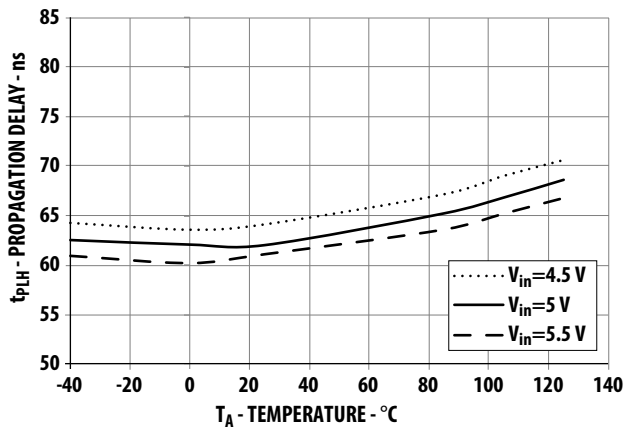


Figure 10  $t_{PHL}$  vs. Temperature

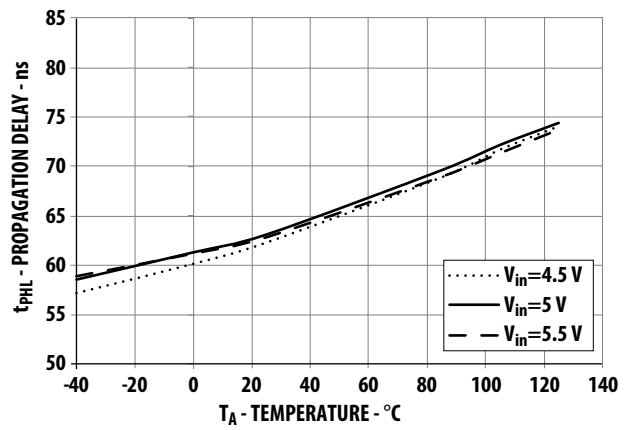


Figure 11 PWD vs. Temperature

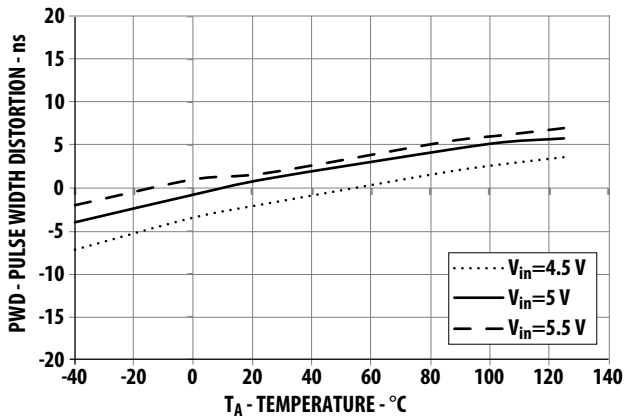


Figure 12  $t_{PLH}$  and  $t_{PHL}$  Test Circuit

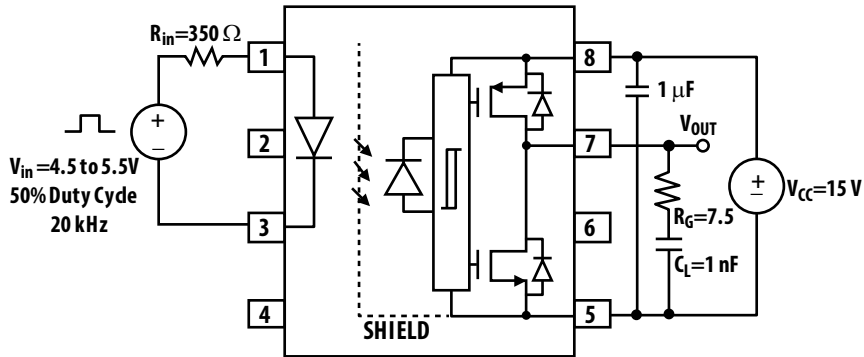


Figure 13  $t_r$  and  $t_f$  Test Circuit

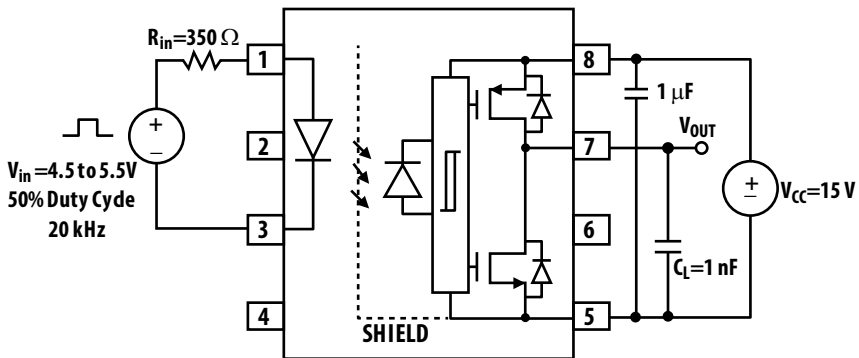


Figure 14  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$  and  $t_f$  Reference Waveforms

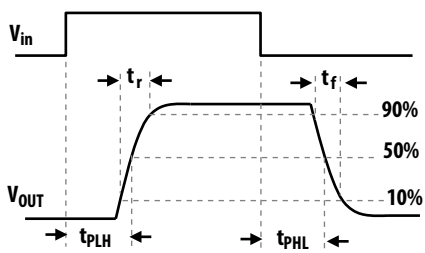
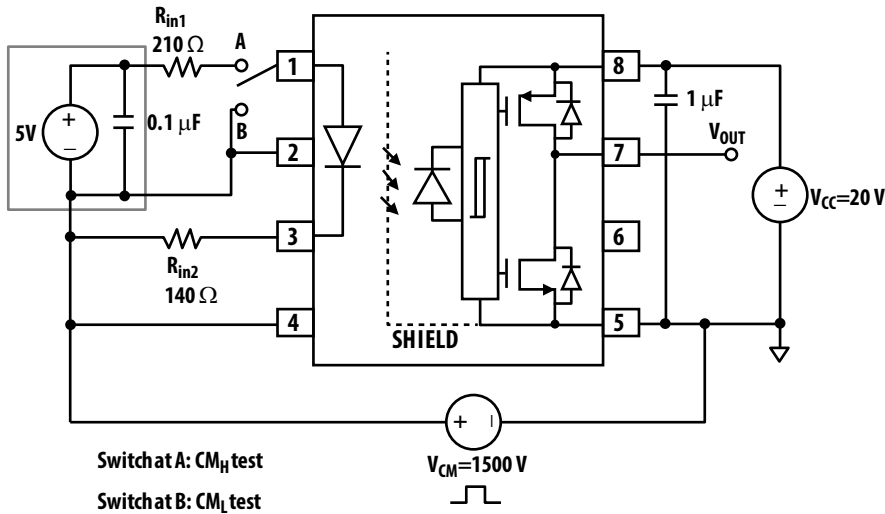
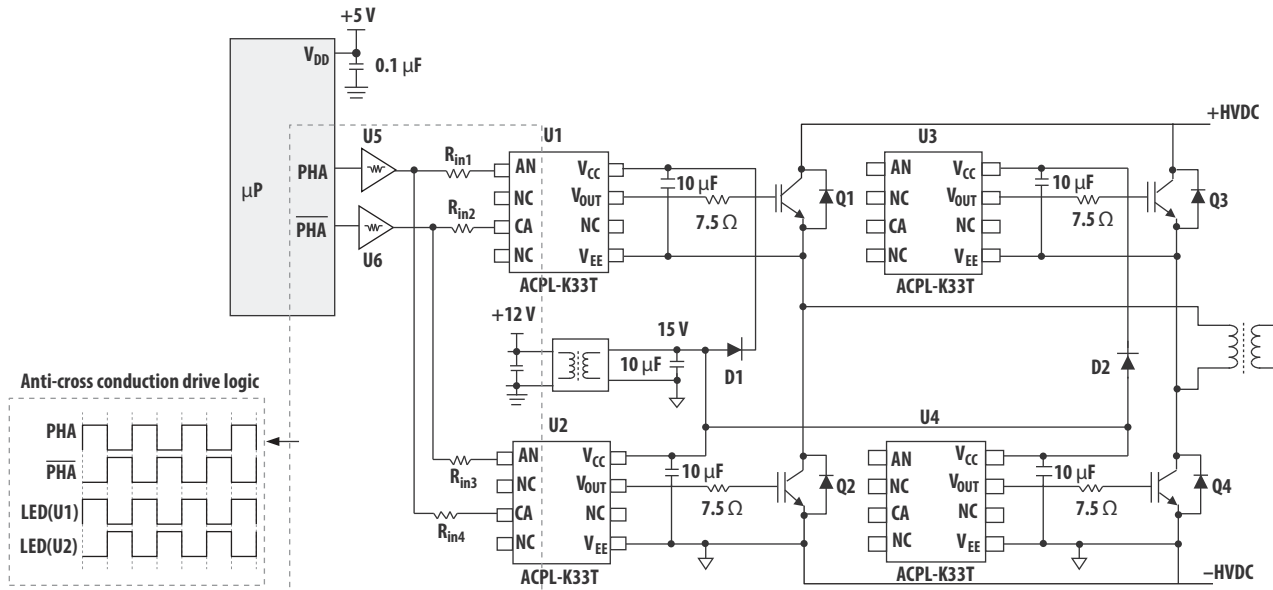


Figure 15 CMR Test Circuit



## Typical High-Speed SiC MOSFET/IGBT Gate Drive Circuit

Figure 16 Typical High-Speed SiC MOSFET/IGBT Gate Drive Circuit



### Anti-Cross Conduction Drive

One of the many benefits of using ACPL-K33T is the ease of implementing anti-cross conduction drive between the high side and the low side gate drivers to prevent a shoot-through event. This safety interlock drive can be realized by interlocking the output of buffer U5 and U6 to both the high and the low side gate drivers, as shown in Figure 16. Due to the difference in propagation delay between optocouplers, however, a certain amount of dead time has to be added to ensure sufficient dead time at the MOSFET gate. For more details, see the “Dead Time and Propagation Delay” section.

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## Recommended LED Drive Circuits

There will be common mode noise whenever there is a difference in the ground level of the optocoupler's input control circuitry and that of the output control circuitry. [Figure 17](#) and [Figure 18](#) show the recommended LED drive circuits that use logic gate (CMOS buffer) for high common mode rejection (CMR) performance of the optocoupler gate driver. Split limiting resistors are used to balance the impedance at both anode and cathode of the input LED for high common mode noise rejection. The output impedance of the CMOS buffer (shown as  $R_O$  in [Figure 17](#) and [Figure 18](#)) has to be included in the calculation for LED drive current.

On the other hand, [Figure 19](#) and [Figure 20](#) show the recommended LED drive circuits that use a single transistor. During the LED off state, M1 and Q1 in [Figure 19](#) and [Figure 20](#) will shunt current, which results in greater power consumption. It is not recommended to have open drain and open collector drive circuits, as shown in [Figure 21](#) and [Figure 22](#). This is because during the off state of the MOSFET/transistor, the cathode of the input LED sees high impedance and becomes sensitive to noise.

## Drive Power

If a CMOS buffer is used to drive the LED, it is recommended that you connect the CMOS buffer at the LED cathode. This is because the sinking capability of the NMOS is usually greater than the driving capability of the PMOS in a CMOS buffer.

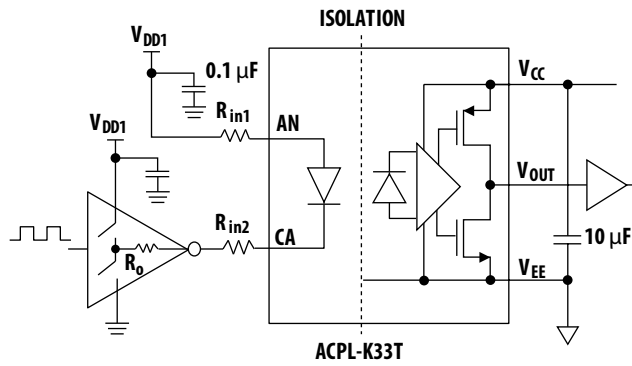
## Drive Logic

The designer can configure LED drive circuits for non-inverting and inverting logic as recommended in [Figure 17](#) and [Figure 18](#). For the inverting and non-inverting logic to work, the external power supply  $V_{DD1}$  must be connected to the CMOS buffer. If the  $V_{DD1}$  supply is lost, the LED will be permanently off and output will be low.

## Bypass and Reservoir Capacitors

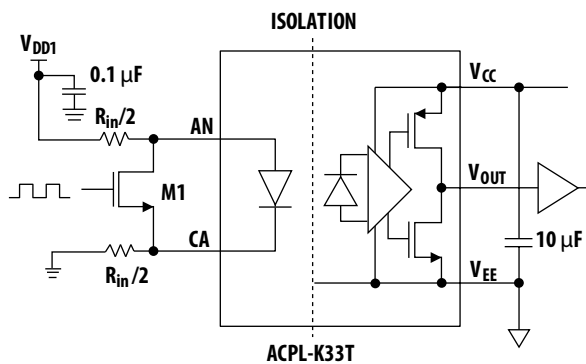
Supply bypass capacitors are necessary at the input buffer and ACPL-K33T output supply pin. A ceramic capacitor with the value of 0.1  $\mu\text{F}$  is recommended at the input buffer to provide high frequency bypass, which also helps to improve CMR performance. At the output supply pin ( $V_{CC} - V_{EE}$ ), it is recommended to use a 10  $\mu\text{F}$ , low ESR and low ESL capacitor as a charge reservoir to supply instant driving current to IGBT at VOUT during switching.

**Figure 17 Recommended Non-Inverting Logic Gate Drive Circuit**



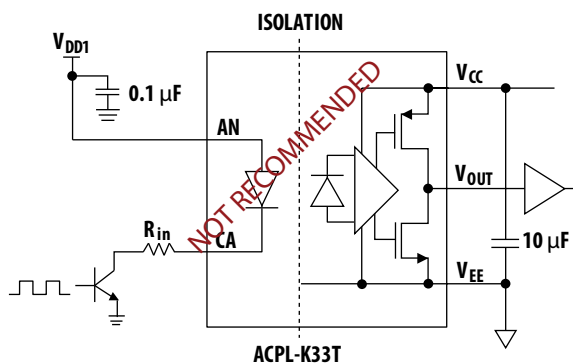
$V_{DD1} = 5\text{ V} \pm 10\%$   
Ratio  $R_{in1} : (R_{in2} + R_o) = 1.5:1$   
Recommended  $R_o + R_{in1} + R_{in2} = 350\ \Omega$

**Figure 19 Recommended Single Transistor Drive Circuit**



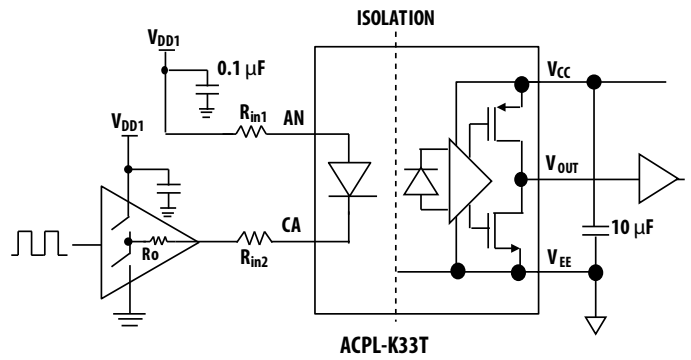
$V_{DD1} = 5\text{ V} \pm 10\%$   
Ratio  $R_{in1} : R_{in2} = 1.5:1$   
Recommended  $R_{in1} + R_{in2} = 350\ \Omega$

**Figure 21 Not Recommended – Open Drain/Open Collector Drive Circuit**



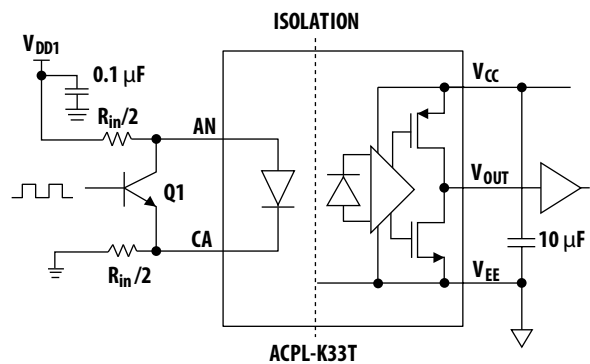
**NOTE** Not recommended.

**Figure 18 Recommended Inverting Logic Gate Drive Circuit**



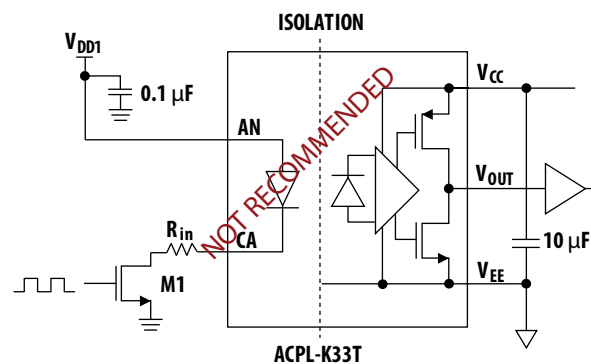
$V_{DD1} = 5\text{ V} \pm 10\%$   
Ratio  $R_{in1} : (R_{in2} + R_o) = 1.5:1$   
Recommended  $R_o + R_{in1} + R_{in2} = 350\ \Omega$

**Figure 20 Recommended Single Transistor Drive Circuit**



$V_{DD1} = 5\text{ V} \pm 10\%$   
Ratio  $R_{in1} : R_{in2} = 1.5:1$   
Recommended  $R_{in1} + R_{in2} = 350\ \Omega$

**Figure 22 Not Recommended – Open Drain/Open Collector Drive Circuit**

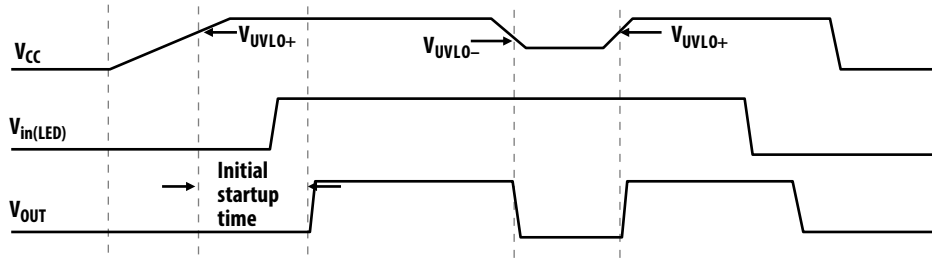


**NOTE** Not recommended.

## Initial Power Up and UVLO Operation

Insufficient gate voltage to IGBT can increase IGBT turn-on resistance, resulting in a large power loss and damage to IGBT due to high heat dissipation. ACPL-K33T constantly monitors the output power supply. During initial power up, the ACPL-K33T requires a maximum of 50  $\mu\text{s}$  initial startup time for the internal bias and circuitry to get ready. The gate driver output ( $V_{\text{OUT}}$ ) is held at off state during initial startup time. Thereafter, when the output power supply is lower than the under voltage lockout ( $V_{\text{UVLO-}}$ ) threshold, the gate driver output will shut off to protect IGBT from low voltage bias. When the output power supply is more than the  $V_{\text{UVLO+}}$  threshold,  $V_{\text{OUT}}$  is released from low state and it follows the input LED drive signal, as shown in Figure 23.

Figure 23 ACPL-K33T Initial Power-Up and UVLO Operation



## Dead Time Distortion and Propagation Delay

Dead time is the period of time during which both high side and low side power transistors (shown as Q1 and Q2 in Figure 16) are off. Originally, the system is required to design in some amount of dead time to compensate for the turn-off delay needed for the MOSFET to discharge the input capacitance after the gate is switched off. In this application note, this amount of dead time is called system original dead time. When an optocoupler is used, the designer has to consider the effect of the optocoupler's dead time distortion (DTD) toward system original dead time. The optocoupler's negative DTD decreases system original dead time; on the other hand, the optocoupler's positive DTD increases system original dead time. Therefore, the designer must add extra dead time to system original dead time to compensate for the optocoupler's negative DTD. Figure 24 and Figure 25 illustrate the effect of the optocoupler's DTD to system original dead time.

## Dead Time and Propagation Delay Waveforms

Figure 24 Negative DTD Reduces Original DT

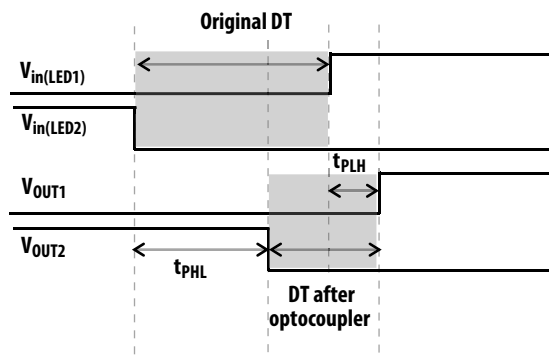
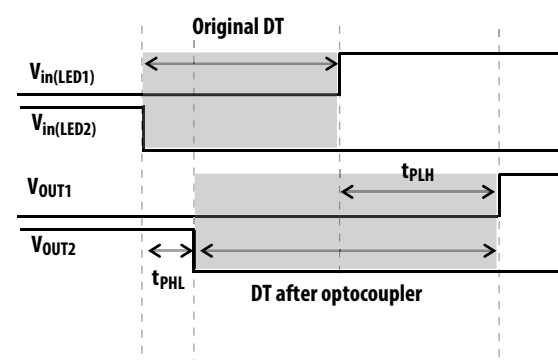


Figure 25 Positive DTD Increases Original DT



Here is an example of total dead time calculation for a typical optocoupler drive circuit for MOSFET.

$$\begin{aligned} \text{Total dead time required} &= \text{System original dead time} + |\text{optocoupler's negative DTD}| \\ &= \text{System original dead time} + |40 \text{ ns}| \\ &\text{where system original dead time} = \text{MOSFET turn-off delay} \end{aligned}$$

**NOTE** The propagation delays used to calculate dead time distortion (DTD) are taken at equal temperatures and test conditions as the optocouplers used under consideration are typically mounted in close proximity to each other and are switching same type of MOSFETs.

## Programmable Dead Time

Programmable dead time can be introduced to an optocoupler gate driver by adding an external capacitor (CDT) across the input LED (Anode and Cathode) as shown in Figure 26. This simple circuitry offers you the flexibility to optimize gate drive switching timing for various MOSFETs and applications through hardware configuration.

The value of the external capacitor (CDT) can be calculated based on the minimum dead time requirement for the system, as shown in the following equation. The added dead time will delay the turn-on timing of the gate signal, as shown in Figure 27.

$$C_{DT(\min)} = - \frac{DT_{(\min)}}{R_{in(\min)} \ln \left( 1 - \frac{V_{F(\min)} - V_{in(\text{off})}}{V_{in(\text{on})} - V_{in(\text{off})}} \right)}$$

where

DT: Total dead time required for a system, inclusive of original dead time and the optocoupler's negative DTD

R<sub>in</sub>: Total input LED current-limiting resistor

C<sub>DT</sub>: External Dead time programming capacitor

V<sub>F</sub>: Input LED forward voltage

V<sub>in</sub>: Input PWM voltage

Figure 26 Add C<sub>DT</sub> for Dead Time Programming

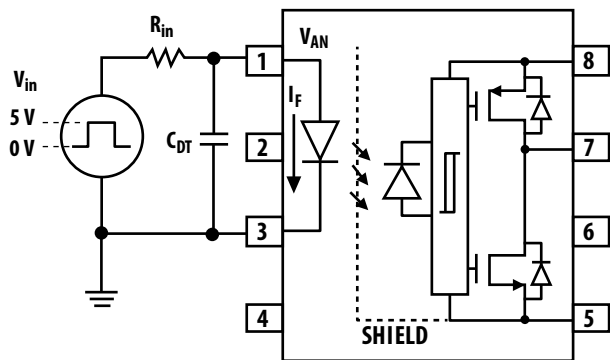
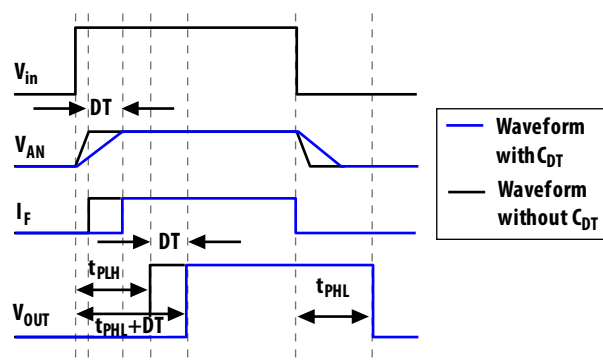


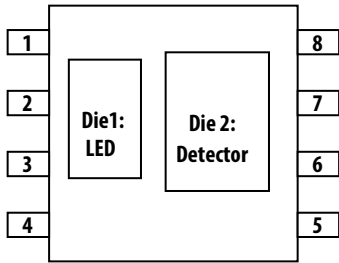
Figure 27 Timing Diagram with and without C<sub>DT</sub>



## Thermal Resistance Model for ACPL-K33T

The diagram for measurement is shown in Figure 28. Here, one die is first heated and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 2 by 2 matrix for our case of two heat sources.

**Figure 28 Diagram of ACPL-K33T for Measurement**



$$\begin{bmatrix} R11 & R12 \\ R21 & R22 \end{bmatrix} \cdot \begin{bmatrix} P1 \\ P2 \end{bmatrix} = \begin{bmatrix} \Delta T1 \\ \Delta T2 \end{bmatrix}$$

R11: Thermal Resistance of Die1 due to heating of Die1 (°C/W)

R12: Thermal Resistance of Die1 due to heating of Die2 (°C/W)

R21: Thermal Resistance of Die2 due to heating of Die1 (°C/W)

R22: Thermal Resistance of Die2 due to heating of Die2 (°C/W)

P1: Power dissipation of Die1 (W)

P2: Power dissipation of Die2 (W)

T1: Junction temperature of Die1 due to heat from all dice (°C)

T2: Junction temperature of Die2 due to heat from all dice (°C)

Ta: Ambient temperature (°C)

ΔT1: Temperature difference between Die1 junction and ambient (°C)

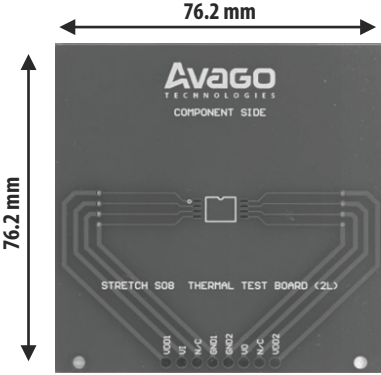
ΔT2: Temperature difference between Die2 junction and ambient (°C)

$$T1 = (R11 \times P1 + R12 \times P2) + Ta \text{ -----(1)}$$

$$T2 = (R21 \times P1 + R22 \times P2) + Ta \text{ -----(2)}$$



Measurement is done on both low and high conductivity boards as shown in the following table.

Layout	Measurement Data	
	<p>Low conductivity board per JEDEC 51-3:                      R11 = 191 °C/W                      R12 = R21 = 68.5 °C/Wx                      R22 = 77 °C/W</p>	<p>High conductivity board per JEDEC 51-7:                      R11 = 155 °C/W                      R12 = R21 = 64 °C/W                      R22 = 41 °C/W</p>

**NOTE** These thermal resistances R11, R12, R21 and R22 can be improved by increasing the ground plane/copper area.

Application and environment design for ACPL-K33T needs to ensure that the junction temperature of the internal IC and LED within the gate drive optocoupler do not exceed 150 °C. Use equation (1) and equation (2) to estimate the junction temperatures. For example:

**Calculation of LED and output IC power dissipation:**

$$\begin{aligned}
 \text{LED power dissipation, } P_E &= I_{F(\text{LED})} (\text{Recommended Max}) \times V_{F(\text{LED})} (\text{at } 125^\circ\text{C}) \times \text{Duty Cycle} \\
 &= 13 \text{ mA} \times 1.25 \text{ V} \times 50\% \\
 &= 8.125 \text{ mW}
 \end{aligned}$$

$$\begin{aligned}
 \text{Output IC power dissipation, } P_O &= V_{CC} (\text{Recommended Max}) \times I_{CC}(\text{Max}) + P_{HS} + P_{LS} \\
 &= 30 \text{ V} \times 4.2 \text{ mA} + 60 \text{ mW} + 34.3 \text{ mW} \\
 &= 220.3 \text{ mW}
 \end{aligned}$$

where

$$\begin{aligned}
 P_{HS} &= \text{High side switching power dissipation} \\
 &= (V_{CC} \times Q_G \times f_{\text{PWM}}) \times R_{DS,OH(\text{MAX})} / (R_{DS,OH(\text{MAX})} + R_{GH}) / 2 \\
 &= (30 \text{ V} \times 80 \text{ nC} \times 200 \text{ kHz}) \times 4 \Omega / (4 \Omega + 12 \Omega) / 2 \\
 &= 60 \text{ mW}
 \end{aligned}$$

$$\begin{aligned}
 P_{LS} &= \text{Low side switching power dissipation} \\
 &= (V_{CC} \times Q_G \times f_{\text{PWM}}) \times R_{DS,OL(\text{MAX})} / (R_{DS,OL(\text{MAX})} + R_{GL}) / 2 \\
 &= (30 \text{ V} \times 80 \text{ nC} \times 200 \text{ kHz}) \times 2 \Omega / (2 \Omega + 12 \Omega) / 2 \\
 &= 34.3 \text{ mW}
 \end{aligned}$$

$Q_G$  = Gate charge at supply voltage

$f_{\text{PWM}}$  = LED switching frequency

$R_{GH}$  = Gate charging resistance

$R_{GL}$  = Gate discharging resistance

**Calculation of LED junction temperature and output IC junction temperature at  $T_a=125\text{ }^\circ\text{C}$  based on a high conductivity board thermal resistance model:**

$$\begin{aligned}\text{LED junction temperature, } T_1 &= (R_{11} \times P_E + R_{12} \times P_O) + T_a \\ &= (155\text{ }^\circ\text{C/W} \times 8.125\text{ mW} + 64\text{ }^\circ\text{C/W} \times 220.3\text{ mW}) + 125\text{ }^\circ\text{C} \\ &= 140\text{ }^\circ\text{C} < T_J(\text{absolute max}) \text{ of } 150\text{ }^\circ\text{C}\end{aligned}$$

$$\begin{aligned}\text{Output IC junction temperature, } T_2 &= (R_{21} \times P_E + R_{22} \times P_O) + T_a \\ &= (64\text{ }^\circ\text{C/W} \times 8.125\text{ mW} + 41\text{ }^\circ\text{C/W} \times 220.3\text{ mW}) + 125\text{ }^\circ\text{C} \\ &= 135\text{ }^\circ\text{C} < T_J(\text{absolute max}) \text{ of } 150\text{ }^\circ\text{C}\end{aligned}$$

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