

## DS32EV100-EVK User Guide DS32EV100 Programmable Equalizer

### Overview

The DS32EV100-EVK evaluation board provides a typical application for the evaluation of the DS32EV100 programmable equalizer.

### Specifications

**DC Input Power (JP1):** 3.3V  $\pm$  10%, or 2.5V  $\pm$  5%

**Serial Data Inputs (IN\_+/-):** High-speed CML inputs. Acceptable data input speed DC – 3.2 Gbps. *For more details, please refer to the datasheet.*

**Serial Data Outputs (OUT\_+/-):** High-speed CML outputs. *For more details, please refer to the datasheet.*

**CML Input Voltage:** -0.5V to 4.0V

**CMOS Input Voltage:** -0.5V to 4.0V

### Jumper Settings

**E101 (EQ\_SEL[0:2]):** These jumpers are control equalization boost levels. The boost setting on the evaluation board is set to 111 with on board pull up resistors R101, R102, R103 connected to VCC.

#### IMPORTANT ERRATA:

**EQUALIZATION SETTINGS E101( EQ\_SEL[2:0]/BST[2:0])** These pins control the boost level and currently only have the option to be connected to ground using jumpers. In order to select maximum equalization the EQ\_SEL[0:2]/BST[0:2] must be hardwired to Vdd. When selecting these EQ settings please use external hardware to force Vdd on these pins.

Please see Table 1 for equalizer boost control settings.

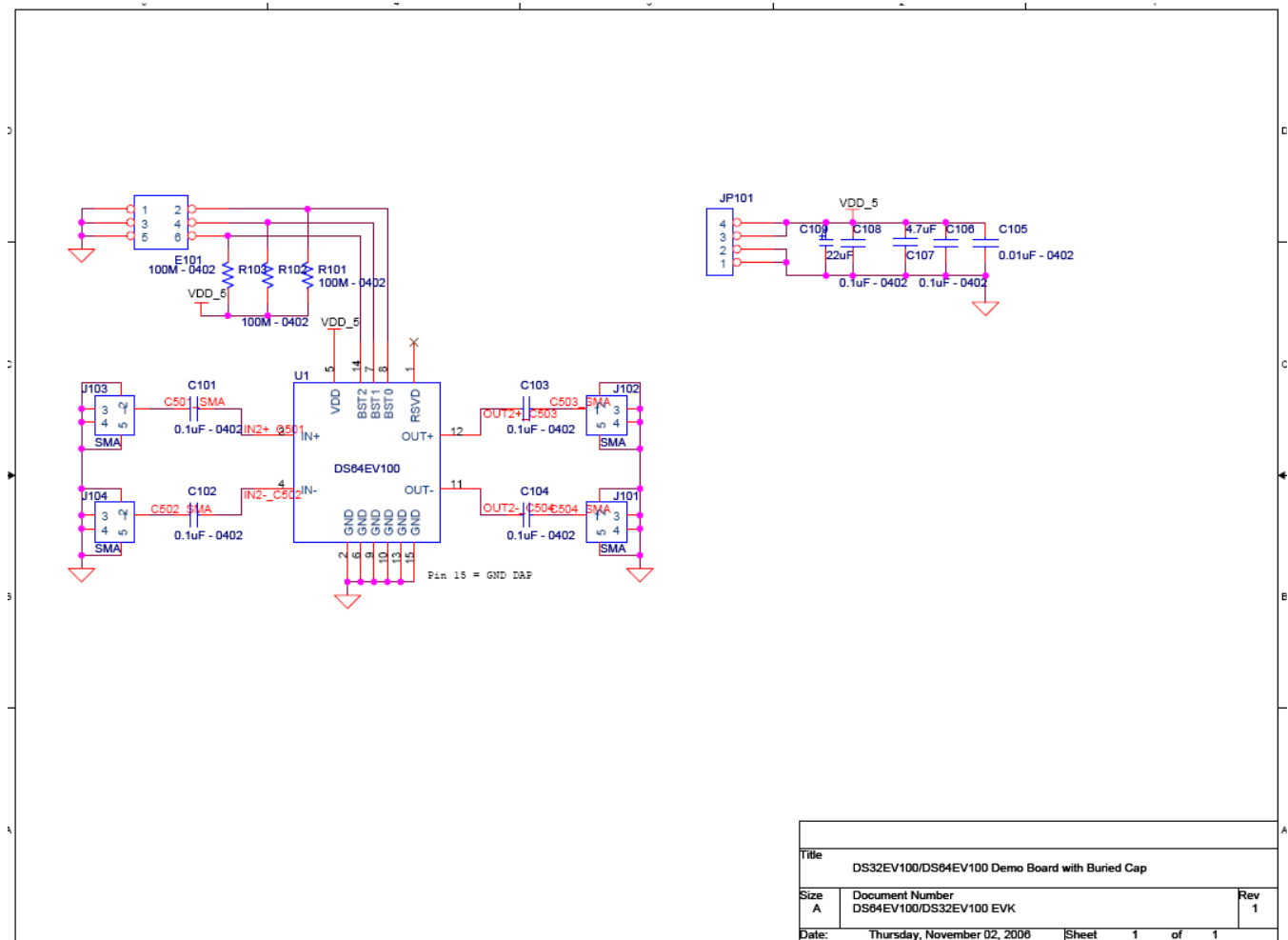
**Table 1. Equalization Boost Controls**

6 mil microstrip FR4 trace length (in)	24 AWG Twin-AX cable length (m)	Channel loss at 1.6 GHz	[BST_2, BST_1, BST_0]
0	0	0 dB	0 0 0
5	2	3 dB	0 0 1
10	3	6 dB	0 1 0
15	4	7 dB	0 1 1
20	5	8 dB	1 0 0 (Default)
25	6	10 dB	1 0 1
30	7	12 dB	1 1 0
40	10	14 dB	1 1 1

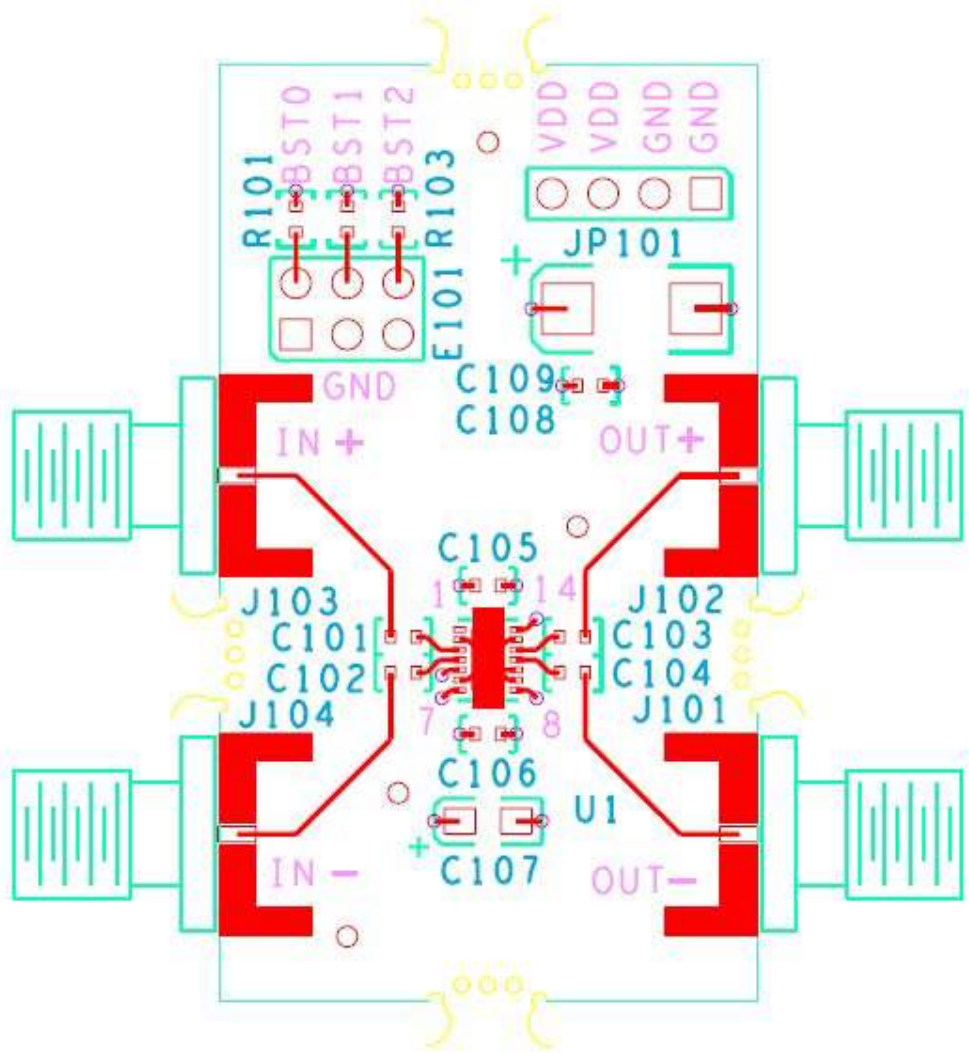
## Bill of Materials

DESIGNATION	QTY	DESCRIPTION
C105	1	0.01uF ±10% Ceramic Capacitor 0402
C101, C102, C103, C104, C106, C108	6	0.1uF ±10% Ceramic Capacitor 0402
C107	1	4.7uF ±10% Ceramic Capacitor 1206
C109	1	22uF +10% Tan Capacitor 6032
R101, R102, R103	3	
JP101	1	4 Pin Header
E101	1	3X2 Pin Header
J101, J102, J103, J104	4	SMA Edge Tab Receptacle
U1	1	National DS32EV100

## Schematics



## Top View Layout



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