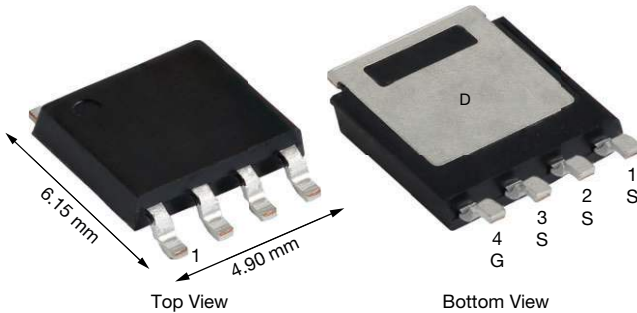
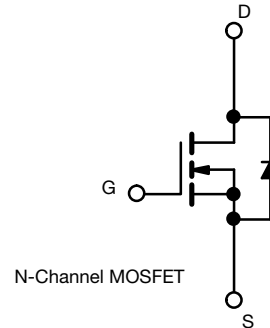


# Automotive N-Channel 60 V (D-S) 175 °C MOSFET

**PowerPAK® SO-8L**

**FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R<sub>g</sub> and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

AUTOMOTIVE GRADE


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**


PRODUCT SUMMARY	
V <sub>DS</sub> (V)	60
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 10 V	0.036
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 4.5 V	0.040
I <sub>D</sub> (A)	24
Configuration	Single
Package	PowerPAK SO-8L

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	60	V
Gate-source voltage		V <sub>GS</sub>	± 20	
Continuous drain current	T <sub>C</sub> = 25 °C <sup>a</sup>	I <sub>D</sub>	24	A
	T <sub>C</sub> = 125 °C		14	
Continuous source current (diode conduction) <sup>a</sup>		I <sub>S</sub>	49	
Pulsed drain current <sup>b</sup>		I <sub>DM</sub>	96	
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	17	
Single pulse avalanche energy		E <sub>AS</sub>	14.4	
Maximum power dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	29.4	W
	T <sub>C</sub> = 125 °C		9.8	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d</sup>			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>c</sup>	R <sub>thJA</sub>	42	°C/W
Junction-to-case (drain)		R <sub>thJC</sub>	2.8	

**Notes**

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = 250 μA		60	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.5	2.0	2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	250	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	30	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A	-	0.029	0.036	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A, T <sub>J</sub> = 125 °C	-	-	0.075	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 15 A, T <sub>J</sub> = 175 °C	-	-	0.096	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 15 A	-	0.032	0.040	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		-	30	-	S
<b>Dynamic <sup>b</sup></b>							
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 25 V, f = 1 MHz	-	705	987	pF
Output capacitance	C <sub>oss</sub>			-	85	119	
Reverse transfer capacitance	C <sub>rss</sub>			-	21	30	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 10 A	-	13	20	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>			-	3	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>			-	2	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz		2.1	4.2	6.3	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 3.0 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	7	11	ns
Rise time <sup>c</sup>	t <sub>r</sub>			-	3	6	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>			-	19	29	
Fall time <sup>c</sup>	t <sub>f</sub>			-	1	2	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>							
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-	-	96	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 15 A, V <sub>GS</sub> = 0 V		-	-	1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 10 A, di/dt = 100 A/μs		-	19	38	ns
Body diode reverse recovery charge	Q <sub>rr</sub>			-	17	34	nC
Reverse recovery fall time	t <sub>a</sub>			-	14	-	ns
Reverse recovery rise time	t <sub>b</sub>			-	5	-	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>					-	1.9

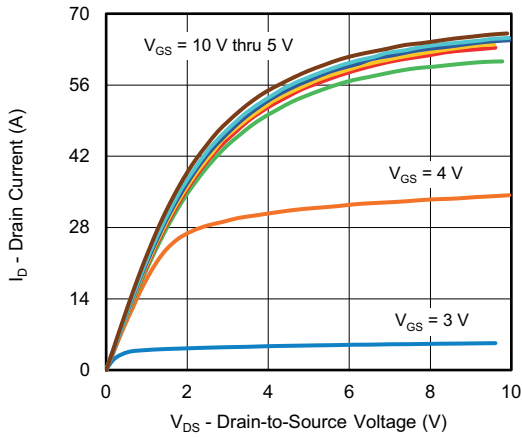
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

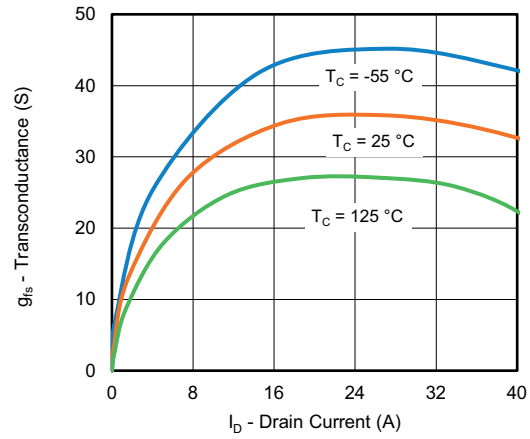
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



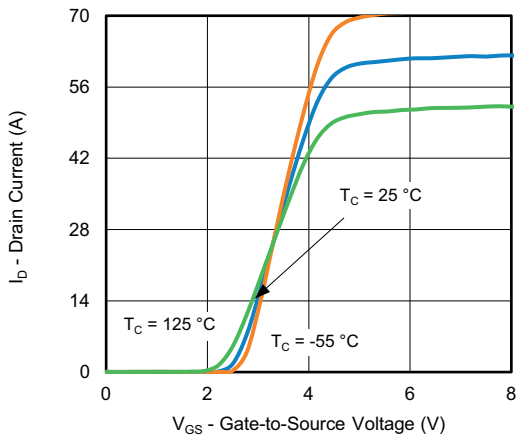
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



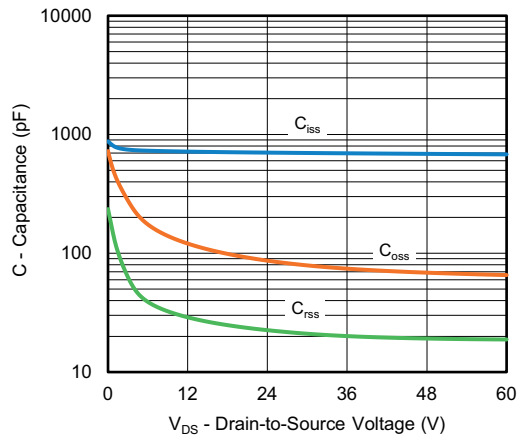
Output Characteristics



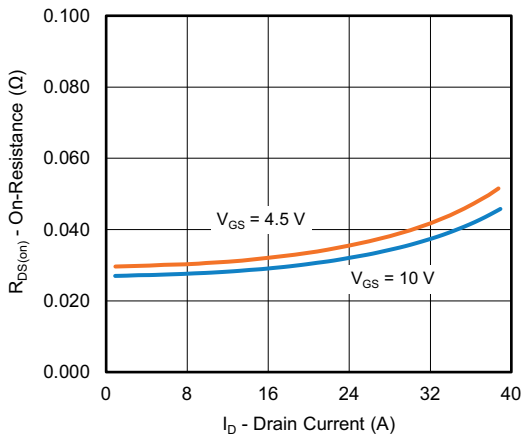
Transconductance



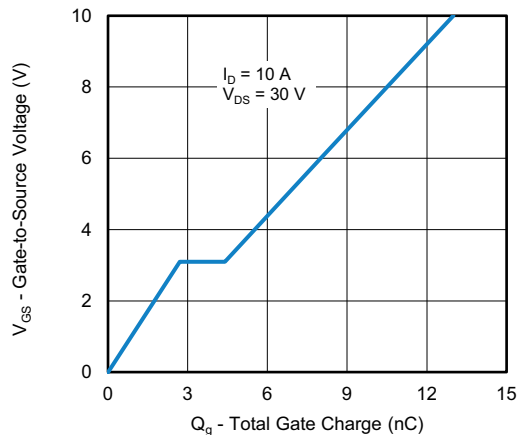
Transfer Characteristics



Capacitance

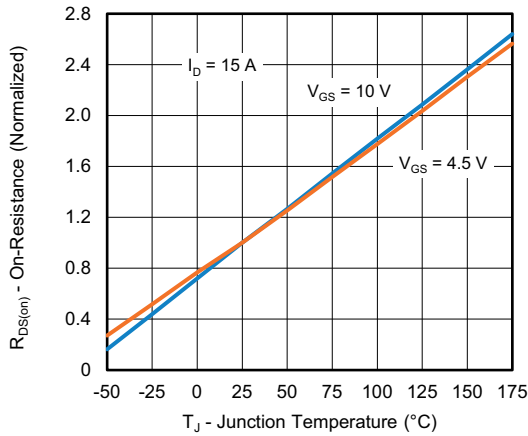


On-Resistance vs. Drain Current

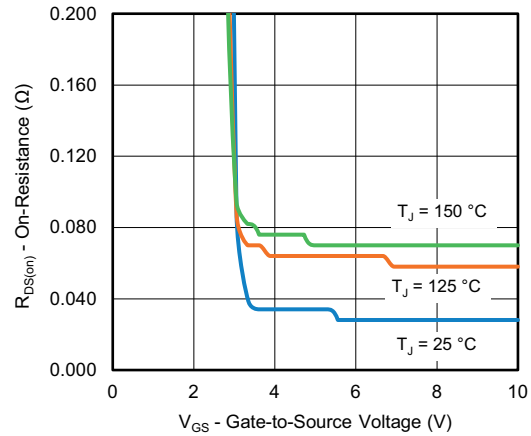


Gate Charge

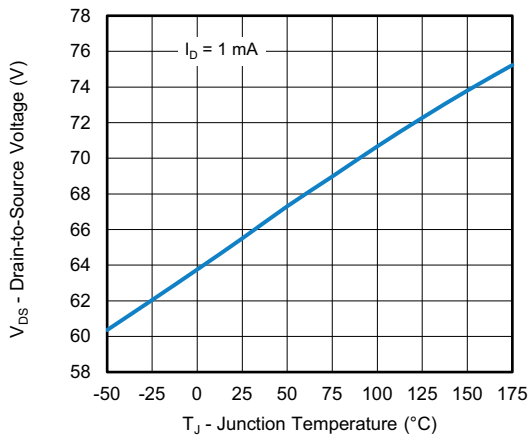
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



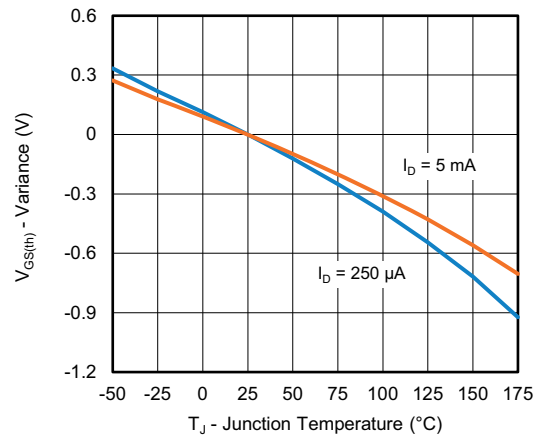
**On-Resistance vs. Junction Temperature**



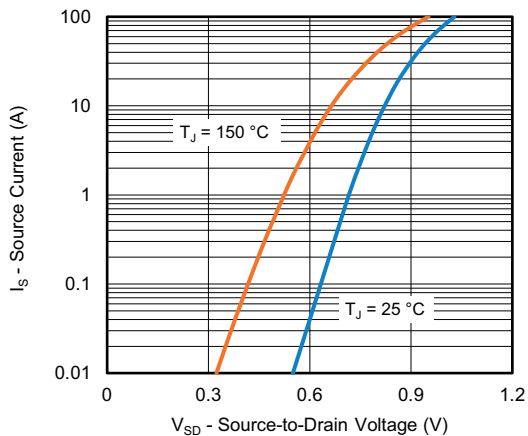
**On-Resistance vs. Gate-to Source Voltage**



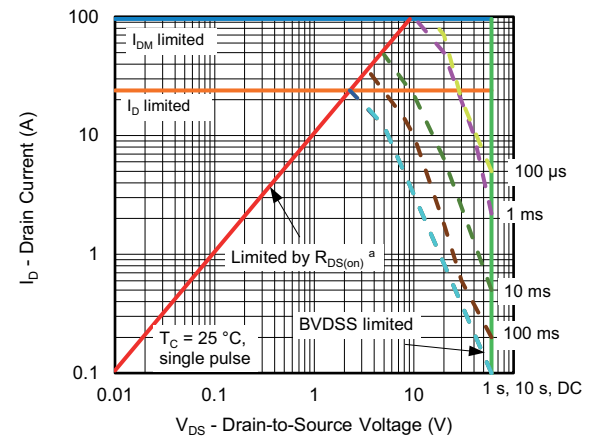
**Drain Source Breakdown vs. Junction Temperature**



**Threshold Voltage**



**Source Drain Diode Forward Voltage**



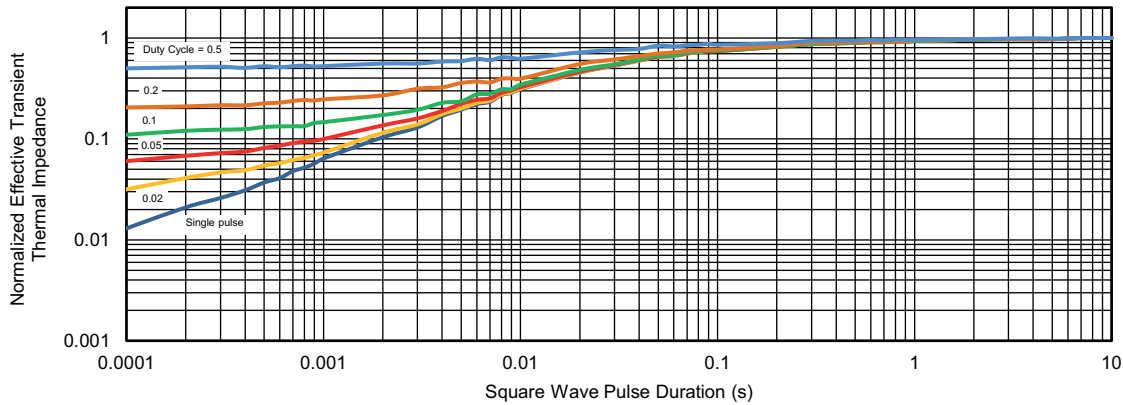
**Safe Operating Area**

**Note**

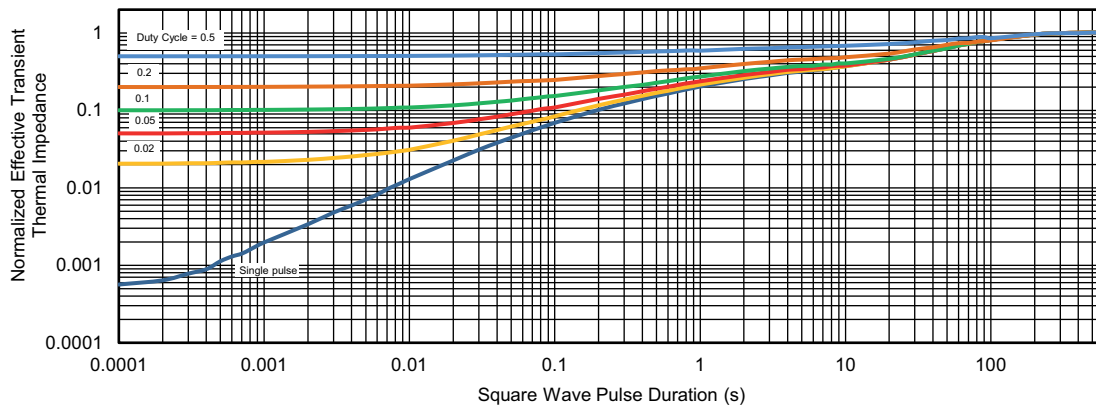
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**

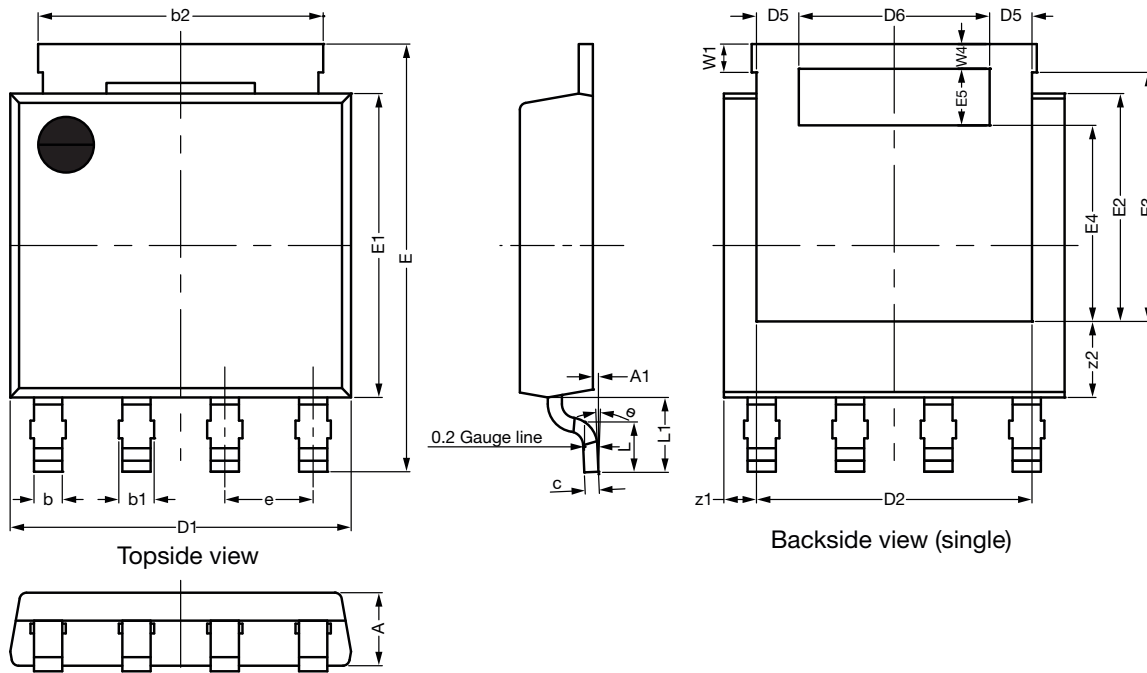


**Normalized Thermal Transient Impedance, Junction-to-Ambient**

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### PowerPAK<sup>®</sup> SO-8L (PPKS08LWLA) Case Outline 3



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.05	1.10	0.039	0.041	0.043
A1	0.00	---	0.127	0.000	---	0.005
b	0.33	0.41	0.49	0.013	0.016	0.019
b1	0.43	0.51	0.59	0.017	0.020	0.023
b2	4.00	4.10	4.20	0.157	0.161	0.165
c	0.15	0.20	0.25	0.006	0.008	0.010
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D5	0.51	0.61	0.71	0.020	0.024	0.028
D6	2.64	2.74	2.84	0.104	0.108	0.112
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
E3	3.48	3.58	3.68	0.137	0.141	0.145
E4	2.72	2.82	2.92	0.107	0.111	0.115
E5	0.71	0.81	0.91	0.028	0.032	0.036
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
W1	0.31	0.41	0.51	0.012	0.016	0.020
W4	0.31	0.36	0.41	0.012	0.014	0.016
z1	0.37	0.47	0.57	0.015	0.019	0.022
z2	0.99	1.09	1.19	0.039	0.043	0.047
θ	0°	---	5°	0°	---	5°

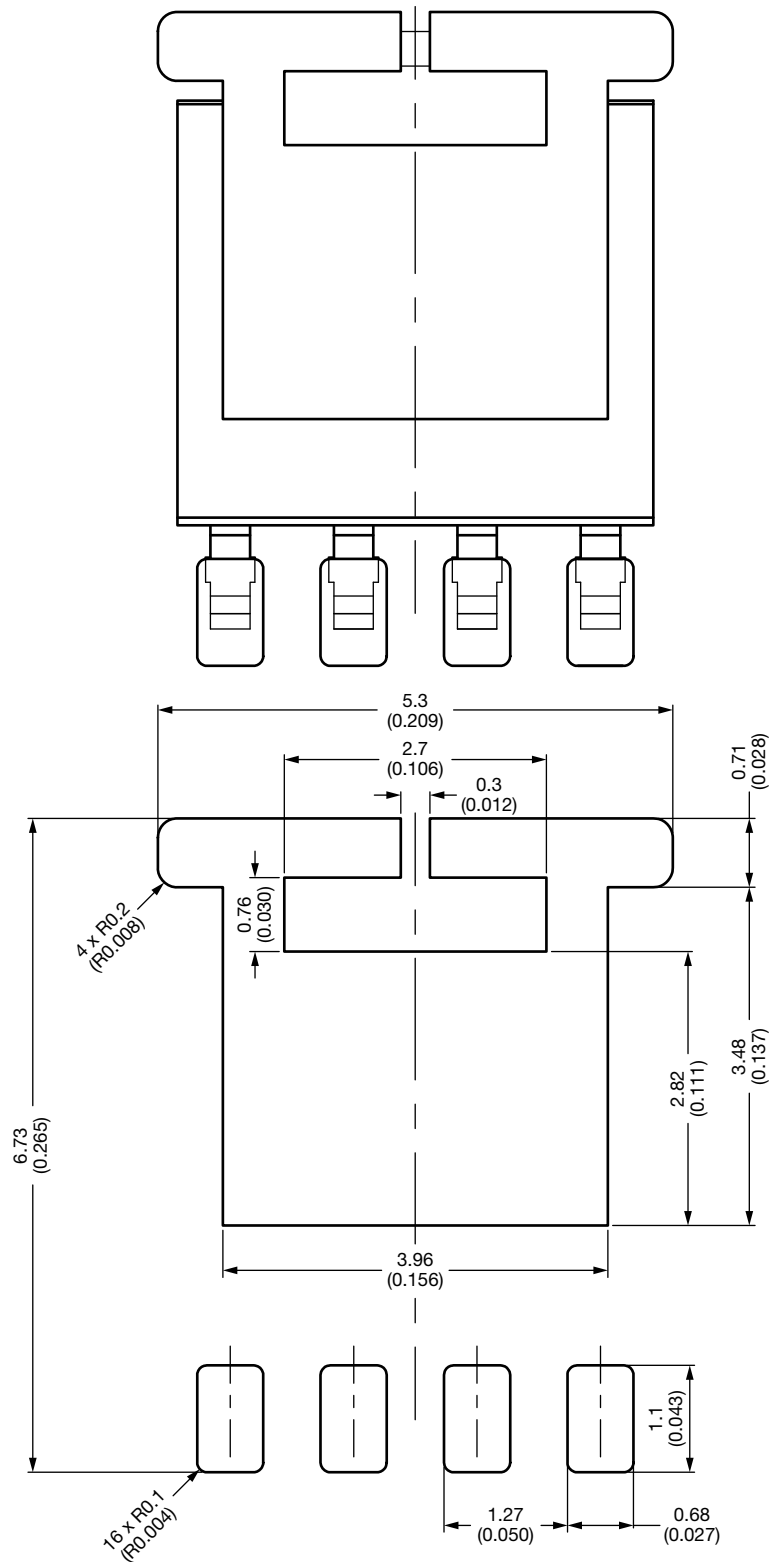
ECN: C22-1223-Rev. C, 19-Dec-2022  
 DWG: 6067

**Note**

- Millimeter will govern



# Recommended Land Pattern PowerPAK<sup>®</sup> SO-8L Single Short Ear



Dimensions in Millimeters (Inches)



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