

# XN01558

## Silicon NPN epitaxial planar type

For low-frequency amplification

### ■ Features

- Two elements incorporated into one package (Emitter-coupled transistors)
- Reduction of the mounting area and assembly cost by one half

### ■ Basic Part Number

- 2SD2623 × 2

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	25	V
Collector-emitter voltage (Base open)	$V_{CEO}$	20	V
Emitter-base voltage (Collector open)	$V_{EBO}$	12	V
Collector current	$I_C$	0.5	A
Peak collector current	$I_{CP}$	1	A
Total power dissipation	$P_T$	300	mW
Junction temperature	$T_j$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

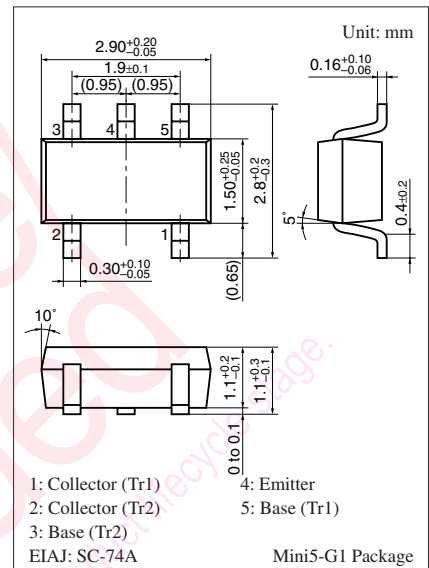
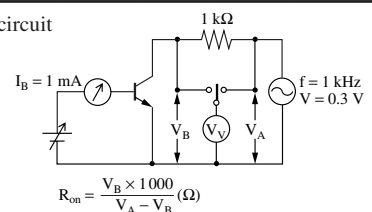
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	$I_C = 10 \mu\text{A}$ , $I_E = 0$	25			V
Collector-emitter voltage (Base open)	$V_{CEO}$	$I_C = 1 \text{ mA}$ , $I_B = 0$	20			V
Emitter-base voltage (Collector open)	$V_{EBO}$	$I_E = 10 \mu\text{A}$ , $I_C = 0$	12			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = 25 \text{ V}$ , $I_E = 0$			100	nA
Forward current transfer ratio *1	$h_{FE}$	$V_{CE} = 2 \text{ V}$ , $I_C = 0.5 \text{ A}$	200		800	—
$h_{FE}$ ratio *1, 2	$h_{FE(\text{Small})}$ $/h_{FE(\text{Large})}$	$V_{CE} = 2 \text{ V}$ , $I_C = 0.5 \text{ A}$	0.50	0.99		—
Collector-emitter saturation voltage *1	$V_{CE(\text{sat})}$	$I_C = 0.5 \text{ A}$ , $I_B = 20 \text{ mA}$		0.14	0.40	V
Base-emitter saturation voltage *1	$V_{BE(\text{sat})}$	$I_C = 0.5 \text{ A}$ , $I_B = 50 \text{ mA}$			1.2	V
Transition frequency	$f_T$	$V_{CB} = 10 \text{ V}$ , $I_E = -50 \text{ mA}$ , $f = 200 \text{ MHz}$		200		MHz
Collector output capacitance (Common base, input open circuited)	$C_{ob}$	$V_{CB} = 10 \text{ V}$ , $I_E = 0$ , $f = 1 \text{ MHz}$		10		pF
ON resistance *3	$R_{on}$			1.0		$\Omega$

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. \*1: Pulse measurement

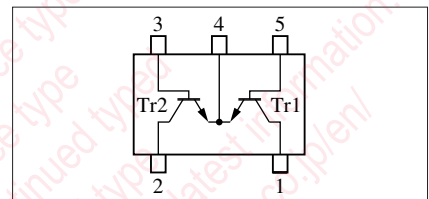
\*2: Ratio between one and another device

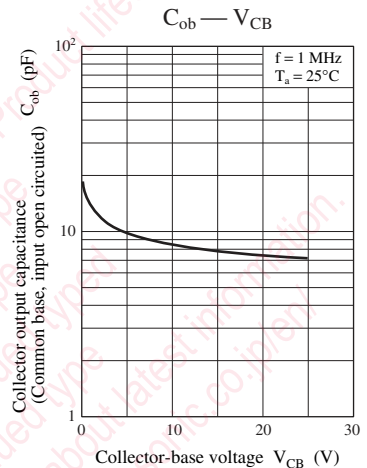
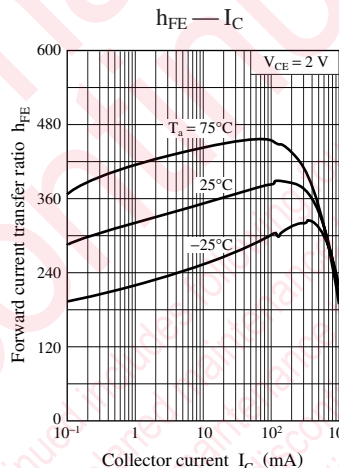
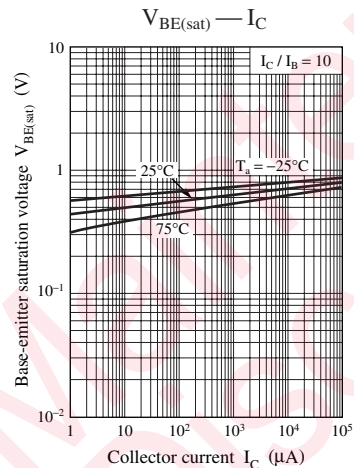
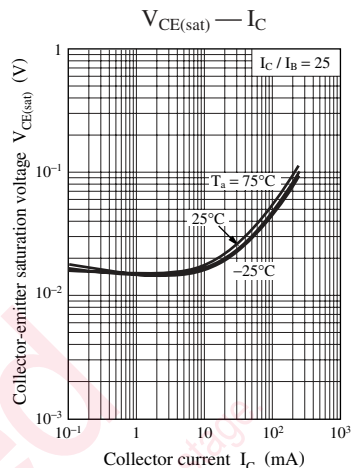
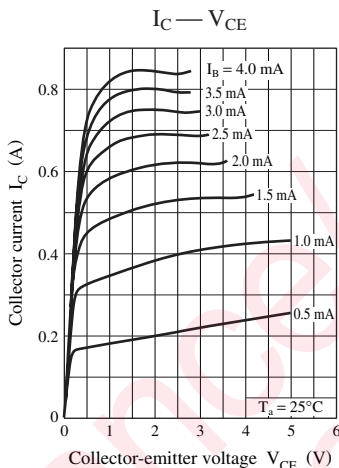
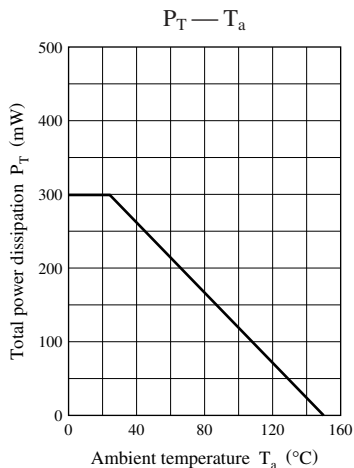
\*3:  $R_{on}$  test circuit



Marking Symbol: 4Z

Internal Connection





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