

MC100EP40

3.3V / 5V ECL Differential Phase-Frequency Detector

Description

The MC100EP40 is a three-state phase-frequency detector intended for phase-locked loop applications which require a minimum amount of phase and frequency difference at lock. Advanced design significantly reduces the dead zone of the detector. For proper operation, the input edge rate of the R and V inputs should be less than 5 ns. The device is designed to work with a 3.3 V / 5 V power supply.

When Reference (R) and Feedback (FB) inputs are unequal in frequency and/or phase the differential UP (U) and DOWN (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO.

When Reference (R) and Feedback (FB) inputs are 80 ps or less in phase difference, the Phase Lock Detect pin will indicate lock by a high state (V_{OH}). The V_{TX} (V_{TR} , $\overline{V_{TR}}$, V_{TFB} , $\overline{V_{TFB}}$) pins offer an internal termination network for 50 Ω line impedance environment shown in Figure 2. An external sinking supply of $V_{CC}-2$ V is required on V_{TX} pin(s). If you short the two differential pins V_{TR} and $\overline{V_{TR}}$ (or V_{TFB} and $\overline{V_{TFB}}$) together, you provide a 100 Ω termination resistance. For more information on termination of logic devices, see AND8020.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

For more information on Phase Lock Loop operation, refer to AND8040.

Special considerations are required for differential inputs under No Signal conditions to prevent instability.

Features

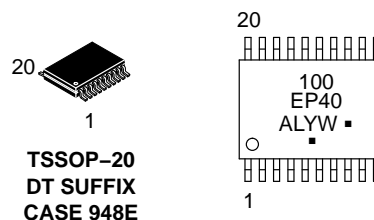
- Maximum Frequency > 2 GHz Typical
- Fully Differential
- Advanced High Band Output Swing of 400 mV
- Theoretical Gain = 1.11
- T_{rise} 97 ps Typical, F_{fall} 70 ps Typical
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC} = 3.0$ V to 5.5 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -3.0$ V to -5.5 V
- 50 Ω Internal Termination Resistor
- These are Pb-Free Devices



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MARKING DIAGRAM*



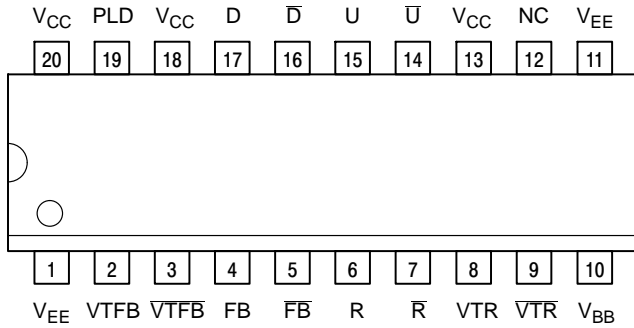
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)
*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View)

Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|-------------------|-----------------------------------|
| U, Ū | ECL Up Differential Outputs |
| D, D̄ | ECL Down Differential Outputs |
| FB, F̄B | ECL Feedback Differential Inputs |
| R, R̄ | ECL Reference Differential Inputs |
| PLD | ECL Phase Lock Detect Function |
| V _{TR} | ECL Internal Termination for R |
| V̄ _{TR} | ECL Internal Termination for R̄ |
| V _{TFB} | ECL Internal Termination for FB |
| V̄ _{TFB} | ECL Internal Termination for F̄B |
| V _{BB} | Reference Voltage Output |
| V _{CC} | Positive Supply |
| V _{EE} | Negative Supply |
| NC | No Connect |

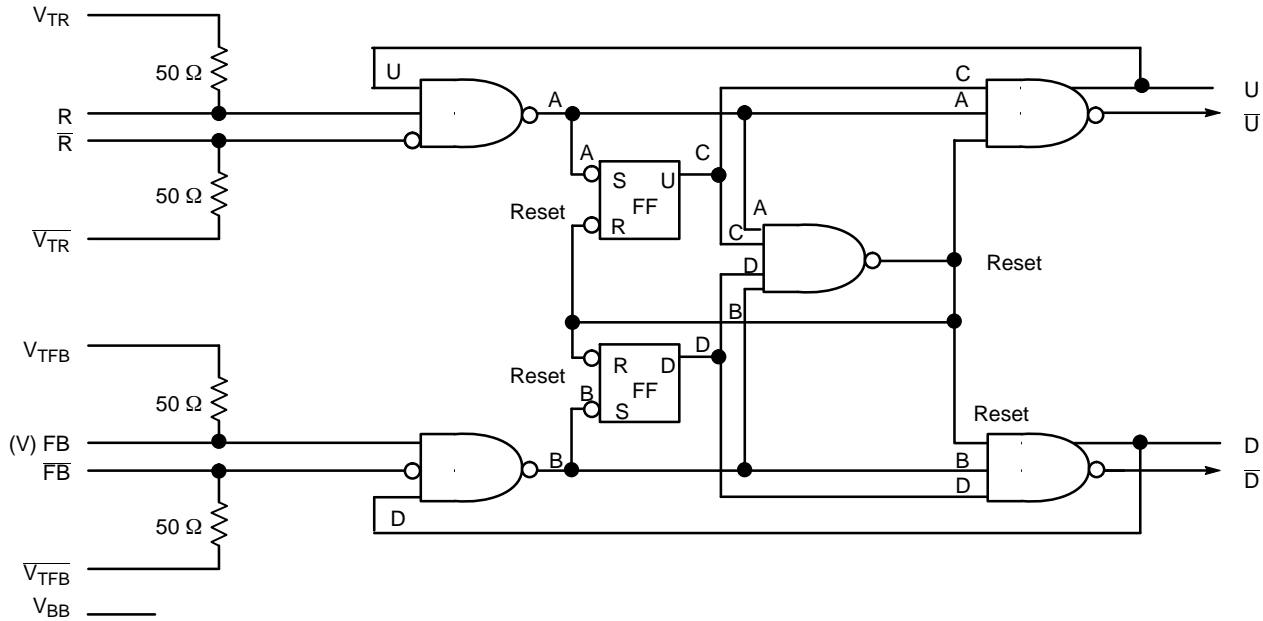


Figure 2. Logic Diagram

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Table 2. ATTRIBUTES

| Characteristics | Value | |
|---|------------------------|----------------------|
| Internal Input Pulldown Resistor | N/A | |
| Internal Input Pullup Resistor | N/A | |
| ESD Protection | Human Body Model | > 4 kV |
| | Machine Model | > 100 V |
| | Charged Device Model | > 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb Pkg | Pb-Free Pkg |
| | TSSOP-20 | Level 1 Level 3 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 699 Devices | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|-----------------------|----------------------------------|-------------|------|
| V _{CC} | PECL Mode Power Supply | V _{EE} = 0 V | | 6 | V |
| V _{EE} | NECL Mode Power Supply | V _{CC} = 0 V | | -6 | V |
| V _I | PECL Mode Input Voltage | V _{EE} = 0 V | V _I ≤ V _{CC} | 6 | V |
| | NECL Mode Input Voltage | V _{CC} = 0 V | V _I ≥ V _{EE} | -6 | V |
| I _{out} | Output Current | Continuous Surge | | 50 | mA |
| | | | | 100 | mA |
| I _{BB} | V _{BB} Sink/Source | | | ± 0.5 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm | TSSOP-20 | 140 | °C/W |
| | | 500 lfpm | TSSOP-20 | 100 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | TSSOP-20 | 23 to 41 | °C/W |
| T _{sol} | Wave Solder | Pb Pb-Free | | 265 | °C |
| | | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 4. 100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 2)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 100 | 128 | 160 | 100 | 130 | 160 | 110 | 140 | 170 | mA |
| V_{OH} | Output HIGH Voltage (Note 3) | 2225 | 2350 | 2475 | 2275 | 2400 | 2525 | 2300 | 2425 | 2550 | mV |
| V_{OL} | Output LOW Voltage (Note 3) U, \bar{U} , B, \bar{B} PLD | 1775 1305 | 1900 1480 | 2025 1605 | 1800 1305 | 1925 1480 | 2050 1605 | 1825 1305 | 1950 1480 | 2075 1605 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 2075 | | 2420 | 2075 | | 2420 | 2075 | | 2420 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 1305 | | 1675 | 1305 | | 1675 | 1305 | | 1675 | mV |
| V_{BB} | Output Voltage Reference | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 2.0 | | 3.3 | 2.0 | | 3.3 | 2.0 | | 3.3 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | -150 | | | -150 | | | -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -2.2 V.

3. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.

4. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. 100EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 5)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current (Note 6) | 100 | 128 | 160 | 100 | 130 | 160 | 110 | 140 | 170 | mA |
| V_{OH} | Output HIGH Voltage (Note 7) | 3925 | 4050 | 4175 | 3975 | 4100 | 4225 | 4000 | 4125 | 4250 | mV |
| V_{OL} | Output LOW Voltage (Note 7) U, \bar{U} , B, \bar{B} PLD | 3475 3005 | 3600 3180 | 3725 3305 | 3500 3005 | 3625 3180 | 3750 3305 | 3525 3005 | 3650 3180 | 3775 3305 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3775 | | 4120 | 3775 | | 4120 | 3775 | | 4120 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3005 | | 3375 | 3005 | | 3375 | 3005 | | 3375 | mV |
| V_{BB} | Output Voltage Reference | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 8) | 2.0 | | 5.0 | 2.0 | | 5.0 | 2.0 | | 5.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | -150 | | | -150 | | | -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.3 V to -2.2 V.

6. For $(V_{CC} - V_{EE}) > 3.3\text{ V}$, 5 Ω to 10 Ω in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend $V_{CC} - V_{EE}$ operation at $\leq 3.3\text{ V}$.

7. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.

8. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 6. 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$; $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 9)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|---|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current (Note 10) | 100 | 128 | 160 | 100 | 130 | 160 | 110 | 140 | 170 | mA |
| V_{OH} | Output HIGH Voltage (Note 11) | -1075 | -950 | -825 | -1025 | -900 | -775 | -1000 | -875 | -750 | mV |
| V_{OL} | Output LOW Voltage (Note 11) U, \bar{U} , B, \bar{B} PLD | -1525 -1995 | -1400 -1820 | -1275 -1695 | -1500 -1995 | -1375 -1820 | -1250 -1695 | -1475 -1995 | -1350 -1820 | -1225 -1695 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1225 | | -880 | -1225 | | -880 | -1225 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1995 | | -1625 | -1995 | | -1625 | -1995 | | -1625 | mV |
| V_{BB} | Output Voltage Reference | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 12) | $V_{EE} + 2.0$ | | 0.0 | $V_{EE} + 2.0$ | | 0.0 | $V_{EE} + 2.0$ | | 0.0 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | -150 | | | -150 | | | -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Input and output parameters vary 1:1 with V_{CC} .

10. For $(V_{CC} - V_{EE}) > 3.3\text{ V}$, $5\ \Omega$ to $10\ \Omega$ in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend $V_{CC} - V_{EE}$ operation at $\leq 3.3\text{ V}$.

11. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

12. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V}$ to -5.5 V or $V_{CC} = 3.0\text{ V}$ to 5.5 V ; $V_{EE} = 0\text{ V}$ (Note 13)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit | |
|--------------------------|---|--------------|-----|------|------|-----|------|------|-----|------|------|----|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| f_{max} | Maximum Frequency (Figure 3) | | > 2 | | | > 2 | | | > 2 | | GHz | |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential FB to D/U R to D/U | 400 | 525 | 700 | 410 | 550 | 750 | 450 | 575 | 775 | ps | |
| t_{JITTER} | Random Clock Jitter (Figure 3) | | 0.2 | < 1 | | 0.2 | < 1 | | 0.2 | < 1 | ps | |
| V_{PP} | Input Voltage Swing (Differential Configuration) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV | |
| t_r , t_f | Output Rise/Fall Times (20% – 80%) | Q, \bar{Q} | 60 | 85 | 130 | 60 | 110 | 150 | 80 | 120 | 160 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

13. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC100EP40

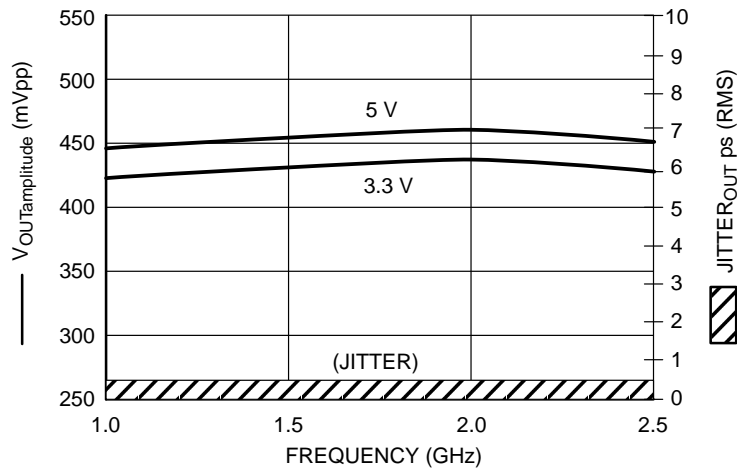


Figure 3. $F_{max}/Jitter @ 25^{\circ}C$

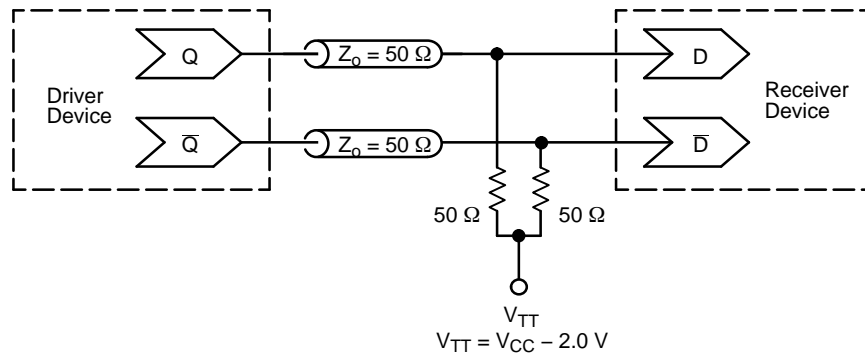


Figure 4. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

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ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|-----------|--------------------|
| MC100EP40DTG | TSSOP-20* | 75 Units / Rail |
| MC100EP40DTR2G | TSSOP-20* | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

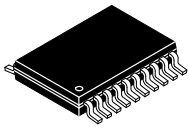
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

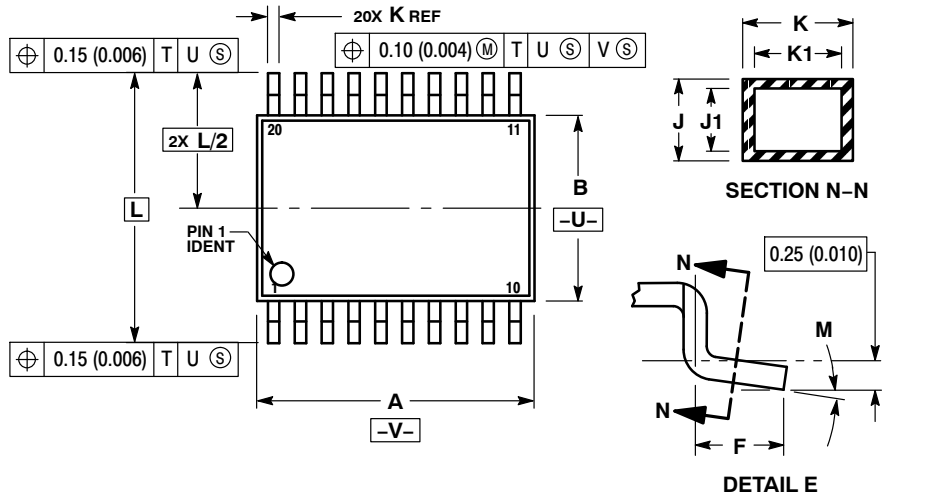
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TSSOP-20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

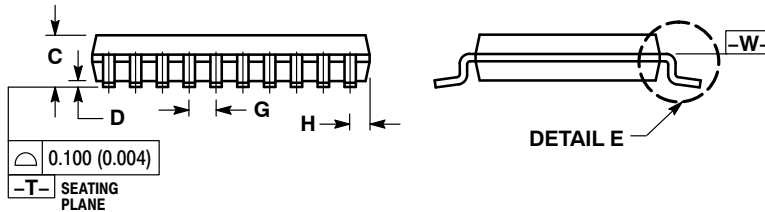
SCALE 2:1



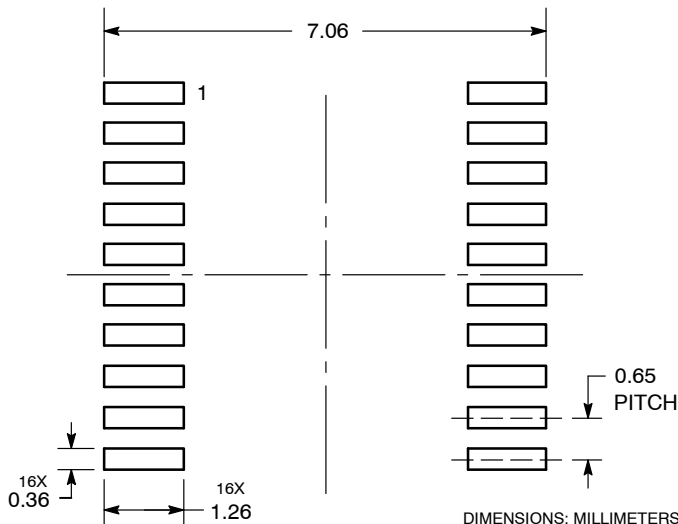
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

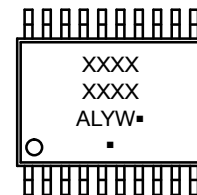
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |



SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
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