# AMD-8132™ HyperTransport™ PCI-X® 2.0 Tunnel Product Summary

## Overview

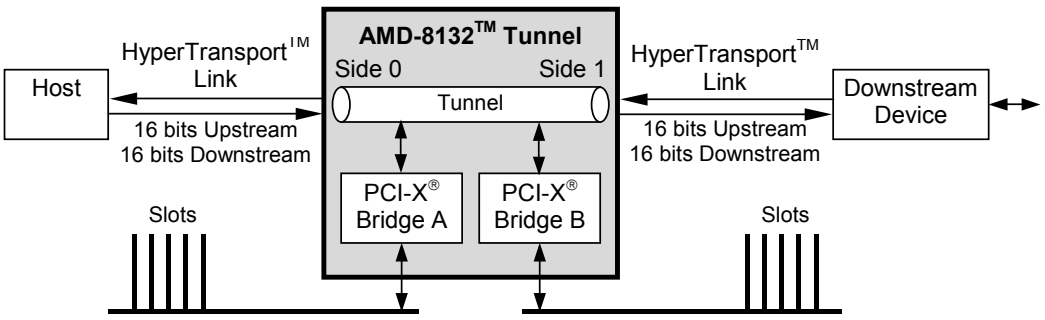
The AMD-8132™ HyperTransport™ PCI-X®2.0 tunnel developed by AMD provides two PCI-X bridges supporting DDR transfer rates. The AMD-8132 tunnel is compliant with *HyperTransport™ I/O Link Specification, Rev 2.0* including errata up to specification Rev 1.05c. The package is a 31 x 31 millimeter, 829 ball, flip-chip organic BGA. The core is 1.2 volts. Power dissipation is 8 watts.

**HyperTransport™ Features:**

- HyperTransport tunnel with side 0 16-bit input/ 16-bit output and side 1 16-bit input/16-bit output.
- Either side can connect to the host or to a downstream HyperTransport technology compliant device.
- Each side supports HyperTransport technology-defined reduced bit widths: 8-bit, 4-bit, and 2-bit.
- Each side supports transfer rates of 2000, 1600, 1200, 1000, 800, and 400 mega-bits per second per wire.
- Maximum bandwidth is 8 gigabytes per second across each side (half upstream and half downstream).
- Independent transfer rate for each side and each direction.
- Independent bit width selection for each side and each direction.
- Link disconnect protocol support.
- HyperTransport interrupt control support.
- 64-bit address support.

**PCI-X® Features:**

- Two PCI-X bridges: bridge A and bridge B.
  - Each bridge supports a 64-bit data bus.
  - Each bridge supports operational Modes 1 and 2 of PCI-X and conventional PCI protocol.
  - In PCI-X Mode 2, bridges support transfer rates of 266 and 200 MHz.
  - In PCI-X Mode 1, bridges support transfer rates of 133, 100, 66, and 50 MHz.
  - In PCI mode, bridges support transfer rates of 66, 50, 33, and 25 MHz.
  - Independent transfer rates and operational modes for each bridge.
  - Each bridge includes support for up to 5 PCI masters with clock, request, and grant signals.
  - Each bridge includes a HyperTransport™ technology compliant interrupt controller. Legacy interrupt controller and IOAPIC modes are also supported.
  - Each bridge can receive PCI device interrupts via INTA/B/C/D pins or via MSI/MSI-X transactions.
  - SHPC-compliant hot-plug controller and support.
- PCI-X Mode 2, 1.5 V link signaling. PCI-X Mode 1, 3.3 V link signaling. PCI, 3.3 V link signaling.




**Example system block diagram.**

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# Revision History

| Rev | Date | Description |
|---|---|---|
| 3.07 | 07/2005 | Fourth public release<br>Updated default register values in Chapter 3 to include revision B2 silicon. Bx indicates that a value is used for revision B1 and revision B2.<br>Updates since Revision 3.00 are marked with revision bars. |
| 3.05 | 06/2005 | Third public release.<br>Updated the OPN on page 195. |
| 3.02 | 04/2005 | Second public release.<br>Updates since Revision 3.00 are marked with revision bars. |
| 3.0 | 03/2005 | Initial public release. |

# Preface

This manual provides the technical specifications for the AMD-8132™ HyperTransport™ PCI-X®2.0 tunnel. Users of this document are expected to be familiar with current revs of the HyperTransport™ I/O link, PCI, and PCI-X protocols.

## References and Resources

*HyperTransport™ I/O Link Specification, Rev 2.0*

*PCI-X Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a*

*PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification, Rev 2.0a*

*PCI Local Bus Specification, Rev 2.3*

*PCI Hot-Plug Specification, Rev 1.1*

*PCI Bus Power Management Interface Specification, Rev 1.1*

*PCI-to-PCI Bridge Architecture Specification, Rev 1.2*

*PCI Standard Hot-Plug Controller and Subsystem Specification, Rev 1.0*

*TPS2340A Dual-Slot PCI Hot-Plug Power Controller Product Data*

*82093AA I/O Advanced Programmable Interrupt Controller (IOAPIC) Product Data*

## Conventions

- HyperTransport, HyperTransport™ technology, and HyperTransport™ all refer to the same technology (formerly LDT).
- For any signal, the suffix _L indicates it is an active low.
- [B,A] in the signal name refers to the B and A PCI bridges or buses.
- [1,0] in the signal name refers to sides 1 and 0 of the tunnel.
- [H,L] are the signals associated with the positive and negative sides of differential pairs.
- Configuration register sets are provided for each logical bridge. Configuration register locations are referenced with mnemonics that take the form of Dev[A|B]:[7:0]x[FF:0] where the first bracket contains the bridge, the second bracket contains the function number, and the last bracket contains the offset.

# Acronyms and Terms

| Acronym/Term | Description |
|---|---|
| ADQ | A 128-byte aligned data quantum as defined by the PCI-X specification, rev 2.0a. |
| Cell | 32 bits of CAD aligned to a 32-bit boundary in the HyperTransport™ protocol with associated CTL bit. |
| CFF | Clock Forwarding FIFO. |
| DDR | In the case of PCI-X® Mode 2, this data transfer rate is two times the common clock. |
| DEST | Destination. |
| DM | Interrupt destination mode. |
| DS | Downstream, away from the host bridge. Also Delivery Status. |
| DW | 32 bits. |
| GCM | Link interface cycle manager. |
| IM | Interrupt Mask. |
| IOAPIC | I/O Advanced Programmable Interrupt Controller. |
| IRR | Interrupt Request Register. |
| IV | Interrupt Vector. |
| LI | AMD-8132™ tunnel HyperTransport™ interface. This interface is the data/command transfer mechanism between the links and the bridges. |
| LR[0,1] | Link receive module. |
| LT[0,1] | Link transmit module. |
| Link | Connection between two HyperTransport™ devices. |
| MT | Interrupt message type. |
| PD | Pulldown. |
| PHY | The physical interface layer of the AMD-8132™ tunnel. |
| POL | Polarity. |
| PU | Pullup. |
| RDR | Interrupt redirection register. |
| SDR | Single Data Rate. This data transfer rate is one time the common clock. |
| SHPC | Standard Hot-Plug Controller |
| TM | Interrupt trigger mode. |

| Acronym/Term | Description |
|---|---|
| TPS* | Combinatorial reference indicating both the TPS2340A and TPS2342 Texas Instruments hot-plug controllers. |
| US | Upstream, toward the host bridge. |

# Chapter 1 Functional Operation

## 1.1 Overview

The AMD-8132™ HyperTransport™ PCI-X®2.0 tunnel provides interfaces to HyperTransport and to PCI-X.

The AMD-8132 tunnel contains a HyperTransport tunnel as defined in the *HyperTransport™ IO Link Specification, Rev. 2.0*. This tunnel consists of two HyperTransport interfaces: side 0 and side 1. HyperTransport packets can be passed through from one interface to the other (tunneled), or they can be accepted and responded to by this device.

The AMD-8132 tunnel contains two HyperTransport-to-PCI-X bridges as defined in the *HyperTransport™ Link Specification, Rev. 2.0; PCI Local Bus Specification, Rev 2.3*; *PCI-X Protocol Addendum to the PCI Local Bus Specification, Rev. 2.0a*; and *PCI-to-PCI Bridge Architecture Specification, Rev 1.2*.

HyperTransport packets can be accepted by the AMD-8132 tunnel and passed to one of the two PCI-X buses (bridged), or routed to configuration registers in each bridge.

PCI-X transactions can be accepted by the AMD-8132 tunnel and passed to the HyperTransport chain.

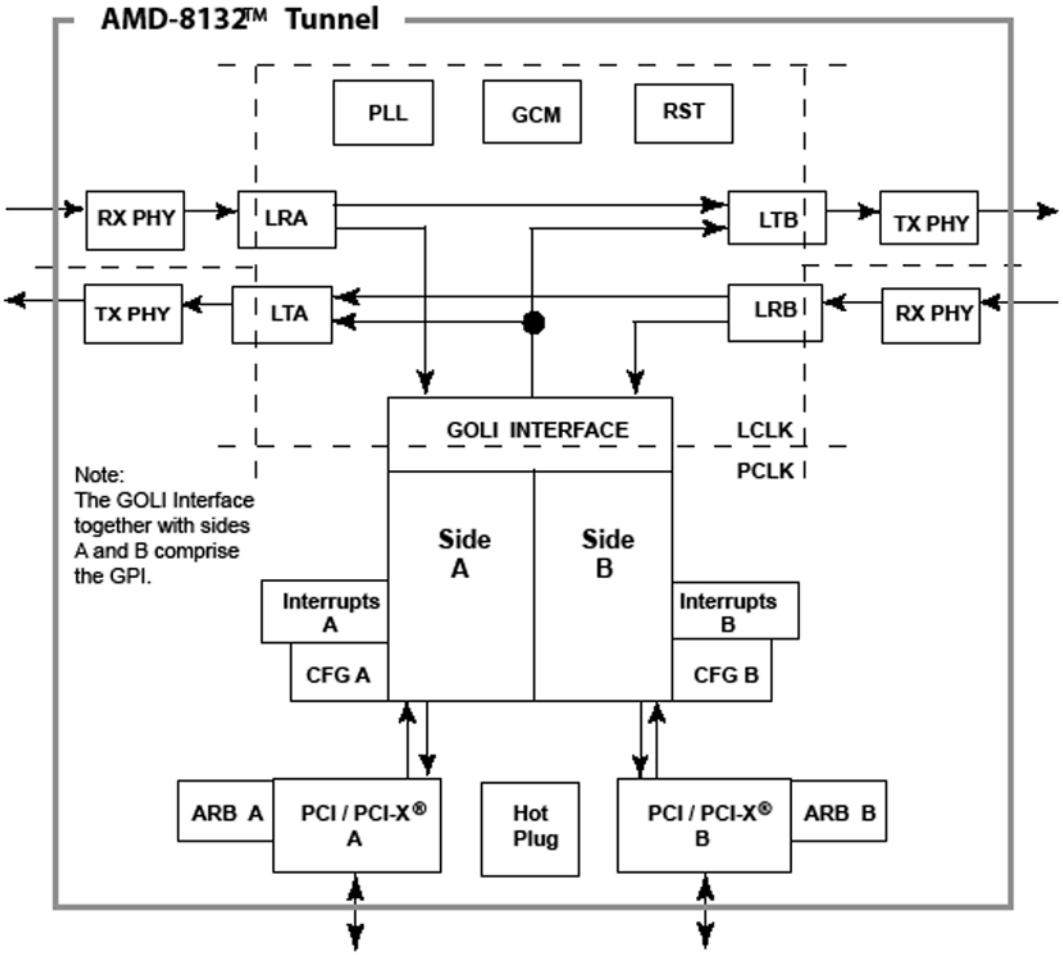
To system software, the AMD-8132 tunnel appears to contain two PCI devices, each of which contains a PCI-to-PCI bridge header as defined in the *PCI-to-PCI Bridge Architecture Specification, Rev 1.2*, with additions as defined in the *PCI-X Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a*. Each bridge actually bridges between a HyperTransport chain (the primary bus) and a PCI-X bus (the secondary bus).

The AMD-8132 tunnel can be connected to the HyperTransport host device through either the side 0 or the side 1 HyperTransport link interface; this is the upstream link. The AMD-8132 tunnel can be attached directly to the host device, or there can be a chain of one or more additional HyperTransport tunnels between the upstream link and the host device. The other HyperTransport link interface on the AMD-8132 tunnel, the downstream link, may or may not be connected to another device or chain of devices.

Host-initiated transactions that do not target the AMD-8132 tunnel or the bridge flow through the tunnel to the downstream device if one exists. Transactions claimed by the device are passed to internal registers or to one of the PCI-X bridges.

- See section 3.1 for details about the software view of the AMD-8132 tunnel.
- See section 3.1.2 for a description of the register naming convention.
- See the *AMD-8132™ HyperTransport™ PCI-X® 2.0 Tunnel Design Guide* for additional information.

**Figure 1. AMD-8132™ Tunnel: Block Diagram**



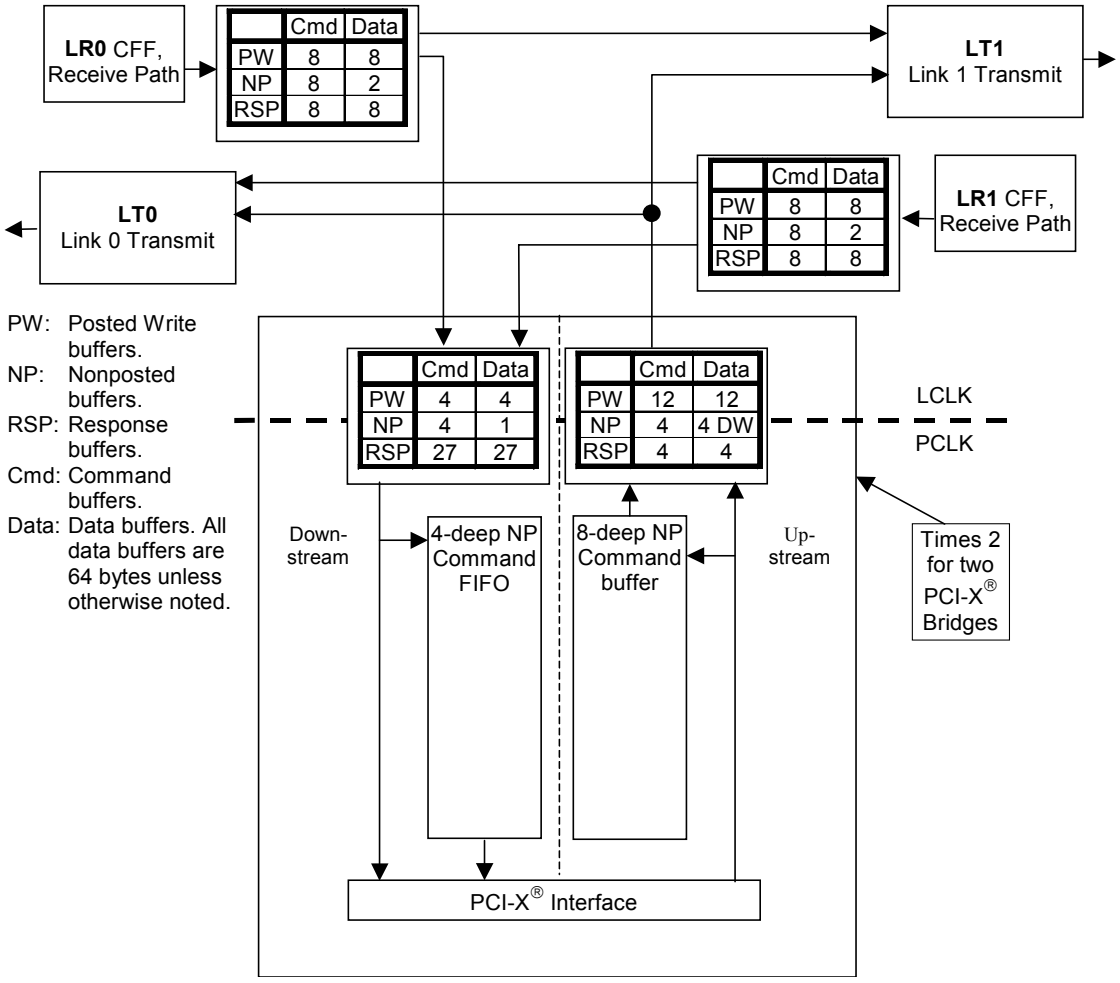

In the Figure 1 block diagram:

- ARB [B,A] - Internal arbiter for the PCI bus.
- CFG [B,A] - Control and status registers for bridge [B,A].
- GCM - Link interface cycle manager.
- GPI - Bridge functions between the HyperTransport primary bus and the PCI/PCI-X secondary buses, split into a bridge B and a bridge A.
- Hot-Plug - Interfaces to the external TPS2340A or TPS2342 hot-plug power controller and provides SHPC functions.
- INT [B,A] - Interrupts/IOAPIC for bridge [B,A].
- LRx - HyperTransport receive logic.
- LTx - HyperTransport transmit logic.
- PCI/ PCI-X [B,A] - Interface and protocol state machines for PCI/PCI-X buses.
- PLL - PLL that generates the core clock (LCLK) and the PCI clocks.
- RST - Module that handles reset and device initialization.
- RX PHY - HyperTransport link receive physical layer.

- TX PHY - HyperTransport link transmit physical layer.

Figure 2 shows buffers in the AMD-8132 tunnel.

**Figure 2. Link Buffer Diagram**




# 1.2 Tunnel Links

## 1.2.1 Link Frequency

Each HyperTransport link supports transmit clock frequencies of 200, 400, 500, 600, 800, and 1000 MHz. Side 0 and side 1 frequencies are independent of each other. The links can operate in asynchronous mode, as defined in *HyperTransport™ I/O Link Specification, Rev 2.0* up to a maximum of 1000 MHz receive clock rate. On cold reset, each link begins transmitting at 200 MHz and then can be reprogrammed for higher clock rates per *HyperTransport™I/O Link Specification, Rev 2.0*.

### 1.2.2 Link Width

Each HyperTransport link supports 2-bit, 4-bit, 8-bit, and 16-bit widths. Side 0 and side 1 widths are independent of each other. On cold reset, each link initializes its width as specified in the *HyperTransport™ I/O Link Specification, Rev 2.0* and then can be reprogrammed.

### 1.2.3 Link Behavior

After a cold or warm reset, the AMD-8132 tunnel initializes its base UnitID (see DevA:0xC0 in section 3.2) to 0. At this point it responds to HyperTransport configuration accesses to device 0 or 1, and passes any other HyperTransport commands on to the other link if the other HyperTransport link is active. Once the base UnitID register is initialized, the AMD-8132 tunnel responds to configuration accesses to this UnitID or this UnitID+1.

All HyperTransport memory or I/O operations pass through to the other HyperTransport link until the appropriate address ranges are programmed into the AMD-8132 tunnel. See section 3.2 PCI-X® Bridge Configuration Registers for details.

The first write to the base UnitID also sets the master host bit to point to the link that received this write, which also determines the default location of the upstream link.

### 1.2.4 Link PHY and Compensation

The electrical specification in *HyperTransport™I/O Link Specification, Rev 2.0* requires an on-die differential termination as well as tightly controlled output impedance. The HyperTransport PHY used in the AMD-8132 tunnel maintains tight control of these parameters, regardless of temperature, voltage, or process variations. The HyperTransport PHY accomplishes this by the use of compensation circuitry. Each HyperTransport link has balls which are connected to external calibration resistors. By default, the PHY periodically samples calibration values and updates the receive and transmit parameters.

## 1.3 PCI-X®2.0 Bridges

The AMD-8132 tunnel includes two 64-bit PCI-X bridges, bridge A and bridge B. See Figure 1.

- Each bridge independently supports conventional PCI mode, or PCI-X Mode 1 or Mode 2.
- Each bridge independently supports clock speeds of 25, 33, 50, 66, 100, 133 MHz; and DDR with the common clock at 100 or 133 MHz.
- Each bridge independently supports SHPC-compatible hot-plug.
- Each bridge includes an interrupt controller register set.
- Each bridge supports 64-bit addressing in PCI-X and conventional PCI modes.

## 1.3.1 Arbiters

### 1.3.1.1 Internal Arbiters

Each bridge contains a PCI/PCI-X arbiter with five request/grant pairs available for each bus. Only a subset of these request/grant pairs are available for hot-plug, 66 MHz PCI, PCI-X Mode 1, or PCI-X Mode 2 operation. See section 4.2.3 for more details.

Depending on the current mode of the bus, the arbiter operates as a conventional PCI arbiter, a PCI-X Mode 1 arbiter, or a PCI-X Mode 2 arbiter. In PCI-X Mode 2 there are CSRs controlling the number of idle cycles before the arbiter goes into low-power mode. See section 3.2, Dev[B,A]:0x48.

The arbiter arbitrates between the external requests, represented by [B,A]_REQ_L[4:0], and internal requests. Internal requests are generated when:

- A HyperTransport operation is accepted by the bridge and will be forwarded to the PCI bus (the bridge wants to be master on the PCI bus).
- A hot-plug command occurs which requires the SHPC to own the PCI bus.

When no internal or external requests are asserted to the arbiter, it parks (asserts a grant) to one master in order to keep the bus from floating. The choice of master is controlled by Dev[B,A]:0x48[PARKATHOST].

### 1.3.1.2 External Arbiters

An external arbiter can be used in all PCI and PCI-X modes except for PCI-X Mode 2. The internal arbiter for the AMD-8132 tunnel can be disabled and an external customer-supplied arbiter used instead. Disabling the internal arbiter can be done on a per PCI bus basis using the setting for EXTARB_L at Dev[B,A]:0x48.

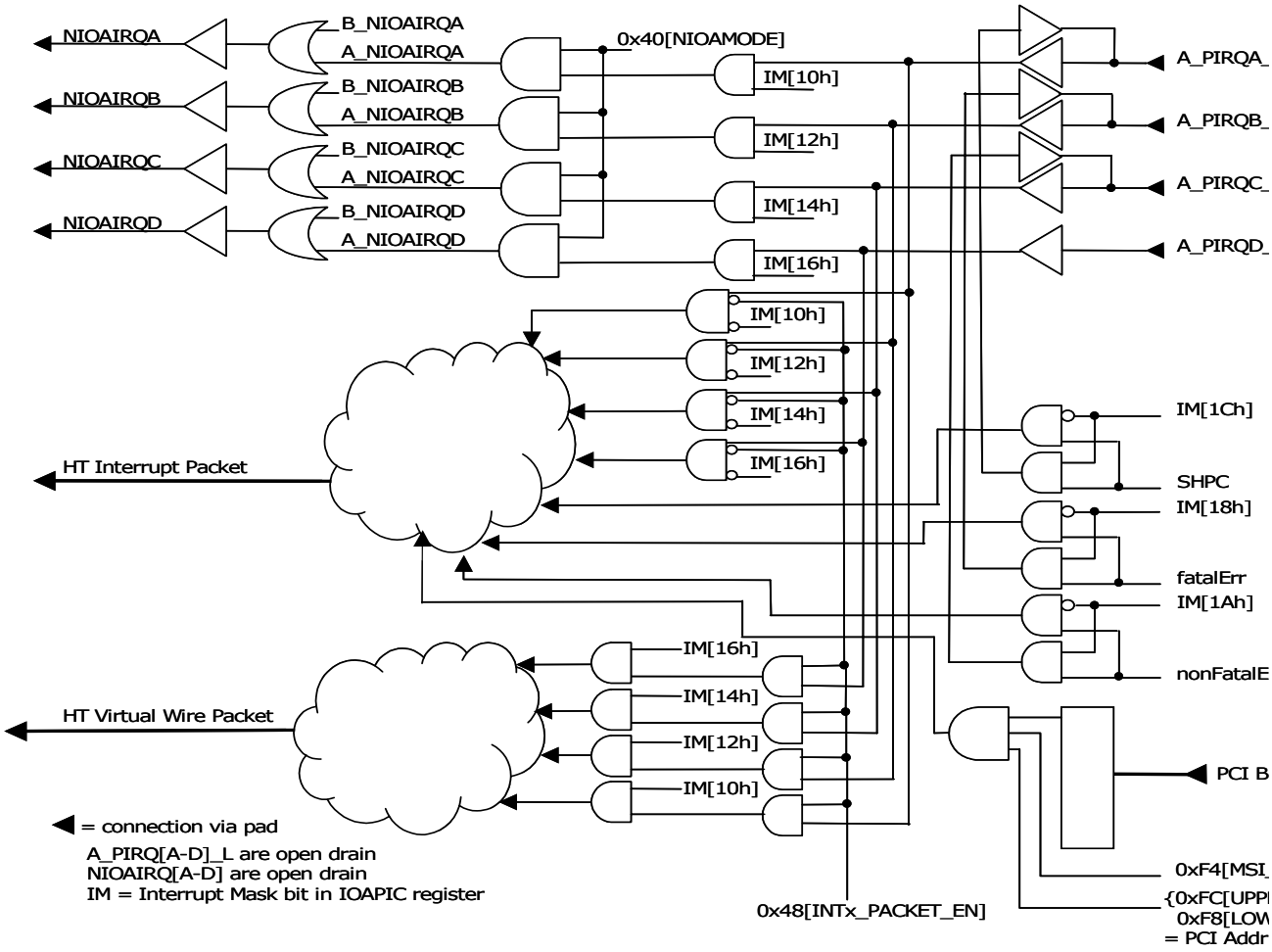
In external arbiter mode, the AMD-8132 tunnel produces a non-preemptable and a preemptable request.

- A non-preemptable request is a request to own the PCI bus for hot-plug. Once asserted, the external arbiter must keep its non-preemptable grant asserted until the AMD-8132 tunnel deasserts its non-preemptable request. The external arbiter should not park the bus on this grant line. The non-preemptable request comes out on the signal [B,A]_GNT_L1. The non-preemptable grant from the external arbiter is driven to the AMD-8132 tunnel on the signal [B,A]_REQ_L1. If this bus is not enabled for hot-plug, the non-preemptable request/grant lines do not need to be implemented and this grant line should be pulled high.
- A preemptable request is a request to own the PCI bus for normal usage. The preemptable request and grant behave as normal PCI or PCI-X request and grant signals. The preemptable request comes out on the signal [B,A]_GNT_L0. The preemptable grant from the external arbiter is driven to the AMD-8132 tunnel on the signal [B,A]_REQ_L0.

## 1.3.2 Interrupts

The AMD-8132 tunnel has capabilities to handle internal and external interrupts. It contains a standard IOAPIC and can accept Message Signalled Interrupts (MSIs) from the PCI buses. Incoming interrupts can result in HyperTransport interrupt packets, HyperTransport virtual wire packets, or assertions of the NIOAIRQ pins. Figure 3 shows interrupt routing possibilities.

**Figure 3. AMD-8132™ Tunnel Interrupt Routing**




## 1.3.2.1 Interrupt Discovery and Configuration

The HyperTransport interrupt discovery and configuration capability block defines the mechanism for declaring the number of interrupt sources for each bridge and allows software to configure each interrupt independently. Each bridge has its own capability block to facilitate mapping interrupt sources to HyperTransport interrupt packets. If existing software cannot use this mapping, then see *HyperTransport™I/O Link Specification, Rev 2.0,* Appendix F.1.4 and section 3.6 herein for APIC compatible interrupt configuration. This alternative method of configuring and mapping interrupts utilizes a standard set of IOAPIC registers. Each bridge has an associated set of IOAPIC registers that includes a standard PCI function header (function 1 of each bridge) and memory mapped registers. This mapping provides an alternate way to access a subset of the interrupt discovery and configuration register set.

Each bridge supports the four PCI-defined interrupt signals, [B,A]_PIRQ[D,C,B,A]_L. Assertion of these interrupt signals may be converted to link interrupt request messages or cause assertion of the

NIOAIRQ[D:A]_L pins. It is expected that system BIOS sets both Dev[B,A]:0x40[NIOAMODE] bits and that the interrupt is determined by the way the operating system programs the interrupt mask bit RDR[IM] of the redirection registers. Non IOAPIC-capable operating systems will not modify the indexing and mask bits of the redirection registers RDR[IM] and interrupts will continue to be delivered through NIOAIRQ[D:A]_L assertions or Virtual Wire INTx packets, as set up by the BIOS. IOAPIC-capable operating systems clear the mask bits resulting in interrupt request messages to the host. The NIOAIRQ[D:A]_L signals from all instances of the AMD-8132 tunnel on a platform can be connected together; respectively: A to A, B to B, etc. These four nodes are expected to be passed to the system's legacy interrupt controller to generate interrupts on behalf of the AMD-8132 tunnel bridges when IOAPIC interrupts are not supported.

Typically for PCI interrupts, the redirection register (RDR; see section 3.6) is set up as follows: MT = fixed; DM = physical mode; POL = active low; TM = level sensitive; and IM = not masked. The RDR fields are mapped into link interrupt request messages as follows:

| RDR Field | Field in HyperTransport Link Packet |
|---|---|
| IV[7:0] (Interrupt Vector) | Vector (bit time 5) |
| MT[2:0] (Message Type) | MT[2:0] (bits[4:2] of bit time 3); MT[3] (bit[7] of bit time 3) should always be low. The encoding of these bits changes between the value in the RDR and the value placed into the link packet because HyperTransport and the APIC standard use different encodings for MT. |
| DM (Destination Mode) | DM (bit[6] of bit time 3) |
| TM (Trigger Mode) | RQEOI (bit[5] of bit time 3) |
| DEST[7:0] (Destination) | IntrInfo[15:8] (bit time 4); IntrInfo[55:16] should always be low. |

DS, POL, IRR, and IM from the RDR are not included in the HyperTransport link interrupt packet.

The state of PASSPW and INTRINFO[55:24, 7] from the IDRDR register (see Dev[B,A]:0x[BC, B8]) are also passed along in the link interrupt packet.

If RDR[TM] = level sensitive for the interrupt request, then the IRR register is set when the interrupt is detected. After the interrupt request message is sent to the host, the host is required to generate an EOI broadcast or CSR write message when finished with that interrupt. IRR is cleared in any RDRs in either bridge with IDRDR/RDR fields that match the IntrInfo fields of the EOI broadcast as follows:

| IntrInfo[15:8] | Match fields |
|---|---|
| 00h | IntrInfo[31:16] = {IDRDR[31:24], RDR/IDRDR[IV]} |
| 01h-FFh | IntrInfo[31:8] = {IDRDR[31:24], RDR/IDRDR[IV], RDR/IDRDR[DEST]} |

If the interrupt signal is still asserted when the corresponding RDR logic receives an IRR-clearing EOI, then IRR is immediately set again and a new interrupt request message is sent. If the interrupt signal is deasserted near the time the corresponding IRR-clearing EOI is received, then it is undefined whether an additional interrupt request message is sent. If RDR[TM] = edge sensitive, then the state of the IRR bit is not specified and the RDR logic for that interrupt does not observe EOIs.

Each RDR in the AMD-8132 tunnel operates independently. If interrupts are received simultaneously by two RDR controllers, then the corresponding interrupt request messages from each are transmitted in an unspecified order. If LDTSTOP_L is asserted near the time that an interrupt is asserted, then the corresponding

interrupt request message may or may not be sent before the disconnect sequence completes. If it is not sent before the disconnect sequence completes, then it is not dropped; it is sent after the link is re-connected.

External devices are required to assert PIRQ[D:A]_L for at least 3 PCLK cycles in order to guarantee that the AMD-8132 tunnel detects the assertion, regardless of the state of the corresponding RDR[TM] field.

### 1.3.2.2 SHPC_INTR and Fatal/Nonfatal Interrupts

In addition to the four PCI interrupt pins on each PCI bus, each bridge contains three internal signals that can generate interrupts. These are the SHPC_INTR signal and the fatal and nonfatal error signals. For each of these three signals there is an Interrupt Definition register/IOAPIC entry, yielding a total of seven for each bridge. See section 3.7 for more about SHPC_INTR. See Chapter 5 for more about error reporting.

### 1.3.2.3 Message Signalled Interrupts (MSI/MSI-X)

The AMD-8132 tunnel responds to MSIs (as specified in *PCI Local Bus Specification, Rev 2.3,* section 6.8) and MSI-Xs (as specified in *PCI Local Bus Specification, Rev 3.0,* section 6.8) with the following restriction imposed by HyperTransport:

MSI/MSI-X transactions are treated as such only if Dev[B,A]:0xF4[MSI_ENABLE] is set and if bits [63:20] of the address match the address created by concatenating Dev[B,A]:0xFC[UPPER_ADDRESS] with Dev[B,A]:0xF8[LOWER_ADDRESS]. Otherwise, they are treated as posted memory writes.

MSI/MSI-X transactions result in a HyperTransport interrupt packet. The address and data from the MSI/MSI-X transaction are distributed across that packet according to Table 1.

**Table 1. MSI/MSI-X Mapping: PCI to HyperTransport™**

| MSI/MSI-X Field | HyperTransport™ Interrupt Field |
|---|---|
| Address[2], Data[15,10:8] | IntrInfo[6:2] (x86 DM, RQEOI, MT[2:0]) |
| Address[19:12] | IntrInfo[15:8] (x86 Destination[7:0]) |
| Data[7:0] | IntrInfo[23:16] (x86 Vector) |
| Address[11:4] | IntrInfo[39:32] (x86 Destination[15:8]) |
| Address[30:20] | IntrInfo[50:40] (x86 Destination[26:16]) |
| Address[3] | IntrInfo[51] (x86 Destination[27]) |
| Data[14:11] | IntrInfo[55:52] (x86 Destination[31:28]) |

**Notes:**
1. Data[15]/IntrInfo[5] (x86 RQEOI) must be set to 0 by software in PCI and PCI-X devices because they do not receive HyperTransport EOI (End of Interrupt) broadcasts.
2. Data[10:8]/IntrInfo[4:2] (x86 Message Type) can be either 000b for fixed destination delivery or 001b for lowest priority delivery.
3. IntrInfo[7] (x86MT[3]) is 0b.
4. IntrInfo[31:24] is F8h.

For more information see *PCI Local Bus Specification, Rev 2.3,* section 6.8.

#### 1.3.2.4 INTx Virtual Wire Messages

There is an alternative method of delivering interrupt information over HyperTransport. Transitions on the PCI interrupt pins can cause INTx virtual wire packets to be issued on the upstream HyperTransport link instead of HyperTransport interrupt packets. Generation of INTx virtual wire packets is enabled with Dev[B,A]:0x48 [INTx_PACKET_EN].

### 1.3.3 Write Chaining

Write chaining refers to issuing two or more write requests from the HyperTransport bus as a single PCI or PCI-X operation. Write chaining is used to maximize available PCI or PCI-X bandwidth by avoiding the protocol overhead of issuing multiple operations that would each have its own address/attribute phases, wait states, and turnaround cycles.

The AMD-8132 tunnel implements chaining posted WrSized requests from the HyperTransport bus under the following conditions:

- The writes must be posted Doubleword WrSized requests (as opposed to byte-sized requests) that are all targeted to the same secondary PCI or PCI-X bus below the AMD-8132 tunnel. Doubleword WrSized requests from one to sixteen doublewords in size can be chained.
- The address of the last doubleword of one write must be adjacent to the address of the first doubleword of the subsequent write. The addresses spanned by the writes must not cross a 128-byte (32-doubleword) address boundary; e.g., a PCI-X ADB, although this restriction also applies to conventional PCI secondary buses.
- For the targeted AMD-8132 tunnel bridge, the WriteChainEnable bit Dev[B,A]:0x40[31] must be set.
- The data for all writes must have been received by the AMD-8132 tunnel internal buffers. A write whose data is still being transferred across the HyperTransport bus won't be chained.
- The writes must not have the COMPAT bit set in the HyperTransport request.
- The writes must not have data errors, or the Downstream Post Data Error Disable bit DevA:0xDC[6] must be set.
- The PassPW, UnitID, SeqID, Isoc, and Coherent attributes in the HyperTransport request packets must be the same for all writes in the chain.

If these conditions are all true when the AMD-8132 tunnel posted channel for one of its bridges wins internal arbitration over the nonposted and response channels to issue its traffic to the PCI or PCI-X bus, up to four WrSized requests from the HyperTransport bus are issued as as a single PCI Memory Write or Memory Write and Invalidate or PCI-X Memory Write Block operation.

### 1.3.4 Prefetching In Conventional PCI Mode

Prefetching refers to the acquisition of memory read data from the host prior to the master’s request for the data. When using the internal arbiter, prefetching in conventional PCI mode is enabled on a per-master basis through Dev[B,A]:0x40[PFEN[4:0]_L]. When using an external arbiter, the prefetching logic cannot distinguish between masters and all traffic is treated as if coming from master 0.

The following are definitions used in the rules for prefetching:

- Memory Read: any of the three PCI commands for reading memory - MR (Memory Read), MRL (Memory Read Line), or MRM (Memory Read Multiple). In this section, memory read is a collective term for all three types of reads. When a specific type of memory read is meant, its acronym is used.

- Burst Request: a cycle in which FRAME_L is held asserted during the first clock in which IRDY_L is asserted, indicating the master wishes to transfer more than one beat of data. In the event that STOP_L is asserted before IRDY_L asserts, FRAME_L always deasserts as IRDY_L asserts (*PCI Local Bus Specification, Rev 2.3*, section 3.3.3.2.1). In such case, the master's intention to burst cannot be determined and the AMD-8132 tunnel pessimistically treats such cycles as burst requests.
- Acquired Line: all or part of a requested line of data within a 64-byte aligned block that has made it back to the AMD-8132 tunnel from the HyperTransport interface.
- Requested Prefetch: the prefetch of up to a line of data in which the master has explicitly requested the line by initiating a transaction in which the address is within the prefetched line.
- Unrequested Prefetch: the speculative prefetch of a full line before a master has generated a transaction that includes the address of the line. If a master bursts up to the end of a requested prefetched line while keeping FRAME_L asserted and the AMD-8132 tunnel disconnects with data at that point, then the next line is still considered an unrequested prefetch even though the master has attempted to burst into the next line. Even if a burst is sustained from a requested line through any or all of an unrequested line, the second line is not considered requested by the master. If after a disconnect before or during data phases of an unrequested line the master subsequently attempts to continue the burst and generates an address phase that resides within the unrequested line, then that line changes from an unrequested prefetch to a requested prefetch.

In general, the PCI specification indicates that MRLs and MRMs are always prefetchable; it is the responsibility of masters to issue them only to prefetchable targets. No such assumption can be made for MRs. If, by means outside the PCI specification, it is known that MRs issued by the devices on this bus are to prefetchable targets, then the Dev[B,A]:0x4C[MRPFEN] bit can be set to enable prefetching for MRs. In this case, the MRL prefetching controls are used to control MR prefetching as well.

When prefetching is disabled for a memory read request (either Dev[B,A]:0x40[PFEN_L] deasserted for the particular master, or the request is an MR with Dev[B,A]:0x4C[MRPFEN] deasserted), these rules are followed:

- The AMD-8132 tunnel generates no unrequested prefetches.
- MRs with prefetching off are one DW, regardless of REQ64_L, and never assert ACK64_L.
- If REQ64_L is asserted, MRLs and MRMs with prefetching off assert ACK64_L and fetch two DW from HyperTransport. If REQ64_L is deasserted, only one DW is fetched.

When prefetching is enabled for a memory read request (Dev[B,A]:0x40[PFEN_L] asserted for the particular master and Dev[B,A]:0x4C[MRPFEN] asserted if the request is an MR), these rules are followed:

- The AMD-8132 tunnel may contain between 0 and 8 cache lines of prefetched data for a memory read at one time.
- If not bursted, all types of memory reads assert ACK64_L if REQ64_L is asserted and fetch two DW from HyperTransport. If REQ64_L is deasserted, only one DW is fetched.
- When there is a memory burst request, then the AMD-8132 tunnel sends out a requested prefetch of data starting from the transaction address up to the end of the line. Additionally, the AMD-8132 tunnel may send out 0 to 7 unrequested prefetches as controlled by Dev[B,A]:0x4C[IPF_x] where x is either an MRL or MRM. Prefetch-enabled MRs use IPF_MRL.
- As soon as the AMD-8132 tunnel completes transferring data for a given line, it may send another unrequested prefetch as controlled by Dev[B,A]:0x4C[CPFEN_x] where x could be an MRL or MRM. Prefetch-enabled MRs use CPF_MRL.

- In no event does prefetching continue past an address range boundary to an address for which the AMD-8132 tunnel would not be a PCI bus target. Range boundaries that are checked include:
  - top of 64-bit memory address space
  - top of 40-bit memory address space (FD_0000_0000h)
  - non-prefetchable memory base, if enabled (Dev[B,A]:0x[D8,20])
  - prefetchable memory base, if enabled (Dev[B,A]:0x[28,24])
  - base of VGA memory space, if enabled (A_0000h)
- A requested prefetch is allowed to burst until it is complete or until the master terminates the burst.
- If the master terminates a burst, all requested and unrequested prefetch data is discarded if Dev[B,A]:0x4C[DPDMD_L] is asserted for that master.
- If the AMD-8132 tunnel terminates a burst because the required next data line was not acquired and if Dev[B,A]:0x4C[DPDTD] is asserted, all unrequested prefetch data for that request is discarded as it arrives. Note that DPDTD should only be set if all Dev[B,A]:0x4C[20:16] DPDMD_L bits are 0 for that bridge. Setting DPDTD when any DPDMD_L bits are set may result in undefined behavior.
- If the discard timer times out for the initial data transfer, then all requested and unrequested prefetch data is discarded and Dev[B,A]:0x3C[DTS] is set and an error may be signalled.
- If a burst is terminated for any reason and the data is not discarded, a separate discard timer value controlled by Dev[B,A]:0x4C[URP_TIMER] is used for reconnections. This timer measures the time between the point of disconnection to when the master attempts to reconnect, regardless of whether the AMD-8132 tunnel has acquired the data. The timer restarts every time reconnection is attempted, whether or not data is transferred. If the timer expires, all prefetched data is discarded but no error is logged.
- The Dev[B,A]:0x4C[MRD_ALIAS] bit can be asserted to relax the requirements for reconnection. For example, if the bit is set and a master issues an MRM for a long burst but then switches to MRL to complete the burst after being disconnected near the end, the MRL will be allowed to reconnect and receive the unrequested prefetch data fetched by the MRM.
- Prefetching automatically stops when a memory window boundary defined by the configuration registers is reached. Optionally, based on Dev[B,A]:0x4C[PFDISC_4K] the prefetch stops on 4-K boundaries.
- If Dev[B,A]:0x4C[DPDH] is asserted, all unrequested prefetch data is discarded when a host request is issued by the AMD-8132 tunnel onto the PCI bus.
- If Dev[B,A]:0x4C[DPDMAC] is asserted, all unrequested prefetch data for a particular master is discarded if that master issues a read request that does not hit the acquired lines.
- The AMD-8132 tunnel can prefetch for up to eight PCI requests at a time, limited by Dev[B,A]:0x4C[OUTSTDELREQ]. Additionally, Dev[B,A]:0x4C[SDRPM] can be set to prevent a single master from having more than one outstanding request. If a request is received that would violate either of these limits, it is retried.

Prefetch CSR values should not be changed while reads from the PCI bus to HyperTransport are outstanding or the resulting behavior is undefined. The PCI bus should be quiesced and any active buffers allowed time to discard before CSR values are changed.

### 1.3.5 HyperTransport™ Requests Claimed by the Bridges

The bridges claim no upstream HyperTransport requests, but do claim the following downstream HyperTransport requests if the COMPAT bit is clear:

- All requests to memory and I/O space specified by Dev[B,A]:0x[30:1C] if Dev[B,A]:0x04[MEMEN, IOEN] are set.
- All configuration and extended configuration requests to the implemented functions of DevA or DevB (also see section 3.1.1).
- All configuration and extended configuration requests to buses behind bridge A or bridge B.

- All EOI broadcasts.
- All Stop Grant and STPCLK broadcasts (see section 4.1.2).

The bridges never claim a HyperTransport device message.

If the COMPAT bit is set and DevA:0x48[COMPAT] = 1, then all memory space, I/O space, and interrupt acknowledge requests are claimed and passed to bridge A.

If the COMPAT bit is set in the transaction and DevA:0x48[COMPAT] = 0, then per the HyperTransport link protocol the AMD-8132 tunnel never claims the transaction. Such transactions are automatically passed to the other side of the tunnel or master aborted if the AMD-8132 tunnel is at the end of the chain.

## 1.3.6 Transaction Considerations

### 1.3.6.1 General

The following are general considerations for AMD-8132 tunnel transactions:

- The PCIXCAP pins are implemented as described in *PCI-X Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a*.
- PCI cache line wrap mode is not supported. If a transaction is initiated that indicates this protocol, it is disconnected at the cacheline boundary.
- PCI-X transactions that cross address space boundaries as defined by the window configuration registers Dev[B,A]:0x[30:1C] result in undefined behavior.
- If there is a downstream nonposted request to PCI-X that results in a device-specific error in a completion message, then the response passed to the link indicates a target abort.
- When the AMD-8132 tunnel asserts [B,A]_DEVSEL_L, it does so as a medium decode speed device in conventional PCI mode and decode speed B device in PCI-X Mode 1 and Mode 2.
- If there is a HyperTransport transaction to I/O or configuration space that targets one of the bridges or is claimed by that bridge and it crosses a naturally aligned doubleword (dword) boundary, then the AMD-8132 tunnel does not send the transaction to the bus and the HyperTransport response is a target abort. Any I/O or config transactions not claimed by the AMD-8132 tunnel are forwarded to the next device on the HyperTransport chain, regardless of the alignment and length.

### 1.3.6.2 Pullups on Upper PCI Bus

While in conventional PCI mode or PCI-X Mode 1, the upper half of the PCI bus [B,A]_AD[63:32], [B,A]_CBE_L[7:4], and [B,A]_PAR64, is pulled high with weak pullups per *PCI Local Bus Specification, Rev 2.3*, section 3.8.1. These pullups are disabled for PCI-X Mode 2 or if Dev[B,A]:0x40[DISPU] is asserted.

### 1.3.6.3 Upstream Transactions

The following apply to AMD-8132 tunnel upstream transactions:

- The AMD-8132 tunnel requires two HyperTransport-defined UnitIDs. The first UnitID applies to bridge A. The second UnitID applies to bridge B and is contained in the following HyperTransport transactions:
  - External master requests associated with the bridge.
  - Interrupt requests associated with the bridge.
  - Responses to host-initiated requests that enter the address space of the bridge including configuration registers (DevA registers for bridge A and DevB registers for bridge B); secondary I/O

or memory spaces; configuration space windows defined in the configuration registers of the bridge; and the base address register spaces defined by the bridge.

The UnitID associated with the bridge is also returned in the response to upstream requests and is used to determine the destination of the response (bridge A or bridge B).

- Upstream PCI-initiated memory writes which include no valid byte enables complete normally over the PCI bus. However, the transaction may be dropped by the AMD-8132 tunnel resulting in no corresponding HyperTransport link transactions. This does not apply to I/O transactions.
- Secondary bus configuration cycles are never claimed by the AMD-8132 tunnel; including configuration cycles to device 31 in which special cycles are encoded per the *PCI-to-PCI Bridge Architecture Specification, Rev 1.2*.
- PCI-X Device ID Messages (DIMs) are never claimed by the AMD-8132 tunnel.
- For each bridge, up to 27 nonposted requests to the link may be outstanding at a given time. Based on the state of Dev[B,A]:0x40[NZSEQID], the AMD-8132 tunnel may or may not generate non-zero SeqID values in the upstream link requests that result from external PCI/PCI-X master read requests. Up to 8 outstanding PCI/PCI-X read sequences can be active at one time. If enabled, each outstanding secondary read sequence is assigned a unique SeqId from 8h to Fh. All bridge-sourced transactions are compliant to PCI or PCI-X ordering rules. As PCI or PCI-X transactions are converted to link transactions, they are translated as described in *HyperTransport™I/O Link Specification, Rev 2.0*.
- The HyperTransport coherent bit in upstream requests is always set for interrupt requests (including MSI/MSI-X transactions) and all requests from the secondary bus when it is in PCI mode. If the secondary bus is in PCI-X mode, the HyperTransport coherent bit is the inverse of the no snoop bit from the PCI-X request.

The following comparisons show the relationship between PCI-X transactions in which the relaxed ordering bit is set and link packets:

| Upstream PCI-X®2.0 Transaction | Corresponding Link Transaction |
|---|---|
| A memory write request in which the relaxed ordering bit of the attribute field is set. | PassPW is set in the request. |
| A read request in which the relaxed ordering bit of the attribute field is set. | Bit[3] of the command field (response may pass posted write) in the read request is set. |
| Any response to a downstream link read request in which bit[3] of the command field (response may pass posted write) is set. | PassPW is set in the response. |

### 1.3.6.4 Downstream Transactions

The following apply to AMD-8132 tunnel downstream transactions:

- Downstream special cycles that are encoded in configuration cycles to device 31 of the bridge secondary bus number (per the *PCI-to-PCI Bridge Architecture Specification, Rev 1.2*) are translated to special cycles on the PCI bus.
- In the translation from type 1 HyperTransport link configuration cycles to secondary bus type 0 configuration cycles, the AMD-8132 tunnel converts the device number to an IDSEL AD signal as follows: device 0 maps to AD[16]; device 1 maps to AD[17]; and so forth. Device numbers 16 through 31

are not valid. When Dev[B,A]:0x40[SSS_L] is low, a config access to device 1 also causes [B,A]_GNT_L1 to be asserted. See section 2.6.

In a system capable of operating in PCI-X Mode 2, there can only be one slot. The IDSEL signal for this slot should be attached to [B,A]_GNT_L1, which has the alternative function of IDSEL for device 1 while Dev[B,A]:0x40[SSS_L] is asserted (low).

- If the bus number matches the secondary bus number of the bridge, HyperTransport type 1 accesses and extended HyperTransport type 1 accesses are forwarded onto the PCI/PCI-X bus as type 0 accesses.

  If the bus number is greater than the secondary bus number of the bridge and less than or equal to the subordinate bus number of the bridge, HyperTransport type 1 accesses and extended HyperTransport type 1 accesses are forwarded onto the PCI/PCI-X bus as type 1 accesses.

  If the PCI/PCI-X bus is not operating in PCI-X Mode 2 and if an extended HyperTransport type 1 access attempts to access a register number above 255, the operation is dropped and a response returned as if it was master aborted on the PCI/PCI-X bus.
- HyperTransport device messages are never claimed by the AMD-8132 tunnel.
- Downstream nonposted HyperTransport link requests to a PCI/PCI-X bus that contain non-zero SeqID values are required to complete on that bus prior to initiating subsequent nonposted requests with the same SeqID value to that PCI/PCI-X bus. Consequently, only one downstream nonposted request with each non-zero SeqID value can be outstanding on a PCI/PCI-X bus at a time.
- The PCI-X no snoop bit is the inverse of the HyperTransport coherent bit for downstream memory requests. For downstream nonmemory requests, no snoop is always be 0.

The following comparisons show the relationship between PCI-X transactions in which the relaxed ordering bit is set and link packets:

| Downstream Link Transaction | Corresponding PCI-X®2.0 Transaction |
|---|---|
| A posted memory write request with PassPW set. | Relaxed ordering bit of the attribute field is set. |
| A read request in which bit[3] of the command field (response may pass posted write) is set. | Relaxed ordering bit of the attribute field is set. |
| A response to an upstream request. | Relaxed ordering bit of the attribute field is copied from the attribute field of the original request. |

## 1.3.7 Hot-Plug

**Note: Where information in this section applies to both the TPS2340A and TPS2342 hot-plug controllers, they are referred to combinatorially as TPS* in the text.**

Each PCI-X bridge includes an SHPC-compliant hot-plug controller that may be used to support hot-plug capable PCI-X or conventional PCI slots. Strapping options on [B,A]_REQ_L4 specify whether hot-plug is supported on bridge A and bridge B. If hot-plug is supported on a bridge, then all slots connected to that bridge are required to include hot-plug support circuitry. With the exception of a single-slot hot-plug implementation, the hot-plug support circuitry includes one or more TPS* hot-plug power controllers, power switches, and associated slot isolation switches to provide electrical isolation for most of the slot signals. For a single-slot hot-plug implementation, the AMD-8132 tunnel provides the bus isolation function so only the TPS* hot-plug power controller and the power switches are required. Each bridge supports a maximum of 4 slots when hot-plug mode is enabled.

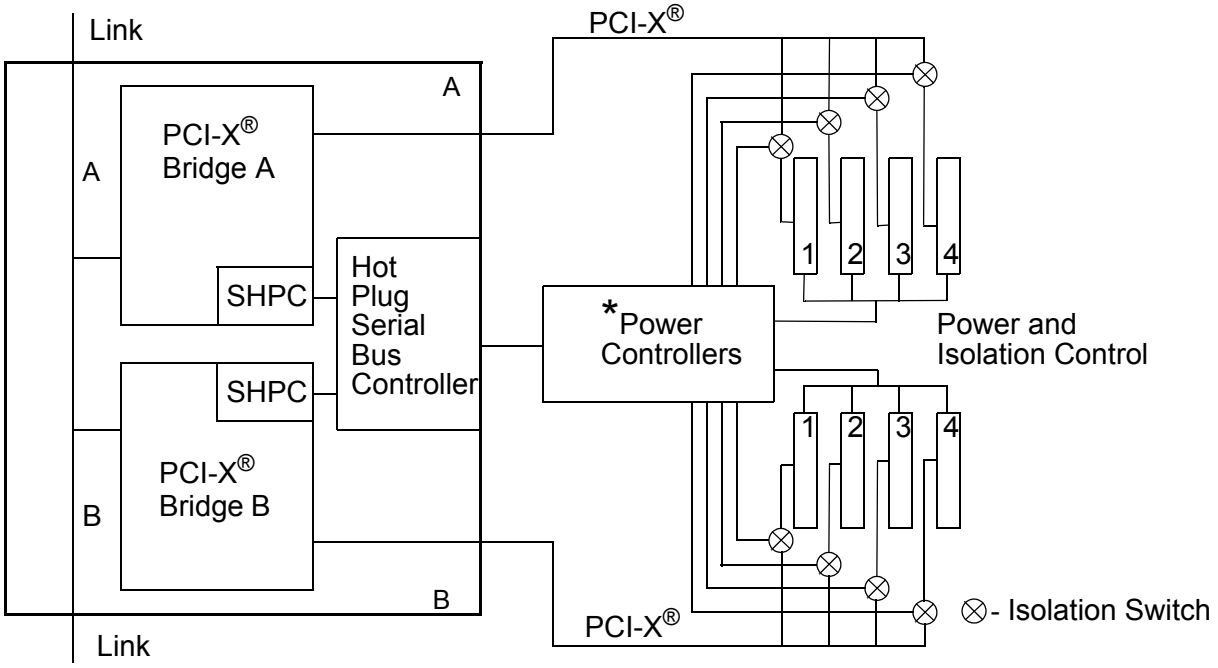
The hot-plug controller is designed to interface with either TPS*. The TPS2342 must be used if PCI-X Mode 2 hot-plug is supported. A strapping option on HPSOD indicates whether the TPS2340A or TPS2342 is used. Each TPS* controls two slots and provides two separate sets of isolation switch controls. TPS* controllers can be cascaded to support additional slots. If the TPS2340A is used, a single hot-plug power controller cannot be shared across bridge A and bridge B. If the TPS2342 is used, a single hot-plug power controller can be shared by bridge A and bridge B. The AMD-8132 tunnel is connected to the power controller via a serial bus. If the TPS2340A is used, one serial interface supports the power controllers for bridge A and bridge B. If the TPS2342 is used, there are two serial interfaces - one for each bridge.

### 1.3.7.1 Multi-Slot Hot-Plug

**Note: Where information in this section applies to both the TPS2340A and TPS2342 hot-plug controllers, they are referred to combinatorially as TPS* in the text.**

If multiple hot-plug slots are supported on a bridge, isolation switches are required for each slot to provide electrical isolation. Each TPS* hot-plug power controller provides two pairs of isolation switch control signals, BUSENx_L and CLKENx_L, to control the state of the switches.

**Figure 4. System Diagram: Multiple Hot-Plug Slots on a Bridge**




*This can be one or more of either the TPS2342 or TPS2340A, but not a combination of these.

Table 2 associates the hot-plug power controller isolation switch control signal with the AMD-8132 tunnel slot signals.

**Table 2. Signal Isolation Groups**

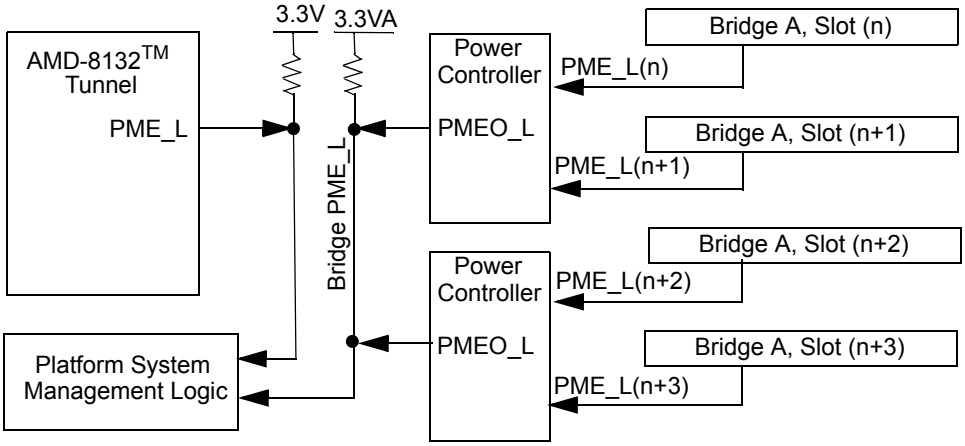
| Power Controller Signal | Slot Signals Isolated |
|---|---|
| BUSENx_L | [B,A]_ACK64L_ECC, [B,A]_AD[63:0], [B,A]_CBE_L[7:0], [B,A]_DEVSEL_L, [B,A]_FRAME_L, [B,A]_GNT_L[3:0], [B,A]_IRDY_L, [B,A]_PAR, [B,A]_PAR64, [B,A]_PERR_L, [B,A]_PIRQ[A, B, C, D]_L, [B,A]_REQ_L[3:0], [B,A]_REQ64_L, [B,A]_SERR_L, [B,A]_STOP_L, [B,A]_TRDY_L |
| CLKENx_L | [B,A]_PCLK[3:0], [B,A]_M66EN |

The TPS* hot-plug power controller controls PCI RESET_L to each slot. The AMD-8132 tunnel [B,A]_RESET_L signals are connected to the TPS* hot-plug power controller serial interface control signal, SORR_L of the TPS2340A or HP_RST[B,A]# of the TPS2342.

Some operating systems require that each configuration space bus number provide a separate PME_L signal to a general purpose set of PME_L status bits provided by the platform system management logic. The AMD-8132 tunnel internal PME_L signals are associated with the power management configuration registers Dev[B,A]:0x[9C:98]. Both registers are observed by software on the primary side of the PCI bridges and are on the same bus number, so the two AMD-8132 tunnel internal signals are connected and observed on the PME_L signal.

Since the slots are observed by software on the AMD-8132 tunnel secondary bus (which is a different bus number from the primary side); each bridge should provide a separate PME_L signal to the platform system management logic that logically connects to all the slots behind the bridge. The TPS* hot-plug power controller's PME_L inputs connect to the PME_L signal of each hot-plug slot. The TPS* hot-plug power controller's PME_L outputs for one bridge should be connected and passed to the platform system management logic.

### Figure 5. System Diagram: PME_L Signals




The slot signals used to communicate the speed, M66EN and PCIXCAP capability, and presence of an adapter card (PRSNT[1:2]_L) are isolated from the other slots in a hot-plug implementation and directly connected from the slot connector to their associated TPS*. The state of these signals is provided to the AMD-8132 tunnel through the serial interface. The AMD-8132 tunnel, in turn, makes the state of these signals available to system software. The [B,A]_PCIXCAP and [B,A]_M66EN pins on the AMD-8132 tunnel are not used for sensing speed and mode. The AMD-8132 tunnel [B,A]_PCIXCAP pins are used as an external power controller serial interface.

The connection and function of the M66EN signal is different for the TPS2340A and the TPS2342.

- If the TPS2340A is used, the connection and function is unique in a hot-plug implementation. M66EN is driven as an output of the AMD-8132 tunnel. Isolation switch control is driven by CLKEN_L rather than BUSEN_L, unlike other PCI/PCI-X control signals. In a hot-plug configuration, the AMD-8132 tunnel [B,A]_M66EN pin is configured as an open drain output. It is driven low by the AMD-8132 tunnel if it is determined that the bus is to run at 33 MHz (conventional PCI mode), as indicated in SHPC[B,A]:x10[MODE].

- If the TPS2342 is used, M66EN for each slot is directly connected to its associated TPS2342. It is driven low by the TPS2342 (via serial interface command from the SHPC) if it is determined that the bus is to run at 33 MHz (conventional PCI mode), as indicated in SHPC[B,A]:x10[MODE].

**Figure 6. System Diagram: M66EN Signals With TPS2340A**

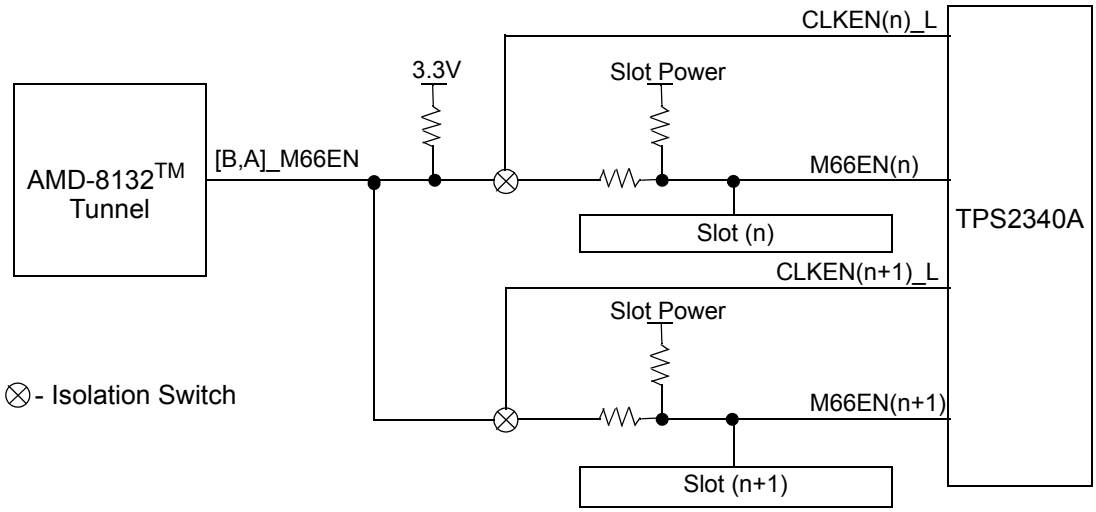
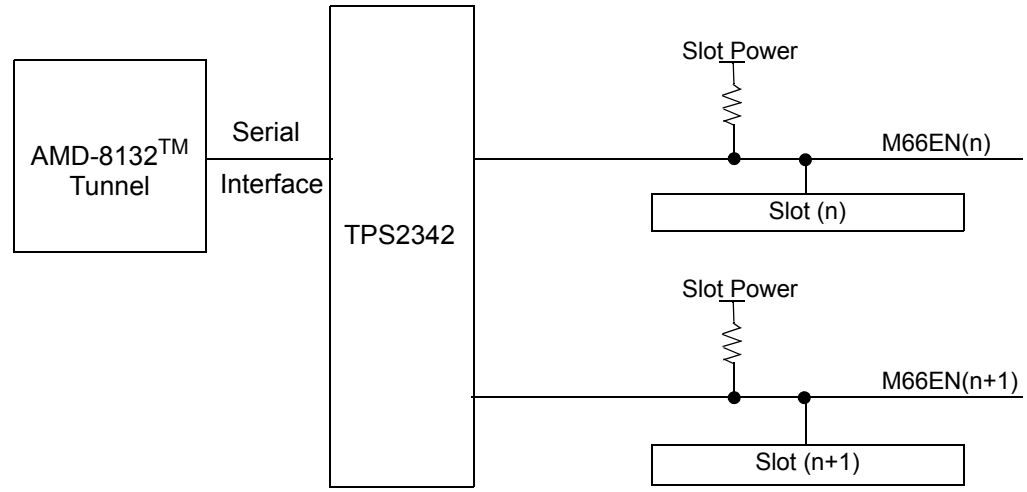



**Figure 7. System Diagram: M66EN Signals With TPS2342.**

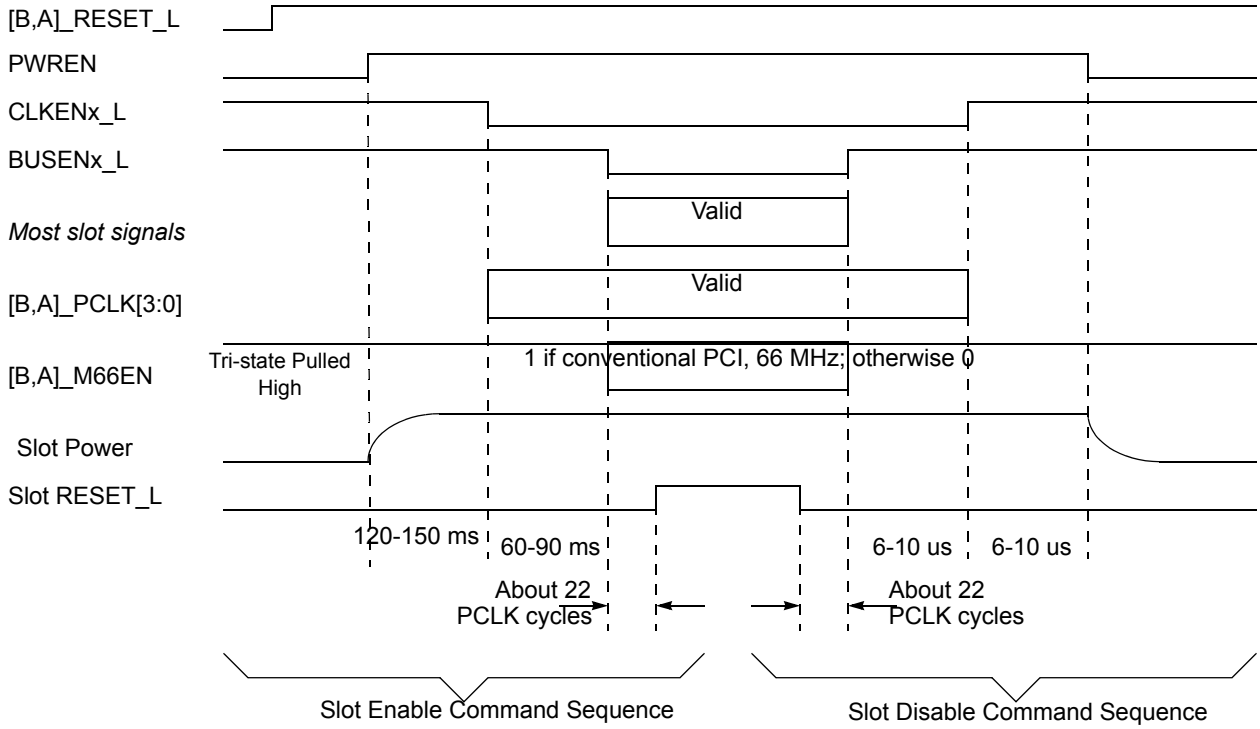



The process of setting the state of [B,A]_M66EN when the bridge is initialized is:

1. The TPS* hot-plug power controller is programmed to apply power to the slots via the SHPC[B,A]:14 Power Only All Slots command.
2. Software observes the state of the speed capability signals for the slots by reading SHPC[B,A]:[30:24][M66_CAP].
3. If the TPS2340A is used, software issues the SHPC[B,A]:14 Set Bus Segment Speed/Mode command which immediately places the appropriate state on [B,A]_M66EN out of the AMD-8132 tunnel.
4. If the TPS2340A is used, software issues the SHPC[B,A]:14 Enable All Slots command which results in the assertion of CLKENx_L so [B,A]_M66EN out of the AMD-8132 tunnel is enabled to the slot. If the

TPS2342 is used, the SHPC sends the appropriate state of [B,A]_M66EN via serial interface command to the TPS2342 and the TPS2342 drives [B,A]_M66EN to the slots.

**Figure 8. Multi-Slot Hot-Plug Enable/Disable Sequence**




**Notes:**
- Signal states are shown from the perspective of the pins of the AMD-8132 tunnel. The perspective from the slot is different due to the isolation switches controlled by CLKENx_L and BUSENx_L.
- *Most slot signals* includes the signals controlled by BUSENx_L.
- M66EN may be driven low after the set bus segment speed/mode command, which is typically sent after the slot is powered.

## 1.3.7.2 Single-Slot Hot-Plug

**Note: Where information in this section applies to both the TPS2340A and TPS2342 hot-plug controllers, they are referred to combinatorially as TPS* in the text.**

Isolation switches are not required if the bridge is connected to a single hot-plug slot. The AMD-8132 tunnel provides the isolation function by appropriately controlling the slot signals. The TPS* hot-plug power controller and power switches are still required.

**Figure 9. System Diagram: Single-Slot Hot-Plug for TPS2340A**

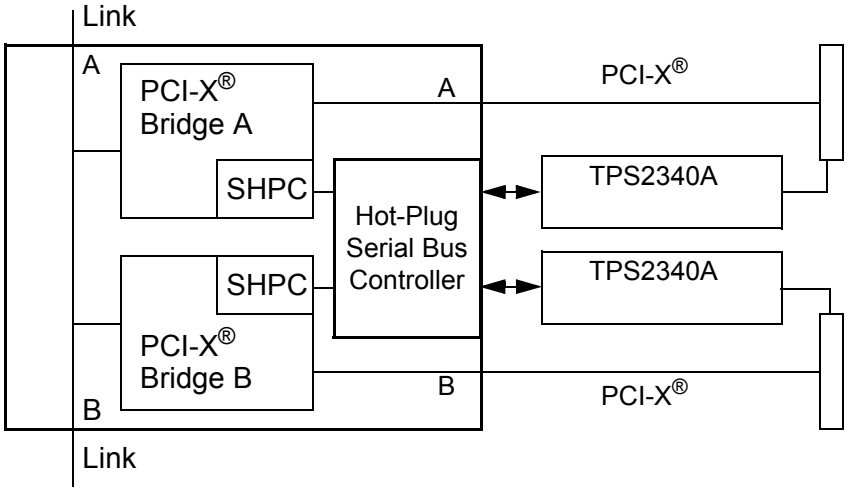
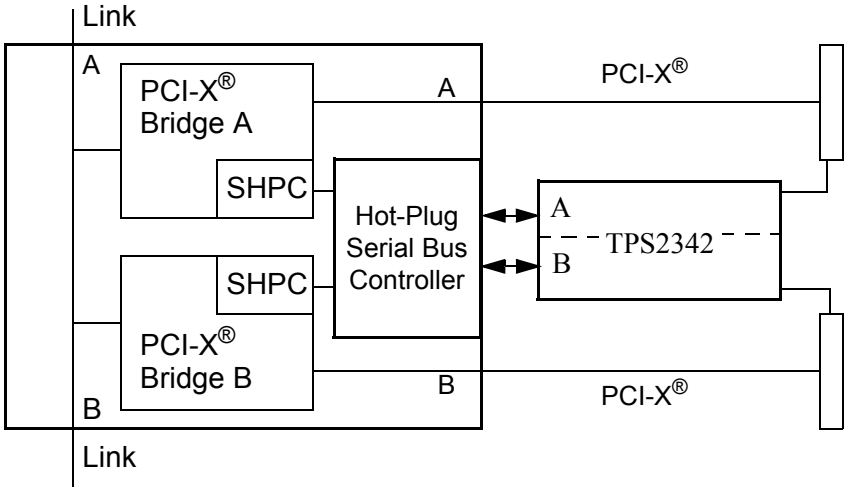


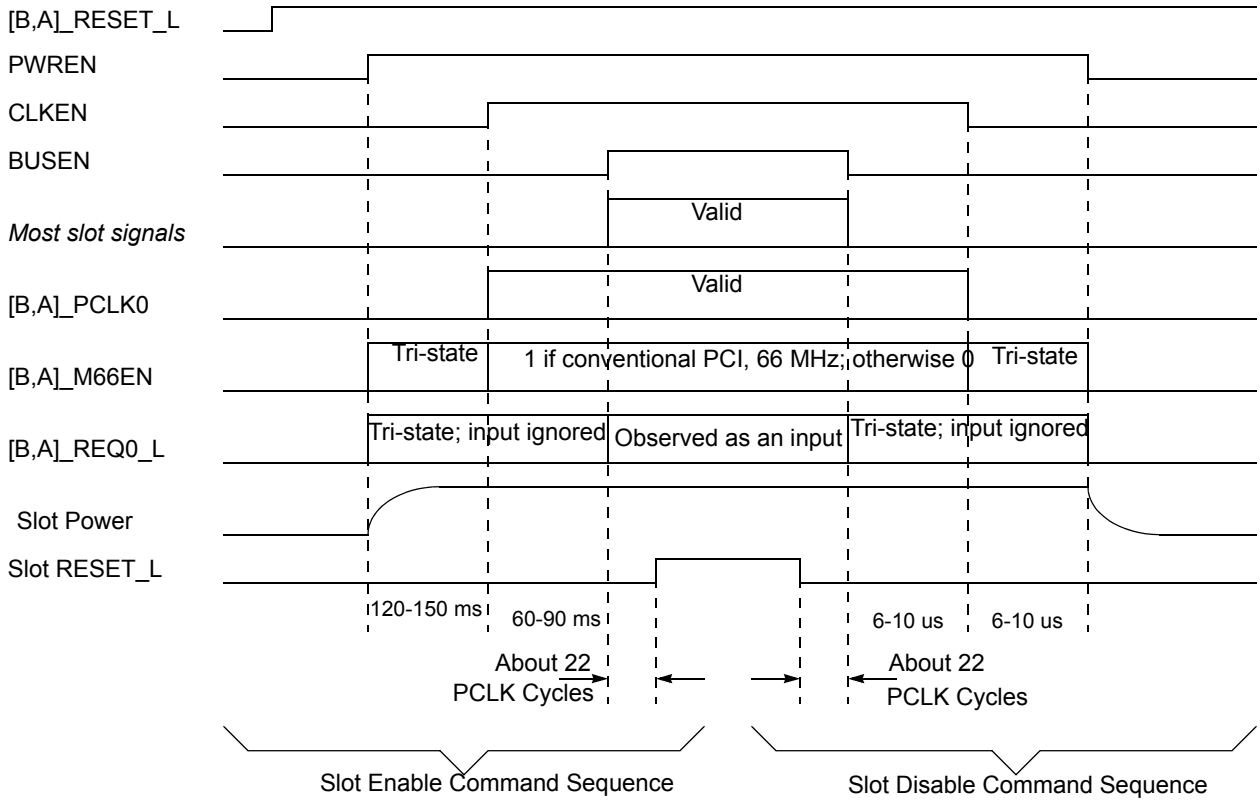

**Figure 10. System Diagram: Single-Slot Hot-Plug for TPS2342**




Single-slot hot-plug support is enabled for each bridge through strapping options on [B,A]_GNT_L4, as reflected in Dev[B,A]:0x40[SSS_L].

The AMD-8132 tunnel drives all slot signals low throughout the duration of a cold reset and continues to do so until after the TPS* hot-plug power controller applies power to the adapter. The AMD-8132 tunnel interprets the SHPC commands to control the signals in the power only, slot enable, and slot disable sequences and to receive BUSEN_L and CLKEN_L output from the TPS* to control its bus signal state. Figure 11 shows how signals are controlled by the AMD-8132 tunnel during the sequence initiated by the slot enable command and the slot disable command.

## Figure 11. Single-Slot Hot-Plug Enable/Disable Sequence




**Notes:**
- CLKEN_L and BUSEN_L are connected to the AMD-8132 tunnel.
- CLKEN and BUSEN represent the approximate times in which the TPS* changes the state of its CLKENx_L and BUSENx_L signals.
- PWREN represents the times in which the TPS* enables power to the slot.
- *Most slot signals* includes the signals controlled by BUSENx_L in section 1.3.7.1.

The AMD-8132 tunnel [B,A]_PCIXCAP pins are used as [B,A]_HP_SID (Serial Input Data). PCIXCAP and PRSNT[1:2]_L from the slot are connected to the TPS* hot-plug power controller.

If the TPS2340A is used, the AMD-8132 tunnel [B,A]_M66EN pins are connected directly to the slot with a pullup resistor to the slot power plane. This pin remains tri-stated until the SHPC enables the slot so the state provided by the card in the slot can be observed. This pin is driven low by the AMD-8132 tunnel if the bus is to run in 33 MHz conventional PCI mode.

If the TPS2342 is used, the AMD-8132 tunnel [B,A]_M66EN pins are left unconnected. The slot M66EN pin is driven low by the TPS2342 if the bus is to run in 33 MHz conventional PCI mode.

The process of setting the state of [B,A]_M66EN is the same as in multi-slot mode.

**Figure 12. Single-Slot Hot-Plug M66EN Connections: TPS2340A**

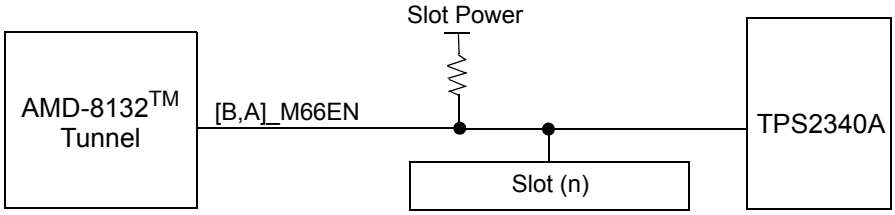
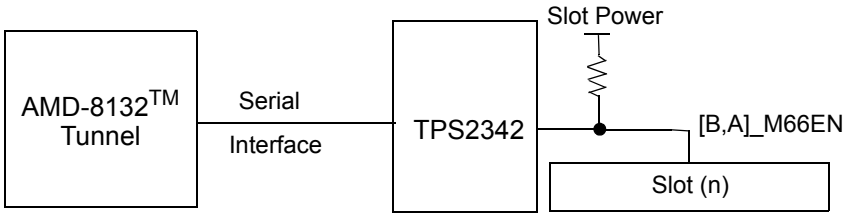



**Figure 13. Single-Slot Hot-Plug M66EN Connections: TPS2342**




The AMD-8132 tunnel is designed so only active-low interrupts from [B,A]_PIRQ[D:A]_L are supported when in single-slot support mode while the slot is not enabled. If the IOAPIC is programmed for active high interrupts in this mode, then spurious interrupt requests are generated.

## 1.3.7.3 TPS2340A Hot-Plug Power Controller

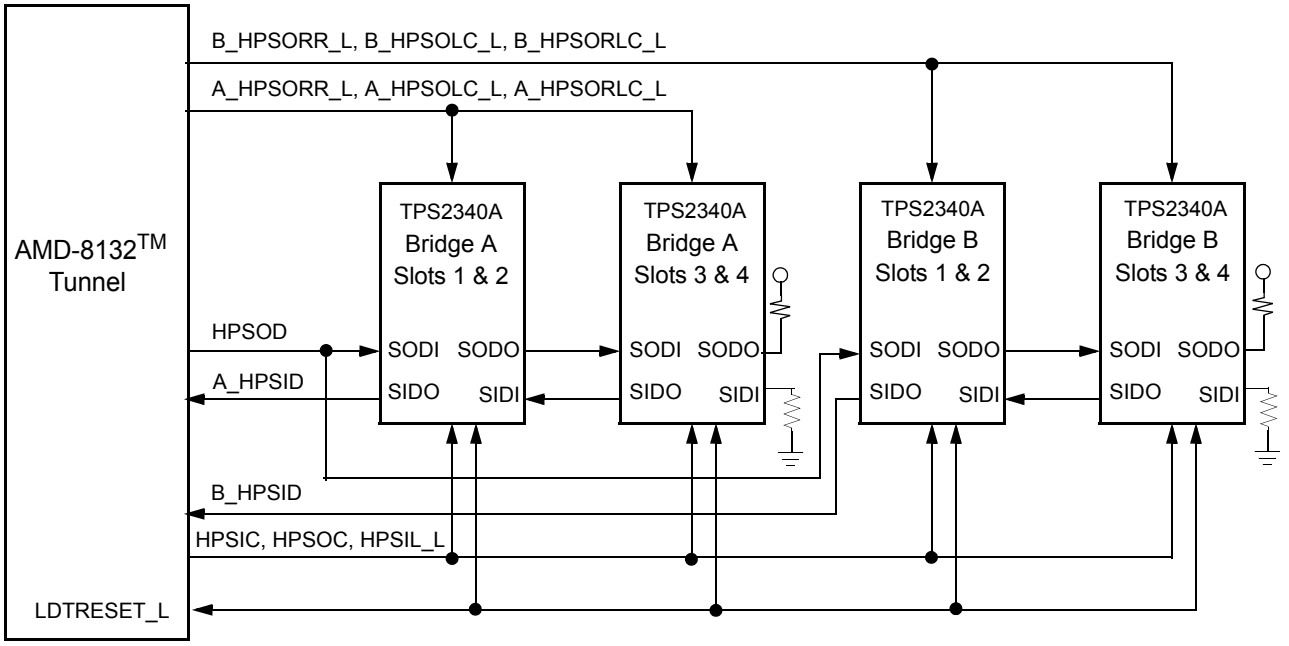
### 1.3.7.3.1 TPS2340A Serial Interface

The hot-plug serial interface operates at 8.33 MHz. It converts SHPC commands to a serial format to communicate with the TPS2340A hot-plug power controllers. It is also used to read status information from the TPS2340A hot-plug power controllers and update the AMD-8132 tunnel SHPC status registers accordingly. There are two different groups of serial interface signals.

- Common serial signals are connections between the AMD-8132 tunnel and all TPS2340A hot-plug power controllers and are shared across both PCI/PCI-X bridges. These signals are: HPSIC, HPSIL_L, HPSOC, HPSOD, HPSOR_L.
- Bridge specific signals are connections between the AMD-8132 tunnel and only those TPS2340A hot-plug power controllers connected to a particular bridge. These signals are: [B,A]_HPSID, [B,A]_HPSOLC_L, [B,A]_HPSORLC_L, [B,A]_HPSORR_L.

For additional information, see the TPS2340A product information.

**Figure 14. TPS2340A Hot-Plug Serial Interface Connections**




### 1.3.7.3.2 TPS2340A Serial Data: Power Controllers to Tunnel

Channel 00b interrupt-capable data and channel 01b non-interrupt-capable data, as defined in the TPS2340A product data, are shifted into the AMD-8132 tunnel from the TPS2340A over [B,A]_HPSID using HPSIC as the clock. This data is continuously shifted into the AMD-8132 tunnel, toggling between channels 00b and 01b. HPSIL_L controls the start of each block and specifies the channel number. HPSIL_L transitions after the falling edge of HPSIC.

Refer to the TPS2340A product data for more information.

### 1.3.7.3.3 TPS2340A Serial Data: Tunnel to Power Controllers

Serial data is transferred over HPSOD to the TPS2340A where it is stored using HPSOC as the clock. The state of the outputs and control signals stored in the power controller does not change until a rising edge of [B,A]_HPSORLC_L for RESETx_L and [B,A]_HPSOLC_L for the rest of the signals. The data is shifted whenever there is a need to change the state of these signals, normally as a result of a command to SHPC[B,A]:14. Regardless of how many slots are actually attached to the bridge, the AMD-8132 tunnel shifts out four slots worth of data followed by pulses on [B,A]_HPSORLC_L and [B,A]_HPSOLC_L. HPSOD transitions after the falling edge of HPSOC.

### 1.3.7.3.4 TPS2340A SHPC Interrupts, Events, And Errors

Under the conditions described by SHPC[B,A]:20, the AMD-8132 tunnel may assert [B,A]_PIRQA_L, PME_L, or indicate a system error on the links.

## 1.3.7.4 TPS2342 Hot-Plug Power Controller

### 1.3.7.4.1 TPS2342 Serial Interface

The hot-plug serial interface operates at 8.33 MHz. This interface converts SHPC commands to a serial format to communicate with the TPS2342 hot-plug power controllers. The hot-plug serial interface is also used to read status information from the TPS2342 hot-plug power controllers and update the AMD-8132 tunnel SHPC status registers accordingly. There are four serial interface signals for each serial interface bus: [B,A]_HP_LC, [B,A]_HP_SID, [B,A]_HP_SOD, [B,A]_HP_CLK.

See the TPS2342 product data for more information.

**Figure 15. TPS2342 Hot-Plug Serial Interface Connections: Single Slot**

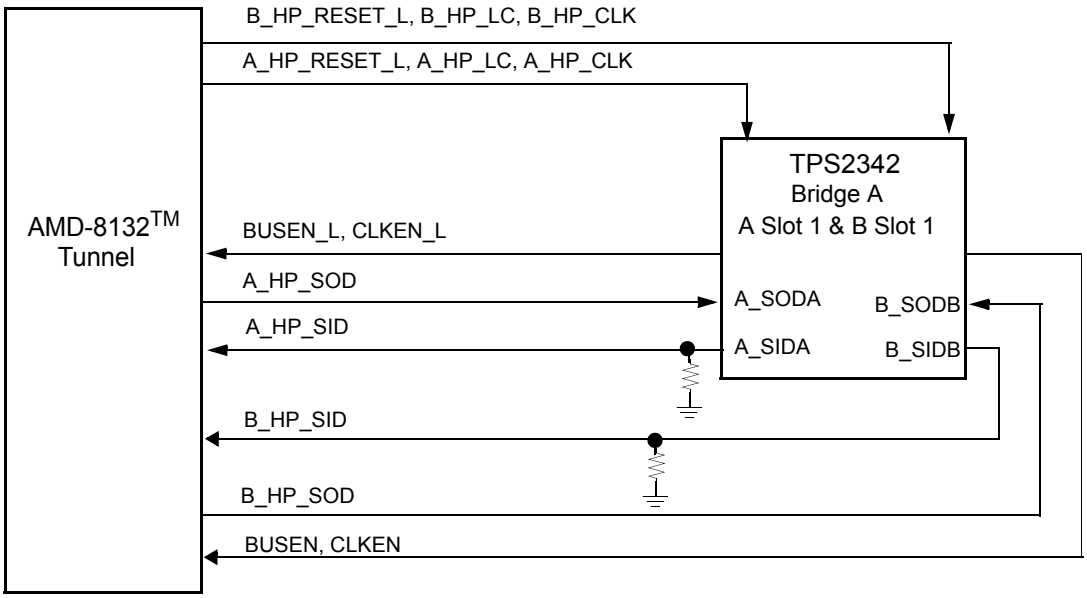
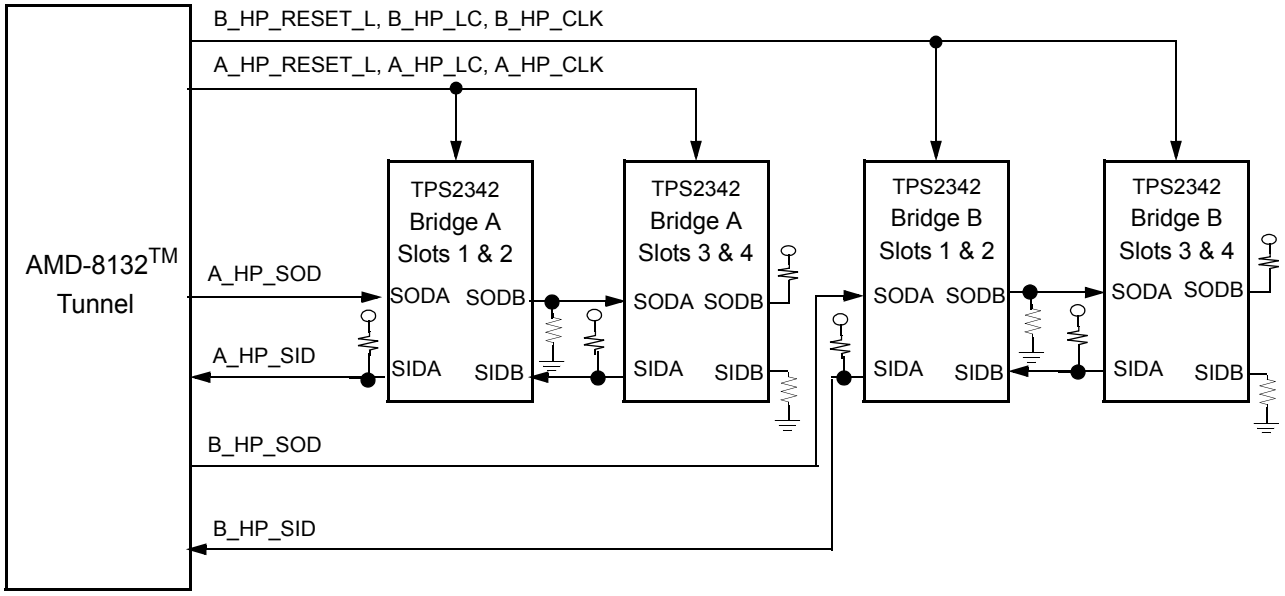


**Figure 16. TPS2342 Hot-Plug Serial Interface Connections: Multi-Slot**




### 1.3.7.4.2 TPS2342 Serial Data: Power Controllers to Tunnel

Channel 00b interrupt-capable data and channel 01b non-interrupt-capable data, as defined in the TPS2342 product data, are shifted into the AMD-8132 tunnel from the TPS2342 over [B,A]_HP_SID using [B,A]_HP_CLK as the clock. Read commands are multiplexed with write commands into the AMD-8132 tunnel, toggling between channels 00b and 01b.

See the TPS2342 product data for more information.

### 1.3.7.4.3 TPS2342 Serial Data: Tunnel to Power Controllers

Serial data is transferred over HP_SOD to the TPS2342 where it is stored using [B,A]_HP_CLK as the clock. The state of the outputs and control signals does not change until a rising edge of [B,A]_HP_LC for RESETx_L and the rest of the signals. Since the TPS2342 shares HP_LC for RESET_L and the other signals to latch, it has internal logic to control using [B,A]_HP_LC to change the state of RESET_L and the other signals. The SHPC global command controls the TPS2342 internal control logic. For more information refer to the TPS2342 product data.

The data is shifted whenever there is a need to change the state of these signals, normally as a result of a command to SHPC[B,A]:14. Regardless of how many slots are actually attached to the bridge, the AMD-8132 tunnel shifts out four slots worth of data followed by pulses on [B,A]_HP_LC.

### 1.3.7.4.4 TPS2342 SHPC Interrupts, Events, And Errors

Under the conditions described by SHPC[B,A]:20, the AMD-8132 tunnel may assert [B,A]_PIRQA_L, PME_L, or indicate a system error on the links.

### 1.3.8 PCI-X®2.0 PHY Compensation Update

The *PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification, Rev 2.0a* requires tightly controlled on-die termination, output impedance matching, and slew rate control. The PCI-X PHY used in the AMD-8132 tunnel maintains tight control of these parameters regardless of temperature, voltage, or process variation. The PCI-X PHY accomplishes this control using compensation circuitry. Each PCI bus has a ball connected to an external calibration resistor. By default, the PHY periodically samples calibration values and updates the input and output parameters. The compensation circuit requires an accurate (1%) pulldown resistor connected to ground. This resistor should be two times the board impedance

The PCI-X PHY calculated compensation values can change at any time. Compensation results driven to the pads change in increments of no more than 1; this means the electrical noise introduced by an update is sufficiently low that updates can occur even while the bus is active. The compensation circuitry runs continuously in PCI-X Mode 2 and continues to run through a warm reset.

# Chapter 2 Signal Descriptions

See the *AMD-8132™ HyperTransport™ PCI-X® 2.0 Tunnel Design Guide* for additional information.

The AMD-8132™ HyperTransport™ PCI-X®2.0 tunnel signals described in this chapter utilize the following I/O cell types:

| Cell Type | Description |
|---|---|
| Analog | Analog signal. |
| I | Input signal only. |
| I/O | Bidirectional input/output signal. |
| IOD | Bidirectional input/open drain output signal. |
| O | Output signal only. This includes outputs that are capable of being in the high-impedance state. |
| OD | Open drain output. These signals can be driven low and are expected to be pulled high by external circuitry. |
| w/PU to V33 | With pull-up to V33. The signal includes an internal pullup resistor to 3.3 volts. The resistor value is nominally 8K ohms. |
| w/PU to VIO | With pullup to VIO. The signal includes an internal pullup resistor to this PCI bus VIO power plane. The resistor value is nominally 8K ohms. |

The following terms are used in this chapter to indicate the different ways that pin functions can be shared. A signal can belong to any combination these categories. For example, it can be both a Alternative Function and a Strapping Function.

- *Alternate Function.* Refers to signals used for different purposes depending on system configuration. A board implementation would use these signals in different ways depending on which features are implemented on that board. For example, [B,A]_PCLK[4] is a PCI clock output under most circumstances, but in hot-plug mode is used as part of the serial interface to the TPS2342 or TPS2340A hot-plug power controller instead.

  For signals that have alternative functions, the signal name and description refer to the most common usage of this signal but contain an Alternative Function note. The alternative functions are described in section 2.6.
- *Multiple Use.* Refers to signals having multiple uses but no requirement for a board designer to treat the signals differently for different configurations. For example, the [B,A]_CBE_L signals are used as data strobes during PCI-X Mode 2 source-synchronous transfers. This does not require any configuration-specific differences on the motherboard.

  For information and clarification, the multiple uses of these signals are indicated in Multiple Use. No special board design restrictions apply other than those indicated by the relevant bus specifications.
- *Strapping Function.* Refers to signals that are weakly pulled up or down to indicate configuration information to the AMD-8132 tunnel. The AMD-8132 tunnel samples these pins at power-up to determine its internal configuration. These strapping functions are discussed in section 2.5.

# 2.1 HyperTransport™ Link Signals

In the following table are signals associated with the HyperTransport links. In the signal names:
- [1,0] refers to the two sides of the tunnel.
- [H,L] refers to the positive and negative sides of differential pairs.
- _L in single-ended signals indicates the signal is active low.

In the table columns:
- During Reset provides the state of the pin while LDTRESET_L is asserted.
- After Reset provides the state of the pin immediately after LDTRESET_L is deasserted.
- Func. indicates the pin is functional and operating per its defined function.

| **Pin Name.** Description | I/O Cell Type | Power Plane | During Reset | After Reset |
|---|---|---|---|---|
| **L[1,0]_CADIN_[H,L][15:0].** HyperTransport™ links 1 and 0 receive command-address-data bus. | I | VLDT | | |
| **L[1,0]_CADOUT_[H,L][15:0].** HyperTransport™ links 1 and 0 transmit command-address-data bus. | O | VLDT | Diff High** | Func. |
| **L[1,0]_CLKIN_[H,L][1:0].** HyperTransport™ links 1 and 0 receive link clocks. | I | VLDT | | |
| **L[1,0]_CLKOUT_[H,L][1:0].** HyperTransport™ links 1 and 0 transmit link clocks. Bit 1 corresponds to CADOUT[15:8]. | O | VLDT | Func. | Func. |
| **L[1,0]_COMP_[PU,PD].** HyperTransport™ impedance compensation pins for both sides of the tunnel. These are designed to be connected through resistors as follows:<br>L[1,0]_COMP_PU = pullup to VDD<br>L[1,0]_COMP_PD = pulldown to VSS | Analog | VLDT | | |
| **L[1,0]_CTLIN_[H,L]0.** HyperTransport™ links 1 and 0 receive control signal. | I | VLDT | | |
| **L[1,0]_CTLOUT_[H,L]0.** HyperTransport™ links 1 and 0 transmit control signal. | O | VLDT | Diff Low** | Func. |
| **LDTREQ_L.** HyperTransport™ wake up. | OD | V33 | | |
| **LDTRESET_L.** Reset input. See section 4.2.1 for details. LDTRESET_L is also used as the hot-plug [B,A]_HPSOR_L reset. When LDTRESET_L is asserted, the hot-plug shift register and control latches are reset. | I | V33 | | |
| **LDTSTOP_L.** Link disconnect control signal. | I | V33 | | |
| **PWROK.** Power OK. 1 = All power planes and REFCLK are valid. The rising edge of this signal is deglitched; it is not observed internally until it is high for more than six consecutive REFCLK cycles. Behavior follows the requirements in *HyperTransport™I/O Link Specification, Rev 2.0*. For more details about this signal, see section 4.2.1. | I | V33 | | |

**Notes:**
** Diff High and Diff Low for these link pins specify differential high and low; e.g: Diff High specifies that the _H signal is high and the _L signal is low.

If the use of a particular link is optional (if it goes to a slot or device that is optionally populated) then this link can be left unconnected. It does not require the termination described below as long as the ENDOCH and TXOFF bits are asserted (see DevA:0xC4 and DevA:0xC8). However, if a link is not connected to anything, then it is recommended that it be treated as follows:

- For every 10 differential pairs, connect all of the _P differential inputs together through a resistor to VSS. Connect all the _N differential inputs together through a resistor to VDD.
- Leave the differential outputs unconnected.
- If there are unused link signals on an active link (because the AMD-8132 tunnel is connected to a device with a reduced bit width), then the unused differential inputs should also be connected as above.

## 2.2 PCI-X® and Hot-Plug Controller Signals

In the following table are signals associated with PCI-X as well as signals interfacing to the TPS* hot-plug power controllers. In the signal names:

- [B,A] is used to differentiate between PCI-X bridge A and PCI-X bridge B.
- Signals with an _L suffix or having L_ in their name (like ACK64_L) are active low.

The AMD-8132 tunnel signals defined as sustained tri-state (s/t/s) in *PCI Local Bus Specification, Rev 2.3* have internal pullups to the appropriate power plane. The pullup value is nominally 8K ohms but may vary due to process variations. These signals are indicated by w/PU in the following table and there is no need to have external pullup resistors on them. The internal pullups can be disabled by writing a 1 to the Dev[B,A]:0x40[DISPU] CSR. No other PCI signals have internal pullups. [B,A]_SERR_L, PME_L, [B,A]_M66EN, [B,A]_PIRQ[D,C,B,A], and the [B,A]_REQ_L signals are not pulled up internally and external pullup resistors must be provided.

The following signals are sorted by pin name.

| **Pin Name.** Description | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| **A_COMPAT.** Specifies whether PCI-X® bridge A is the default bus in the system. This can only be associated with PCI-X bridge A. Also see DevA:0x48[COMPAT].<br>Low = PCI bus A is not the compatibility bus.<br>High = PCI bus A is the compatibility bus. | I | V33 |
| **[B,A]_ACK64_L__ECC1.** PCI-X® acknowledge for 64-bit transfer registers.<br>*Multiple Use:*<br>During PCI-X ECC mode, this pin is used as [B,A]_ECC[1]. | I/O | w/PU to VIO |
| **[B,A]_AD[63:50], [B,A]_AD49__CBE_L4, [B,A]_AD48__CBE_L5, [B,A]_AD[47:0].** PCI-X® address-data bus. The pullup to VIO is only enabled if not in PCI-X Mode 2. See *PCI-X Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a* for details.<br>Note: [B,A]_AD[31:0] are always just VIO.<br>*Multiple Use:*<br>During PCI-X Mode 2 operation, the [B,A]_AD48__CBE_L5 and [B,A]_AD49__CBE_L4 signals are used to carry [B,A]_CBE_L[5:4] information and as data strobes during source-synchronous operations. | I/O | w/PU to VIO |

| **Pin Name.** Description | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| **[B,A]_CAL.** PCI-X® calibration pins. These pins should be attached to ground through a resistor, see section 1.3.8. Under no conditions, including JTAG boundary scan, should these pins be driven above 1.5 V. | Analog | VIO |
| **[B,A]_CBE_L[7:0], [B,A]_CBE_L5__AD48, [B,A]_CBE_L4__AD49, [B,A]_CBE_L[3:0].** PCI-X® command-byte enable bus. The pullup to VIO is only enabled if not in PCI-X Mode 2. See *PCI-X Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a* for details.<br>Note: [B,A]_CBE_L[3:0] are always just VIO.<br>*Multiple Use:*<br>During PCI-X Mode 2 operation, CBE[7:6] and CBE[3:0] are also used as data strobes; [B,A]_CBE_L4__AD49 and [B,A]_CBE_L5__AD48 carry data bits [49:48]. | I/O | w/PU to VIO |
| **[B,A]_DEVSEL_L.** PCI-X® device select signal. Based on the requirements of the PCI-X initialization pattern, during reset these signals may be tri-state or they may be driven. | I/O | w/PU to V33 |
| **[B,A]_ECC[5:2].** PCI-X® ECC check bits.<br>*Alternate Function:*<br>When not in PCI-X ECC mode, these signals can be used as additional PCI request and grant lines. See section 2.6. | I/O | VIO |
| **[B,A]_FRAME_L.** PCI-X® frame signal. | I/O | w/PU to V33 |

| **Pin Name.** Description | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| **[B,A]_GNT_L[4,1,0].** PCI-X® grant signals.<br>[B,A]_GNT_L[3,2] do not exist as separate signals. These signals are shared with [B,A]_ECC[5,4]. See section 2.6.<br><br>**[B,A]_GNT_L4.** This signal is an input while PWROK is low (strapping function). At all other times this signal is a PCI grant output. This signal is only used as a grant output if the following three conditions are true:<br>1. The internal PCI arbiter is used: Dev[B,A]:0x48[EXTARB_L] is not asserted (low).<br>2. Hot-plug is not enabled for this bus: Dev[B,A]:0x48[HPEN] is not asserted.<br>3. Single slot mode is not enabled for this bus: Dev[B,A]:0x40[SSS_L] is not asserted (low).<br>*Alternate Function:*<br>If Dev[B,A]:0x48[HPEN] is asserted and DevA:0x48[HP_IS_TPS2342] is not asserted, this is [B,A]_HPSORLC. See section 2.6.<br>*Strapping Function:*<br>This signal must be pulled high to indicate multiple slots on this bus, or low to indicate a single slot on this bus. See section 2.5.<br><br>**[B,A]_GNT_L1.** This signal is an input while PWROK is low (strapping function). At all other times this signal is a PCI grant output. This signal is only used as a grant output if the following two conditions are true:<br>1. The internal PCI arbiter is used: Dev[B,A]:0x48[EXTARB_L] is not asserted (low).<br>2. Single slot mode is not enabled for this bus: Dev[B,A]:0x40[SSS_L] is not asserted (low).<br>*Alternate Function:*<br>This signal has two alternate functions. In external arbiter mode, it is a PCI request output from the AMD-8132 tunnel. In single slot mode, it is the IDSEL signal for the single external device. See section 2.6.<br><br>**[B,A]_GNT_L0.** This signal is an input while PWROK is low (strapping function). At all other times this signal is a PCI grant output. This signal is only used as a grant output if the internal PCI arbiter is used: Dev[B,A]:0x48[EXTARB_L] is not asserted (low).<br>*Alternate Function:*<br>In external arbiter mode this is a PCI request output from the AMD-8132 tunnel. | I/O (See left) | V33 |
| **[B,A]_IRDY_L.** PCI-X® initiator ready signal. | I/O | w/PU to V33 |
| **[B,A]_M66EN.** Frequency select input for [B,A]_PCLK while in conventional PCI mode. When not in hot-plug mode, the state of this signal is captured at the rising edge of [B,A]_RESET_L, see section 4.2.3. After the corresponding [B,A]_RESET_L signal goes high, the state of [B,A]_M66EN is ignored. In hot-plug mode, this signal may be driven low as an output after initialization. | IOD | V33 |
| **[B,A]_PAR__ECC0.** This is the PCI parity signal.<br>*Multiple Use:*<br>This signal is used as [B,A]_ECC[0] during PCI-X ECC mode. | I/O | VIO |
| **[B,A]_PAR64__ECC7.** This is the PCI upper 32-bit parity signal. The pullup to VIO is only enabled if not in PCI-X Mode 2.<br>*Multiple Use:*<br>This signal is used as [B,A]_ECC[7] during PCI-X ECC mode. | I/O | w/PU to VIO |

| **Pin Name.** Description | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| **[B,A]_PCIXCAP.** PCI-X® frequency capabilities selection; used to determine the mode of the PCI bus. The state of this signal is captured during a cold reset at the rising edge of LDTRESET_L (see section 4.2.1). After LDTRESET_L is deasserted, the state of [B,A]_PCIXCAP is ignored. The state of this signal is recaptured at any cold reset but is not recaptured during warm resets.<br>*Alternate Function:*<br>If hot-plug is enabled for this bus, [B,A]_PCIXCAP is the hot-plug input data from either the TPS2342 or TPS2340A. | I | V33 |
| **[B,A]_PCLK[4:0].** These are the PCI-X® clock outputs. The maximum frequency is 133 MHz. See section 4.2.3 for bus frequency selection.<br>• [B,A]_PCLK[3:0] can be used as slot/device PCI clocks.<br>• [B,A]_PCLK[4] can also be used as a slot/device PCI clock, unless this bus is in single-slot mode: Dev[B,A]:0x40[SSS_L] is asserted (low).<br>*Alternate Function:*<br>• If Dev[B,A]:0x48[HPEN] is asserted and Dev[B,A]:0x40[SSS_L] is asserted (low), [B,A]_PCLK[4] is used as the hot-plug BUSEN_L input from either the TPS2342 or TPS2340A.<br>• If Dev[B,A]:0x48[HPEN] is not asserted and Dev[B,A]:0x40[SSS_L] is asserted (low), [B,A]_PCLK[4] is used as VIO[B,A]_OVERRIDE_DELAY (see section 7.1.4). | I/O (See left) | V33 |
| **[B,A]_PERR_L.** PCI-X uncorrectable error. | I/O | w/PU to V33 |
| **[B,A]_PIRQ[A, B, C, D]_L.** PCI-X® interrupt requests; these are all inputs to the AMD-8132 tunnel.<br>• [B,A]_PIRQA_L can additionally be driven as an open-drain output in support of the hot-plug controller.<br>• [B,A]_PIRQB_L can additionally be driven as an open-drain output in support of the [B,A]_Fatal signal.<br>• [B,A]_PIRQC_L can additionally be driven as an open-drain output in support of the [B,A]_Nonfatal signal.<br>• If TEST is high, A_PIRQC_L is used to indicate test mode. See section 2.6. | IOD | V33 |
| **[B,A]_PLLCLKO.** PLL clock output, see section 4.1 for details. | O | V33 |
| **[B,A]_PLLCLKI.** PLL clock input, see section 4.1 for details. | I | V33 |

| **Pin Name.** Description | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| **[B,A]_REQ_L[4,1,0].**<br>[B,A]_REQ_L[3,2] do not exist as separate signals. These signals are shared with [B,A]_ECC[3,2]. See section 2.6 for details.<br><br>**[B,A]_REQ_L4.** This is a PCI request input. It is only used as a request input if the following three conditions are true:<br>1. The internal PCI arbiter is used: Dev[B,A]:0x48[EXTARB_L] is not asserted (low).<br>2. Hot-plug is not enabled for this bus: Dev[B,A]:0x48[HPEN] is not asserted.<br>3. Single slot mode is not enabled for this bus: Dev[B,A]:0x40[SSS_L] is not asserted (low).<br>*Alternate Function:*<br>In hot-plug mode, this signal is used for interfacing to the TPS2342 or TPS2340A. See section 2.6.<br>*Strapping Function:*<br>This signal must be pulled high to indicate there is no hot-plug controller for this bus; or pulled low to indicate there is a hot-plug controller. See section 2.5.<br><br>**[B,A]_REQ_L1.** This is a PCI request input. It is only used as a request input if the following two conditions are true:<br>1. The internal PCI arbiter is used: Dev[B,A]:0x48[EXTARB_L] is not asserted (low).<br>2. Single slot mode is not enabled for this bus: Dev[B,A]:0x40[SSS_L] is not asserted (low).<br>*Alternate Function:*<br>This signal has three alternate functions.<br>1. In external arbiter mode, it is a PCI grant input to the AMD-8132 tunnel.<br>2. In single slot non-hot-plug mode, it is the VIOSEL output for a PCI-X Mode 2 capable power supply.<br>3. In single slot hot-plug mode, it is the CLKEN_L input from either the TPS2340A or TPS2342.<br><br>**[B,A]_REQ_L0.** This is a PCI request input. It is only used as a request input if the internal PCI arbiter is used: Dev[B,A]:0x48[EXTARB_L] is not asserted (low).<br>*Alternate Function:*<br>In external arbiter mode, this signal is a PCI grant input to the AMD-8132 tunnel.<br>If TEST is high, A_REQ_L0 is used to indicate the test mode. See section 2.6. | I/O (See left) | V33 |
| **[B,A]_REQ64_L__ECC6.** PCI-X® request for 64-bit transfers. The AMD-8132 tunnel drives this signal to the asserted state while [B,A]_RESET_L is asserted, indicating the PCI bus is 64 bits. *Multiple Use:*<br>This signal is used as [B,A]_ECC[6] during PCI-X ECC mode. | I/O | w/PU to VIO |
| **[B,A]_RESET_L.** Secondary PCI bus reset. This signal is asserted whenever LDTRESET_L is asserted or when programmed by Dev[B,A]:0x3C[SBRST].<br>In hot-plug mode, this signal should also be connected to HPSORR_L of the TPS2340A or [B,A]_HP_RST_L in the TPS2342. See section 1.3.7.3.1. | O | V33 |
| **[B,A]_SERR_L.** PCI-X® system error signal. | I | V33 |
| **[B,A]_STOP_L.** PCI-X® stop signal. Based on the requirements of the PCI-X initialization pattern, during reset these signals may be tri-state or they may be driven. | I/O | w/PU to V33 |

| **Pin Name.** Description | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| **[B,A]_TRDY_L.** PCI-X® target ready signal. Based on the requirements of the PCI-X initialization pattern, during reset these signals may be tri-state or they may be driven. | I/O | w/PU to V33 |
| **HPSIC.** This signal is an input while PWROK is low (strapping function). For the TPS2340A, this signal is the hot-plug serial input clock.<br>*Alternate Function:*<br>A_HP_CLK. This signal is the hot-plug serial clock for the TPS2342. See section 2.6.<br>*Strapping Function:*<br>For normal operation, this signal should always be pulled high. | I/O (See left) | V33 |
| **HPSIL_L.** This signal is an input while PWROK is low (strapping function). This signal is an output at all other times. For the TPS2340A, this signal is the hot-plug serial input load.<br>*Alternate Function:*<br>B_HP_CLK. This signal is the hot-plug serial clock for the TPS2342. See section 2.6.<br>*Strapping Function:*<br>This pin should be pulled high to indicate the internal PCI arbiters are used. See section 2.5. | I/O (See left) | V33 |
| **HPSOC.** This signal is an input while PWROK is low (strapping function). This signal is an output at all other times. For the TPS2340A, this signal is the hot-plug serial output clock.<br>*Alternate Function:*<br>B_HP_SOD. This signal is the hot-plug serial output data to the TPS2342. See section 2.6. | I/O (See left) | V33 |
| **HPSOD.** This signal is an input while PWROK is low (strapping function). This signal is an output at all other times. For the TPS2340A, this signal is the hot-plug serial output data.<br>*Alternate Function:*<br>A_HP_SOD. This signal is the hot-plug serial output data for the TPS2342. See section 2.6.<br>*Strapping Function:*<br>• If this pin is pulled high at the rising edge of PWROK, the AMD-8132 tunnel is configured to interface to the TPS2340A. See section 2.5.<br>• If this pin is pulled low at the rising edge of PWROK, the AMD-8132 tunnel is configured to interface to the TPS2342. See section 2.5. | I/O (See left) | V33 |
| **NIOAIRQ[A, B, C, D]_L.** Non-IOAPIC interrupt request outputs. Each of these signals require a weak pullup resistor to V33. See section 1.3.2 and Dev[B,A]:0x40[NIOAMODE] for details about the function of these pins.<br>*Alternate Function:*<br>If TEST is asserted, then NIOAIRQD_L is used to indicate the test mode. See section 2.6. | IOD (See left) | V33 |
| **PME_L.** Power management event interrupt. The AMD-8132 tunnel asserts this signal when SHPC-defined power management events occur. This signal is typically connected to the system Southbridge, where it may be used to initiate system state transitions. This pin is asserted by either PCI bus SHPC to signal a power management event. | OD | V33 |

If a bridge is to be left unused, the signals associated with that bridge should be connected as follows:

- The following signals do not require any connection: [B,A]_AD[63:50], [B,A]_AD49__CBE_L4, [B,A]_AD48__CBE_L5, [B,A]_AD[47:0], [B,A]_CBE_L[7:6], [B,A]_CBE_L5__AD48, [B,A]_CBE_L4__AD49, [B,A]_CBE_L[3:0], [B,A]_PAR, [B,A]_PAR64, [B,A]_PCLK[4:0], [B,A]_RESET_L, [B,A]_ECC[5:4], [B,A]_TRDY_L, [B,A]_IRDY_L, [B,A]_STOP_L, [B,A]_REQ64_L, [B,A]_ACK64_L, [B,A]_FRAME_L, [B,A]_DEVSEL_L, [B,A]_PERR_L.

- The following signals should be tied high through resistors: [B,A]_ECC[3:2], [B,A]_GNT_L[4,1,0], [B,A]_PIRQ[D:A]_L, [B,A]_REQ_L[4,1,0], [B,A]_SERR_L.
- The following signals should be grounded: [B,A]_PCIXCAP, [B,A]_M66EN.
- [B,A]_PLLCLKO should be connected to [B,A]_PLLCLKI.

## 2.3 Miscellaneous Signals

The following signals are sorted by pin name.

| **Pin Name.** Description | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| **[B,A]_PCLK[3].**In single-slot mode, these pins are used as straps for AMD internal use and should be pulled high. | | |
| **CMPOVR.** This pin is required to be tied low for normal operation. | I | V33 |
| **DIFFOUT_[H,L].** Reserved (should be left unconnected). | O | VLDT |
| **NC.** Reserved (should be left unconnected). | | |
| **PCIXA_100, PCIXB_100.** For strapping options see section 2.5. | | |
| **REFCLK_[H,L].** 200 MHz differential reference clock. This signal is required to be operational and valid for a minimum of 200 microseconds prior to the rising edge of PWROK and always while PWROK is high. | I | (See section 7.2) |
| • **STRAPL[1:0].** Strapping options to be tied low. These pins should be tied to ground. | I | V33 |
| **TEST.** This pin is required to be tied low for functional operation. See Chapter 6.<br>Note: | I | V33 |

| **Pin Name.** Description | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| **VDDOK.** This signal indicates to the AMD-8132 tunnel that VDD core power is at 1.2 V and stable.<br>• This signal should not be asserted until VLDT and VDD core are known to be at 1.2 V and stable. VDDOK should be asserted with, or prior to, PWROK being asserted.<br>• When VDDOK is deasserted, the PCI/PCI-X® I/O cells are put into determinate states even if VDD and VLDT power supplies have not reached their nominal levels.<br>• The following PCI/PCI-X signals are driven low while VDDOK is deasserted as part of the power on sequence:<br>A_AD0_PAD, A_AD1_PAD, A_AD2_PAD, A_AD3_PAD, A_AD4_PAD, A_AD5_PAD, A_AD6_PAD, A_AD7_PAD, A_AD8_PAD, A_AD9_PAD, A_AD10_PAD, A_AD11_PAD, A_AD12_PAD, A_AD13_PAD, A_AD14_PAD, A_AD15_PAD, A_AD16_PAD, A_AD17_PAD, A_AD18_PAD, A_AD19_PAD, A_AD20_PAD, A_AD21_PAD, A_AD22_PAD, A_AD23_PAD, A_AD24_PAD, A_AD25_PAD, A_AD26_PAD, A_AD27_PAD, A_AD28_PAD, A_AD29_PAD, A_AD30_PAD, A_AD31_PAD<br>A_CBE_L0_PAD, A_CBE_L1_PAD, A_CBE_L2_PAD, A_CBE_L3_PAD<br>A_PCLK1_PAD<br>A_RESET_L_PAD<br>B_AD0_PAD, B_AD1_PAD, B_AD2_PAD, B_AD3_PAD, B_AD4_PAD, B_AD5_PAD, B_AD6_PAD, B_AD7_PAD, B_AD8_PAD, B_AD9_PAD, B_AD10_PAD, B_AD11_PAD, B_AD12_PAD, B_AD13_PAD, B_AD14_PAD, B_AD15_PAD, B_AD16_PAD, B_AD17_PAD, B_AD18_PAD, B_AD19_PAD, B_AD20_PAD, B_AD21_PAD, B_AD22_PAD, B_AD23_PAD, B_AD24_PAD, B_AD25_PAD, B_AD26_PAD, B_AD27_PAD, B_AD28_PAD, B_AD29_PAD, B_AD30_PAD, B_AD31_PAD<br>B_CBE_L0_PAD, B_CBE_L1_PAD, B_CBE_L2_PAD, B_CBE_L3_PAD<br>B_PCLK1_PAD<br>B_RESET_L_PAD | | |

## 2.3.1 JTAG Signals

A standard JTAG controller is implemented in the AMD-8132 tunnel using the following signals sorted by pin name.

| **Pin Name.** Description | **IO Cell Type** | **Power Plane** |
|---|---|---|
| **TCK.** JTAG test clock. | I | V33 |
| **TDI.** JTAG test data input. | I | w/PU to V33 |
| **TDO.** JTAG test data output. | OD | V33 |
| **TMS.** JTAG test mode select. | I | w/PU to V33 |
| **TRST_L.** JTAG reset.<br>Note: If a system does not implement JTAG, this signal should be pulled low on the systemboard with a strong enough resistor to overcome the nominally 8K internal resistor. | I | w/PU to V33 |

## 2.4 Power and Ground

The following signals are sorted by pin name.

| **Pin Name.** Description |
|---|
| **PLL_VDDA[2:1].** Analog 3.3-volt power plane for PLLs in the core of the AMD-8132™ tunnel. Filtering this power plane from digital noise is required. |
| **V33.** 3.3-volt power plane for I/O. |
| **VDD.** 1.2-volt power plane for the core of the AMD-8132 tunnel. |
| **VDD3FB_H.** VDD3 feedback. VDD3FB_H is tied to V33 on the die and can be used to measure the power supply noise at the die. Potentially, it can be used as the feedback to a V33 regulator to boost the supply in compensation for the package drop. |
| **VDDFB_[H,L].** Core feedback. VDDFB_[H, L] are routed on the package as a differential pair to the to die. VDDFB_H is tied to VDD12 on the die and VDDFB_L is tied to ground. |
| **VIO[B,A].** In systems not capable of running in Mode 2, this is always 3.3 volts. In systems that can run in Mode 2, VIOSEL ([B,A]_REQ_L1) is high to select 3.3 volts and low to select 1.5 volts. |
| **VLDT.** 1.2 volt power plane for the HyperTransport™ technology pins. |
| **VSS.** Ground. |

## 2.5 Straps During Initialization

During reset, the state of several pins is monitored to configure the bridges. These pins require either a weak pullup to V33 (value = 1) or weak pulldown to VSS (value = 0). All of the strap information is latched at the rising edge of PWROK. The following are sorted by pin name.

| **Pin** | **Strap.** Description. | **Low/High** |
|---|---|---|
| PCIXA_100 | **DevA:0x48[PCIX100].** Sets the maximum speed of the DevA PCI-X® common clock.<br>For PCI-X Mode 1:<br>• Low (133) = 133 MHz clock<br>• High (100) = 100 MHz clock<br>For PCI-X Mode 2 DDR:<br>• Low (133) = a data rate of 266 MHz<br>• High (100) = a data rate of 200 MHz | Low = 133<br>High = 100 |
| PCIXB_100 | **DevB:0x48:[PCIX100].** Sets the maximum speed of the DevB PCI-X® common clock.<br>For PCI-X Mode 1:<br>• Low (133) = 133 MHz clock<br>• High (100) = 100 MHz clock<br>For PCI-X Mode 2 DDR:<br>• Low (133) = a data rate of 266 MHz<br>• High (100) = a data rate of 200 MHz | Low = 133<br>High = 100 |

| Pin | **Strap.** Description. | Low/High |
|---|---|---|
| [B,A]_GNT_L4 | **Dev[B,A]:0x40[SSS_L].** For details, see Dev[B,A]:0x40, PCI-X® Miscellaneous. | Low = Single Slot<br>High = Multi-Slot |
| [B,A]_PCLK[3] | **[B,A]_PCLK[3].** In single-slot mode, these pins are used as straps for AMD internal use and should be pulled high. | |
| [B,A]_REQ_L4 | **Dev[B,A]:0x48[HPEN].** For details, see Dev[B,A]:0x48, PCI-X® Misc II and Pins Latched at Rising Edge of PWROK. | Low = Hot-Plug<br>High = Not Hot-Plug |
| HPSIC | For normal operational mode, HPSIC should have a weak pullup to V33. | High = Normal Operation |
| HPSIL_L | **Dev[B,A]:0x48[EXTARB_L].** When internal arbitration is in use, EXTARB_L should have a weak pullup to V33. A weak pulldown to VSS disables internal arbitration for both bridges. BIOS code can subsequently enable the individual internal arbiters. See section 1.3.1. | Low = External Arbiter<br>High = Internal Arbiter |
| HPSOC | For normal operational mode, HPSOC should have a weak pullup to V33. | High = Normal Operation |
| HPSOD | **Dev[B,A]:0x48[HP_IS_TPS2342].** For details see Dev[B,A]:0x48, PCI-X® Misc II and Pins Latched at Rising Edge of PWROK. | Low = TPS2342<br>High = TPS2340A |

# 2.6 Pins With Alternate Functions

The following entries are sorted by pin name. The alternate function is listed under the pin name.

| Pin Name<br><br>**Alternate Function.** Description. | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| [B,A]_ECC[3,2]<br><br>**[B,A]_REQ_L[3,2].**<br>• If the PCI-X® bus is in PCI-X ECC mode, these signals are ECC signals.<br>• If the PCI-X® bus is not in ECC mode but is in single slot mode, Dev[B,A]:0x40[SSS_L] is asserted (low) and these signals are treated as unused ECC signals (outputs disabled, input receivers disabled).<br>• If the PCI-X® bus is in parity mode and is not in single slot mode and if the internal arbiter is enabled for this bus, these signals are available as additional REQ lines:<br>[B,A]_ECC3 --> [B,A]_REQ_L3<br>[B,A]_ECC2 --> [B,A]_REQ_L2 | I/O | VIO |

| Pin Name<br><br>**Alternate Function.** Description. | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| [B,A]_ECC[5,4]<br><br>**[B,A]_GNT_L[3,2].**<br>• If the PCI-X® bus is in PCI-X ECC mode, these signals are ECC signals.<br>• If the PCI-X® bus is not in ECC mode but is in single slot mode, Dev[B,A]:0x40[SSS_L] is asserted (low) and these signals are treated as unused ECC signals (outputs disabled, input receivers disabled).<br>• If the PCI-X® bus is in parity mode and is not in single slot mode and if the internal arbiter is enabled for this bus, these signals are available as additional GNT lines:<br>[B,A]_ECC5 --> [B,A]_GNT_L3<br>[B,A]_ECC4 --> [B,A]_GNT_L2 | I/O | VIO |
| [B,A]_GNT_L0<br><br>**[B,A]_P_REQ_L.** If Dev[B,A]:0x48[EXTARB_L] is asserted (low), this signal is used as the preemptable REQ_L to the arbiter. | O | V33 |
| [B,A]_GNT_L1<br><br>**[B,A]_IDSEL.** When Dev[B,A]:0x40[SSS_L] is asserted (low), this is an output and the PCI-X® IDSEL signal for slot 0.<br>Note: The AMD-8132 tunnel is always device 0 on the secondary PCI bus. So, this IDSEL is asserted for configuration accesses to device 1 on the secondary PCI bus, corresponding to AD[17] in the type 0 configuration access.<br><br>**[B,A]_NP_REQ_L.** If Dev[B,A]:0x48[EXTARB_L] is asserted (low), this signal is used as the non-preemptable REQ_L to the arbiter. | O<br><br>O | V33<br><br>V33 |
| [B,A]_GNT_L4<br><br>**[B,A]_HPSORLC.** When Dev[B,A]:0x48[HPEN] is set, this is the [B,A]_HPSORLC output to a TPS2340A compatible controller. See section 1.3.7. | O | V33 |
| [B,A]_PCIXCAP<br><br>**[B,A]_HPSID.** If Dev[B,A]:0x48[HPEN] is asserted, this is the hot-plug serial input data output for the TPS2340A. See section 1.3.7.3.1.<br><br>**[B,A]_HP_SID.** If Dev[B,A]:0x48[HPEN] is asserted, this is the hot-plug serial input data output for the TPS2342. See section 1.3.7.3.1. | I/O<br><br>I/O | V33<br><br>V33 |
| [B,A]_PCLK[1]<br><br>**[B,A]_VIOEN.** If Dev[B,A]:0x40[SSS_L] is asserted (low), this is an output and is the [B,A]_VIOEN signal for the VIO[B,A] power controller. See section 7.1.4. | O | V33 |

| Pin Name<br><br>**Alternate Function.** Description. | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| [B,A]_PCLK[4]<br><br>**[B,A]_BUSEN_L.** When Dev[B,A]:0x48[HPEN] and Dev[B,A]:0x40[SSS_L] are asserted, this is the BUSEN_L input. See section 1.3.7.2.<br><br>**VIO[B,A]_OVERRIDE_DELAY.** When Dev[B,A]:0x48[HPEN] is not asserted and Dev[B,A]:0x40[SSS_L] is asserted (low), this is the VIO[B,A]_OVERRIDE_DELAY input. See section 7.1.4. | I/O<br><br>I/O | V33<br><br>V33 |
| [B,A]_REQ_L0<br><br>**[B,A]_P_GNT_L.** If Dev[B,A]:0x48[EXTARB_L] is asserted (low), this signal is used as the preemptable GNT_L from the arbiter. | I | V33 |
| [B,A]_REQ_L1<br><br>**[B,A]_NP_GNT_L.** If Dev[B,A]:0x48[EXTARB_L] is asserted (low), this signal is used as the non-preemptable GNT_L from the arbiter.<br><br>**[B,A]_VIOSEL.** When Dev[B,A]:0x48:[HPEN] is not asserted and Dev[B,A]:0x40[SSS_L] is asserted (low), this is an output and is the [B,A]_VIOSEL signal for the VIO[B,A] power controller. See section 7.1.4.<br><br>**CLKEN_L.** When Dev[B,A]:0x48[HPEN] and Dev[B,A]:0x40[SSS_L] are asserted, this is the CLKEN_L input. | I/O<br><br>I/O<br><br>I/O | V33<br><br>V33<br><br>V33 |
| [B,A]_REQ_L4<br><br>**[B,A]_HPSOLC.** When a hot-plug controller is connected to the bridge this is an output:<br>• [B,A]_HPSOLC for a TPS2340A compatible controller. See section 1.3.7.<br>• [B,A]_HP_LC for a TPS2342 compatible controller. See section 1.3.7. | I/O | V33 |
| [B,A]_RESET_L<br><br>**[B,A]_HP_RST_L.** This a reset output to the TPS2342.<br><br>**[B,A]_HPSORR_L.** This is a reset output to the TPS2340A.<br>Note: The function does not change for the different hot-plug controllers, but the controllers name the signal differently . | O<br><br>O | V33<br><br>V33 |
| HPSIC<br><br>**A_HP_CLK.** When DevA:0x48[HP_IS_TPS2342] is asserted, this signal is the hot-plug serial bus clock for bus A. | O | V33 |
| HPSIL_L<br><br>**B_HP_CLK.** When DevA:0x48[HP_IS_TPS2342] is asserted, this signal is the hot-plug serial bus clock for bus B. | O | V33 |

| Pin Name<br><br>**Alternate Function.** Description. | **I/O Cell Type** | **Power Plane** |
|---|---|---|
| HPSOC<br><br>**B_HP_SOD.** When DevA:0x48[HP_IS_TPS2342] is asserted, this is the bridge B hot-plug serial data output to a TPS2342 controller. | O | V33 |
| HPSOD<br><br>**A_HP_SOD.** When DevA:0x48[HP_IS_TPS2342] is asserted, this is the bridge A hot-plug serial data output to a TPS2342 controller. | O | V33 |

# 2.7 AMD-8132™ Tunnel Configurations: Their Effect on Alternate Functions

The AMD-8132 tunnel can be used in several different configurations. The following tables show how the AMD-8132 tunnel signals are used in these configurations. The configuration choices are:

- Whether a bus is using an internal arbiter or an external arbiter.
- Whether a bus is single slot or multi-slot. See the discussion of Dev[B,A]:0x40[SSS_L] in section 3.2.
- Whether a bus is capable of running in PCI-X ECC mode.
- Whether a bus is hot-plug capable. See the discussion of Dev[B,A]:0x48[HPEN] in section 3.2.
- Whether a hot-plug capable bus is using the TPS2340A or the TPS2342. See the discussion of Dev[B,A]:0x48[HP_IS_TPS2342] in section 3.2.
- Whether a hot-plug capable bus is using one hot-plug power controller or two.

## 2.7.1 Internal Arbiter

### 2.7.1.1 Single Slot: Mode 2

Capable of operating in PCI-X Mode 2, PCI-X Mode 1 with ECC, PCI-X Mode 1 with parity, and conventional PCI. A bus capable of running in PCI-X Mode 2 must only have a single slot or device and must connect [B,A]_GNT_L1 (alternative function [B,A]_IDSEL) to the IDSEL pin of the slot or device. A bus capable of running in PCI-X Mode 2 or PCI-X Mode 1 with ECC must connect [B,A]_ECC[5:2] to the ECC[5:2] pins of the slots/devices.

| Pin Name | A and B PCI-X® Mode 2 Single Slot Not Hot-Plug | A and B PCI, PCI-X® Mode 1 Single Slot One Hot-Plug TPS2340A | A and B PCI, PCI-X® Mode 2 Single Slot One Hot-Plug TPS2342 |
|---|---|---|---|
| A_ECC2 | A_ECC2 | A_ECC2 | A_ECC2 |
| A_ECC3 | A_ECC3 | A_ECC3 | A_ECC3 |
| A_ECC4 | A_ECC4 | A_ECC4 | A_ECC4 |
| A_ECC5 | A_ECC5 | A_ECC5 | A_ECC5 |
| A_GNT_L0 | A_GNT_L0 | A_GNT_L0 | A_GNT_L0 |
| A_GNT_L1 | A_IDSEL | A_IDSEL | A_IDSEL |
| A_GNT_L4 | -- | A_HPSORLC | -- |
| A_PCLK1 | A_VIOEN | -- | -- |
| A_PCLK4 | VIOA_OVERRIDE_DELAY | A_BUSEN_L | A_BUSEN_L |
| A_REQ_L0 | A_REQ_L0 | A_REQ_L0 | A_REQ_L0 |
| A_REQ_L1 | A_VIOSEL | A_CLKEN_L | A_CLKEN_L |
| A_REQ_L4 | -- | A_HPSOLC | A_HP_LC |
| A_PCIXCAP | A_PCIXCAP | A_HPSID | A_HP_SID |
| B_ECC2 | B_ECC2 | B_ECC2 | B_ECC2 |
| B_ECC3 | B_ECC3 | B_ECC3 | B_ECC3 |
| B_ECC4 | B_ECC4 | B_ECC4 | B_ECC4 |
| B_ECC5 | B_ECC5 | B_ECC5 | B_ECC5 |
| B_GNT_L0 | B_GNT_L0 | B_GNT_L0 | B_GNT_L0 |
| B_GNT_L1 | B_IDSEL | B_IDSEL | B_IDSEL |
| B_GNT_L4 | -- | B_HPSORLC | -- |
| B_PCLK1 | B_VIOEN | -- | -- |
| B_PCLK4 | VIOB_OVERRIDE_DELAY | B_BUSEN_L | B_BUSEN_L |
| B_REQ_L0 | B_REQ_L0 | B_REQ_L0 | B_REQ_L0 |
| B_REQ_L1 | B_VIOSEL | B_CLKEN_L | B_CLKEN_L |
| B_REQ_L4 | -- | B_HPSOLC | B_HP_LC |
| B_PCIXCAP | B_PCIXCAP | B_HPSID | B_HP_SID |
| HPSIC | -- | HPSIC | A_HP_CLK |
| HPSIL_L | -- | HPSIL_L | B_HP_CLK |
| HPSOC | -- | HPSOC | B_HP_SOD |
| HPSOD | -- | HPSOD | A_HP_SOD |

### 2.7.1.2 Multiple Slots: Mode 1 ECC

Capable of running in PCI-X Mode 1 with ECC, PCI-X Mode 1 with parity, and conventional PCI. A bus capable of running in PCI-X Mode 1 with ECC must connect [B,A]_ECC[5:2] to the ECC[5:2] pins of the slots/devices. A non-single-slot system capable of running in PCI-X Mode 1 with ECC must provide pullups on [B,A]_ECC[3:2] since these will be treated as PCI requests until the bus is configured in ECC mode. Up to three slots are supported if not in hot-plug mode, up to two slots are supported in hot-plug mode.

| Pin Name | A and B PCI-X® Mode 1 Two or Three Slot Not Hot-Plug | A and B PCI-X® Mode 1 Two Slot One Hot-Plug TPS2340A Per Bus | A and B PCI-X® Mode 1 Two Slot One Hot-Plug TPS2342 Per Bus |
|---|---|---|---|
| A_ECC2 | A_ECC2 | A_ECC2 | A_ECC2 |
| A_ECC3 | A_ECC3 | A_ECC3 | A_ECC3 |
| A_ECC4 | A_ECC4 | A_ECC4 | A_ECC4 |
| A_ECC5 | A_ECC5 | A_ECC5 | A_ECC5 |
| A_GNT_L0 | A_GNT_L0 | A_GNT_L0 | A_GNT_L0 |
| A_GNT_L1 | A_GNT_L1 | A_GNT_L1 | A_GNT_L1 |
| A_GNT_L4 | A_GNT_L4 | A_GNT_L4 | A_GNT_L4 |
| A_PCLK1 | A_PCLK1 | A_PCLK1 | A_PCLK1 |
| A_PCLK4 | A_PCLK4 | A_PCLK4 | A_PCLK4 |
| A_REQ_L0 | A_REQ_L0 | A_REQ_L0 | A_REQ_L0 |
| A_REQ_L1 | A_REQ_L1 | A_REQ_L1 | A_REQ_L1 |
| A_REQ_L4 | A_REQ_L4 | A_REQ_L4 | A_REQ_L4 |
| A_PCIXCAP | A_PCIXCAP | A_HPSID | A_HP_SID |
| B_ECC2 | B_ECC2 | B_ECC2 | B_ECC2 |
| B_ECC3 | B_ECC3 | B_ECC3 | B_ECC3 |
| B_ECC4 | B_ECC4 | B_ECC4 | B_ECC4 |
| B_ECC5 | B_ECC5 | B_ECC5 | B_ECC5 |
| B_GNT_L0 | B_GNT_L0 | B_GNT_L0 | B_GNT_L0 |
| B_GNT_L1 | B_GNT_L1 | B_GNT_L1 | B_GNT_L1 |
| B_GNT_L4 | B_GNT_L4 | B_GNT_L4 | B_GNT_L4 |
| B_PCLK1 | B_PCLK1 | B_PCLK1 | B_PCLK1 |
| B_PCLK4 | B_PCLK4 | B_PCLK4 | B_PCLK4 |
| B_REQ_L0 | B_REQ_L0 | B_REQ_L0 | B_REQ_L0 |
| B_REQ_L1 | B_REQ_L1 | B_REQ_L1 | B_REQ_L1 |
| B_REQ_L4 | B_REQ_L4 | B_REQ_L4 | B_REQ_L4 |
| B_PCIXCAP | B_PCIXCAP | B_HPSID | B_HP_SID |
| HPSIC | -- | HPSIC | A_HP_CLK |
| HPSIL_L | -- | HPSIL_L | B_HP_CLK |
| HPSOC | -- | HPSOC | B_HP_SOD |
| HPSOD | -- | HPSOD | A_HP_SOD |

### 2.7.1.3 Multiple Slots: Mode1 Without ECC

Capable of running in PCI-X Mode 1 with parity, and conventional PCI. In this mode the [B,A]_ECC[5:2] pins are available as extra [B,A]_REQ_L[3:2] and [B,A]_GNT_L[3:2] signals and up to five devices are supported. Up to four devices are supported in hot-plug mode.

| Pin Name | A and B PCI, PCI-X® Multi-Slot Mode Not Hot-Plug | A and B PCI, PCI-X® Multi-Slot Mode One or Two Hot-Plug TPS2340A Per Bus | A and B PCI, PCI-X® Multi-Slot Mode One or Two Hot-Plug TPS2342 Per Bus |
|---|---|---|---|
| A_ECC2 | A_REQ_L2 | A_REQ_L2 | A_REQ_L2 |
| A_ECC3 | A_REQ_L3 | A_REQ_L3 | A_REQ_L3 |
| A_ECC4 | A_GNT_L2 | A_GNT_L2 | A_GNT_L2 |
| A_ECC5 | A_GNT_L3 | A_GNT_L3 | A_GNT_L3 |
| A_GNT_L0 | A_GNT_L0 | A_GNT_L0 | A_GNT_L0 |
| A_GNT_L1 | A_GNT_L1 | A_GNT_L1 | A_GNT_L1 |
| A_GNT_L4 | A_GNT_L4 | A_HPSORLC | -- |
| A_PCLK1 | A_PCLK1 | A_PCLK1 | A_PCLK1 |
| A_PCLK4 | A_PCLK4 | -- | -- |
| A_REQ_L0 | A_REQ_L0 | A_REQ_L0 | A_REQ_L0 |
| A_REQ_L1 | A_REQ_L1 | A_REQ_L1 | A_REQ_L1 |
| A_REQ_L4 | A_REQ_L4 | A_HPSOLC | A_HP_LC |
| A_PCIXCAP | A_PCIXCAP | A_HPSID | A_HP_SID |
| B_ECC2 | B_REQ_L2 | B_REQ_L2 | B_REQ_L2 |
| B_ECC3 | B_REQ_L3 | B_REQ_L3 | B_REQ_L3 |
| B_ECC4 | B_GNT_L2 | B_GNT_L2 | B_GNT_L2 |
| B_ECC5 | B_GNT_L3 | B_GNT_L3 | B_GNT_L3 |
| B_GNT_L0 | B_GNT_L0 | B_GNT_L0 | B_GNT_L0 |
| B_GNT_L1 | B_GNT_L1 | B_GNT_L1 | B_GNT_L1 |
| B_GNT_L4 | B_GNT_L4 | B_HPSORLC | -- |
| B_PCLK1 | B_PCLK1 | B_PCLK1 | B_PCLK1 |
| B_PCLK4 | B_PCLK4 | -- | -- |
| B_REQ_L0 | B_REQ_L0 | B_REQ_L0 | B_REQ_L0 |
| B_REQ_L1 | B_REQ_L1 | B_REQ_L1 | B_REQ_L1 |
| B_REQ_L4 | B_REQ_L4 | B_HPSOLC | B_HP_LC |
| B_PCIXCAP | B_PCIXCAP | B_HPSID | B_HP_SID |
| HPSIC | -- | HPSIC | A_HP_CLK |
| HPSIL_L | -- | HPSIL_L | B_HP_CLK |
| HPSOC | -- | HPSOC | B_HP_SOD |
| HPSOD | -- | HPSOD | A_HP_SOD |

## 2.7.2 External Arbiter

### 2.7.2.1 Single Slot

Single slot PCI-X Mode 2 is not supported with an external arbiter.

### 2.7.2.2 Multiple Slots: Mode 1

Capable of running in PCI-X Mode 1 with ECC, PCI-X Mode 1 with parity, and conventional PCI. A bus capable of running in PCI-X Mode 1 with ECC must connect [B,A]_ECC[5:2] to ECC[5:2] pins of the slots/ devices. In external arbiter mode, [B,A]_ECC[5:2] are never used as request/grant signals, so up to 4 slots can be supported as PCI-X Mode 1 with ECC (limited by electrical constraints).

| Pin Name | A and B Two Slot PCI-X® Mode 1 Not Hot-Plug | A and B Two Slot PCI-X® Mode 1 One or Two Hot-Plug TPS2340A Per Bus | A and B Two Slot PCI-X® Mode 1 One or Two Hot-Plug TPS2342 Per Bus |
|---|---|---|---|
| A_ECC2 | A_ECC2 | A_ECC2 | A_ECC2 |
| A_ECC3 | A_ECC3 | A_ECC3 | A_ECC3 |
| A_ECC4 | A_ECC4 | A_ECC4 | A_ECC4 |
| A_ECC5 | A_ECC5 | A_ECC5 | A_ECC5 |
| A_GNT_L0 | A_P_REQ_L | A_P_REQ_L | A_P_REQ_L |
| A_GNT_L1 | A_NP_REQ_L | A_NP_REQ_L | A_NP_REQ_L |
| A_GNT_L4 | -- | A_HPSORLC | -- |
| A_PCLK1 | A_PCLK1 | A_PCLK1 | A_PCLK1 |
| A_PCLK4 | A_PCLK4 | -- | -- |
| A_REQ_L0 | A_P_GNT_L0 | A_P_GNT_L0 | A_P_GNT_L0 |
| A_REQ_L1 | A_NP_GNT_L1 | A_NP_GNT_L1 | A_NP_GNT_L1 |
| A_REQ_L4 | -- | A_HPSOLC | A_HP_LC |
| A_PCIXCAP | A_PCIXCAP | A_HPSID | A_HP_SID |
| B_ECC2 | B_ECC2 | B_ECC2 | B_ECC2 |
| B_ECC3 | B_ECC3 | B_ECC3 | B_ECC3 |
| B_ECC4 | B_ECC4 | B_ECC4 | B_ECC4 |
| B_ECC5 | B_ECC5 | B_ECC5 | B_ECC5 |
| B_GNT_L0 | B_P_REQ_L0 | B_P_REQ_L0 | B_P_REQ_L0 |
| B_GNT_L1 | B_NP_REQ_L1 | B_NP_REQ_L1 | B_NP_REQ_L1 |
| B_GNT_L4 | -- | B_HPSORLC | -- |
| B_PCLK1 | B_PCLK1 | B_PCLK1 | B_PCLK1 |
| B_PCLK4 | B_PCLK4 | -- | -- |
| B_REQ_L0 | B_P_GNT_L | B_P_GNT_L | B_P_GNT_L |
| B_REQ_L1 | B_NP_GNT_L | B_NP_GNT_L | B_NP_GNT_L |
| B_REQ_L4 | -- | B_HPSOLC | B_HP_LC |
| B_PCIXCAP | B_PCIXCAP | B_HPSID | B_HP_SID |
| HPSIC | -- | HPSIC | A_HP_CLK |
| HPSIL_L | -- | HPSIL_L | B_HP_CLK |
| HPSOC | -- | HPSOC | B_HP_SOD |
| HPSOD | -- | HPSOD | A_HP_SOD |

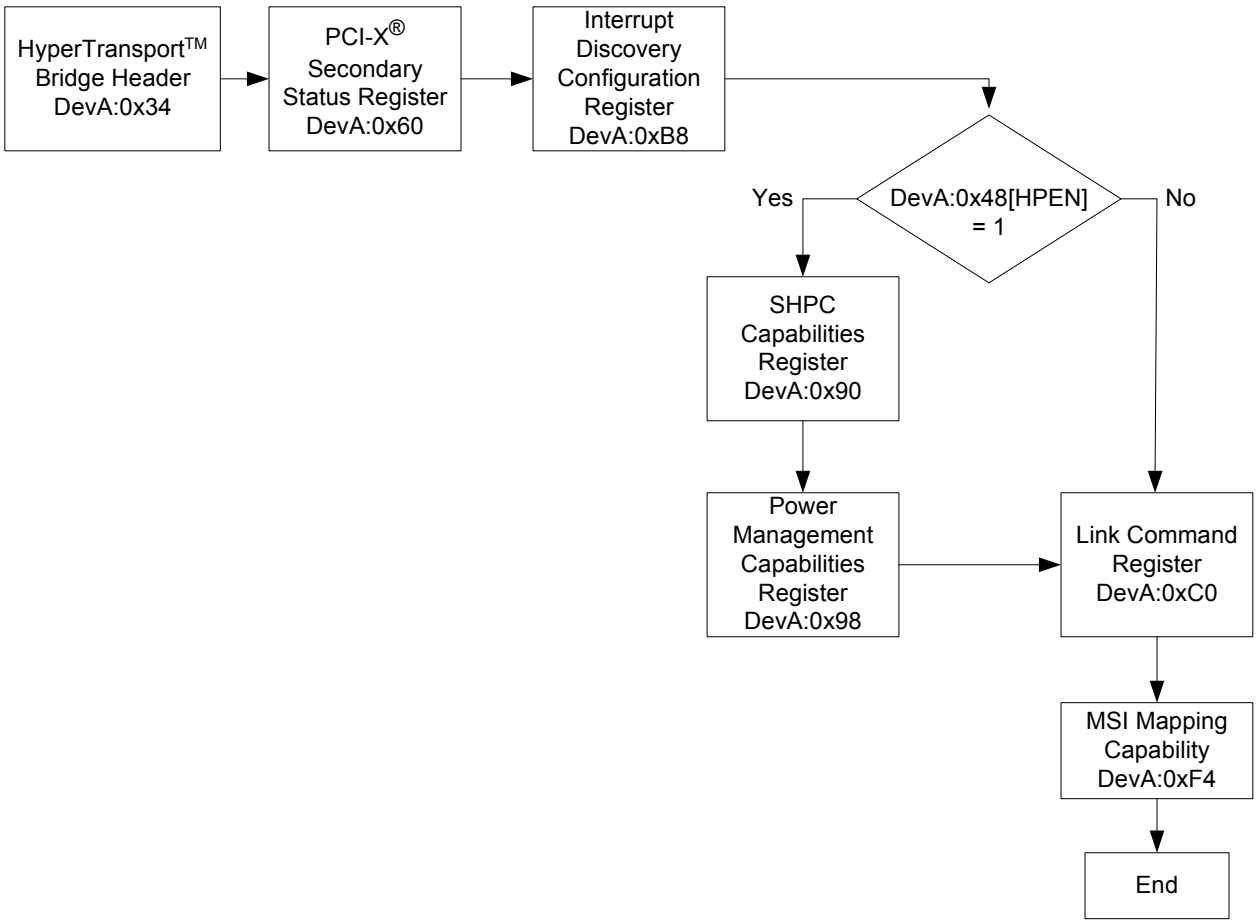
# Chapter 3 Registers

## 3.1 Register Overview

The AMD-8132™ HyperTransport™ PCI-X®2.0 tunnel includes several sets of registers accessed through a variety of address spaces. Except where otherwise noted, all registers are reset to their default values by LDTRESET_L.

Configuration and status information specific to HyperTransport technology is mapped into configuration space using the capabilities list methodology described in the *PCI Local Bus Specification, Rev 2.3*. Figure 17 is an example of the capability block chain for device A.

**Figure 17. Example Capability Block Chain: Device A.**




### 3.1.1 Configuration Space

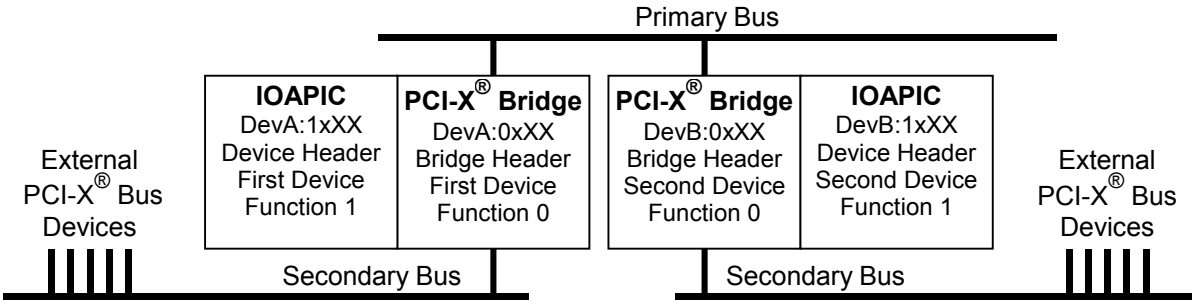
The address space for the AMD-8132 tunnel configuration registers is broken up into devices, functions, and offsets as defined by *HyperTransport™ I/O Link Specification, Rev 2.0*. The address space is accessed by HyperTransport-defined type 0 configuration or extended configuration cycles. The device number is mapped

into bits[15:11] of the configuration address. The function number is mapped into bits[10:8] of the configuration address. The offset is mapped to bits[7:0] of the configuration address.

The address space for the AMD-8132 tunnel configuration space can be reached with either a HyperTransport type 0 access, or with an extended HyperTransport type 0 access. When using an extended type 0 access, all registers with an address above 255 bytes are reserved.

The following diagram shows the devices in configuration space as viewed by software.

**Figure 18. Configuration Space.**




Device A, above, is programmed to be DevA:0xC0[BUID] and device B is DevA:0xC0[BUID] plus 1. See the Link Command register for details. Also see section 1.3.5 HyperTransport™ Requests Claimed by the Bridges.

## 3.1.2 Register Naming and Description Conventions

Configuration register locations are referenced with mnemonics that take the form of Dev[A|B]:[7:0]x[FF:0], where the first bracket contains the device, the second bracket contains the function number, and the last bracket contains the offset.

The AMD-8132 tunnel does not claim configuration register accesses to unimplemented functions within its devices, they are forwarded to the other side of the tunnel. Accesses to unimplemented register locations within implemented functions are claimed, those registers are Reserved.

**Table 3. Register Naming Conventions**

| Device | Function | Mnemonic | Registers |
|---|---|---|---|
| A | 0 | DevA:0xXX | PCI-PCI bridge A registers; link and PCI-X® capabilities block. |
| A | 1 | DevA:1xXX | IOAPIC for PCI-X® bridge A. |
| B | 0 | DevB:0xXX | PCI-PCI bridge B registers; PCI-X® capabilities block. |
| B | 1 | DevB:1xXX | IOAPIC for PCI-X® bridge B. |

Other register locations (e.g., memory mapped registers) are referenced with an assigned mnemonic that specifies the address space and offset. These mnemonics start with four characters that identify the space followed by characters that identify the offset within the space.

**Table 4. Memory Mapped Address Spaces**

| Base Address Register | Size (bytes) | Mnemonic | Registers |
|---|---|---|---|
| Dev[B,A]:1x10/48 | 4K | APIC[B,A]:XX | IOAPIC registers. Base address register at offset 10h enabled by Dev[B,A]:1x44[OSVISBAR]. |
| Dev[B,A]:0x10 | 4K | SHPC[B,A]:XX | Standard hot-plug controller register set. Access is enabled by Dev[B,A]:0x48[HPEN]. Access to these registers is provided through both memory space and configuration space. To access through configuration space, Dev[B,A]:0x90[SELECT] specifies the DWORD offset and Dev[B,A]:0x94 provides the DWORD data port. |

Register fields within register locations are also identified with a name or bit group in brackets following the register location mnemonic.

**Table 5. Register Attributes**

| Type | Description |
|---|---|
| Read or Read Only | Capable of being read by software. Read Only implies that the register cannot be written to by software. |
| Write | Capable of being written by software. |
| Set by Hardware | Register bit is set high by hardware. |
| Write Once | After LDTRESET_L, these registers may be written to once. After being written, they become Read Only until the next LDTRESET_L assertion. The Write Once control is byte based. So, for example, software may write each byte of a Write Once DWORD as four individual transactions. As each byte is written, that byte becomes Read Only. |
| Write 1 to clear | Software must write a 1 to the bit to clear it. Writing a 0 to these bits has no effect. |
| Write 1 only | Software can set the bit high by writing a 1 to it. However, subsequent writes of 0 have no effect. LDTRESET_L must be asserted in order to clear the bit. |
| Reserved | For AMD internal use only. When reading Reserved bits, ignore the data. When writing to Reserved bits, preserve the data and merge it with the write; failure to do this results in undefined behavior. |
| **Note:** Unless otherwise noted or described as being assigned a value at the assertion of PWROK, all registers are reset to their default values by LDTRESET_L. | |

**Table 6. AMD-8132™ Tunnel Registers and Register Addresses**

| Register Name | Register Address |
|---|---|
| PCI-X® Bridge Vendor and Device ID | Dev[B,A]:0x00 |
| PCI-X Bridge Status and Command | Dev[B,A]:0x04 |
| PCI-X Bridge Revision and Class Code | Dev[B,A]:0x08 |
| PCI-X Bridge BIST-Header-Latency-Cache | Dev[B,A]:0x0C |
| PCI-X SHPC Base Address Low | Dev[B,A]:0x10 |
| PCI-X SHPC Base Address High | Dev[B,A]:0x14 |
| PCI-X Bridge Bus Numbers and Secondary Latency | Dev[B,A]:0x18 |
| PCI-X Bridge Memory Base/Limit, I/O Base/Limit, and Secondary Status | Dev[B,A]:0x[30:1C] |
| PCI-X Bridge Capabilities Pointer | Dev[B,A]:0x34 |
| PCI-X Bridge Interrupt and Bridge Control | Dev[B,A]:0x3C |
| PCI-X Miscellaneous | Dev[B,A]:0x40 |
| PCI-X Scratch | Dev[B,A]:0x44 |
| PCI-X Misc II and Pins Latched at Rising Edge of PWROK | Dev[B,A]:0x48 |
| Prefetch Control | Dev[B,A]:0x4C |
| PCI-X Secondary Status | Dev[B,A]:0x60 |
| PCI-X Bridge Status | Dev[B,A]:0x64 |
| PCI-X Upstream Split Transaction | Dev[B,A]:0x68 |
| PCI-X Downstream Split Transaction | Dev[B,A]:0x6C |
| PCI-X ECC Control and Status | Dev[B,A]:0x70 |
| PCI-X ECC First Address | Dev[B,A]:0x74 |
| PCI-X ECC Second Address | Dev[B,A]:0x78 |
| PCI-X ECC Attribute | Dev[B,A]:0x7C |
| Misc Bridge Errors | Dev[B,A]:0x80 |
| Misc Error Enables | Dev[B,A]:0x84 |
| SHPC Capabilities | Dev[B,A]:0x90 |
| SHPC Data | Dev[B,A]:0x94 |
| Power Management Capabilities | Dev[B,A]:0x98 |
| Power Management Status and Control | Dev[B,A]:0x9C |
| Extended Configuration Address Range | DevA:0xB4 |
| Interrupt Discovery and Configuration | Dev[B,A]:0x[BC,B8] |
| HyperTransport™ Revision ID Capability Block | DevB:0xC0 |
| Link Command | DevA:0xC0 |
| Link Configuration and Control | DevA:0xC4 and DevA:0xC8 |

**Table 6. AMD-8132™ Tunnel Registers and Register Addresses (Continued)**

| Register Name | Register Address |
|---|---|
| Link Revision, Errors, and Frequency Capability 0 | DevA:0xCC |
| Feature, Link Errors, and Frequency Capability 1 | DevA:0xD0 |
| Error Handling and Link Enumeration | DevA:0xD4 |
| Link Non-Prefetchable Memory Space Extension | DevA:0xD8 |
| Tunnel Control | DevA:0xDC |
| Clock Control | DevA:0xF0 |
| MSI Mapping Capability Block Header | Dev[B,A]:0xF4 |
| MSI Mapping Capability Block Lower Address | Dev[B,A]:0xF8 |
| MSI Mapping Capability Block Upper Address | Dev[B,A]:0xFC |
| IOAPIC Vendor and Device ID | Dev[B,A]:1x00 |
| IOAPIC Status and Command | Dev[B,A]:1x04 |
| IOAPIC Revision and Class Code | Dev[B,A]:1x08 |
| IOAPIC Device BIST-Header-Latency-Cache | Dev[B,A]:1x0C |
| IOAPIC Base Address Low | Dev[B,A]:1x10 and Dev[B,A]:1x48 |
| IOAPIC Base Address High | Dev[B,A]:1x14 and Dev[B,A]:1x4C |
| IOAPIC Device Subsystem ID and Subsystem Vendor ID | Dev[B,A]:1x2C |
| Pointer to Capabilities Block | Dev[B,A]:1x34 |
| IOAPIC Control | Dev[B,A]:1x44 |
| HyperTransport Revision Capabilities Block | Dev[B,A]:1x50 |
| PCI-X PHY Compensation Control | Dev[B,A]:1x[94,90,8C,88,84,80] |
| Link PHY Compensation Control | Dev[B,A]:1x[D8,D4,C8,C4,C0] |
| Performance Counters and Control | DevA:1x[AC,A8,A4,A0] |
| IOAPIC Register Space | APIC[B,A]:00[7:0] |
| SHPC Base Offset | SHPC[B,A]:00 |
| SHPC Slots Available I | SHPC[B,A]:04 |
| SHPC Slots Available II | SHPC[B,A]:08 |
| SHPC Slot Configuration | SHPC[B,A]:0C |
| SHPC Secondary Bus Configuration | SHPC[B,A]:10 |
| SHPC Command and Status | SHPC[B,A]:14 |
| SHPC Interrupt Locator | SHPC[B,A]:18 |
| SHPC SERR Locator | SHPC[B,A]:1C |
| SHPC SERR-INT | SHPC[B,A]:20 |
| SHPC Logical Slot | SHPC[B,A]:[30,2C,28,24] |

# 3.2 PCI-X® Bridge Configuration Registers

These registers are located in PCI configuration space in the first device (device A) and second device (device B), function 0. See section 3.1.2 for a description of the register naming convention.

### PCI-X® Bridge Vendor and Device ID — Dev[B,A]:0x00

Default: 7458 1022h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:16 | **Device ID.** PCI bridge device ID is 7458. |
| 15:0 | **Vendor ID.** AMD's vendor ID is 1022. |

### PCI-X® Bridge Status and Command — Dev[B,A]:0x04

Default: 0010 0000h — Attribute: See Below

| Bits | Description |
|---|---|
| 31 | **Detected Parity Error [DPE].** Read. Set by hardware. Write 1 to clear. Set if the AMD-8132™ tunnel accepts a HyperTransport™ read response or posted request with data error indicated.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 30 | **Signalled System Error [SSE].** Read. Set by hardware. Write 1 to clear.<br>1 = A system error was signalled (both links were flooded with sync packets) due to error detection by this device. This bit cannot be set unless Dev[B,A]:0x04[SERREN] is high.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 29 | **Received Master Abort [RMA].** Read. Set by hardware. Write 1 to clear.<br>1 = A request sent to the host bus received a master abort.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 28 | **Received Target Abort [RTA].** Read. Set by hardware. Write 1 to clear.<br>1 = A request sent to the host bus received a target abort.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 27 | **Signalled Target Abort [STA].** Read. Set by hardware. Write 1 to clear.<br>1 = A target abort was signalled to the host.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 26:25 | Reserved. |
| 24 | **Master Data Uncorrectable Error [MDPE].** Read. Set by hardware. Write 1 to clear. Set if the AMD-8132 tunnel issues a HyperTransport™ posted request or accepts a HyperTransport response with data error indicated and Dev[B,A]:0x04[PERSP] is set.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 23:21 | Reserved. |
| 20 | **Capabilities Pointer.** Read Only. This bit is fixed in the high state. |

| | |
|---|---|
| 19 | **Interrupt Status [INTSTATUS].** Read Only. Status of interrupts generated by the AMD-8132 tunnel. If this bit is a 1, then the AMD-8132 tunnel has detected an SHPC interrupt, a fatal error, or a nonfatal error, and is configured to drive this interrupt onto the [B,A]_PIRQA_L, [B,A]_PIRQB_L, or [B,A]_PIRQC_L interrupt pins respectively, unless gated by the interrupt disable bit [INTDISABLE].<br>Note: This bit is set regardless of the state of the interrupt disable bit; i.e., if the interrupt disable bit is set but all other conditions that would cause interrupt pins to be asserted are true, then this bit is still set. |
| 18:11 | Reserved. |
| 10 | **Interrupt Disable [INTDISABLE].** Read-Write. Disables assertion of [B,A]_PIRQA_L, [B,A]_PIRQB_L, and [B,A]_PIRQC_L by the AMD-8132 tunnel. Other devices may still assert these interrupts; the AMD-8132 tunnel response to those assertions is not affected by this bit.<br>0 = Enable assertion of [B,A]_PIRQA_L, [B,A]_PIRQB_L, and [B,A]_PIRQC_L. This bit is 0 after LDTRESET_L.<br>1 = Disable assertion of [B,A]_PIRQA_L, [B,A]_PIRQB_L, and [B,A]_PIRQC_L. |
| 9 | Reserved. |
| 8 | **SERR_L Enable [SERREN].** Read-Write.<br>0 = Dev[B,A]:0x04[SSE] cannot be set high and the AMD-8132 tunnel does not initiate flooding the links with sync packets although it can still propagate sync flooding.<br>1 = Dev[B,A]:0x04[SSE] is enabled to be set high and the AMD-8132 tunnel is enabled to flood the links with sync packets in response to detected system errors. |
| 7 | Reserved. |
| 6 | **Parity Error Response [PERSP].** Read-Write. Enables setting Dev[B,A]:0x04[MDPE] because of data errors on the HyperTransport™ chain. Enables the propagation of data errors from the PCI/PCI-X® bus to the HyperTransport chain in target done responses. If clear, MDPE may never be set and target done responses from PCI/PCI-X are always issued with the data error bit clear. |
| 5 | Reserved. |
| 4 | **Memory Write And Invalidate Enable [MWIEN].** Read-Write. Enables the generation of the Memory Write and Invalidate command on the PCI bus. |
| 3 | **Special Cycle Enable.** Read Only. This bit is hardwired low. |
| 2 | **PCI Master Enable [MASEN].** Read-Write.<br>0 = Disables secondary bus masters from initiating cycles to the host but does not block interrupt packet generation by the AMD-8132 tunnel.<br>1 = Enables secondary bus masters to initiate cycles to the host. |
| 1 | **Memory Enable [MEMEN].** Read-Write.<br>0 = Not enabled.<br>1 = Enables access to the secondary bus memory space and to the SHPC register space through the memory space BAR, Dev[B,A]:0x10. This bit does not affect access to SHPC registers through configuration space Dev[B,A]:0x[94:90]. |
| 0 | **I/O Enable [IOEN].** Read-Write. 1 = Enables access to the secondary bus I/O space. |

## PCI-X® Bridge Revision and Class Code — Dev[B,A]:0x08

Default: A1: 0604 0?01h, B1: 0604 0?11h, B2: 0604 0?12h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:8 | **CLASSCODE.** Provides the bridge class code as defined in *PCI Local Bus Specification, Rev 2.3*. Bits[3:1] of this field are zero. DevA:0x08[8] is the same as DevA:0x48[COMPAT]. DevB:0x08[8] is zero. |
| 7:0 | **REVISION.** AMD-8132™ tunnel revision— 01h = revision A1, 11h = revision B1, and 12h = revision B2. |

## PCI-X® Bridge BIST-Header-Latency-Cache — Dev[B,A]:0x0C

Default: 0081 0000h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:24 | **BIST.** Read Only. These bits are fixed at their default values. |
| 23:16 | **HEADER.** Read Only. These bits are fixed at their default values. |
| 15:8 | **LATENCY.** Read-Write. These bits control no hardware. |
| 7:0 | **CACHE.** Read-Write. This register is used to control the generation of Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate commands to the PCI bus. HyperTransport™ reads to prefetchable memory of more than one doubleword, but less than or equal to the next boundary aligned to the value of this register, generate Memory Read Line on PCI. If reading past the boundary, Memory Read Multiple is generated. HyperTransport posted writes generate Memory Write and Invalidate PCI commands if the write will write to every byte in the cache line, and if Dev[B,A]:0x04[MWIEN] is asserted.<br>Note: Only 8 or 16 doubleword cache line sizes are supported. If the register is set to any value other than 8 or 16, then no Memory Read Line, Memory Read Multiple, or Memory Write and Invalidate commands will be issued on PCI. |

## PCI-X® SHPC Base Address Low — Dev[B,A]:0x10

Default: 0000 000?h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:12 | **SHPC Base Address Register [SHPCBAR] Low.** Read-Write. These bits specify bits [31:12] of the memory address space of the SHPC register set SHPC[B,A]:XX. If Dev[B,A]:0x48[HPEN] is low, the SHPCBAR is forced to read only 0. |
| 11:0 | **Hardwired.** Read Only.<br>• If Dev[B,A]:0x48[HPEN] is high, these bits read 004h to indicate a 4-Kbyte block of 64-bit, non-prefetchable memory space.<br>• If Dev[B,A]:0x48[HPEN] is low, these bits read all 0s. |

## PCI-X® SHPC Base Address High — Dev[B,A]:0x14

Default: 0000 0000h — Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:0 | **SHPC Base Address Register [SHPCBAR] High.** These bits specify bits [63:32] of the memory address space of the SHPC register set SHPC[B,A]:XX. If Dev[B,A]:0x48[HPEN] is low, the SHPCBAR is forced to read only 0. |

## PCI-X® Bridge Bus Numbers and Secondary Latency — Dev[B,A]:0x18

Default: ?000 0000h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:27 | **Secondary Latency Timer [SECLAT[7:3]].** Read-Write. The default value of SECLAT[7:0] after the deassertion of LDTRESET_L is 00h when the bridge is in conventional PCI mode and 40h when the bridge is in PCI-X® mode.<br>• In conventional PCI mode, this functions per the *PCI Local Bus Specification, Rev 2.3*.<br>• In PCI-X mode, the latency timer is not used when the AMD-8132 tunnel is the master of host-initiated transactions to the PCI-X bus. In PCI-X mode, the latency timer limits the number of clocks that the AMD-8132 tunnel owns the bus as the completer (master) only during split completions. For these transactions, the latency timer counts while [B,A]_FRAME_L is asserted. If the latency timer exceeds SECLAT and the arbiter has deasserted the grant signal for the AMD-8132 tunnel because another master is requesting the bus, then the transaction is disconnected by the AMD-8132 tunnel at the next convenient 128-byte boundary.<br>Note: This register is not reset on a secondary ([B,A]_RESET_L) reset assertion. If the bus mode is changed between PCI and PCI-X through a secondary reset event, it is the responsibility of software to set SECLAT for the new mode. |
| 26:24 | **Secondary Latency Timer [SECLAT[2:0]].** Read Only (000b). |
| 23:16 | **Subordinate PCI Bus Number [SUBBUS].** Read-Write. |
| 15:8 | **Secondary PCI Bus Number [SECBUS].** Read-Write. |
| 7:0 | **Primary PCI Bus Number [PRIBUS].** Read-Write. |

## PCI-X® Bridge Memory Base/Limit, I/O Base/Limit, and Secondary Status — Dev[B,A]:0x[30:1C]

These registers specify the address windows for I/O space Dev[B,A]:0x1C and Dev[B,A]:0x3; non-prefetchable memory space Dev[B,A]:0x20; and prefetchable memory space Dev[B,A]:0x24, Dev[B,A]:0x28, and Dev[B,A]:0x2C. These address windows are for transactions mapped from the HyperTransport link address space to the secondary PCI bus.

The links support 25 bits of I/O space. PCI-X supports 32 bits of I/O space. Host accesses to the link-defined I/O region are mapped to the PCI-X I/O window with the 7 MSB always zero. PCI-X I/O accesses in which any of the 7 MSBs are other than zero are ignored. The PCI-X I/O space window is defined as follows:

```
PCI-X IO window =
{Dev[B,A]:0x30[31:16], Dev[B,A]:0x1C[15:12], 12'hFFF} >= {7'h00,address[24:0]} >=
{Dev[B,A]:0x30[15:0],   Dev[B,A]:0x1C[7:4],  12'h000};
```

The links and PCI-X support 40 bits of non-prefetchable memory space. The PCI-X non-prefetchable memory space window is defined as follows:

```
PCI-X non-prefetchable memory window =
{24'h00, DevA:0xD8[15:8], Dev[B,A]:0x20[31:20], 20'hF_FFFF} >= address >=
{24'h00, DevA:0xD8[7:0],  Dev[B,A]:0x20[15:4],  20'h0_0000};
```

The links and PCI-X support 64 bits of prefetchable memory space. All link memory mapped I/O space may be within the PCI-X prefetchable memory window. The PCI-X prefetchable memory space window is defined as follows:

```
PCI-X prefetchable memory window =
{Dev[B,A]:0x2C[31:0], Dev[B,A]:0x24[31:20], 20'hF_FFFF} >= address >=
{Dev[B,A]:0x28[31:0], Dev[B,A]:0x24[15:4],  20'h0_0000};
```

These windows may also be altered by Dev[B,A]:0x3C[VGAEN, ISAEN].

When the address from either the host or a secondary bus master is inside one of the windows, then the transaction is assumed to be intended for a target that sits on the secondary bus. Therefore, the following transactions are possible:

- Host-initiated transactions inside the windows are routed to the secondary bus.
- Secondary PCI-initiated transactions inside the windows are not claimed by the AMD-8132 tunnel.
- Host-initiated transactions outside the windows are passed through the tunnel or master aborted if the AMD-8132 tunnel is at the end of a chain.
- Secondary PCI-initiated transactions outside the windows are claimed by the AMD-8132 tunnel and passed to the host.

For example: if IOBASE > IOLIM and Dev[B,A]:0x3C[VGAEN] is 0, then no host-initiated I/O space transactions are forwarded to the secondary bus and all secondary PCI bus-initiated I/O space (not configuration) transactions are forwarded to the host. If MEMBASE > MEMLIM and PMEMBASE > PMEMLIM and Dev[B,A]:0x3C[VGAEN] is 0, then no host-initiated memory space transactions are forwarded to the secondary bus and all secondary PCI bus-initiated memory space transactions are forwarded to the host.

The windows may be overridden for compatibility traffic, enabled by DevA:0x48[COMPAT] as defined in the *HyperTransport™ I/O Link Specification, Rev 2.0*.

**Dev[B,A]:0x1C**

Default: 0220 01F1h Attribute: See Below

| Bits | Description |
|---|---|
| 31 | **Detected Uncorrectable Error [DPE].** Read. Set by hardware. Write 1 to clear. Set if the AMD-8132™ tunnel detects an uncorrectable error on the PCI-X® bus during an address/attribute cycle, or while accepting read data or write data.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 30 | **Received System Error [RSE].** Read. Set by hardware. Write 1 to clear.<br>1 = The AMD-8132 tunnel detected either [B,A]_SERR_L or [B,A]_SHPC_SERR asserted. In order to clear this bit, these signals must be deasserted.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 29 | **Received Master Abort [RMA].** Read. Set by hardware. Write 1 to clear.<br>1 = The AMD-8132 tunnel received a master abort as a master on the secondary bus.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 28 | **Received Target Abort [RTA].** Read. Set by hardware. Write 1 to clear.<br>1 = The AMD-8132 tunnel received a target abort as a master on the secondary PCI bus.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 27 | **Signalled Target Abort [STA].** Read. Set by hardware. Write 1 to clear.<br>1 = The AMD-8132 tunnel generated a target abort as a target on the secondary PCI bus.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 26:25 | **Device Select Timing.** Read Only. These bits are hardwired to indicate medium decoding speed. |
| 24 | **Master Data Uncorrectable Error [MDPE].** Read. Set by hardware. Write 1 to clear.<br>1 = The AMD-8132 tunnel sets this bit if Dev[B,A]:0x3C[PEREN] is set and one of these conditions occurs:<br>• An uncorrectable error is detected during a data phase of a read.<br>• The detection of [B,A]_PERR_L asserted during a write as a master on the secondary bus.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 23 | **Fast Back-to-Back Enable [FBBEN].** Read Only. This bit is fixed low, indicating the AMD-8132 tunnel does not support fast back-to-back transactions. |
| 22:16 | Read Only. These bits are fixed in their default state. |
| 15:12 | **IO Limit Address [IOLIM].** Address bits[15:12]. See Dev[B,A]:0x[30:1C]. |
| 11:8 | Read Only. Returns 0001 indicating the I/O upper limit is implemented. |
| 7:4 | **IO Base Address [IOBASE].** Address bits[15:12]. See Dev[B,A]:0x[30:1C]. |
| 3:0 | Read Only. Returns 0001 indicating the I/O upper base is implemented. |

**Dev[B,A]:0x20**

Default: 0000 FFF0h Attribute: See Below

| Bits | Description |
|---|---|
| 31:20 | **Non-Prefetchable Memory Limit Address [MEMLIM].** Address bits[31:20]. See Dev[B,A]:0x[30:1C]. |
| 19:16 | Reserved. |
| 15:4 | **Non-Prefetchable Memory Base Address [MEMBASE].** Address bits[31:20]. See Dev[B,A]:0x[30:1C]. |
| 3:0 | Reserved. |

**Dev[B,A]:0x24**

Default: 0001 FFF1h Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:20 | **Prefetchable Memory Limit Address [PMEMLIM].** Address bits[31:20]. See Dev[B,A]:0x[30:1C]. |
| 19:16 | Read Only. Returns 0001 indicating prefetchable memory limit upper is implemented. |
| 15:4 | **Prefetchable Memory Base Address [PMEMBASE].** Address bits[31:20]. See Dev[B,A]:0x[30:1C]. |
| 3:0 | Read Only. Returns 0001 indicating prefetchable memory base upper is implemented. |

**Dev[B,A]:0x28**

Default: 0000 0000h Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:0 | **Prefetchable Memory Base Address [PMEMBASE].** Address bits[63:32]. See Dev[B,A]:0x[30:1C]. |

**Dev[B,A]:0x2C**

Default: 0000 0000h Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:0 | **Prefetchable Memory Limit Address [PMEMLIM].** Address bits[63:32]. See Dev[B,A]:0x[30:1C]. |

**Dev[B,A]:0x30**

Default: 0000 FFFFh Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:16 | **IO Limit Address [IOLIM].** Address bits[31:16]. See Dev[B,A]:0x[30:1C]. |
| 15:0 | **IO Base Address [IOBASE].** Address bits[31:16]. See Dev[B,A]:0x[30:1C]. |

## PCI-X® Bridge Capabilities Pointer — Dev[B,A]:0x34

Default: 0000 0060h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:8 | Reserved. |
| 7:0 | **CAPABILITIES_PTR.** Points to the next capability block. See Dev[B,A]:0x60. |

## PCI-X® Bridge Interrupt and Bridge Control — Dev[B,A]:0x3C

Default: 0000 0?FFh — Attribute: See Below

| Bits | Description |
|---|---|
| 31:28 | Reserved. |
| 27 | **Discard Timer Sync Flood Enable [DTSE].** Read-Write. If Dev[B,A]:0x3C[DTS] is high and this bit is set, indicate an error as follows:<br>• If Dev[B,A]:0x04[SERREN] is asserted and Dev[B,A]:0x40[PCIErrorSerrDisable] is deasserted, then Dev[B,A]:0x04[SSE] is set and the links are flooded with sync packets.<br>• If Dev[B,A]:0x40[PCIErrorNonfatalEn] or Dev[B,A]:0x40[PCIErrorFatalEn] is asserted, then assert the nonfatal or fatal signal respectively. |
| 26 | **Discard Timer Status [DTS].** Read. Set by hardware. Write 1 to clear.<br>1 = The secondary discard timer discard timer timed out. This bit is not capable of being set when the secondary bus is in PCI-X® mode.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 25 | **Secondary Discard Timer [SDT].** Read-Write. This bit is used to decrease the number of clocks used by the PCI-defined discard timer.<br>0 = Discard timer times out after 32K PCLK cycles.<br>1 = Discard timer times out after 1K PCLK cycles. |
| 24:23 | Reserved. |
| 22 | **Secondary Bus Reset [SBRST].** Read-Write.<br>0 = [B,A]_RESET_L not asserted.<br>1 = [B,A]_RESET_L asserted; secondary PCI bus placed into reset state. |
| 21 | **Master Abort Response [MARSP].** Read-Write.<br>0 = Master aborts to nonposted requests result in normal responses on the originating bus. Read responses are sent with the appropriate amount of data, which are all 1s. Posted requests from HyperTransport™ that are master aborted on PCI/PCI-X® are silently dropped.<br>1 = The responses to nonposted requests that come from the host bus or secondary bus that result in master aborts indicate a target abort to the initiating bus (through PCI bus protocol or link protocol). Master aborts on PCI/PCI-X result in the assertion of Dev[B,A]:0x80[DISCARDED_POST]. |

| | |
|---|---|
| 20 | **VGA 16 Bit Decode [VGA16DEC].** Read-Write. Resets to 0.<br>• If set, bits [15:10] are compared when decoding VGA-compatible I/O addresses.<br>• If clear, address bits [15:10] are ignored; allowing VGA-compatible I/O addresses to alias through the first 64 Kbytes of I/O space.<br>See bit 19, [VGAEN]. |
| 19 | **VGA Decoding Enable [VGAEN].** Read-Write.<br>0 = The AMD-8132™ tunnel does not decode VGA-compatible address ranges.<br>1 = Route host-initiated commands targeting VGA-compatible address ranges to the secondary bus. These include memory accesses from A0000h to BFFFFh and I/O accesses in which address bits [9:0] range from 3B0h to 3BBh or 3C0h to 3DFh. If Dev[B,A]:0x3C[VGA16DEC] is asserted, bits [15:10] are 0. If Dev[B,A]:0x3C[VGA16DEC] is clear, bits [15:10] are ignored in the decode. Bits [31:16] are 0. Secondary bus accesses to these ranges are not claimed by the AMD-8132 tunnel. |
| 18 | **ISA Decoding Enable [ISAEN].** Read-Write.<br>0 = The PCI I/O window is the whole range specified by Dev[B,A]:0x1C[15:0] and Dev[B,A]:0x30.<br>1 = The I/O address window specified by Dev[B,A]:0x1C[15:0] and Dev[B,A]:0x30 is limited to the first 256 bytes of each 1-Kbyte block specified; this only applies to the first 64 Kbytes of I/O space. |
| 17 | **System Error Enable [SERREN].** Read-Write. If this bit is set and Dev[B,A]:0x04[SERREN] is set and Dev[B,A]:0x1C[RSE] is set (indicating that SERR assertion has been detected on the secondary bus), then the AMD-8132 tunnel responds by flooding both outgoing HyperTransport™ links with sync packets and setting Dev[B,A]:0x04[SSE]. |
| 16 | **Uncorrectable Error Response Enable [PEREN].** Read-Write. Enables setting Dev[B,A]:0x1C[MDPE] in response to uncorrectable errors on the local PCI/PCI-X® bus.<br>See Chapter 5 Error Conditions and Handling. |
| 15:8 | **INTERRUPT_PIN.** Read Only.<br>• If Dev[B,A]:0x48[HPEN] is low, then Dev[B,A]:0x3C[INTERRUPT_PIN] is 00h.<br>• If Dev[B,A]:0x48[HPEN] is high, then Dev[B,A]:0x3C[INTERRUPT_PIN] is 01h.<br>Note: When hot-plug mode is enabled, [B,A]_PIRQA_L can be asserted for hot-plug events. |
| 7:0 | **INTERRUPT_LINE.** Read-Write. These bits control no internal logic. |

## PCI-X® Miscellaneous — Dev[B,A]:0x40

Default: 001F 0001h — Attribute: See Below

| Bits | Description |
|---|---|
| 31 | **WriteChainEnable.** Read-Write. If this bit is asserted, allow multiple write packets from HyperTransport™ directed at this PCI bus to be chained together. See section 1.3.3.<br>Note: Programming of this bit may vary based on platform requirements. This bit should be clear for systems with devices or device drivers that do not operate correctly if writes are combined by the AMD-8132 tunnel. |
| 30 | **PCIMemWrBufMode.** Read-Write. After reset deasserts, value = 1.<br>0 = The AMD-8132™ tunnel will retry PCI Memory Writes if it does not have at least one internal buffer available.<br>1 = The AMD-8132 tunnel will retry PCI Memory Writes to the lower half of a 64-byte HyperTransport™ cache line if it does not have at least two internal buffers available. This behavior results in more efficient use of HyperTransport bus bandwidth for PCI Memory Writes when all byte enables are set. |
| 29 | **ENABLE_SNOOP_HP.** Read-Write. If this bit is asserted, the SNOOP_HP bit is set whenever the PCI bus is disabled during hot-plug events. This bit is only used in single slot mode. When not in single slot mode, writing a 1 to this bit can result in undefined behavior. |
| 28 | **SNOOP_HP.** Read. Set by hardware. Write 1 to clear. This bit is only set if ENABLE_SNOOP_HP is set, hot-plug is enabled for this bus, and this bus is disabled due to a hot-plug event. If this bit does become set, all operations intended for this PCI bus that would have been master aborted because this bus is disabled get a non-error response instead. For the period of time that SNOOP_HP is set, the behavior is the same as if MARSP was not set; except that the data returned on the HyperTransport™ bus is all 0s instead of all 1s. This bit is only used in single slot mode.<br>Note: This bit should be cleared by software writing a 1 to this location after the bus is re-enabled. |
| 27 | **NONPOSTFPEN.** Read-Write. Resets to 0.<br>0 = Disable forward progress logic for PCI/PCI-X® nonposted request buffers.<br>1 = Enable forward progress logic for PCI/PCI-X® nonposted request buffers. The AMD-8132 tunnel ensures each PCI/PCI-X master continues to make forward progress in the event more nonposted requests are being received than the AMD-8132 tunnel can accept simultaneously. If only one nonposted buffer is available, it will be reserved for the PCI/PCI-X master that has been waiting longest. All other devices will be retried until that master gets its request accepted by the AMD-8132 tunnel or until additional buffers become available. This logic should not be enabled when the AMD-8132 tunnel is in external arbiter mode since the internal arbiter grants are used to track which device is the current bus master. |
| 26 | **POSTFPEN.** Read-Write. Resets to 0.<br>0 = Disable forward progress logic for PCI/PCI-X® posted buffers.<br>1 = Enable forward progress logic for PCI/PCI-X® posted buffers. The AMD-8132 tunnel ensures each PCI/PCI-X master continues to make forward progress in the event more posted requests are being received than the AMD-8132 tunnel can accept simultaneously. If only enough posted buffers are available to satisfy one PCI/PCI-X master they will be reserved for the PCI/PCI-X master waiting the longest. All other devices will be retried until that master gets its request accepted by the AMD-8132 tunnel or until additional buffers become available. This logic should not be enabled when the AMD-8132 tunnel is in external arbiter mode since the internal arbiter grants are used to track which device is the current bus master. |

| | |
|---|---|
| 25 | **MSIErrorNonfatalEn.** Read-Write. Resets to 0. When this bit is set, it causes a nonfatal error interrupt to be issued whenever Dev[B,A]:0x80[DROPPED_MSI] is asserted. |
| 24 | **MSIErrorFatalEn.** Read-Write. Resets to 0. When this bit is set, it causes a fatal error interrupt to be issued whenever Dev[B,A]:0x80[DROPPED_MSI] is asserted. |
| 23 | **PCIErrorNonfatalEn.** Read-Write. Resets to 0. When this bit is set, it causes a nonfatal error interrupt to be sent whenever one of the error conditions listed in the description of PCIErrorSerrDisable occurs. |
| 22 | **PCIErrorFatalEn.** Read-Write. Resets to 0. When this bit is set, it bit causes a fatal error interrupt to be sent whenever one of the error conditions listed in the description of PCIErrorSerrDisable occurs. |
| 21 | **PCIErrorSerrDisable.** Read-Write. Resets to 0. When this bit is set, it prevents errors detected on the secondary bus from causing HyperTransport™ sync flood. The gated errors are:<br>• Address or attribute phase uncorrectable error while the AMD-8132 tunnel is a potential target of the operation and secondary parity error response is enabled. Indicated by the assertion of Dev[B,A]:0x80[ADDR_OR_ATTR_ERR], qualified with Dev[B,A]:0x3C[PEREN].<br>• Detecting a master abort, qualified by Dev[B,A]:0x3C[MARSP]; target abort, or PERR_L assertion ,qualified by Dev[B,A]:0x3C[PEREN], while the AMD-8132 tunnel is the master for a posted write operation. Indicated by the assertion of Dev[B,A]:0x80[DISCARDED_POST].<br>• Detecting a master abort, qualified by Dev[B,A]:0x3C[MARSP], or target abort while the AMD-8132 tunnel is the master for a split completion operation. Indicated by the assertion of Dev[B,A]:0x60[SCD].<br>• Detecting an uncorrectable error while the AMD-8132 tunnel is the target of a split completion message, qualified by Dev[B,A]:0x3C[PEREN]. Indicated by the assertion of Dev[B,A]:0x80[SCM_PAR_ERR].<br>• The secondary discard timer timed out, qualified by Dev[B,A]:0x3C[DTSE]. Indicated by the assertion of Dev[B,A]:0x3C[DTS]. |
| 20:16 | **PCLKEN[4:0].** Read-Write. Each of these bits controls a [B,A]_PCLK[4:0] signal. Bit 16 controls PCLK 0, bit 17 controls PCLK1, and so forth.<br>0 = The PCLK signal is forced low. The intended use is to disable PCLK signals that correspond to unimplemented PCI-X® devices or slots.<br>1 = The PCLK signal is enabled to toggle. |
| 15 | Reserved. |
| 14 | **DIS64.** Read-Write. If this bit is a 1, the AMD-8132 tunnel only generates and responds to transactions on this PCI bus as a 32-bit device. The AMD-8132 tunnel never asserts [B,A]_REQ64_L in the address phase and never asserts [B,A]_ACK64_L while asserting [B,A]_DEVSEL_L. |
| 13 | **DISPU.** Read-Write. If this bit is a 1, internal pullups on this PCI bus are disabled and external pullups must be provided. |

| | |
|---|---|
| 12:8 | **PFEN[4:0]_L.** Read-Write. Prefetch Enables (active low). Each of these bits apply to the master attached to one [B,A]_REQ_L/GNT_L pair, Dev[B,A]:0x40[PFEN0_L] applies to [B,A]_REQ0_L/GNT_L[0] and so forth. In external arbiter mode, PFEN[0]_L applies to all external masters.<br>0 = Prefetching is enabled for the specified external master in conventional PCI mode, as controlled by the fields in the prefetch control register Dev[B,A]:0x4C.<br>1 = Prefetching is not enabled. All types of memory reads from the given master result in requests being issued to the HyperTransport™ chain for the initial PCI beat only, and are completed as non-burst accesses on PCI. This field is ignored when the bridge is in PCI-X® mode, Dev[B,A]:0x60[SCF] is not zero. It is expected that these bits are normally left at 0. See section 1.3.4. |
| 7 | Reserved. Must be set to 1 by BIOS. |
| 6 | Reserved. |
| 5 | Reserved. |
| 4 | **Non-Zero Sequence ID [NZSEQID].** Read-Write.<br>0 = The SeqID value is 0h in the upstream link requests resulting from the bridge's external PCI/PCI-X® master read sequences.<br>1 = The SeqID value is not 0h in the upstream link requests resulting from the bridge's external PCI/PCI-X master read sequences. Instead, a unique SeqID is assigned in the range 8h-Fh for each read sequence outstanding on the PCI/PCI-X bus. Setting these bits high may reduce host memory efficiency and bandwidth. It is not expected that these bits will need to be set; the order in which read requests are delivered to destinations does not matter in most cases. For details see the SeqId definition in *HyperTransport™ I/O Link Specification, Rev 2.0.* |
| 3 | Note: Reserved. |

| | |
|---|---|
| 2 | **Single Slot Support [SSS_L].** Read Only. This CSR being asserted (low) indicates there is a single slot present. If it is inactive, there may be multiple slots present. This CSR is latched from [B,A]_GNT_L4 at the rising edge of PWROK and the information is used for several purposes:<br>• Hot-Plug:<br>If the bridge is in hot-plug mode as specified by Dev[B,A]:0x48[HPEN] and SSS_L is low, then the bridge supports a single hot-plug slot without external isolation switches. In this mode, external isolation switches between the AMD-8132 tunnel and the slot are not required and should not be used. See section 1.3.7.<br>If the bridge is in hot-plug mode as specified by Dev[B,A]:0x48[HPEN] and SSS_L is high, then the bridge requires external isolation switches for all hot-plug slots.<br>• PCIXCAP:<br>If SSS_L is low, this indicates there is a single slot present and it may be a PCI-X® Mode 2 capable slot. The bridge will compare the PCIXCAP input to the five voltage levels used by PCI-X Mode 2 devices.<br>If SSS_L is high, this indicates there may be multiple slots present. If there are multiple slots present, then they cannot be Mode 2 capable (the MODE2 connector pin must not be asserted to these slots). The bridge will compare the PCIXCAP input to the three voltage levels used by PCI-X Mode 1 devices.<br>• PCI-X Mode 2:<br>If SSS_L is low, then there is only one slot. This slot is required to use [B,A]_REQ_L0, [B,A]_GNT_L0, and [B,A]_PCLK0, rather than any of the other REQ/GNT/CLK signals. In this mode, [B,A]_GNT_L1 is redefined to be an IDSEL line for an external device; [B,A]_REQ_L1 is redefined to be a VIOSEL signal for the power supply; and [B,A]_PCLK1 is redefined to be a VIOEN signal for the power supply.<br>If SSS_L is high, [B,A]_GNT_L1 and [B,A]_REQ_L1 are available for use as request lines for PCI slots and [B,A]_PCLK1 is available for use as a PCI clock. |
| 1 | **Conventional PCI Mode Frequency [CPCI66].** Read Only. If Dev[B,A]:0x60[SCF] = 0h, then the bridge is in conventional PCI mode and this bit is valid. Otherwise, its state is undefined.<br>0 = [B,A]_PCLK[4:0] toggle at 33 MHz.<br>1 = [B,A]_PCLK[4:0] toggle at 66 MHz.<br>Note: The default state for this field is determined by strapping options described in section 2.5. |
| 0 | **Non-IOAPIC Mode [NIOAMODE].** Read-Write. This bit is used to enable [B,A]_PIRQ[D,C,B,A]_L to the NIOAIRQ[D,C,B,A]_L pins.<br>0 = The state of the PIRQ[D:A]_L pins are not OR'd into the NIOAIRQ[D:A]_L pins. See the equation below.<br>1 = The state of the PIRQ[D:A]_L pin from the bridge is OR'd with the state from the other bridge and passed to the NIOAIRQ[D:A]_L pin. This is shown in the following equations:<br>`NIOAIRQA_L = ~( DevA:0x40[NIOAMODE] & ~A_PIRQA_L & RDRA0[IM]`<br>`\| DevB:0x40[NIOAMODE] & ~B_PIRQA_L & RDRB0[IM] );`<br>`NIOAIRQB_L = ~( DevA:0x40[NIOAMODE] & ~A_PIRQB_L & RDRA1[IM]`<br>`\| DevB:0x40[NIOAMODE] & ~B_PIRQB_L & RDRB1[IM] );`<br>Similarly for NIOAIRQ[C and D]_L, where RDR[B,A][3:0][IM] is the interrupt mask field of the redirection register (see section 3.6), [B,A] = the bridge letter; [3:0] = the redirection register index.<br>Note: The NIOAIRQ[D:A]_L pins are open drain outputs. So a high on the PIRQ input is translated to the high impedance state on the NIOAIRQ output. See section 1.3.2 for more details about interrupt routing. It is expected that this bit is normally left high by system BIOS. |

## PCI-X® Scratch — Dev[B,A]:0x44

Default: 0000 0000h — Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:0 | These bits control no hardware. |

## PCI-X® Misc II and Pins Latched at Rising Edge of PWROK — Dev[B,A]:0x48

The values for bits 7:0 in this register are latched at the rising edge of PWROK.

Default: 0000 00??h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:24 | **LPMARBCOUNT.** Read-Write. In PCI-X® Mode 2, this is the number of idle cycles counted prior to putting the PCI-X arbiter in low power mode. |
| 23 | **LPMARBENABLE.** Read-Write. Setting this bit to 1 allows the PCI-X® Mode 2 arbiter to go into low power mode.<br>Note: If this bit is set, Dev[B,A]_LPMARBCOUNT should be set to a value other than 0; otherwise results are undefined. |
| 22 | **SERR Fatal Enable.** Read-Write. When asserted, this bit causes the fatal error interrupt to be asserted whenever Dev[B,A]:0x1C[RSE] (indicating SERR assertion detected on the secondary bus) is asserted.<br>Note: There is no SERR Flood Enable because this function is covered by Dev[B,A]:0x3C[SERREN]. |
| 21 | **SERR Nonfatal Enable.** Read-Write. When asserted, this bit causes the nonfatal error interrupt to be asserted whenever Dev[B,A]:0x1C[RSE] (indicating SERR assertion detected on the secondary bus) is asserted. |
| 20 | **PERR Flood Enable.** Read-Write. When asserted and [B,A]:0x04[SERREN] is asserted, this bit causes the link to be flooded with sync packets whenever [B,A]:0x80[PERR_OBSERVED] is asserted. |
| 19 | **PERR Fatal Enable.** Read-Write. When asserted, this bit causes the fatal error interrupt to be asserted whenever [B,A]:0x80[PERR_OBSERVED] is asserted. |
| 18 | **PERR Nonfatal Enable.** Read-Write. When asserted, this bit causes the nonfatal error interrupt to be asserted whenever [B,A]:0x80[PERR_OBSERVED] is asserted. |
| 17 | **Correctable Fatal Enable.** Read-Write. When asserted, this bit causes the fatal error interrupt to be asserted whenever a correctable error (Dev[B,A]:0x70[ECC Error Corrected] is 1 and Dev[B,A]:0x70[ECC Error Phase] is not 0) is detected on the PCI-X® bus. |
| 16 | **Correctable Nonfatal Enable.** Read-Write. When asserted, this bit causes the nonfatal error interrupt to be asserted whenever a correctable error (Dev[B,A]:0x70[ECC Error Corrected] is 1 and Dev[B,A]:0x70[ECC Error Phase] is not 0) is detected on the PCI-X® bus. |

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| 15 | **CLEARPCILOG_L.** Read-Write.<br>• If this bit is asserted (0), it causes the following PCI/PCI-X® bus log bits to get cleared immediately after they are set: Dev[B,A]:0x80[SCM_PAR_ERR], Dev[B,A]:0x80[ADDR_OR_ATTR_ERR], and Dev[B,A]:0x80[DISCARDED_POST].<br>• If this bit is deasserted (1), the log bits remain set until cleared by software or a PWROK deassertion.<br>The purpose of this bit is to prevent the above log bits from causing unexpected sync flooding or fatal/nonfatal interrupt assertion in a system that only understands standard PCI-to-PCI bridge error reporting and doesn't query or clear these log bits following a warm reset. When this bit is in its default state, the log bits pulse and potentially cause sync flooding or fatal/nonfatal interrupts when the error initially happens, but there will be no leftover state. To preserve the log bits so they can be polled after a warm reset, set this bit to 1.<br>Note: Reset by PWROK, not LDTRESET_L. |
| 14 | **INTx_PACKET_EN.** Read-Write.<br>• When this CSR is set, transitions on the pins [B,A]_PIRQ[D,C,B,A]_L create INTx virtual wire packets as specified in *HyperTransport™ I/O Link Specification, Rev 2.0*.<br>• When this CSR is cleared, no INTx virtual wire packets are generated.<br>Default = 0. |
| 13 | Reserved. |
| 12 | **PARKATHOST.** Read-Write. This bit controls the parking behavior of the AMD-8132™ tunnel internal PCI/PCI-X® arbiter.<br>• When asserted, the arbiter grants the PCI/PCI-X bus to the AMD-8132 tunnel when there is no request asserted.<br>• When deasserted, the bus remains granted to the last bus master when there is no request.<br>• This bit has no effect in external arbiter mode, Dev[B,A]:0x48[EXTARB_L] = 0. |
| 11 | **SHPC_PI_1.** SHPC Programming Interface 1. If this bit is set, the AMD-8132 tunnel uses an SHPC Programming Interface (PI) of 1 instead of 2 and provides the functions and CSRs associated with PI = 1 instead of PI = 2. Intended for use with older SHPC device drivers which do not support SHPC PI = 2.<br>Note: The value of this bit should not be changed after any SHPC commands have been issued. If it does change, results are undefined. |
| 10 | **PCIX100.** Read-Write. If this bit is set, PCI-X® Mode 1 operates at 100 MHz instead of 133 MHz; PCI-X mode 2 operates at 200 MHz instead of 266 MHz. The default value of this bit is determined by straps on PCIXA_100 for DevA:0x48[PCIX100] and PCIXB_100 for DevB:0x48[PCIX100].<br><br>If the value of this bit or Dev[B,A]:0x48[PSLOW_L] is written to after initial power-up, this change only affects the PCI/PCI-X clock through the following sequence:<br>1. Write the new value to Dev[B,A]:0x48[PCIX100] or Dev[B,A]:0x48[PSLOW_L]; this will not directly modify the PCI clock speed.<br>2. Set Dev[B,A]:0x3C[SBRST]; this will cause the clock frequency to change to the new value.<br>3. Wait at least 1 ms to allow the PCI devices to lock to the new clock frequency.<br>4. Clear Dev[B,A]:0x3C[SBRST]. |

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| 9 | **SCF25.** Read Only. This bit can be used to determine the actual PCI clock speed, used in conjunction with Dev[B,A]:0x40[CPCI66] and Dev[B,A]:0x60[SCF].<br>• If this bit is set, then when Dev[B,A]:0x60[SCF] = 0, the clock speed is 25 or 50 rather than 33 or 66.<br>• When Dev[B,A]:0x60[SCF] is 1 or 5, the clock speed is 50 rather than 66.<br>The value of this register is determined by the value in Dev[B,A]:0x48[PSLOW_L], but the value in Dev[B,A]:0x48[SCF25] is not updated until after the sequence described in Dev[B,A]:0x48[PCIX100]. |
| 8 | Reserved. |
| 7 | **PSLOW_L.** Read-Write. If this bit is 0, conventional PCI runs at either 25 MHz or 50 MHz instead of 33 MHz or 66 MHz; 66 MHz PCI-X® runs at 50 MHz instead of 66 MHz. Higher PCI-X speeds are unaffected by this bit, see section 4.2.2. This bit generally defaults to 1 at cold reset, unless the following is detected on A_COMPAT:<br><br>If A_COMPAT is high at the rising edge of PWROK, stays high for at least an additional 120 ns and then goes low prior to LDTRESET_L deassertion, Dev[B,A]:0x48[PSLOW_L] defaults to 0. If the value of A_COMPAT or Dev[B,A]:0x48[PSLOW_L] is written to after initial power-up in non hot-plug mode, this change only affects the PCI/PCI-X clock through the following sequence:<br>1. Write the new value to Dev[B,A]:0x48[PCIX100] or Dev[B,A]:0x48[PSLOW_L]; this will not directly modify the PCI clock speed.<br>2. Set Dev[B,A]:0x3C[SBRST]; this will cause the clock frequency to change to the new value.<br>3. Wait at least 1 ms to allow the PCI devices to lock to the new clock frequency.<br>4. Clear Dev[B,A]:0x3C[SBRST].<br><br>If the PCI bus is in hot-plug mode and needs to be run at 25 MHz or 50 MHz, then software should write 0 to PSLOW_L after initial powerup and before writing to SHPC[B,A]:0x0C[NSI]. The frequency change occurs immediately and software should wait 1 ms to allow the PCI devices to lock the new clock frequency.<br><br>Note: The state of this signal is captured during a cold reset at the rising edge of LDTRESET_L (see section 4.2.1). The state of this signal is recaptured at any cold reset but is not recaptured during warm resets. |
| 6 | Reserved.<br>Note: |
| 5 | Reserved.<br>Note: |
| 4 | Reserved.<br>Note: |
| 3 | **EXTARB_L.** Read-Write. Setting this bit to 0 allows the use of an external PCI/PCI-X® arbiter. HPSIL_L controls the default state for both DevA:0x48[EXTARB_L] and DevB:0x48[EXTARB_L].<br>• If HPSIL_L is 1 at the rising edge of PWROK, then EXTARB_L is reset to 1.<br>• If HPSIL_L is 0 at the rising edge of PWROK, then EXTARB_L is reset to 0.<br>Note: This bit is not affected by LDTRESET_L. |
| 2 | **Hot-Plug Enable [HPEN].** Read Only. This bit captures and inverts the state of [B,A]_REQ_L4 at the rising edge of PWROK.<br>0 = Hot-plug mode is not enabled on this bridge.<br>1 = Hot-plug mode is enabled on this bridge. See section 1.3.7.<br>Note: This bit is not affected by LDTRESET_L. |

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| 1 | **HP_IS_TPS2342.** Read Only. This bit captures the state of HPSOD at the rising edge of PWROK. It only has meaning if DevA:0x48[HPEN] or DevB:0x48[HPEN] is asserted.<br>0 = Interface to TPS2340A.<br>1 = Interface to TPS2342.<br>Note: This bit only exists in DevA:0x48 and is reserved in DevB:0x48. This bit is not affected by LDTRESET_L. |
| 0 | **Compatibility Bus [COMPAT].** Read-Write.<br>1 = The AMD-8132 tunnel routes all host initiated accesses in which the link-defined compat bit is set to the secondary bus. The default state of this bit is latched off of A_COMPAT at the trailing edge of PWROK reset.<br>Note: This bit only exists in DevA:0x48 and is reserved in DevB:0x48. This bit is not affected by LDTRESET_L.<br>• |

## Prefetch Control — Dev[B,A]:0x4C

This register specifies the prefetching policy when a bridge is in conventional PCI mode. Bits [28:0] are ignored in PCI-X mode. For more information see section 1.3.4.

Default: E700 2C00h — Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:29 | **Outstanding Inbound Delayed/Split Request Limit [OUTSTDELREQ].** Resets to 111b. This field controls the number of outstanding inbound nonposted delayed (in PCI mode) or split (in PCI-X® mode) requests the bridge can handle at once. The maximum number outstanding is given by OUTSTDELREQ+1. Additional nonposted requests beyond that number are retried until one of those currently outstanding completes on the PCI/ PCI-X bus. In the case of PCI, a nonposted read is not complete in the bridge until all prefetched data is either returned to the PCI bus or discarded. |
| 28 | **Discard Prefetch Data on Master Address Change [DPDMAC].** If set, unrequested prefetch data for a particular master is discarded any time that master issues a request that does not hit the outstanding unrequested prefetches. When running with an external arbiter, all requests are treated as coming from the same master. |
| 27 | **Memory Read Alias Enable [MRD_ALIAS].**<br>• If set, the various flavors of memory read command and states of REQ64_L are treated as interchangeable for purposes of determining whether a read may reconnect to complete a delayed transaction after data has transferred. The initial reconnection must always match the command and REQ64_L exactly, as required by the PCI specification. When this bit is set, and DPDMD_L/ DPDTD are in a state allowing data to be retained in the prefetch buffers following a disconnect, subsequent memory reads are allowed to reconnect to the buffer regardless of the specific memory read command or value of REQ64_L.<br>• If clear, the read command and REQ64_L must match exactly on both the initial and subsequent reconnections. |
| 26:24 | **Unrequested Prefetch Timer [URP_TIMER].** Resets to 111b. This field controls the number of cycles unrequested prefetch data will be held following a master or target disconnect; assuming that disconnect itself does not cause the prefetch data to be discarded (see DMDMD_L and DPDTD). If the master does not reissue the request within 2^(URP_TIMER+4) PCI cycles, the data is discarded. This field allows the discard timeout to range from 2^4 to 2^11 cycles. |

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| 23:22 | Reserved. |
| 21 | **Single Delayed Request Per Master [SDRPM].** When this bit is asserted in PCI mode, each master is only allowed to have a single delayed request outstanding at a time. Additional inbound nonposted requests are retried until the first one either completes or is discarded.<br>• When running with an external arbiter, all requests are treated as coming from the same master.<br>• When this bit is clear, masters are allowed to use all available delayed request buffers up to the limit set by Dev[B,A]:0x4C[OUTSTDELREQ].<br>Note: This bit should not be set unless all Dev[B,A]:0x4C[DPDMD_L] bits are 0. |
| 20:16 | **Discard Prefetch Data on Master Disconnect [DPDMD[4:0]_L].** Active low. There is one DPDMD_L bit for each PCI master, as described for Dev[B,A]:0x40[PFEN_L].<br><br>If asserted (0), the AMD-8132™ tunnel discards prefetch data for a particular request if the master disconnects that request after transferring data as required by the PCI-To-PCI Bridge Architecture Specification, Revision 1.2, section 5.6.2, Stale Data. The discard includes prefetch data already prefetched into the AMD-8132 tunnel and outstanding prefetch requests that complete after the disconnect.<br><br>If deasserted (1), the AMD-8132 tunnel retains prefetch data for a particular request if the master disconnects that request after transferring data in violation of the PCI-To-PCI Bridge Architecture Specification. This setting should not be used unless the system can guarantee that the stale prefetch data hazard can be avoided by the requester. For devices and device drivers that may use retained data in the AMD-8132 tunnel buffers that has become stale, the system must be configured to flush these buffers. Besides the DPDMD_L bits, the AMD-8132 tunnel prefetch controls (such as the DPDMAC bit, the URP_TIMER value, the PFDISC_4K bit, and the DPDH bit) may allow system designers to guarantee their particular PCI devices and device drivers will not receive stale prefetch data but verification of correct device operation is the responsibility of the system designer.<br><br>The deasserted (1) setting can provide significantly increased PCI read bandwidth to PCI devices and device drivers that can safely use it. For example: a PCI device that master disconnects when it fills a relatively small on-chip buffer, but is actually trying to do a read data transfer much larger than its small buffer allows it to do as a single operation on the PCI bus, would perform better if the AMD-8132 tunnel retains prefetch data after its master disconnect. |
| 15 | **Discard Prefetch Data on Target Disconnect [DPDTD].** If set, the AMD-8132 tunnel discards prefetch data for a request if it is forced to disconnect that request as a target after transferring data. The discard includes prefetch data already prefetched into the AMD-8132 tunnel and outstanding prefetch requests that complete after the disconnect.<br>Note: DPDTD should only be set if all DPDMD_L (Dev[B,A]:0x4C[20:16]) bits are 0 for that bridge. Setting DPDTD when any DPDMD_L bits are set may result in undefined behavior. |
| 14 | **PFDISC_4K.**<br>0 = Prefetches can cross a 4-Kbyte boundary.<br>1 = Prefetches stop when reaching a 4-Kbyte boundary. |
| 13 | **Continuous Prefetch Enable For Memory Read Multiple Request [CPFEN_MRM].** Enabled at reset. When a master initiates a burst read to the host with a memory read multiple command code, this bit specifies whether continuous prefetching is enabled.<br>0 = There are no new requests for prefetch data after the initial batch specified by IPF_MRM.<br>1 = One new request for a cache line of prefetch data is sent to the host by the AMD-8132 tunnel when data from an earlier cache line is transferred to the requesting master over the PCI bus (as long as prefetching isn't stopped for some other reason). |

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| 12:10 | **Initial Prefetch For Memory Read Multiple Request [IPF_MRM].** Resets to 3. This register specifies the number of additional cache line prefetches (after the initial fetch of up to one cache line) when a PCI master initiates a burst read to the host with a Memory Read Multiple (MRM) command code. Hitting an address boundary that prefetching is prevented from crossing may stop prefetching sooner. If prefetching is disabled in Dev[B,A]:0x40[PFEN_L], then the value of this register is ignored.<br>0 = No additional prefetches; 1 = 1 additional prefetch; 2 = 2 additional prefetches, and so forth. |
| 9 | **Continuous Prefetch Enable For Memory Read Line Request [CPFEN_MRL].** Disabled at reset. See bit 13, CPFEN_MRM. |
| 8:6 | **Initial Prefetch For Memory Read Line Request [IPF_MRL].** Disabled at reset. See bits 12:10, IPF_MRM. |
| 5 | **Memory Read Prefetch Enable. [MRPFEN].** Disabled at reset.<br>• If this bit is set, allow prefetching for Memory Read (MR) commands using the MRL IPF, and CPF controls.<br>• If this bit is clear, MRs are treated as not prefetchable. |
| 4:1 | Reserved. |
| 0 | **Discard Unrequested Prefetch Data Upon Host Request [DPDH].**<br>0 = Host requests do not affect prefetching.<br>1 = If the AMD-8132 tunnel issues a host request to the PCI bus, then all unrequested prefetch data is discarded. The master is allowed to reconnect and transfer the requested prefetch data and then be disconnected.<br>Note: Programming of this bit may vary based on platform requirements. This bit can be programmed high by system BIOS to protect against stale prefetch data scenarios as described in the PCI specification. |

## PCI-X® Secondary Status — Dev[B,A]:0x60

Default: 6??? B807h — Attribute: See Below

| Bits | Description |
|---|---|
| 31 | **PCI-X® 533 Capable.** Read Only. This bit indicates whether the bridge secondary interface is capable of PCI-X® 533 operation.<br>0 = Not capable.<br>1 = Capable. |
| 30 | **PCI-X** 2.0 **Capable.** Read Only. This bit indicates whether the bridge secondary interface is capable of PCI-X 2.0 operation.<br>0 = Not capable.<br>1 = Capable. |
| 29:28 | **PCI-X Capabilities List Item Version.** Read Only. Always reads 10b. This value indicates that ECC is supported in both PCI-X® Mode 1 and PCI-X® Mode 2. |
| 27:26 | Reserved. |
| 25:22 | **Secondary Bus Mode And Frequency [SCF].** Read Only. This register enables configuration software to determine to which mode and, in PCI-X® mode, frequency the bridge set the secondary bus the last time secondary [B,A]_RESET_L was asserted.<br><br>Register / Mode / Error Protection / Max Clock MHz<br>0h / Conventional PCI / Parity / N/A<br>1h / PCI-X Mode 1 / Parity / 66<br>2h / PCI-X Mode 1 / Parity / 100<br>3h / PCI-X Mode 1 / Parity / 133<br>4h / PCI-X Mode 1 / ECC / Reserved<br>5h / PCI-X Mode 1 / ECC / 66<br>6h / PCI-X Mode 1 / ECC / 100<br>7h / PCI-X Mode 1 / ECC / 133<br>8h / PCI-X 266 / ECC / Reserved<br>9h / PCI-X 266 (Not Supported) / ECC / 66<br>Ah / PCI-X 266 (Mode 2) / ECC / 100<br>Bh / PCI-X 266 (Mode 2) / ECC / 133<br>Ch / PCI-X2 533 / ECC / Reserved<br>Dh / PCI-X2 533 (Not Supported) / ECC / 66<br>Eh / PCI-X2 533 (Not Supported) / ECC / 100<br>Fh / PCI-X2 533 (Not Supported) / ECC / 133 |
| 21 | **Split Request Delayed [SRD].** Read Only. Hardwired low. The AMD-8132™ tunnel automatically limits the number of upstream link read requests to the number of downstream buffers available; so there is no reason to limit the number of ADQs in read requests it accepts.<br>Default = 0 |
| 20 | **Split Completion Overrun [SCO].** Read Only. Hardwired low. The AMD-8132 tunnel automatically limits the number of downstream PCI-X® read requests to the number of upstream response buffers available; so there is no reason to terminate a split completion.<br>Default = 0 |

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| 19 | **Unexpected Split Completion [USC].** Read Only. Always 0.<br>Default = 0 |
| 18 | **Split Completion Discarded [SCD].** Read. Set by hardware. Write 1 to clear.<br>1 = The bridge discarded a split completion moving toward the secondary bus because the requester would not accept it.<br>Default = 0<br>Note: Cleared by PWROK, not LDTRESET_L. |
| 17 | **133 MHz Capable.** Read Only. This bit is hardwired high to indicate support for 133 MHz. |
| 16 | **64-bit Device.** Read Only. The value of this register is the inverse of Dev[B,A]:0x40[DIS64]. |
| 15:8 | **Capabilities Pointer.** Read Only. Points to the next capability block. See Dev[B,A]:0x[BC,B8]. |
| 7:0 | **Capability ID.** Read Only. Specifies the capability ID for PCI-X® configuration space. |

## PCI-X® Bridge Status — Dev[B,A]:0x64

Default: A1: 0003 0000h, Bx: 0003 0008h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:30 | Reserved. |
| 29 | **Device ID Messaging Capable.** Read Only. This bit is zero, indicating the bridge does not forward Device ID Messages between the primary and secondary interfaces. |
| 28:22 | Reserved. |
| 21 | **Split Request Delayed [SRD].** Read Only. Hardwired low. The AMD-8132™ tunnel automatically limits the number of downstream PCI-X® read requests to the number of upstream buffers available; so there is no reason to limit the number of ADQs in read requests it accepts. |
| 20 | **Split Completion Overrun.** Read Only. This bit is hardwired low; it has no meaning since the primary bus is not PCI-X®. |
| 19 | **Unexpected Split Completion.** Read Only. This bit is hardwired low; it has no meaning since the primary bus is not PCI-X®. |
| 18 | **Split Completion Discarded.** Read Only. This bit is hardwired low; it has no meaning since the primary bus is not PCI-X®. |
| 17 | **133 MHz Capable.** This bit is set high arbitrarily; it has no meaning since the primary bus is not PCI-X®. |
| 16 | **64-bit Device.** Read Only. This bit is set high arbitrarily; it has no meaning since the primary bus is not PCI-X®. |
| 15:8 | **Bus Number.** Read Only. These bits reflect the state of Dev[B,A]:0x18[PRIBUS]. |
| 7:3 | **Device Number.** Read Only. For DevA, these bits reflect the state of DevA:0xC0[BUID]. For DevB, these bits reflect the state of DevA:0xC0[BUID] plus 1. |
| 2:0 | **Function Number.** Read Only. This is 0h to reflect the value of this function. |

## PCI-X® Upstream Split Transaction — Dev[B,A]:0x68

Default: A1: FFFF 000Eh, Bx: FFFF 000Dh — Attribute: See Below

| Bits | Description |
|---|---|
| 31:16 | **Upstream Split Transaction Commitment Limit [USTCL].** Read-Write. This register controls no hardware. The AMD-8132™ tunnel automatically limits the number of upstream HyperTransport™ link read requests to the number of downstream buffers available; so there is no reason to limit the number of ADQs in read requests it accepts. This field is required to be greater than or equal to Dev[B,A]:0x68[USTC]. A value of FFFFh specifies that there is no limit. It is expected that this register will be left at its default value by software. |
| 15:0 | **Upstream Split Transaction Capacity [USTC].** Read Only. This field specifies the number of downstream response ADQs that can be stored for completion on the secondary bus. |

## PCI-X® Downstream Split Transaction — Dev[B,A]:0x6C

Default: FFFF 0002h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:16 | **Downstream Split Transaction Commitment Limit [DSTCL].** Read-Write. This register controls no hardware. The AMD-8132™ tunnel automatically limits the number of downstream PCI-X® read requests to the number of upstream buffers available; so there is no reason to limit the number of ADQs in read requests it generates. This field is required to be greater than or equal to Dev[B,A]:0x6C[DSTC]. A value of FFFFh specifies that there is no limit. It is expected that this register will be left at its default value by software. |
| 15:0 | **Downstream Split Transaction Capacity [DSTC].** Read Only. This field specifies the number of upstream response ADQs that can be stored for completion to the link. |

## PCI-X® ECC Control and Status Dev[B,A]:0x70

This register displays primary interface information if the Select Secondary ECC Registers bit is cleared, and secondary interface information if the Select Secondary ECC Registers bit is set. Since the primary interface is not PCI-X, it will never receive an ECC error and these registers return 0s if the Select Secondary ECC Registers bit is cleared. See bit 0 in this register.

Default: ?000 0000h Attribute: See Below

| Bits | Description |
|---|---|
| 31 | **ECC Mode.** PCI-X® Mode 1: Read-Write. PCI-X® Mode 2: Read Only. Conventional PCI: Read Only. Unless the ECC Control Update Enable bit = 1 in the data pattern being written, writes to this register do not affect this bit.<br>• If this bit = 0, the PCI-X interface of the bridge is in parity mode.<br>• If this bit = 1, the PCI-X interface of the bridge is in ECC mode.<br>In PCI-X Mode 2 this bit is always 1. In Conventional PCI mode, this bit is always 0. |
| 30 | **Disable Single-Bit-Error Correction.** Read-Write.<br>• If the PCI bus is in ECC mode and this bit = 0, correctable errors occurring on that interface are corrected.<br>• If this bit = 1, correctable errors that occur on the PCI bus are not corrected and are treated as uncorrectable errors (including the setting of status bits and assertion of error indicator signals on the bus).<br>Writes to this register do not affect this bit unless the ECC Control Update Enable bit is a 1 in the data pattern being written.<br>Default = 0 |
| 29 | Reserved. |
| 28 | **ECC Control Update Enable.** Write. This bit always reads as a 0.<br>• If this bit is 1 during a write to this configuration register, the Disable Single-Bit-Error Correction and ECC mode bits are also updated (written).<br>• If this bit is 0 in a write, the Disable Single-Bit-Error Correction and ECC mode bits are not updated. |
| 27:24 | **Error Upper Attributes.** Read Only. If the ECC Error Phase register is non-zero, this register indicates the contents of the C/BE_L[3:0] bus for the attribute phase of the transaction that included the error.<br>Note: This register is cleared by PWROK, not by LDTRESET_L. |
| 23:20 | **Error Second Command.** Read Only. If the ECC Error Phase register is non-zero and the transaction that included the error used a dual address cycle, this register indicates the contents of the C/BE[3:0]_L bus for the second address phase of the transaction that included the error.<br>Note: This register is cleared by PWROK, not by LDTRESET_L. |
| 19:16 | **Error First (or only) Command.** Read Only. If the ECC Error Phase register is non-zero, this register indicates the contents of the C/BE_L[3:0] bus for the first (or only) address phase of the transaction that included the error.<br>Note: This register is cleared by PWROK, not by LDTRESET_L. |

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| 15:8 | **Syndrome.** Read Only. The syndrome indicates information about the bit or bits in error. For 32-bit transfers, E6 to E0 are the syndrome sequence. For 64-bit transfers, E7 to E0 are the syndrome sequence. For details see section 5.1.2 of *PCI-X Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a*.<br><br>Bit — Syndrome<br>8 — E0<br>9 — E1<br>10 — E2<br>11 — E3<br>12 — E4<br>13 — E5<br>14 — E6<br>15 — E7 for 64-bit data, 0b for 32-bit data<br><br>Note: This register is cleared by PWROK, not by LDTRESET_L. |
| 7 | **ECC Error Corrected.** Read Only.<br>0 = The captured error was not corrected.<br>1 = The captured error was corrected.<br>• If the ECC Error Phase register is non-zero, this bit indicates whether the error that was captured was corrected. Correctable ECC errors occurring while the Disable Single-Bit-Error Correction bit is 0 are the only errors that are corrected.<br>• If the ECC Error Phase register is zero, this bit is undefined.<br><br>Note: This register is cleared by PWROK, not by LDTRESET_L. |
| 6:4 | **ECC Error Phase.** Write 1 to clear.<br>• If the bridge detects either a correctable or uncorrectable ECC error, this register indicates in which phase of the transaction the error occurred. For data phase errors, this register indicates whether it was a 32-bit data error (7-bit ECC) or 64-bit data error (8-bit ECC).<br>• If this register is set to 0, the bridge is enabled to latch information about an ECC error. If the device detects an error, it latches the phase of the error in this register and stores status information for the error in the ECC Status, ECC Address, and ECC Attribute registers. Writing a 1 to any of these bits clears this register and enables the bridge to capture the next error.<br><br>Register — ECC Error Phase<br>0 — No error<br>1 — First 32 bits of address<br>2 — Second 32 bits of address<br>3 — Attribute phase<br>4 — 32-bit data phase<br>5 — 64-bit data phase<br>6 — Reserved<br>7 — Reserved<br><br>Note: This register is cleared by PWROK, not by LDTRESET_L. |

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|---|---|
| 3 | **Additional Uncorrectable ECC Error.** Write 1 to clear. This bit is set if the bridge detects an uncorrectable ECC error while already indicating some other ECC error (i.e., the ECC Error Phase register is non-zero). Once set, this bit remains set until software writes a 1 to this location.<br>0 = No additional uncorrectable ECC error detected.<br>1 = One or more additional uncorrectable ECC errors detected.<br>Note: This register is cleared by PWROK, not by LDTRESET_L. |
| 2 | **Additional Correctable ECC Error.** Write 1 to clear. This bit is set if the bridge detects a correctable ECC error while already indicating some other ECC error (i.e., the ECC Error Phase register is non-zero). Once set, this bit remains set until software writes a 1 to this location.<br>0 = No additional correctable ECC error detected.<br>1 = One or more additional correctable ECC errors detected.<br>Note: This register is cleared by PWROK, not by LDTRESET_L. |
| 1 | **Error Present in Other ECC Register Bank.** Read Only. If this bit = 1, the ECC error logging registers for the other interface hold information about an ECC error.<br>• If the Select Secondary ECC Registers bit is 1, the primary ECC error logging registers hold information about an ECC error for the primary interface. Since the primary bus is HyperTransport™ and not PCI-X®, this is always 0.<br>• If the Select Secondary ECC Registers bit is 0, the secondary ECC error logging registers hold information about an ECC error for the secondary interface.<br>Note: This register is cleared by PWROK, not by LDTRESET_L. |
| 0 | **Select Secondary ECC Registers.** Read-Write. There is a single Select Secondary ECC Registers bit that controls reading and writing of both primary and secondary ECC registers in the bridge.<br>• If this bit is 1, reading from the ECC error logging registers (ECC Control and Status, ECC First Address, ECC Second Address, and ECC Attribute registers) reads the values latched for the secondary interface.<br>• If the bit is 1 in the data written to the ECC Control and Status register, the ECC Control and Status register for the secondary interface is affected.<br>• If this bit is 0, reading from the ECC error logging registers reads the values latched for the primary interface. Since the primary interface is HyperTransport™ and not PCI-X®, there will never be an ECC error on the primary interface.<br>• If this bit is 0 in the data written to the ECC Control and Status register, the ECC Control and Status register for the primary interface is affected. Since the primary interface is HyperTransport, there are no relevant ECC registers. |

## PCI-X® ECC First Address — Dev[B,A]:0x74

Default: 0000 0000h

If the Select Secondary ECC Registers bit Dev[B.A]:0x70[0] is cleared, this register displays primary interface information. If the Select Secondary ECC Registers bit is set, this register displays secondary interface information. Since the primary interface is not PCI-X, it never receives an ECC error and these registers return undefined values if the Select Secondary ECC Registers bit is cleared. The description below assumes that the Select Secondary ECC Registers bit is set. If the ECC Error Phase register for the interface is zero, the register contents are undefined.

Regardless of the type, length, or width of the transaction, or the phase in which the error occurred, the ECC First Address register records the least significant 32 bits of the address. Registers that store information from the failing transaction always store information directly from the bus (uncorrected), even if error correction is possible. These registers are Read Only.

**Note:** This register is cleared by PWROK, not by LDTRESET_L.

## PCI-X® ECC Second Address — Dev[B,A]:0x78

Default: 0000 0000h

If the Select Secondary ECC Registers bit Dev[B.A]:0x70[0] is cleared, this register displays primary interface information. If the Select Secondary ECC Registers bit is set, this register displays secondary interface information. Since the primary interface is not PCI-X, it never receives an ECC error and these registers return undefined values if the Select Secondary ECC Registers bit is cleared. The description below assumes that the Select Secondary ECC Registers bit is set. If the ECC Error Phase register for the interface is zero, the register contents are undefined.

If the transaction used a dual address cycle, the Second 32 Bits of Address register records the most significant 32 bits of the address. If the transaction used a single address cycle, the contents of the Second 32 Bits of Address register are 0. Registers that store information from the failing transaction always store information directly from the bus (uncorrected), even if error correction is possible. These registers are Read Only.

**Note:** This register is cleared by PWROK, not by LDTRESET_L.

## PCI-X® ECC Attribute — Dev[B,A]:0x7C

Default: 0000 0000h

If the Select Secondary ECC Registers bit Dev[B.A]:0x70[0] is cleared, this register displays primary interface information. If the Select Secondary ECC Registers bit is set, this register displays secondary interface information. Since the primary interface is not PCI-X, it never receives an ECC error and these registers return undefined values if the Select Secondary ECC Registers bit is cleared. The description below assumes that the Select Secondary ECC Registers bit is set.

- If the ECC Error Phase register for the PCI bus is non-zero (indicating that an error has been captured), the ECC Attribute register indicates the contents of the AD[31:00] bus for the attribute phase of the transaction that included the error.
- If the ECC Error Phase register is zero, the contents of this register are undefined.

This register records the contents of the bus during the attribute phase, regardless of the type or length of the transaction, or the phase in which the error occurred. Registers that store information from the failing transaction always store information directly from the bus (uncorrected), even if error correction is possible. This register is Read Only.

**Note:** This register is cleared by PWROK, not by LDTRESET_L.

## Misc Bridge Errors — Dev[B,A]:0x80

Default: 0000 0000h Attribute: See Below

| Bits | Description |
|---|---|
| 31:20 | Reserved. |
| 19 | **Primary Signalled Master Abort.** Read. Write 1 to clear. This bit is set if the AMD-8132™ tunnel is the end of chain device and the AMD-8132 tunnel receives a nonposted operation on the HyperTransport™ bus that goes to the end of chain. This bit exists only in DevA:0x80 and is reserved in DevB:0x80.<br>Note: Reset by PWROK, not LDTRESET_L. |
| 18 | **PCI Busy Time Out Error.** Read. Reset the AMD-8132 tunnel PCI bridge and write 1 to clear. This bit is set if the AMD-8132 tunnel detects that the PCI-X® bus has been non-idle (FRAME# or IRDY# asserted) for 49152 PCI clocks.<br>Note: Reset by PWROK, not LDTRESET_L. |
| 17 | **SCM_Class 1_TargetAbortError.** Read. Write 1 to clear. This bit is set if the AMD-8132 tunnel receives a Split Completion Message of Class 1, index 01h (Target Abort).<br>Note: Reset by PWROK, not LDTRESET_L. |
| 16 | **SCM_Class2_ByteCountOutOfRangeError.** Read. Write 1 to clear. This bit is set if the AMD-8132 tunnel receives a Split Completion Message of Class 2, index 00h (Byte Count Out of Range).<br>Note: Reset by PWROK, not LDTRESET_L. |

| | |
|---|---|
| 15 | **SCM_Class 2_ DeviceSpecificError.** Read. Write 1 to clear. This bit is set if the AMD-8132™ tunnel receives a Split Completion Message of Class 2, index 8Xh (Device-Specific Error).<br>Note: Reset by PWROK, not LDTRESET_L. |
| 14 | **DROPPED_MSI.** Set by hardware. Read. Write 1 to clear. This bit is set whenever an MSI request is dropped due to an uncorrectable data error.<br>Note: Reset by PWROK, not LDTRESET_L. |
| 13 | **CLASS2_SCM_ERR_CLEAR.** Write Only. Write 1 to clear CLASS2_SCM_ERR bit. |
| 12:10 | **CLASS2_MSG_IDXHI.** Read Only. Set by hardware. This register indicates the top three bits of the message index of the first detected Class 2 split completion message that was not an uncorrectable split write data error. If Dev[B,A]:0x80[CLASS2_SCM_ERR] is not asserted, this register is undefined.<br>Note: Reset by PWROK, not LDTRESET_L. |
| 9 | **CLASS2_SCM_ERR.** Read. Set by hardware. Write 1 to bit 13 (CLASS2_SCM_ERR_CLEAR) to clear. A Class 2 (completer error) split completion message was received that was not an uncorrectable split write data error (the message index did not equal 1). The message index of the first detected Class 2 split completion message that was not an uncorrectable split write data error is recorded in Dev[B,A]:0x80[CLASS2_MSG_IDX].<br>Note: Reset by PWROK, not LDTRESET_L. |
| 8:4 | **CLASS2_MSG_IDXLO.** Read Only. Set by hardware. This indicates the bottom five bits of the message index of the first detected Class 2 split completion message that was not an uncorrectable split write data error. If Dev[B,A]:0x80[CLASS2_SCM_ERR] is not asserted, this register is undefined.<br>Note: Reset by PWROK, not LDTRESET_L. |
| 3 | **SCM_PAR_ERR.** Read. Set by hardware. Write 1 to clear. Cleared by hardware immediately after assertion if Dev[B,A]:0x48[CLEARPCILOG_L] is asserted (0). This bit is set if the AMD-8132 tunnel detects an uncorrectable error in the data phase while receiving a split completion message.<br>Note: Reset by PWROK, not LDTRESET_L. |
| 2 | **ADDR_OR_ATTR_ERR.** Read. Set by hardware. Write 1 to clear. Cleared by hardware immediately after assertion if Dev[B,A]:0x48[CLEARPCILOG_L] is asserted (0). This bit is set if the AMD-8132 tunnel detects an uncorrectable error on the PCI bus during an address or attribute phase.<br>Note: Reset by PWROK, not LDTRESET_L. |
| 1 | **DISCARDED_POST.** Read. Set by hardware. Write 1 to clear. Resets to 0. Cleared by hardware immediately after assertion if Dev[B,A]:0x48[CLEARPCILOG_L] is asserted (0). Indicates the bridge was forced to discard a posted request it was trying to forward to PCI/PCI-X® due to receiving a master abort, target abort, or uncorrectable data error on the transfer.<br>Note: Reset by PWROK, not LDTRESET_L. |
| 0 | **PERR_OBSERVED.** Read. Set by hardware. Write 1 to clear. This bit is set whenever PERR_L is asserted on PCI-X® bus [B,A] and remains set until cleared by software. This bit is also used in the equations for the fatal and nonfatal interrupts. See DevA:0xDC and Chapter 5.<br>Note: This bit is set whenever PERR_L is asserted regardless of whether the AMD-8132 tunnel or another device asserted it. Reset by PWROK, not LDTRESET_L. |

## Misc Error Enables — Dev[B,A]:0x84

Default: 0000 0000h — Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:17 | Reserved. |
| 16 | **Discarded Post Log Override.** When asserted, this bit causes the discarded post log bit Dev[B,A]:0x80[1] to be set if, due to receiving a master abort or a target abort, the bridge is forced to discard a posted request it was trying to forward to PCI/PCI-X® even if the master abort mode bit Dev[B,A]:0x3C[21] is cleared. |
| 15 | **Received Secondary Master Abort Nonfatal Enable.** When asserted, this bit causes nonfatal error interrupt assertion whenever the log bit Dev[B,A]:0x1C[29] is set. |
| 14 | **Received Secondary Master Abort Fatal Enable.** When asserted, this bit causes fatal error interrupt assertion whenever the log bit Dev[B,A]:0x1C[29] is set. |
| 13 | **Primary Signalled Master Abort Fatal Enable.** When asserted, this bit causes fatal error interrupt assertion whenever the log bit DevA:0x80[19] is set.<br>Note: This CSR only exists in DevA. This bit is Reserved in DevB. |
| 12 | **Primary Signalled Master Abort Nonfatal Enable.** When asserted, this bit causes nonfatal error interrupt assertion whenever the log bit DevA:0x80[19] is set.<br>Note: This CSR only exists in DevA. This bit is Reserved in DevB. |
| 11 | **PCI Busy Time Out Fatal Enable.** When asserted, this bit causes fatal error interrupt assertion whenever the log bit Dev[B,A]:0x80[18] is set.<br>Depending on how the secondary bus hangs, the AMD-8132 tunnel can be involved in the operation in such a way that the error log bit will be set but the system software interrupt cannot be issued from the AMD-8132 tunnel to the HyperTransport™ bus because internal resources are in use as part of the hung bus operation, thus blocking the interrupt packet. |
| 10 | **PCI Busy Time Out Nonfatal Enable.** When asserted, this bit causes nonfatal error interrupt assertion whenever the log bit Dev[B,A]:0x80[18] is set.<br>Depending on how the secondary bus hangs, the AMD-8132 tunnel can be involved in the operation in such a way that the error log bit will be set but the system software interrupt cannot be issued from the AMD-8132 tunnel to the HyperTransport™ bus because internal resources are in use as part of the hung bus operation, thus blocking the interrupt packet. |
| 9 | **Signalled Secondary Target Abort Nonfatal Enable.** When asserted, this bit causes nonfatal error interrupt assertion whenever the log bit Dev[B,A]:0x1C[27] is set. |
| 8 | **Signalled Secondary Target Abort Fatal Enable.** When asserted, this bit causes fatal error interrupt assertion whenever the log bit Dev[B,A]:0x1C[27] is set. |
| 7 | **Received Secondary Target Abort Nonfatal Enable.** When asserted, this bit causes nonfatal error interrupt assertion whenever the log bit Dev[B,A]:0x1C[28] is set. |
| 6 | **Received Secondary Target Abort Fatal Enable.** When asserted, this bit causes fatal error interrupt assertion whenever the log bit Dev[B,A]:0x1C[28] is set. |
| 5 | **SCM_Class 1_TargetAbortErrNonfatalEn.** When asserted, this bit causes nonfatal error interrupt assertion whenever the log bit Dev[B,A]:0x80[17] is set. |
| 4 | **SCM_Class 1_TargetAbortErrFatalEn.** When asserted, this bit causes fatal error interrupt assertion whenever the log bit Dev[B,A]:0x80[17] is set. |

| | |
|---|---|
| 3 | **SCM_Class 2_ByteCountOutOfRangeNonfatalEn.** When asserted, this bit causes nonfatal error interrupt assertion whenever the log bit Dev[B,A]:0x80[16] is set. |
| 2 | **SCM_Class 2_ByteCountOutOfRangeFatalEn.** When asserted, this bit causes fatal error interrupt assertion whenever the log bit Dev[B,A]:0x80[16] is set. |
| 1 | **SCM_Class 2_DeviceSpecificErrNonfatalEn.** When asserted, this bit causes nonfatal error interrupt assertion whenever the log bit Dev[B,A]:0x80[15] is set. |
| 0 | **SCM_Class 2_DeviceSpecificErrFatalEn.** When asserted, this bit causes fatal error interrupt assertion whenever the log bit Dev[B,A]:0x80[15] is set. |

## SHPC Capabilities — Dev[B,A]:0x90

This register is reserved if Dev[B,A]:0x48[HPEN] is low.

Default: 0000 980Ch Attribute: See Below

| Bits | Description |
|---|---|
| 31 | **Controller Interrupt Pending [CIP].** Read Only.<br>0 = All bits in SHPC[B,A]:18 are cleared.<br>1 = One or more bits in SHPC[B,A]:18 are set. |
| 30 | **Controller System Error Pending [CSERRP].** Read Only.<br>0 = All bits in SHPC[B,A]:1C are cleared.<br>1 = One or more bits in SHPC[B,A]:1C are set. |
| 29:24 | Reserved. |
| 23:16 | **DWORD Select [SELECT].** Read-Write. Specifies the DWORD from the SHPC[B,A]:XX register set that is accessible through Dev[B,A]:0x94. 00h selects SHPC[B,A]:00; 01h selects SHPC[B,A]:04; and so on. |
| 15:8 | **Capabilities Pointer.** Read Only. Points to the next capability block. See Dev[B,A]:0x98. |
| 7:0 | **Capability ID.** Read Only. Specifies the capabilities ID for SHPC. |

## SHPC Data — Dev[B,A]:0x94

This register is reserved if Dev[B,A]:0x48[HPEN] is low.

Default: 0000 0000h Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:0 | **SHPC Data Port [DATA].** Accesses to this port access the register of the SHPC[B,A]:XX register set indexed by Dev[B,A]:0x90[SELECT]. |

## Power Management Capabilities — Dev[B,A]:0x98

This register is reserved if Dev[B,A]:0x48[HPEN] is low.

Default: 480A C001h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:27 | **PME Support [PMES].** Indicates PME_L support in device state D0 (system state S0) and device state D3 hot (system state S1). |
| 26 | **D2 Support [D2S].** Indicates that D2 device power state is not supported. |
| 25 | **D1 Support [D1S].** Indicates that D1 device power state is not supported. |
| 24:22 | **Auxiliary Current Requirements [AUXCR].** Indicates there is no requirement for auxiliary current since the D3 cold device power state is not supported. |
| 21 | **Device Specific Initialization [DSI].** Indicates there is no special initialization requirement. |
| 20 | Reserved. |
| 19 | **PME Clock [PMECLK].** Indicates the PCI clock is required for PME_L generation. |
| 18:16 | **Version.** Specifies the PCI function complies with *PCI Bus Power Management Interface Specification*, *Rev 1.1*. |
| 15:8 | **Capabilities Pointer.** Points to the next capability block. See Dev[B,A]:0xC0. |
| 7:0 | **Capability ID.** Specifies the Capabilities ID for PCI Power Management. |

## Power Management Status and Control — Dev[B,A]:0x9C

This register is reserved if Dev[B,A]:0x48[HPEN] is low.

Default: 0000 0000h Attribute: See Below

| Bits | Description |
|---|---|
| 31:24 | Reserved. |
| 23 | **Bus Power/Clock Control Enable [BPCC_EN].** Read Only. Indicates the bus power/clock control policies defined in section 4.7.1 of the *PCI Bus Power Management Interface Specification, Rev. 1.1,* have been disabled. |
| 22:16 | Reserved. |
| 15 | **PME_L Status [PME_STS].** Read. Set by hardware. Write 1 to clear. Set when [B,A]_PME_L is asserted as a result of an SHPC PME event. See SHPC[B,A]:20. |
| 14:9 | Reserved. |
| 8 | **PME Enable [PME_EN].** Read-Write.<br>0 = Not enabled.<br>1 = Enables [B,A]_PME_L assertion if Dev[B,A]:0x9C[PME_STS] is set. |
| 7:2 | Reserved. |
| 1:0 | **Power State [PWRS].** Read-Write. Indicates the current power state of the function. 00b = D0. 11b = D3 hot. If software attempts to write unsupported state to this field (01b = D1 or 10b = D2), the write operation completes normally on the bus; however, the data is discarded and no state change occurs. |

## Extended Configuration Address Range DevA:0xB4

**Note:** This register only exists in device A.

Default: 0000 07F0h Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:11 | Reserved. |
| 10:0 | The HyperTransport™ defined address range for extended configuration space is FE_0xxx_xxxx (Type 0) and FE_1xxx_xxxx (Type 1). There is a mechanism in the AMD-8132™ tunnel allowing this address range to be redefined to a different location. DevA:0xB4[10:0] redefines bits [39:29] of this address space. Bits [63:40] of the address space are still required to be 0, and bit [28] still distinguishes between Type 0 and Type 1.<br><br>If the address is redefined via DevA:0xB4, a HyperTransport operation that matches this redefined address space will have the identical behavior to the specified HyperTransport behavior for accesses to FE_0xxx_xxxx or FE_1xxx_xxxx.<br><br>All HyperTransport devices that can be the target of an extended configuration access should have their address ranges programmed to accept the same address range (for address bits [63:29]). This address range must be defined in the processor/host such that the generated HyperTransport operations have the same attributes as configuration accesses (non-posted, single DW, or smaller). |

## Interrupt Discovery and Configuration Dev[B,A]:0x[BC,B8]

These two locations provide access to a superset of the IOAPIC register space defined in section 3.6 in this document. Dev[B,A]:0xB8[INDEX] provides the index and Dev[B,A]:0xBC provides the data port. The definition of the indexed registers is as described in section 3.6. Some fields of the IDRDR register are identical to RDR fields (IM, IV, POL, TM, DM, MT, DEST, IRR); these represent duplicate access to the same physical registers (not duplicate registers). Other IDRDR fields (INTRINFO, PASSPW) represent new functionality. Legal values of 0xB8[INDEX] are 0x10 to 0x1D. Even values cause accesses to 0xBC to access the low 32 bits of the corresponding IDRDR. Incrementing the even value by one causes accesses to 0xBC to access the upper 32 bits of the corresponding IDRDR. For more information see *HyperTransport™I/O Link Specification, Rev 2.0* and section 1.3.2 in this document.

**Dev[B,A]:0xB8.**

Default: 8000 ??08h Attribute: See Below

| Bits | Description |
|---|---|
| 31:24 | **Capability Type.** Read Only. This field is hardwired to indicate the HyperTransport™ link-defined interrupt discovery and configuration block. |
| 23:16 | **INDEX.** Read-Write. Specifies the register accessed through the Dev[B,A]:0xBC dataport. This index references the same registers as APIC[B,A]:00[7:0] described in section 3.6, with the exception that it references the IDRDR view of registers 10h through 1Dh instead of the RDR view described in section 3.4. |

| | |
|---|---|
| 15:8 | **Capabilities Pointer.** Read Only. Points to the next capability block. The value of this register varies as follows:<br>• If Dev[B,A]:0x48[HPEN] = 0, then Dev[B,A]:0xB8[15:8] = C0h (HyperTransport™ capability block).<br>• If Dev[B,A]:0x48[HPEN] = 1, then Dev[B,A]:0xB8[15:8] = 90h (hot-plug capability block). |
| 7:0 | **Capability ID.** Read only. Specifies this is a HyperTransport™ capabilities block. |

**IDRDR.**

Default: 0000 0000 F800 0001h Attribute: See Below

| Bits | Description |
|---|---|
| 63 | **IRR.** Read. Set by hardware. Cleared by hardware or Write 1 to clear. This bit provides duplicate access to RDR[IRR] described in section 3.6. However, writing a 1 to this bit clears this register; which is not the case with RDR[IRR]. |
| 62 | **PASSPW.** Read-Write. The state of this bit is reflected in the PassPW bit of the HyperTransport™ link interrupt request packet. |
| 61:56 | Reserved. |
| 55:24 | **INTRINFO[55:24].** Read-Write. IntrInfo[55:24] in the HyperTransport™ link interrupt request packet. |
| 23:16 | **IV.** Read-Write. IntrInfo[23:16] in the HyperTransport™ link interrupt request packet; this provides duplicate access to RDR[IV] described in section 3.6. |
| 15:8 | **DEST.** Read-Write. IntrInfo[15:8] in the HyperTransport™ link interrupt request packet; this provides duplicate access to RDR[DEST] described in section 3.6. |
| 7 | **INTRINFO[7].** Read-Write. IntrInfo[7] in the HyperTransport™ link interrupt request packet. |
| 6 | **DM.** Read-Write. IntrInfo[6] in the HyperTransport™ link interrupt request packet; this provides duplicate access to RDR[DM] described in section 3.6. |
| 5 | **TM.** Read-Write. IntrInfo[5] in the HyperTransport™ link interrupt request packet; this provides duplicate access to RDR[TM] described in section 3.6. |
| 4:2 | **MT.** Read-Write. IntrInfo[4:2] in the HyperTransport™ link interrupt request packet. Accesses to RDR[MT] described in section 3.6. result in translated accesses to this field. See RDR[MT]. |
| 1 | **POL.** Read-Write. This bit provides duplicate access to RDR[POL] described in section 3.6. This bit is Read Only for IDRDR indices of 0x18, 0x1A, 0x1C (internal interrupts are always active high). |
| 0 | **IM.** Read-Write. This bit provides duplicate access to RDR[IM] described in section 3.6. |

## HyperTransport™ Revision ID Capability Block DevB:0xC0

**Note:**This is the version of the HyperTransport capability block for device B.

Default: A1: 8825 F408h, Bx: 8840 F408h Attribute: Read Only

| Bits | Description |
|---|---|
| 31:24 | **Capability Type.** Capability type is Revision ID. |

| | |
|---|---|
| 23:16 | **Revision ID.** Indicates to which rev of the *HyperTransport™I/O Link Specification* the AMD-8132™ tunnel is compliant.<br>Note: Rev A1 of the AMD-8132 tunnel only indicates support for *HyperTransport™I/O Link Specification, Rev 1.05*. |
| 15:8 | **Capabilities Pointer.** Points to the next capability block in the chain. See Dev[B,A]:0xF4. |
| 7:0 | **Capability ID.** Capability ID is 08, indicating HyperTransport™. |

## Link Command DevA:0xC0

**Note:** This is the version of the HyperTransport capability block for device A. Registers 0xC4 through 0xF0 only exist for device A.

Default: 0040 F408h Attribute: See Below

| Bits | Description |
|---|---|
| 31:29 | **Capability Type.** Read Only. Indicates slave/primary interface. |
| 28 | **Drop On Uninitialized Link [DOUI].** Read-Write. This bit specifies the behavior of transactions that are sent to uninitialized links.<br>For transactions that are received by the AMD-8132™ tunnel and forwarded to a side of the tunnel:<br>0 = When DevA:0x[C4/C8][INITCPLT and ENDOCH] for that side of the tunnel are both low, transactions remain in buffers awaiting transmission indefinitely (waiting for INITCPLT to be set high).<br>1 = When DevA:0x[C4/C8][INITCPLT and ENDOCH] for that side of the tunnel are both low, transactions behave as if ENDOCH were high.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 27 | **Default Direction [DEFDIR].** Read-Write.<br>0 = Send secondary PCI bus master requests to the link host as specified by DevA:0xC0[MASHST].<br>1 = Send secondary PCI bus master requests to the opposite side of the tunnel. |
| 26 | **Master Host [MASHST].** Read. Set and cleared by hardware. This bit indicates which link is the path to the master (or only) host bridge on the HyperTransport™ chain.<br>0 = The hardware cleared this bit as a result of a write command from side 0 of the tunnel to any of the bytes of DevA:0xC0[31:16].<br>1 = The hardware set this bit as a result of a write command from side 1 of the tunnel to any of the bytes of DevA:0xC0[31:16]. |
| 25:21 | **UnitID Count.** Read Only. Specifies the number of UnitIDs used by the AMD-8132 tunnel (two). |
| 20:16 | **Base UnitID [BUID].** Read-Write. Specifies the link protocol base UnitID for bridge A. Bridge B is assigned BUID+1. Setting BUID $\geq$ 1Fh results in undefined behavior.<br>The AMD-8132 tunnel logic uses this value to determine the UnitIDs for HyperTransport™ link request and response packets, and the DeviceID to respond to in configuration requests. When a new value is written to this field, the response includes a UnitID that is based on the new value in this register. |
| 15:8 | **Capabilities Pointer.** Read Only. Points to next capability block. See Dev[B,A]:0xF4. |
| 7:0 | **Capability ID.** Read Only. Capability ID is 08, indicating HyperTransport™. |

## Link Configuration and Control — DevA:0xC4 and DevA:0xC8

DevA:0xC4 applies to side 0 of the tunnel and DevA:0xC8 applies to side 1 of the tunnel. The default value for bit 5 may vary, see the Descriptions.

Default: ??11 0020h — Attribute: See Below

| Bits | Description |
|---|---|
| 31 | Reserved. |
| 30:28 | **Link Width Out [LWO].** Read-Write. Specifies the operating width of the outgoing link. Legal values are:<br>001b (16 bits)<br>000b (8 bits)<br>101b (4 bits)<br>100b (2 bits)<br>111b (not connected).<br>Note: This field is cleared by PWROK reset but not by LDTRESET_L. The default value of this field depends on the widths of the links of the connecting device, per the link specification. After this field is updated, the link width does not change until either LDTRESET_L is asserted or a link disconnect sequence occurs through an LDTSTOP_L assertion. |
| 27 | Reserved. |
| 26:24 | **Link Width In [LWI].** Read-Write. Specifies the operating width of the incoming link. Legal values are:<br>001b (16 bits)<br>000b (8 bits)<br>101b (4 bits)<br>100b (2 bits)<br>111b (not connected)<br>Note: This field is cleared by PWROK reset but not by LDTRESET_L. The default value of this field depends on the widths of the links of the connecting device, per the link specification. After this field is updated, the link width does not change until either LDTRESET_L is asserted or a link disconnect sequence occurs through an LDTSTOP_L assertion. |
| 23 | Reserved. |
| 22:20 | **Max Link Width Out.** Read Only. Specifies the maximum width of the outgoing link to 16 bits. |
| 19 | Reserved. |
| 18:16 | **Max Link Width In.** Read Only. Specifies the maximum width of the incoming link to 16 bits. |
| 15 | **64-Bit Address Enable [64BEn].** Read-Write. |
| 14 | **Extended Control Time During Initialization [EXTCTL].** Read-Write. Specifies the time that L[1,0]_CTLOUT_[H,L]0 is held asserted during the initialization sequence that follows an LDTSTOP_L deassertion after L[1,0]_CTLIN_[H,L]0 is detected asserted.<br>0 = At least 16 bit times.<br>1 = About 50 microseconds.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. See section 4.2.1.2. |

| | |
|---|---|
| 13 | **Link Three-State Enable [LDT3SEN].** Read-Write.<br>0 = During the LDTSTOP_L disconnect sequence the link transmitter signals are driven but in an undefined state, and the link receiver signals are assumed to be driven.<br>1 = During the LDTSTOP_L disconnect sequence, the link transmitter signals are placed into the high impedance state and the receivers are prepared for the high impedance mode. For the receivers, this includes cutting power to the receiver differential amplifiers and ensuring that there are no resultant high-current paths in the circuits.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. AMD recommends that this bit be set high in single-processor systems and be set low in multi-processor systems. |
| 12:10 | Reserved. |
| 9:8 | **CRC Error [CRCERR].** Read. Set by hardware. Write 1 to clear.<br>1 = Hardware detected a CRC error on the incoming link. Bit[9] applies to the upper byte of the link and bit[8] applies to the lower byte.<br>Note: This bit is cleared by PWROK reset but not by LDTRESET_L. |
| 7 | **Transmitter Off [TXOFF].** Read. Write 1 only.<br>1 = No output signals on the link toggle. The input link receivers are disabled and the pins may float. |
| 6 | **End Of Chain [ENDOCH].** Read. Write 1 only or set by hardware.<br>1 = The link is not part of the logical HyperTransport™ chain. Packets issued or forwarded to this HyperTransport link are either dropped or result in an NXA error response. Packets received from this HyperTransport link are ignored and CRC is not checked. If the transmitter is still enabled (TXOFF not asserted), then it drives only NOP packets with good CRC. ENDOCH can be set by writing a 1 to it or it may be set by hardware if the HyperTransport link is determined to be disconnected at the rising edge of LDTRESET_L during a cold reset. |
| 5 | **Initialization Complete [INITCPLT].** Read Only. This bit is set by hardware when low-level HyperTransport™ link initialization has successfully completed. If there is no device on the other end of the HyperTransport link, or if the device on the other side of the HyperTransport link is unable to properly perform HyperTransport link initialization, then the bit is not set.<br>Note: This bit is cleared when LDTRESET_L is asserted; it is not cleared when LDTSTOP_L is asserted. |
| 4 | **Link Failure [LKFAIL].** Read. Set by hardware. Write 1 to clear. This bit is set high by hardware when an error is detected on the link that causes the AMD-8132 tunnel to issue sync flood or if the HyperTransport™ link is not used in the system.<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. |
| 3 | **CRC Error Command [CRCERRCMD].** Read-Write. This bit is intended to be used to check the CRC failure detection logic of the device on the other side of the link.<br>0 = Transmitted CRC values match the values calculated per the link specification.<br>1 = The HyperTransport™ link transmission logic generates erroneous CRC values. |
| 2 | Reserved. CRC test mode is not supported. |
| 1 | **CRC Flood Enable [CRCFEN].** Read-Write.<br>0 = CRC errors do not result in sync packets or setting the LKFAIL bit.<br>1 = If DevA:0x04[SERREN] is also enabled, CRC errors (in HyperTransport™ link 0 for DevA:0xC4[CRCFEN]; in HyperTransport link 1 for DevA:0xC8[CRCFEN]) result in sync packets to both outgoing HyperTransport links and the LKFAIL bit is set. |
| 0 | Reserved. |

## Link Revision, Errors, and Frequency Capability 0 — DevA:0xCC

Default: A1: 007D 0025h, Bx: 007D 0040h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:16 | **Link 0 Frequency Capability [FREQCAP0].** Read Only. These bits indicate that side 0 of the tunnel supports 200, 400, 500, 600, 800, and 1000 MHz link frequencies. |
| 15 | **CTL Timeout.** Read-Write. Resets to 0. This bit indicates how long CTL can be low before indicating a protocol error. A value of 0 in this bit = one millisecond; a value of 1 = one second. |
| 14 | **End of Chain Error.** Read. Write 1 to clear. This bit indicates that a posted request or response packet has been given to this transmitter to issue when link 0 is the end of chain or a 64-bit posted request reaches link 0 with 64-bit support disabled. Receiving a device message with the silent drop bit set does not set this bit.<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. |
| 13 | **Overflow Error.** Read. Write 1 to clear. This bit indicates a receive buffer overflow error has been detected on link 0.<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. |
| 12 | **Protocol Error.** Read. Write 1 to clear. This bit indicates a protocol error has been detected on link 0.<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. |
| 11:8 | **Link 0 Frequency [FREQ0].** Read-Write. Specifies the link side 0 transmit frequency. Legal values are 0h (200 MHz), 2h (400 MHz), 3h (500 MHz), 4h (600 MHz), 5h (800 MHz), and 6h (1000 MHz).<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. After this field is updated, the link frequency does not change until either LDTRESET_L is asserted or a link disconnect sequence occurs through LDTSTOP_L. |
| 7:0 | **REVISION.** Read Only. Indicates to which rev of the *HyperTransport™I/O Link Specification* the AMD-8132™ tunnel is compliant.<br>Note: Rev A1 of the AMD-8132 tunnel only indicates support for *HyperTransport™I/O Link Specification, Rev 1.05*. |

## Feature, Link Errors, and Frequency Capability 1 — DevA:0xD0

Default: 007D 0012h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:16 | **Link 1 Frequency Capability [FREQCAP1].** Read Only. These bits indicate that side 1 of the tunnel supports 200, 400, 500, 600, 800, and 1000 MHz link frequencies. |
| 15 | **CTL Timeout.** Read-Write. Resets to 0. This bit indicates how long CTL can be low before indicating a protocol error. A value of 0 in this bit = one millisecond; a value of 1 = one second. |
| 14 | **End of Chain Error.** Read-Write. Write 1 to clear. This bit indicates that a posted request or response packet has been given to this transmitter to issue when link 1 is the end of chain or a 64-bit request reaches link 1 with 64-bit support disabled. Receiving a device message with the silent drop bit set does not set this bit.<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. |

| | |
|---|---|
| 13 | **Overflow Error.** Read-Write. Write 1 to clear. This bit indicates a receive buffer overflow error has been detected on link 1.<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. |
| 12 | **Protocol Error.** Read-Write. Write 1 to clear. This bit indicates a protocol error has been detected on link 1.<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. |
| 11:8 | **Link 1 Frequency [FREQ1].** Read-Write. Specifies the link side 1 transmit frequency. Legal values are 0h (200 MHz), 2h (400 MHz), 3h (500 MHz), 4h (600 MHz), 5h (800 MHz), and 6h (1000 MHz).<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. After this field is updated, the link frequency does not change until either LDTRESET_L is asserted or a link disconnect sequence occurs through LDTSTOP_L. |
| 7:6 | Reserved. |
| 5 | **UnitId Reorder Disable.** Read-Write. When set, for the purpose of ordering the AMD-8132™ tunnel will treat all packets as being from the same UnitId. When clear, the AMD-8132 tunnel is able to perform limited reordering among packets from different sources. |
| 4 | **64 Bit Addressing.** Read Only. The AMD-8132 tunnel supports 64-bit HyperTransport™ addresses. |
| 3 | **Extended CTL Time Required.** Read Only. The AMD-8132 tunnel does not require an extended CTL assertion period following a link disconnect. |
| 2 | **CRC Test Mode.** Read Only. The AMD-8132 tunnel does not support CRC test mode. |
| 1 | **LDTSTOP.** Read Only. The AMD-8132 tunnel supports the LDTSTOP-based link disconnection protocol. |
| 0 | **Isoc.** Read Only. The AMD-8132 tunnel does not support isochronous flow control. |

## Error Handling and Link Enumeration — DevA:0xD4

Default: 0000 0000h — Attribute: See Below

| Bits | Description |
|---|---|
| 31 | Reserved. |
| 30 | **CRC Error Nonfatal Enable.** Read-Write. When asserted, this bit causes nonfatal error interrupt assertion whenever any of the CRCERR bits are asserted in either of the link control registers DevA:0xC4 or DevA:0xC8. |
| 29 | **Response Error Nonfatal Enable.** Read Only. Always 0. The AMD-8132™ tunnel never reports response errors. |
| 28 | **End of Chain Error Nonfatal Enable.** Read-Write. When asserted, this bit causes nonfatal error interrupt assertion whenever the end of chain error bit is asserted in one of the link error registers DevA:0xCC or DevA:0xD0. |
| 27 | **Overflow Error Nonfatal Enable.** Read-Write. When asserted, this bit causes nonfatal error interrupt assertion whenever the overflow error bit is asserted in one of the link error registers DevA:0xCC or DevA:0xD0. |

| | |
|---|---|
| 26 | **Protocol Error Nonfatal Enable.** Read-Write. When asserted, this bit causes nonfatal error interrupt assertion whenever the protocol error bit is asserted in one of the link error registers DevA:0xCC or DevA:0xD0. |
| 25 | **Response Error.** Read Only. Always 0. The AMD-8132 tunnel never reports response errors. |
| 24:23 | Reserved. |
| 22 | **CRC Error Fatal Enable.** Read-Write. When asserted, this bit causes fatal error interrupt assertion whenever any of the CRCERR bits are asserted in either of the link control registers DevA:0xC4 or DevA:0xC8. |
| 21 | **Response Error Fatal Enable.** Read Only. Always 0. The AMD-8132 tunnel never reports response errors. |
| 20 | **End of Chain Error Fatal Enable.** Read-Write. When asserted, this bit causes fatal error interrupt assertion whenever the end of chain error bit is asserted in one of the link error registers DevA:0xCC or DevA:0xD0. |
| 19 | **Overflow Error Fatal Enable.** Read-Write. When asserted, this bit causes fatal error interrupt assertion whenever the overflow error bit is asserted in one of the link error registers DevA:0xCC or DevA:0xD0. |
| 18 | **Protocol Error Fatal Enable.** Read-Write. When asserted, this bit causes fatal error interrupt assertion whenever the protocol error bit is asserted in one of the link error registers DevA:0xCC or DevA:0xD0. |
| 17 | **Overflow Error Flood Enable.** Read-Write. If DevA:0x04[SERREN] is enabled, when asserted this bit causes the link to be flooded with sync packets whenever the overflow error bit is asserted in one of the link error registers DevA:0xCC or DevA:0xD0. |
| 16 | **Protocol Error Flood Enable.** Read-Write. If DevA:0x04[SERREN] is enabled, when asserted this bit causes the link to be flooded with sync packets whenever the protocol error bit is asserted in one of the link error registers DevA:0xCC or DevA:0xD0. |
| 15:0 | **Enumeration Scratchpad [ESP].** Read-Write. This field controls no hardware within the AMD-8132 tunnel.<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. |

## Link Non-Prefetchable Memory Space Extension — DevA:0xD8

Default: 0000 0000h — Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:16 | Reserved. |
| 15:8 | **Non-Prefetchable Upper Memory Limit [NPUML].** This field provides bits[39:32] of the non-prefetchable memory space address limit specified by Dev[B,A]:0x20[MEMLIM]. See Dev[B,A]:0x1C.<br>Note: NPUML and NPUMB are both device A registers but they affect both device A and device B non-prefetchable memory ranges. It is recommended that these registers are left at 0. |

| | |
|---|---|
| 7:0 | **Non-Prefetchable Upper Memory Base [NPUMB].** This field provides bits[39:32] of the non-prefetchable memory space address base specified by Dev[B,A]:0x20[MEMBASE]. See Dev[B,A]:0x1C.<br>Note: NPUML and NPUMB are both device A registers but they affect both device A and device B non-prefetchable memory ranges. It is recommended that these registers are left at 0. |

## Tunnel Control — DevA:0xDC

Default: 0303 000Ch — Attribute: See Below

| Bits | Description |
|---|---|
| 31:27 | **RxLookahd1.** Read-Write. Resets to 0. This field allows software to cause the link 1 receive sync FIFO to look at data ahead of the FIFO entries that its edge synchronizers currently show as valid. This value indicates the minimum number of receive clock edges to be received in the time the edge synchronizer takes to operate, thus hiding some part of the synchronizer latency.<br>Default = 0 (meaning no lookahead, and is therefore safe)<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. After this field is updated, the new value is not applied to the logic until either LDTRESET_L is asserted or a link disconnect sequence occurs through LDTSTOP_L. |
| 26 | **RxHwLookahdEn1.** Read-Write. Resets to 0. Setting this bit enables hardware generation of lookahead values based on sampled frequency. If this bit is 0, the software-written value in RxLookahd1 is used. BIOS is expected to set this bit to 1.<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. After this field is updated, the new value is not applied to the logic until either LDTRESET_L is asserted or a link disconnect sequence occurs through LDTSTOP_L. |
| 25:24 | **TxSlack1.** Read-Write. This register adds slack to synchronization time in the link 1 transmit clock forwarding FIFO in units of 1.5 ns. Slack is added to the minimum time that data must be valid in the FIFO before it is safe to look at in the Tx domain. This field is expected to be written to 0 by BIOS for lowest-latency operation.<br>Default = 4.5 ns (most conservative operation)<br>Note: This bit is initialized by PWROK reset, not by LDTRESET_L. After this field is updated, the new value is not applied to the logic until either LDTRESET_L is asserted or a link disconnect sequence occurs through LDTSTOP_L. |
| 23:19 | **RxLookahd0.** Read-Write. Resets to 0. This field allows software to cause the link 0 receive sync FIFO to look at data ahead of the FIFO entries that its edge synchronizers currently show as valid. This value indicates the minimum number of receive clock edges to be received in the time the edge synchronizer takes to operate, thus hiding some part of the synchronizer latency.<br>Default = 0 (meaning no lookahead, and is therefore safe)<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. After this field is updated, the new value is not applied to the logic until either LDTRESET_L is asserted or a link disconnect sequence occurs through LDTSTOP_L. |
| 18 | **RxHwLookahdEn0.** Read-Write. Resets to 0. Setting this bit enables hardware generation of lookahead values based on sampled frequency. If this bit is 0, the software-written value in RxLookahd0 is used. BIOS is expected to set this bit to 1.<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. After this field is updated, the new value is not applied to the logic until either LDTRESET_L is asserted or a link disconnect sequence occurs through LDTSTOP_L. |

| | |
|---|---|
| 17:16 | **TxSlack0.** Read-Write. This register adds slack to synchronization time in the link 0 transmit clock forwarding FIFO in units of 1.5 ns. Slack is added to the minimum time that data must be valid in the FIFO before it is safe to look at in the Tx domain. This field is expected to be written to 0 by BIOS for lowest-latency operation.<br>Default = 4.5 ns (most conservative operation)<br>Note: This bit is cleared by PWROK reset, not by LDTRESET_L. After this field is updated, the new value is not applied to the logic until either LDTRESET_L is asserted or a link disconnect sequence occurs through LDTSTOP_L. |
| 15:12 | **RxFreq1.** Read Only. Contains the link frequency, as determined by the link 1 receiver, for the transmitter to which it is connected. This field is only valid if DevA:0xC8[INITCPLT] is set. It uses the same frequency encodings as DevA:0xCC[FREQ0] with the addition that 1h is also a legal encoding indicating 300 MHz. |
| 11:8 | **RxFreq0.** Read Only. Contains the link frequency, as determined by the link 0 receiver, for the transmitter to which it is connected. This field is only valid if DevA:0xC4[INITCPLT] is set. It uses the same frequency encodings as DevA:0xCC[FREQ0] with the addition that 1h is also a legal encoding indicating 300 MHz. |
| 7 | **Upstream Response Data Error Disable.** Read-Write. Resets to 0. When set, this bit prevents the tunnel from issuing RdResponse or TgtDone packets to the HyperTransport™ chain containing the Data Error encoding on the error bits. Instead, packets that would normally be issued with a Data Error encoding are issued as normal (no error) responses. This bit does not affect packets being forwarded through the tunnel. |
| 6 | **Downstream Post Data Error Disable.** Read-Write. Resets to 0. When set, this bit causes the tunnel to ignore the data error bit in received HyperTransport™ posted request packets. The bit is still preserved in forwarded packets, but the tunnel treats the packet as if the bit were 0. |
| 5 | **Chain Disable.** Read-Write. Resets to 0. When set, this bit causes the tunnel to ignore the chain bit in received HyperTransport™ posted request packets. The bit is still preserved in forwarded packets, but the tunnel treats the packet as if the bit were 0. |
| 4 | **DBLINSRATE.** Read-Write.<br>• If clear (default), the maximum insertion rate onto a busy HyperTransport™ link for packets originating from the two bridges is computed according to the fairness algorithm given in *HyperTransport™ I/O Link Specification, Rev 2.0*.<br>• If set, the maximum insertion rate is double the specification-calculated rate. |
| 3:2 | **Posted Weight.** Read-Write. Resets to 11b. Arbitration between virtual channels to send packets to any output port (either HyperTransport™ link or the PCI buses) uses a weighted round-robin scheme: nonposted requests and responses having unit weight and posted requests weighted more weakly. The weight used for posted requests is determined by this CSR and is equal to 2^-PW. Setting this CSR to 0 results in posted requests having equal weight with the other two virtual channels. With the default value, posted requests have 1/8th the weight of other channels. |
| 1 | **Stream Disable 1-to-0.** Read-Write.<br>0 = Begin sending packets without waiting for all data to be received. If data is not available for transmission when needed, NOPs will be inserted on link 0.<br>1 = Require all data associated with a posted request or response to be received from link 1 before the packet can be forwarded to link 0.<br>Note: The default value is to stream for lower latency. In general, the bits should only get set when the link bandwidths on each side are mismatched. |

| | |
|---|---|
| 0 | **Stream Disable 0-to-1.** Read-Write.<br>0 = Begin sending packets without waiting for all data to be received. If data is not available for transmission when needed, NOPs will be inserted on link 1.<br>1 = Require all data associated with a posted request or response to be received from link 0 before the packet can be forwarded to link 1.<br>Note: The default value is to stream for lower latency. In general, the bits should only get set when the link bandwidths on each side are mismatched. |

## Clock Control DevA:0xF0

See section 4.1.2 for details on clock gating. AMD system recommendations for System Management Action Field (SMAF) codes are: 0=ACPI C2; 1=ACPI C3; 2=FID/VID change; 3=ACPI S1; 4=ACPI S3; 5=Throttling; 6=ACPI S4/S5. AMD recommends setting this register to 0004_0008h to gate clocks during S1.

Default: 0000 0000h Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:19 | Reserved. |
| 18 | **Clock Gate Enable [CGEN].**<br>0 = Not enabled.<br>1 = Internal clock gating, as specified by bits[7:0] of this register, is enabled. |
| 17 | Reserved. |
| 16 | Reserved. |
| 15:8 | Reserved. |
| 7:0 | **Internal Clock Gating System Management Action Fields [ICGSMAF].** Each of the bits of this field correspond to SMAF values captured in STOP_GRANT cycles from the host. For each bit:<br>0 = No power reduction while LDTSTOP_L is asserted.<br>1 = When LDTSTOP_L is asserted after a STOP_GRANT cycle in which the SMAF field matches the ICGSMAF bit that is asserted, then the AMD-8132™ tunnel power is reduced through gating of internal clocks.<br>For example: if clock gating is required for SMAF values of 3 and 5, then ICGSMAF[3, 5] must be high. See section 4.1.2. |

### MSI Mapping Capability Block Header — Dev[B,A]:0xF4

Default: A800 0008h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:24 | Read Only. 0xA8 indicates this is an MSI/MSI-X Mapping Capability Block. |
| 23:18 | Reserved. |
| 17 | A1: Reserved.<br>B1: Read Only. 0 indicates the MSI window may be located anywhere in 64-bit memory mapped space. |
| 16 | **MSI_ENABLE.** Read-Write. If this bit is a 1, PCI and PCI-X® MSI/MSI-Xs are mapped to HyperTransport™ interrupts as specified in this capability block. |
| 15:8 | **Next Capabilities Pointer.** Read Only (0x00). All 0s indicates this is the last capability block for this device/function. |
| 7:0 | **Capability ID.** Read Only. Capability ID is 08, indicating HyperTransport™. |

### MSI Mapping Capability Block Lower Address — Dev[B,A]:0xF8

Default: FEE0 0000h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:20 | **Lower Address.** Read-Write. This stores address bits 31:20 of the MSI/MSI-X address range. |
| 19:0 | Reserved. |

### MSI Mapping Capability Block Upper Address — Dev[B,A]:0xFC

Default: 0000 0000h — Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:0 | **Upper Address.** This stores address bits 63:32 of the MSI/MSI-X address. If the enable bit in Dev[B,A]:0xF4[MSI_ENABLE] is set and a PCI memory write transaction or a PCI-X® memory write or memory write block matches the address created by concatenating this upper address with the lower address (address bits 19:0 are ignored when matching these addresses), then the PCI operation is an MSI/MSI-X and is translated to a HyperTransport™ interrupt as described in section 1.3.2.3. |

## 3.3 PCI-X® IOAPIC Configuration Registers

These registers are located in PCI configuration space: function 1 in the first device (device A) and function 1 in the second device (device B).

- See section 3.1.2 for a description of the register naming convention.

- See *82093AA I/O Advanced Programmable Interrupt Controller (IOAPIC) Product Data* for more information.

The IOAPIC registers have two modes of operation:

1. If Dev[B,A]:1x44[OSVISBAR] is a 0, then the IOAPIC register space is not accessible through a standard BAR, but only through the memory range defined in Dev[B,A]:1x48. In this mode Dev[B,A]:1x04[MASEN] and Dev[B,A]:1x04[MEMEN] have no effect.
2. If Dev[B,A]:1x44[OSVISBAR] is a 1, then the IOAPIC register space is accessible through a standard BAR location and is also accessible through the same memory range defined in Dev[B,A]:1x48. In this mode, Dev[B,A]:1x04[MASEN] and Dev[B,A]:1x04[MEMEN] function as stated in their bit descriptions

## IOAPIC Vendor and Device ID — Dev[B,A]:1x00

Default: 7459 1022h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:16 | **Device ID.** IOAPIC device ID is 7459. |
| 15:0 | **Vendor ID.** AMD's vendor ID is 1022. |

## IOAPIC Status and Command — Dev[B,A]:1x04

Default: 0200 0000h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:3 | Read Only. These bits are fixed in their default state. |
| 2 | **PCI Master Enable [MASEN].** Read-Write.<br>0 = Not enabled.<br>1 = Enables IOAPIC to initiate interrupt requests to the host.<br>Note: Dev[B,A]:1x44[IOAEN] must be high to enable interrupt requests, regardless of the state of this bit. If Dev[B,A]:1x44[OSVISBAR] = 0, then the state of this bit is ignored. |
| 1 | **Memory Enable [MEMEN].** Read-Write.<br>0 = Not enabled.<br>1 = Enables access to the memory space specified by DevA:1x10.<br>Note: If Dev[B,A]:1x44[OSVISBAR] = 0, then the state of this bit is ignored. Dev[B,A]:1x44[IOAEN] must be high to enable access to the register space, regardless of the state of this bit. |
| 0 | **IO Enable.** Read Only. This bit is fixed in the low state. |

## IOAPIC Revision and Class Code — Dev[B,A]:1x08

Default: A1: 0800 1001h, Bx: 0800 1011h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:8 | **CLASSCODE.** Provides the IOAPIC class code. |
| 7:0 | **REVISION.** AMD-8132™ tunnel revision. 01h = revision Ax. 11h = revision B1. |

## IOAPIC Device BIST-Header-Latency-Cache — Dev[B,A]:1x0C

Default: 0000 0000h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:24 | **BIST.** These bits are fixed at their default values. |
| 23:16 | **HEADER.** These bits are fixed at their default values. |
| 15:8 | **LATENCY.** These bits are fixed at their default values. |
| 7:0 | **CACHE.** These bits are fixed at their default values. |

**Note:** **IOAPIC Base Address Registers**. Offsets 10h/14h and 48h/4Ch provide access to the same 8-byte register. Offsets 48h/4Ch are always accessible. However, offsets 10h/14h can be disabled from read and write access through Dev[B,A]:1x44[OSVISBAR].

## IOAPIC Base Address Low — Dev[B,A]:1x10 and Dev[B,A]:1x48

Default: 0000 000?h — Attribute: See Below

| Bits | Description |
|---|---|
| 31:12 | **IOAPIC Base Address Register [IOABAR] Low.** Read-Write. These bits specify address space bits [31:12] of the IOAPIC register set APIC[B,A]:XX. |
| 11:0 | Read Only.<br>• If Dev[B,A]:1x44[OSVISBAR] is high, these bits read 004h to indicate a 4-Kbyte block of 64-bit, non-prefetchable memory space.<br>• If Dev[B,A]:1x44[OSVISBAR] is low, these bits read all 0s. |

### IOAPIC Base Address High — Dev[B,A]:1x14 and Dev[B,A]:1x4C

Default: 0000 0000h — Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:0 | **IOAPIC Base Address Register [IOABAR] High.** These bits specify address space bits [63:32] of the IOAPIC register set APIC[B,A]:XX. |

### IOAPIC Device Subsystem ID and Subsystem Vendor ID — Dev[B,A]:1x2C

Default: 0000 0000h — Attribute: Read; Write Once

| Bits | Description |
|---|---|
| 31:16 | **Subsystem ID.** This field controls no hardware. |
| 15:0 | **Subsystem Vendor ID.** This field controls no hardware. |

### Pointer to Capabilities Block — Dev[B,A]:1x34

Default: 0000 0050h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:8 | Reserved. |
| 7:0 | **Capabilities Pointer.** Points to HyperTransport™ Revision Capability Block. |

### IOAPIC Control — Dev[B,A]:1x44

Default: 0000 0000h — Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:2 | Reserved. |
| 1 | **IOAPIC Enable [IOAEN].**<br>0 = Not enabled.<br>1 = Access to the IOAPIC registers pointed to by Dev[B,A]:1x10/48 is enabled and the IOAPIC is enabled to generate interrupt requests. |
| 0 | **Operating System Visible Base Address Register [OSVISBAR].**<br>0 = Dev[B,A]:1x10 is not visible; reads provide all zeros and writes are ignored. The state of Dev[B,A]:1x04[MASEN, MEMEN] are also ignored.<br>1 = The IOAPIC BAR is read-write accessible through Dev[B,A]:1x10 and Dev[B,A]:1x04[MASEN, MEMEN] function as specified. |

## HyperTransport™ Revision Capabilities Block — Dev[B,A]:1x50

Default: A1: 8825 0008h, Bx: 8840 0008h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:24 | **Capability Type.** Indicates this capability block is a HyperTransport™ Revision ID Capability Block. |
| 23:16 | **Revision ID.** Indicates to which rev of the *HyperTransport™I/O Link Specification* the AMD-8132™ tunnel is compliant.<br>Note: Rev A1 of the AMD-8132 tunnel only indicates support for *HyperTransport™I/O Link Specification, Rev 1.05*. |
| 15:8 | **Capabilities Pointer.** (0x00) All 0s indicates this is the last capability block for this device/function. |
| 7:0 | **Capability ID.** This is a HyperTransport™ Capability Block. |

# 3.4 PHY Compensation Control

## PCI-X® PHY Compensation Control Dev[B,A]:1x[94,90,8C,88,84,80]

### Dev[B,A]:1x80 Horizontal

Default: See individual fields. Attribute: See Below

| Bits | Description |
|---|---|
| 31 | Reserved. |
| 30 | **COMPOFFSETPADD.** Read-Write.<br>• Setting this bit to 1 to causes COMPOFFSETP to be added to the result of the compensation averager.<br>• Setting this bit to 0 causes COMPOFFSETP to be subtracted from the result of the compensation averager.<br>Default = 0 |
| 29:25 | Reserved. |
| 24:20 | **COMPPAVGP.** Read Only. The most recent result from the pullup compensation moving averager. |
| 19:15 | Reserved. |
| 14:10 | **COMPOFFSETP.** Read-Write. This value is combined with the result of the pullup compensation averager, the manner of combination depending upon the state of COMPOFFSETPADD.<br>• If Dev[B,A]:1x90[COMPOVERRIDEP] is 0, the result gets driven to the pullup compensation resistors. The result in case of overflow/underflow is 0xF/0x0.<br>• If Dev[B,A]:1x90[COMPOVERRIDEP] is 1, this value gets driven directly to the PCI compensation pullup resistors. COMPOVERRIDE takes precedence over COMPOFFSETNADD. Values greater than 0x11 are rounded down to 0x11 before being used.<br>Default: A1 = 0x00 if the pin CMPOVR is clear at PWROK, 0x10 otherwise.<br>B1 = 0 if the pin CMPOVR is clear at PWROK, 0x8 otherwise. |
| 9:5 | Reserved. |
| 4:0 | Reserved. |

### Dev[B,A]:1x84 Horizontal

Default: See individual fields. Attribute: See Below

| Bits | Description |
|---|---|
| 31:25 | Note: Reserved. |
| 24 | **COMPOVERRIDEI.** Read-Write. Setting this bit causes Dev[B,A]:1x90[4:0] COMPOFFSETI to be driven directly to the compI ports on the pclamp pads. The results of the averager are ignored.<br>Default = value of CMPOVR pin at PWROK |
| 23:0 | **COMPCOUNT.** Read Only. This counter increments each time the PCI compensation resistors get updated with a new value. It rolls to 0 when all 1s has been reached.<br>Note: This value is derived from the horizontal component of the calibration mechanism. |

### Dev[B,A]:1x88 Vertical

Default: See individual fields. Attribute: See Below

| Bits | Description |
|---|---|
| 31 | Reserved. |
| 30 | **COMPOFFSETPADD.** Read-Write.<br>• Setting this bit to 1 to causes COMPOFFSETP to be added to the result of the compensation averager.<br>• Setting this bit to 0 causes COMPOFFSETP to be subtracted from the result of the compensation averager.<br>Default = 0 |
| 29:25 | Reserved. |
| 24:20 | **COMPPAVGP.** Read Only. The most recent result from the pullup compensation moving averager. |
| 19:15 | Reserved. |
| 14:10 | **COMPOFFSETP.** Read-Write. This value is combined with the result of the pulldown compensation averager, the manner of combination depending upon the state of COMPOFFSETPADD.<br>• If Dev[B,A]:1x94[COMPOVERRIDEP] is 0, the result gets driven to the pulldown compensation resistors. The result in case of overflow/underflow is 0xF/0x0.<br>• If Dev[B,A]:1x94[COMPOVERRIDEP] is 1, this value gets driven directly to the PCI compensation pullup resistors. COMPOVERRIDE takes precedence over COMPOFFSETNADD. Values greater than 0x11 are rounded down to 0x11 before being used.<br>Default: A1 = 0x00 if the pin CMPOVR is clear at PWROK, 0x10 otherwise.<br>B1 = 0 if the pin CMPOVR is clear at PWROK, 0x8 otherwise. |
| 9:5 | Reserved. |
| 4:0 | Reserved. |

### Dev[B,A]:1x8C Vertical

Default: See individual fields. Attribute: See Below

| Bits | Description |
|---|---|
| 31 | Reserved. |
| 30 | Note: Reserved. |
| 29 | Note: Reserved. |
| 28 | Note: Reserved. |
| 27:25 | Reserved. |
| 24 | **COMPOVERRIDEI.** Read-Write. Setting this bit causes Dev[B,A]:1x94[4:0] COMPOFFSETI to be driven directly to the compI ports on the pclamp pads. The results of the averager are ignored.<br>Default = value of CMPOVR pin at PWROK |
| 23:0 | Note: Reserved. |

### Dev[B,A]:1x90 Horizontal

Default: See individual fields. Attribute: See Below

| Bits | Description |
|---|---|
| 31:13 | Reserved. |
| 12 | Reserved. |
| 11 | Reserved. |
| 10 | **COMPOFFSETIADD.** Read-Write.<br>• Setting this bit to 1 to causes COMPOFFSETI to be added to the result of the compensation averager.<br>• Setting this bit to 0 causes COMPOFFSETI to be subtracted from the result of the compensation averager.<br>Default = 0b |
| 9:5 | **COMPPAVGI.** Read Only. The most recent result from the compI moving averager. |
| 4:0 | **COMPOFFSETI.** Read-Write. This value is combined with the result of the horizontal compI compensation averager, the manner of the combination depending upon the state of COMPOFFSETIADD.<br>• If COMPOVERRIDEI is 0, this result gets driven to compI of the pclamps. In case of overflow/ underflow, the result is 00000b/11111b.<br>• If COMPOVERRIDEI is 1, this value gets driven to compI of the pclamps. COMPOVERRIDEI takes precedence over COMPOFFSETIADD.<br>Default = 0x00 if the pin CMPOVR is clear at PWROK, 0x10 otherwise. |

### Dev[B,A]:1x94 Vertical

Default: See individual fields. Attribute: See Below

| Bits | Description |
|---|---|
| 31:18 | Reserved. |
| 17 | Note: Reserved. |
| 16:13 | Note: Reserved. |
| 12 | Reserved. |
| 11 | Reserved. |
| 10 | **COMPOFFSETIADD.** Read-Write.<br>• Setting this bit to 1 to causes COMPOFFSETI to be added to the result of the compensation averager.<br>• Setting this bit to 0 causes COMPOFFSETI to be subtracted from the result of the compensation averager.<br>Default = 0b |
| 9:5 | **COMPPAVGI.** Read Only. The most recent result from the compI moving averager. |
| 4:0 | **COMPOFFSETI.** Read-Write. This value is combined with the result of the vertical compI compensation averager, the manner of the combination depending upon the state of COMPOFFSETIADD.<br>• If COMPOVERRIDEI is 0, this result gets driven to compI of the pclamps. In case of overflow/underflow, the result is 00000b/11111b.<br>• If COMPOVERRIDEI is 1, this value gets driven to compI of the pclamps. COMPOVERRIDEI takes precedence over COMPOFFSETIADD.<br>Default = 0x00 if the pin CMPOVR is clear at PWROK, 0x10 otherwise. |

## Link PHY Compensation Control Dev[B,A]:1x[D8,D4,C8,C4,C0]

### Dev[B,A]:1xC0

Default: See individual fields. Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:30 | **TXADJMODE.** Same functional description as Dev[B,A]:0xC8[IREFADJMODE], but applied to TX[3:0]ADJ. Values written to this CSR do not take effect until a 1 has been written to Dev[B,A]:1xC4[TXUPDATE].<br>Default = 00b if the pin CMPOVR is clear at PWROK, 11b otherwise.<br>Note: Set to its default value at the rising edge of PWROK and unaffected by LDTRESET_L. |
| 29:28 | Note: Reserved. |
| 27:22 | Note: Reserved. |
| 21:15 | **TX1ADJ.** The actual adjustment value that gets applied according to the setting of TXADJMODE. Values written to this CSR do not take effect until a 1 has been written to TXUPDATE.<br>• A write to this CSR updates it with the written value.<br>• A read from this CSR returns the most recently calculated TX1 result.<br>Default = 0000000b<br>Note: Set to its default value at the rising edge of PWROK and unaffected by LDTRESET_L. |

| | |
|---|---|
| 14:13 | Note: Reserved. |
| 12:7 | Reserved.<br>Note: |
| 6:0 | **TX0ADJ.** For TX0, the actual adjustment value that gets applied according to the setting of TXADJMODE. Values written to this CSR do not take effect until a 1 has been written to TXUPDATE.<br>• A write to this CSR updates it with the written value.<br>• A read from this CSR returns the most recently calculated TX1 result.<br>Default = 1000000b<br>Note: Set to its default value at the rising edge of PWROK and unaffected by LDTRESET_L. |

**Dev[B,A]:1xC4**

Default: See individual fields. Attribute: Read-Write

| Bits | Description |
|---|---|
| 31 | Reserved. |
| 30 | **TXUPDATE.** A write of 0 followed by a write of 1 to this CSR causes the values in other TX CSRs to take effect allowing an atomic update despite the fact TX CSRs occupy more than one doubleword.<br>Default = 0 |
| 29:28 | Note: Reserved. |
| 27:22 | Note: Reserved. |
| 21:15 | **TX3ADJ.** Applied to TX3, the actual adjustment value that gets applied according to the setting of TXADJMODE. Values written to this CSR do not take effect until a 1 has been written to TXUPDATE.<br>• A write to this CSR updates it with the written value.<br>• A read from this CSR returns the most recently calculated TX3 result.<br>Default = 0b<br>Note: Set to its default value at the rising edge of PWROK and unaffected by LDTRESET_L. |
| 14:13 | Note: Reserved. |
| 12:7 | Note: Reserved. |
| 6:0 | **TX2ADJ.** Applied to TX2, the actual adjustment value that gets applied according to the setting of TXADJMODE. Values written to this CSR do not take effect until a 1 has been written to TXUPDATE.<br>• A write to this CSR updates it with the written value.<br>• A read from this CSR returns the most recently calculated TX2 result.<br>Default = 1000000b<br>Note: Set to its default value at the rising edge of PWROK and unaffected by LDTRESET_L. |

**Dev[B,A]:1xC8**

Default: See individual fields. Attribute: Read-Write

| Bits | Description |
|---|---|
| 31 | Reserved. |
| 30 | Note: Reserved. |

| | |
|---|---|
| 29 | Note: Reserved. |
| 28 | Note: Reserved. |
| 27 | Note: Reserved. |
| 26 | Note: Reserved. |
| 25 | Note: Reserved. |
| 24:23 | **IREFADJMODE.** Encodings for adjustments:<br>00 = No adjustment.<br>01 = Add IREFADJ to calculated result before updating transmitters.<br>10 = Subtract IREFADJ from calculated result before updating transmitters.<br>11 = IREFADJ replaces calculated result.<br>The addition and subtraction do not wrap.<br>Default = 00b if the pin CMPOVR is clear at PWROK, 11b otherwise.<br>Note: Set to its default value at the rising edge of PWROK and unaffected by LDTRESET_L. |
| 22:17 | Note: Reserved. |
| 16:13 | **IREFADJ.** Applied to IREF, the actual adjustment value that gets applied according to the setting of IREFADJMODE. Values written to this CSR do not take effect until a 1 has been written to 1xD8[IREFUPDATE].<br>• A write to this CSR updates it with the written value.<br>• A read from this CSR returns the most recently calculated IREF result.<br>Default = 0111b<br>Note: Set to its default value at the rising edge of PWROK and unaffected by LDTRESET_L. |
| 12:11 | **RXADJMODE.** Encodings for adjustments applied to RX:<br>00 = No adjustment.<br>01 = Add IREFADJ to calculated result before updating transmitters.<br>10 = Subtract IREFADJ from calculated result before updating transmitters.<br>11 = IREFADJ replaces calculated result.<br>The addition and subtraction do not wrap.<br>Default = 00b if the pin CMPOVR is clear at PWROK, 11b otherwise.<br>Note: Set to its default value at the rising edge of PWROK and unaffected by LDTRESET_L. |
| 10:5 | Note: Reserved. |
| 4:0 | **RXADJ.** Applied to RX, the actual adjustment value that gets applied according to the setting of RXADJMODE. Values written to this CSR do not take effect until a 1 has been written to 1xD8[RXUPDATE].<br>• A write to this CSR updates it with the written value.<br>• A read from this CSR returns the most recently calculated RX result.<br>Default = 01000b<br>Note: Set to its default value at the rising edge of PWROK and unaffected by LDTRESET_L. |

### Dev[B,A]:1xD4

Default: See individual fields. Attribute: Read-Write

This block of CSRs provides a mechanism where by the HyperTransport calibration block can be controlled solely by reading and writing CSRs and is active when the CSR HT_DIRECT is asserted.

| Bits | Description |
|---|---|
| 31 | **HT_DIRECT.**<br>• When asserted, the pins of the HyperTransport™ calibration block are controlled directly by the CSRs in the doubleword 1xD4.<br>• When clear, the HyperTransport calibration block is controlled by a block of hardware that automatically derives the HyperTransport calibration values before applying them to the pads.<br>Default = value of CMPOVR pin at rising edge of PWROK |
| 30 | Reserved. |
| 29 | Reserved. |
| 28 | Reserved. |
| 27:22 | Reserved. |
| 21 | Reserved. |
| 20 | Reserved. |
| 19:16 | **I_REF.** When HT_DIRECT is asserted, this CSR directly controls the I_REF port of the HyperTransport™ calibration block.<br>Default = 0x0 |
| 15 | **RX_REF_UPDATE.** When HT_DIRECT is asserted, this CSR directly controls the RX_REF_UPDATE port of the HyperTransport™ calibration block.<br>Default = 0b |
| 14:10 | Reserved. |
| 9 | Reserved. |
| 8 | Reserved. |
| 7 | **TX_PHY_UPDATE.** When HT_DIRECT is asserted, this CSR directly controls the TX_PHY_UPDATE port of the HyperTransport™ calibration block.<br>Default = 0b |
| 6:0 | Reserved. |

### Dev[B,A]:1xD8

Default: See individual fields. Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:30 | Reserved. |
| 29 | **IREFUPDATE.** This csr should be set to 1 when a new set of IREF CSR values is present. This CSR is written to 0 by the hardware when it has absorbed the new values. The associated CSRs are Dev[B,A]:1xC8[IREFCOMPREF, IREFINVDIFFSE, IREFADJ]; Dev[B,A]:1xD0[IREFBYPINVDIFFSE]; Dev[B,A]:1xE0[IREF_MIN, IREF_MAX].<br>Default = 1b |

| | |
|---|---|
| 28 | **RXUPDATE.** This csr should be set to 1 when a new set of RX CSR values is present. This CSR is written to 0 by hardware when it has absorbed the new values. The associated CSRs are Dev[B,A]:1xC8[RXCOMPREF, RXADJ]; Dev[B,A]:1xD0[RXINVDIFFSE, Dev[B,A]:RXBYPINVDIFFSE]; Dev[B,A]:1xE0[RX_MIN, RX_MAX].<br>Default = 1b |
| 27:21 | Reserved. |
| 20:14 | Reserved. |
| 13:7 | Reserved. |
| 6:0 | Reserved. |

# 3.5 Performance Counters

### Performance Counters and Control — DevA:1x[AC,A8,A4,A0]

The AMD-8132™ tunnel implements two performance counters, DevA:1x[A0,A4]. The counter DevA:1xA0 is controlled by register DevA:1xA8; the counter DevA:1xA4 is controlled by register DevA:1xAC. Both counters require the count enable bit DevA:1xA8[0] = 1 to start counting and otherwise work identically. The DevA:1xA4 counter also requires its own private enable bit DevA:1xAC[0] = 1 to start counting. The DevA:1xAC[0] bit has no effect on DevA:1xA0.

For the rest of this description:

- Counter0 refers to DevA:1xA0
- Counter1 refers to DevA:1xA4
- Control0 refers to DevA:1xA8
- Control1 refers to DevA:1xAC
- Counter refers to descriptions that apply to DevA:1xA0 or DevA:1xA4.
- Control refers to descriptions that apply to DevA:1xA8 or DevA:1xAC.

Both counters can access information from one of four sources:

- To access information from HyperTransport™ link 0: {Control[1],Control[4]} = 0
- To access information from HyperTransport™ link 1: {Control[1],Control[4]} = 1
- To access information from PCI/PCI-X® bus A: {Control[1],Control[4]} = 2
- To access information from PCI/PCI-X® bus B: {Control[1],Control[4]} = 3

The counter implemented is 36 bits. If Control[2] is zero, then the counter behaves as a 32-bit counter. The counter overflows if it exceeds 'hffff_ffff and a write to the counter will affect bits [31:0]. If Control[2] is one, then the counter behaves as a 36-bit counter with bits [35:4] readable in the Counter CSR. The counter overflows if it exceeds 'hf_ffff_ffff, and writes to the counter set bits [35:4] and clear bits [3:0].

Writing to the counter always clears the overflow bit.

The lower order bits of the control register often affect the meaning of the upper bits of the control register.

### DevA:1x[A0,A4] Counter

Default: See individual fields. Attribute: Read-Write

| Bits | Description |
|---|---|
| 31:0 | • If Control[2] = 0, these are counter bits[31:0]. The count wraps to zero after FFFF_FFFFh and sets the overflow bit Control[3]. A write to the counter writes bits [31:0] and always clears the overflow bit Control[3].<br>• If Control[2] = 1, these are counter bits[35:4]. The count wraps to zero after F_FFFF_FFFFh and sets the overflow bit Control[3]. A write to the counter writes bits [35:4], sets bits [3:0] to zero, and always clears the overflow bit Control[3].<br>Default = 0 |

### DevA:1x[A8,AC] Counter Control

Default: See individual fields. Attribute: Read-Write

| Bits | Description |
|---|---|
| 31 | **Counter Clear.** Writing a 1 to this bit sets Counter[35:0] to zero and clears the overflow bit Control[3].<br>Default = 0 |
| 30:28 | Reserved. |
| 27:24 | **PCI/PCI-X® Commands.**<br>• If Control[1] = 0, these bits are Reserved.<br>• If Control[1] = 1, Command [3:0] is compared with PCI CBE command bits. Counting commands is enabled by bit 23 in this register.<br>Default = 0 |
| 23 | **Count Commands.**<br>• If Control[1] = 0, this bit is Reserved.<br>• If Control[1] = 1 and this bit is set to 0, the count commands defined in bits [27:24] are disabled. If Control[1] = 1 and this bit is set to 1, the count commands defined in bits [27:24] are enabled and controlled by Control[14:13].<br>Default = 0 |
| 22 | **Count Command Buffers Almost Full / Count Source Tags.**<br>• If Control[1] = 0 and this bit is set to 0, counting the total command buffers used is enabled. If Control[1] = 0 and this bit is set to 1, counting the cycles when all but one of the command buffers are full is enabled.<br>• If Control[1] = 1 and this bit is set to 0, counting outbound PCI-X® tags in use or inbound source tags in use is disabled. If Control[1] = 1 and this bit is set to 1, counting outbound PCI-X tags in use or inbound source tags in use is enabled. The count can be the number of PCLK cycles that gpids_pclk has 0 free outbound PCI-X tags with the CountXTagsAllInUse signal indicating the maximum number of outbound nonposted requests (4) have already been split on PCI-X and are waiting for split completions. Or, the count can be the number of inbound source tags in use each PCLK. Controlled by Control[14:13]; takes precedence over Control[23].<br>Default = 0<br>Note: If Control[1] = 0, this bit affects Control[20:18]. |

| | |
|---|---|
| 21 | **Count Command Buffers Full / Count Nonposted Buffers Full.**<br>• If Control[1] = 0 and this bit is set to 0, counting the total command buffers used is enabled.<br>If Control[1] = 0 and this bit is set to 1, counting the cycles when all command buffers are full is enabled.<br>• If Control[1] = 1 and this bit is set to 0, counting full outbound nonposted FIFOs or the inbound nonposted stream count is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting full outbound nonposted FIFOs or the inbound nonposted stream count is enabled. The count can be the cycles in which the outbound nonposted request FIFO is full or the number of inbound nonposted request entries in use each PCLK. Controlled by Control[14:13]; takes precedence over Control[23:22].<br>Default = 0<br>Note: If Control[1] = 0, this bit affects Control[20:18]. |
| 20 | **Count Response Buffers / Count Posted Buffer Full.**<br>• If Control[1] = 0 and this bit is set to 0, counting response command buffers is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting response command buffers is enabled. Any combination of Control[20:18] can be set, the count will be the total for all operations selected.<br>• If Control[1] = 1 and this bit is set to 0, counting the full outbound posted FIFOs or full inbound posted buffers is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting the full outbound posted FIFOs or full inbound posted buffers is enabled. The count is the cycles in which the outbound or inbound posted request FIFO is full. Controlled by Control[14:13]; takes precedence over Control[23:21].<br>Default = 0<br>Note: If Control[1] = 0, this bit is affected by Control[22:21]. |
| 19 | **Count Nonposted Buffers / Count Doublewords Transferred.**<br>• If Control[1] = 0 and this bit is set to 0, counting nonposted command buffers is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting nonposted command buffers is enabled. Any combination of Control[20:18] can be set, the count will be the total for all operations selected.<br>• If Control[1] = 1 and this bit is set to 0, counting doublewords transferred is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting doublewords transferred is enabled. Controlled by Control[16:13]; takes precedence over Control[23:20].<br>Default = 0<br>Note: If Control[1] = 0, this bit is affected by Control[22:21]. |
| 18 | **Count Posted Buffers / Count Disconnects.**<br>• If Control[1] = 0 and this bit is set to 0, counting posted command buffers is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting posted command buffers is enabled. Any combination of Control[20:18] can be set, the count will be the total for all operations selected.<br>• If Control[1] = 1 and this bit is set to 0, counting disconnects is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting disconnects is enabled. Controlled by Control[16:13]; takes precedence over Control[23:19].<br>Default = 0<br>Note: If Control[1] = 0, this bit is affected by Control[22:21]. |

| | |
|---|---|
| 17 | **Count Target Done / Count Retries.**<br>• If Control[1] = 0 and this bit is set to 0, counting target done commands is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting target done commands is enabled. Any combination of Control[17:10] can be set, the count will be the total for all operations selected.<br>• If Control[1] = 1 and this bit is set to 0, counting retries is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting retries is enabled. Controlled by Control[16:13]; takes precedence over Control[23:18].<br>Default = 0<br>Note: If Control[1] = 0, this bit is affected by Control[9:7]. |
| 16 | **Count Flushes / Count Reads.**<br>• If Control[1] = 0 and this bit is set to 0, counting flush commands is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting flush commands is enabled. Any combination of Control[17:10] can be set, the count will be the total for all operations selected.<br>• If Control[1] = 1 and this bit is set to 0, counting read operations is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting the read operation selected in Control[19:17] is enabled. Operations selected here do not affect operations selected by bits Control[22:20].<br>Default = 0<br>Note: If Control[1] = 0, this bit is affected by Control[9:7]. |
| 15 | **Count Broadcasts / Count Writes.**<br>• If Control[1] = 0 and this bit is set to 0, counting broadcast commands is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting broadcast commands is enabled. Any combination of Control[17:10] can be set, the count will be the total for all operations selected.<br>• If Control[1] = 1 and this bit is set to 0, counting write operations is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting the write operation selected in Control[19:17] is enabled. Operations selected here do not affect operations selected by Control[22:20].<br>Default = 0<br>Note: If Control[1] = 0, this bit is affected by Control[9:7]. |
| 14 | **Count Fences / Count Outbound Operations.**<br>• If Control[1] = 0 and this bit is set to 0, counting fence commands is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting fence commands is enabled. Any combination of Control[17:10] can be set, the count will be the total for all operations selected.<br>• If Control[1] = 1 and this bit is set to 0, counting outbound operations is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting outbound operations selected in Control[22:17] is enabled.<br>Default = 0<br>Note: If Control[1] = 0, this bit is affected by Control[9:7]. |
| 13 | **Count Nonposted Reads / Count Inbound Operations.**<br>• If Control[1] = 0 and this bit is set to 0, counting nonposted read commands is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting nonposted read commands is enabled. Any combination of Control[17:10] can be set, the count will be the total for all operations selected.<br>• If Control[1] = 1 and this bit is set to 0, counting inbound operations is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting inbound operations selected in Control[22:17] is enabled.<br>Default = 0<br>Note: If Control[1] =0, this bit is affected by Control[9:7]. |

| | |
|---|---|
| 12 | **Count Read Responses / Count Discards.**<br>• If Control[1] = 0 and this bit is set to 0, counting read response commands is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting read response commands is enabled. Any combination of Control[17:10] can be set, the count will be the total for all operations selected.<br>• If Control[1] = 1 and this bit is set to 0, counting discards is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting the amount of discarded data (0h to Fh) is enabled for every PCLK where prefetched data gets discarded.<br>Default = 0<br>Note: If Control[1] = 0, this bit is affected by Control[9:7]. |
| 11 | **Count Nonposted Writes / Count Chained Posts.**<br>• If Control[1] = 0 and this bit is set to 0, counting nonposted write or RMW commands is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting nonposted write or RMW commands is enabled. Any combination of Control[17:10] can be set, the count will be the total for all operations selected.<br>• If Control[1] = 1 and this bit is set to 0, counting chained posts is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting chained posts is enabled. The count is the number of packets (2, 3, or 4) chained together when a chained post transfers its first data on PCI/PCI-X®.<br>Default = 0<br>Note: If Control[1] = 0, this bit is affected by Control[9:7]. |
| 10 | **Count Posted Writes / Count Inbound Read Latency.**<br>• If Control[1] = 0 and this bit is set to 0, counting posted write commands is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting posted write commands is enabled. Any combination of Control[17:10] can be set, the count will be the total for all operations selected.<br>• If Control[1] = 1 and this bit is set to 0, counting inbound read latency is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting inbound read latency is enabled.<br>Default = 0<br>Note: If Control[1] = 0, this bit is affected by Control[9:7]. |
| 9 | **Count Data Words / Count Wait State PCLKs.**<br>• If Control[1] = 0 and this bit is set to 0, counting commands is enabled.<br>If Control[1] = 0 and this bit is set to 1, counting the data words associated with the commands selected in Control[17:10] is enabled.<br>• If Control[1] = 1 and this bit is set to 0, counting wait state PCLKs is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting wait state PCLKs is enabled.<br>Default = 0<br>Note: If Control[1] = 0, this bit affects Control[17:10]. |
| 8 | **Bridge Destination / Count Idle PCLKs.**<br>• If Control[1] = 0 and this bit is set to 0, counting operations whose destination is the GPI is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting operations whose destination is the GPI is enabled.<br>• If Control[1] = 1 and this bit is set to 0, counting idle PCLKs (no FRAME/IRDY/TRDY) is disabled.<br>If Control[1] = 1 and this bit is set to 1, counting idle PCLKs (no FRAME/IRDY/TRDY) is enabled.<br>Default = 0<br>Note: If Control[1] = 0, this bit affects Control[17:10]. |

| | |
|---|---|
| 7 | **Tunnel Destination.**<br>• If Control[1] = 0 and this bit is set to 0, counting operations whose destination is the far (other side of the chip) transmitter is disabled.<br>If Control[1] = 0 and this bit is set to 1, counting operations whose destination is the far (other side of the chip) transmitter is enabled.<br>• If Control[1] = 1, this bit is Reserved.<br>Default = 0<br>Note: If Control[1] = 0, this bit affects Control[17:10]. |
| 6 | **Count Clocks.**<br>• If this bit is set to 0, count information is determined by other Control bits.<br>• If this bit is set to 1, only the total number of clocks since the counter was cleared are counted. So, if this bit is 1 and<br>if Control[1] = 0, core clocks are counted.<br>if Control[1] = 1, PCI/PCI-X® bus A clocks are counted.<br>if Control[6] = 1, Control[30:7] are unused.<br>Default = 0 |
| 5 | **Assert Nonfatal Interrupt on Counter Overflow.**<br>• If this bit is set to 0, asserting a nonfatal interrupt on a counter overflow is disabled.<br>• If this bit is set to 1, asserting a nonfatal interrupt on a counter overflow is enabled.<br>Default = 0<br>Note: Overflow for the 32- or 36-bit counter is defined by Control[2]. |
| 4 | **Counter Port Select.** Port selects are as follows:<br>• If Control[1] = 0 and this bit is set to 0, HyperTransport™ link 0 is selected.<br>If Control[1] = 0 and this bit is set to 1, HyperTransport™ link 1 is selected.<br>• If Control[1] = 1 and this bit is set to 0, PCI/PCI-X® bus A is selected.<br>If Control[1] = 1 and this bit is set to 1, PCI/PCI-X® bus B is selected.<br>Default = 0 |
| 3 | **Counter Overflow.** Write 1 to clear.<br>• If this bit is 0, the counter has not wrapped.<br>• If this bit is 1, the counter has wrapped.<br>Default = 0<br>Note:<br>If the Counter Domain Select = 0, the count wraps to zero after FFFF_FFFFh and sets the overflow bit.<br>If the Counter Domain Select = 1, the count wraps to zero after F_FFFF_FFFFh and sets the overflow bit. |
| 2 | **Counter Domain Select.**<br>• If this bit is set to 0, the DevA:1x[A0,A4] Counter CSR displays counter bits[31:0]. The count wraps to zero after FFFF_FFFFh and sets the Control[3] counter overflow bit. A write to the Counter CSR writes bits [31:0] and always clears the Control[3] counter overflow bit.<br>• If this bit is set to 1, the DevA:1x[A0,A4] Counter CSR displays counter bits[35:4]. The count wraps to zero after F_FFFF_FFFFh and sets the Control[3] counter overflow bit. A write to the Counter CSR writes bits [35:4], sets bits [3:0] to zero, and always clears the Control[3] counter overflow bit.<br>Default = 0 |
| 1 | **Select PCI/PCI-X®.**<br>• If this bit is set to 0, the counter counts information from HyperTransport™ link 0 or link 1.<br>• If this bit is set to 1, the counter counts information from PCI/PCI-X® bus A or bus B.<br>Default = 0 |

| | |
|---|---|
| 0 | **Counter Enable.** Enables/disables for this bit differ for Control0 and Control1 as follows:<br>Control1[0] / Control0[0] / Counter1 / Counter0<br>0 / 0 / Disabled / Disabled<br>0 / 1 / Disabled / Enabled<br>1 / 0 / Disabled / Disabled<br>1 / 1 / Enabled / Enabled<br>Default = 0 |

# 3.6 IOAPIC Register Space

These registers are located in APIC[B,A]:XX memory space. The base address register for these registers is found at Dev[B,A]:1x48, and Dev[B,A]:1x10 if enabled.

- See section 3.1.2 for a description of the register naming convention.
- See section 1.3.2 for more details about interrupt operation.
- See Dev[B,A]:0x[BC,B8] for a description of alternative access to these registers and expanded programmability.
- See *82093AA I/O Advanced Programmable Interrupt Controller (IOAPIC) Product Data* for more information.

The IOAPIC register set supports 7 interrupts and corresponding redirection registers. The space is indexed through two memory-mapped ports:

- APIC[B,A]:00h (offset 00h of the address space indicated by Dev[B,A]:1x10/Dev[B,A]:1x48) provides the 8-bit index register.
- APIC[B,A]:10h (offset 10h of the address space indicated by Dev[B,A]:1x10/Dev[B,A]:1x48) provides the 32-bit data port. All accesses (reads or writes) to APIC registers must fit within a 32-bit aligned block.

Accesses that span multiple 32-bit blocks result in undefined behavior. Writes to APIC[B,A]:10h (the 32-bit data port) must be 32-bit aligned accesses, other than 32-bit writes result in undefined behavior. Reads provide all four bytes regardless of the byte enables.

Only bits 7:0 of APIC[B,A]:00 are used. The index written to APIC[B,A]:00 selects one from the following table.

| APIC[B,A]: 00[7:0] | Description | Default |
|---|---|---|
| 00h | **APIC ID Register.** Bits[31:24] are Read-Write; they control no hardware. All other bits are reserved. | 0000 0000h |
| 01h | **IOAPIC Version Register.**<br>Bits[31:24] are reserved.<br>Bits[23:16] Maximum Redirection Entry are Read Only. This field contains the entry number (0 being the lowest) of the highest entry in the I/O redirection table. The value is equal to one less than the number of redirection entries. This IOAPIC has 7 entries, so this value is 6h.<br>Bits [15:8] are reserved.<br>Bits [7:0] APIC Version are Read Only. The version number assigned to this IOAPIC is 11h. | 0006 0011h |
| 02h | **IOAPIC Arbitration ID Register.** Bits[31:24] are Read-Write; they control no hardware. All other bits are reserved. | 0000 0000h |
| 10h-1Dh | **RDR. Redirection Registers.** Each of the 7 redirection registers utilizes two indexes. Bits[63:32] are accessed through the odd indexes. Bits[31:0] are accessed through the even indexes. They are mapped to the interrupts as follows:<br>Pin — IO[B,A]00 for Bits[31:0] — IO[B,A]00 for Bits[63:32]<br>[B,A]_PIRQA_L — 10h — 11h<br>[B,A]_PIRQB_L — 12h — 13h<br>[B,A]_PIRQC_L — 14h — 15h<br>[B,A]_PIRQD_L — 16h — 17h<br>[B,A]_Fatal — 18h — 19h<br>[B,A]_Nonfatal — 1Ah — 1Bh<br>[B,A]_SHPC_INTR — 1Ch — 1Dh | Bits[63:32] = 0000 0000h<br>Bits[31:0] = 0001 0000h |
| 1Eh-FFh | Reserved. | |

**RDR.** Default: 0000 0000 0001 0000h. The redirection registers are defined as follows:

| Bits | Description |
|---|---|
| 63:56 | **Destination [DEST].** Read-Write. IntrInfo[15:8] in the HyperTransport™ link interrupt request packet.<br>• In physical mode, bits[59:56] specify the APIC ID of the target processor.<br>• In logical mode, bits[63:56] specify a set of processors. |
| 55:17 | Reserved. |
| 16 | **Interrupt Mask [IM].** Read-Write.<br>1 = Interrupt is masked.<br>• When the interrupt is specified to be in edge-sensitive mode and this bit transitions from 1 to 0, then no interrupt request is generated regardless of the state of the interrupt line.<br>• When the interrupt is specified to be in level-sensitive mode and the interrupt line is in the asserted state, then when this bit transitions from 1 to 0 an interrupt request is generated.<br>Note: The state of this bit is also used for the NIOAIRQ[D:A]_L pins; see Dev[B,A]:0x40[NIOAMODE]. |

| | |
|---|---|
| 15 | **Trigger Mode [TM].** Read-Write. IntrInfo[5] in the HyperTransport™ link interrupt request packet.<br>0 = Edge sensitive.<br>1 = Level sensitive.<br>Note: Normally, it is expected that this bit be programmed for level-sensitive interrupts. This bit is ignored for delivery modes of SMI, NMI, Init, and ExtINT, which are always treated as edge sensitive. |
| 14 | **Interrupt Request Receipt [IRR].** Read Only. This bit is not defined for edge-triggered interrupts. For level-triggered interrupts, this bit is set by the hardware after an interrupt is detected. It is cleared by receipt of EOI as specified in section 1.3.2. |
| 13 | **Polarity [POL].** Read-Write.<br>• If this is a 0, the interrupt is active high.<br>• If this is a 1, the interrupt is active low.<br>• For the RDRs associated with [B,A]PIRQ[D,C,B,A]_L this bit applies to the polarity of the [B,A]PIRQ[D,C,B,A]_L pins as they enter the AMD-8132 tunnel. Normally, this bit is expected to be programmed for active low interrupts. This bit has no effect on the NIOAIRQ[D,C,B,A]_L pins.<br>• For the RDRs associated with the fatal, nonfatal, and SHPC interrupts, this bit is reserved and always 0. These internal interrupts are always active high. |
| 12 | **Delivery Status [DS].** Read Only.<br>0 = Idle.<br>1 = Interrupt message pending. |
| 11 | **Destination Mode [DM].** Read-Write. IntrInfo[6] in the HyperTransport™ link interrupt request packet.<br>0 = Physical mode.<br>1 = Logical mode. |
| 10:8 | **Message Type [MT].** Read-Write. These bits are physically located in IDRDR[MT], see Dev[B,A]:0x[BC,B8]. Accesses to this field result in translated accesses to the register bits in IDRDR[MT]. The value in IDRDR[MT] becomes the IntrInfo[4:2] field in HyperTransport™ link interrupt request packets. The translation is as follows:<br><br>Access to RDR[MT] / Interrupt type / Value in IDRDR[MT]<br>000b / Fixed / 000b<br>001b / Lowest priority / 001b<br>010b / SMI / 010b<br>011b / Reserved / 111b<br>100b / NMI / 011b<br>101b / Init / 100b<br>110b / Reserved / 101b<br>111b / ExtINT / 110b<br>For example: a write of 111b to RDR[MT] results in a write of 110b in IDRDR[MT]. Subsequent reads of RDR[MT] provide 111b. Subsequent reads of IDRDR[MT] provide 110b. The value placed in link interrupt request packets is as specified in IDRDR[MT] (110b). A write of 110b in IDRDR[MT] would be read as 111b through RDR[MT]. |
| 7:0 | **Interrupt Vector [IV].** Read-Write. IntrInfo[23:16] in the HyperTransport™ link interrupt request packet. |

# 3.7 SHPC Working Registers

These registers are accessed through either indexed configuration space (see Dev[B,A]:0x90[SELECT] and Dev[B,A]:0x94[DATA]) or non-indexed memory space (see SHPC[B,A]:00). All accesses (reads or writes) to SHPC registers must fit within a 32-bit aligned block. Accesses that span multiple 32-bit blocks result in undefined behavior.

- If Dev[B,A]:0x48[HPEN] = 0 then the SHPC[B,A]:XX registers are all reserved.
- See section 3.1.2 for a description of the register naming convention.
- See the TPS* hot-plug power controller product data sheets for more information.

### SHPC Base Offset — SHPC[B,A]:00

Default: 0000 0000h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:0 | **BASE_OFFSET.** This register is hardwired low to indicate the memory space base address of the SHPC register set is specified only by Dev[B,A]:0x10[SHPCBAR]. |

### SHPC Slots Available I — SHPC[B,A]:04

Default: 0000 0000h — Attribute: Write Once

| Bits | Description |
|---|---|
| 31:29 | Reserved. |
| 28:24 | **N_133PCIX.** Indicates the maximum number of hot-plug slots available to be enabled when the bus is running at 133 MHz in PCI-X® mode. |
| 23:21 | Reserved. |
| 20:16 | **N_100PCIX.** Indicates the maximum number of hot-plug slots available to be enabled when the bus is running at 100 MHz in PCI-X mode. |
| 15:13 | Reserved. |
| 12:8 | **N_66PCIX.** Indicates the maximum number of hot-plug slots available to be enabled when the bus is running at 66 MHz in PCI-X mode. |
| 7:5 | Reserved. |
| 4:0 | **N_33CONV.** Indicates the maximum number of hot-plug slots available to be enabled when the bus is running at 33 MHz in conventional PCI mode. |

## SHPC Slots Available II — SHPC[B,A]:08

Default: 0000 0000h — Attribute: Write Once

| Bits | Description |
|---|---|
| 31:28 | Reserved. |
| 27:24 | Reserved. |
| 23:20 | Reserved. |
| 19:16 | **N_133PCIX266.** Indicates the maximum number of hot-plug slots to be enabled when the bus is running at 133 MHz PCI-X®2.0. If [B,A]:0x48[SHPC_PI_1] is 1, then the write-once value written to this register should be 0s. |
| 15:12 | **N_100PCIX266.** Indicates the maximum number of hot-plug slots to be enabled when the bus is running at 100 MHz PCI-X 2.0. If [B,A]:0x48[SHPC_PI_1] is 1, then the write-once value written to this register should be 0s. |
| 11:8 | **N_66PCIX266.** Indicates the maximum number of hot-plug slots to be enabled when the bus is running at 66 MHz PCI-X 2.0. If [B,A]:0x48[SHPC_PI_1] is 1, then the write-once value written to this register should be 0s. |
| 7:5 | Reserved. |
| 4:0 | **N_66CONV.** Indicates maximum number of hot-plug slots available to be enabled when the bus is running at 66 MHz in conventional PCI mode. |

## SHPC Slot Configuration — SHPC[B,A]:0C

Default: 0000 0000h — Attribute: Write Once

| Bits | Description |
|---|---|
| 31 | **Attention Button Implemented [ABI].**<br>0 = Hot-plug slots do not implement the attention button.<br>1 = Hot-plug slots implement the attention button. |
| 30 | **MRL Sensor Implemented [MRLSI].**<br>0 = Hot-plug slots do not implement the MRL sensor.<br>1 = Hot-plug slots implement the MRL sensor. |
| 29 | **Physical Slot Number Up/Down [PSN_UP].**<br>0 = Each external slot label decrements by 1 from the value in SHPC[B,A]:0C[PSN].<br>1 = Each external slot label increments by 1 from the value in SHPC[B,A]:0C[PSN]. |
| 28:27 | Reserved. |
| 26:16 | **Physical Slot Number [PSN].** Specifies the physical slot number of the device specified by SHPC[B,A]:0C[FDN]. |
| 15:13 | Reserved. |

| | |
|---|---|
| 12:8 | **First Device Number [FDN].** Specifies the device number assigned to the first hot-plug slot on the secondary bridge bus. |
| 7:5 | Reserved. |
| 4:0 | **Number Of Slots Implemented [NSI].** Specifies the number of hot-plug slots on the bridge. |

## SHPC Secondary Bus Configuration — SHPC[B,A]:10

Default: 0?00 0?00h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:24 | **SHPC Programming Interface.** Identifies the format of the SHPC working register set. The value read is 2 unless Dev[B,A]:0x48[SHPC_PI_1] = 1, in which case the value read is 1. |
| 23:9 | Reserved. |
| 8 | If Dev[B,A]:0x48[SHPC_PI_1] is a 0, this reads 1 indicating that this device supports Mode 1 ECC. If Dev[B,A]:0x48[SHPC_PI_1] is a 1, this is reserved and reads 0. |
| 7:4 | Reserved. |
| 3:0 | **MODE.** Indicates the current speed and mode at which the secondary bridge bus operates. MHz value below is the common clock. |

| Encoding | Speed MHz | Mode | Data Transfer Rate |
|---|---|---|---|
| 0000b | 33/25 | Conventional PCI | N/A |
| 0001b | 66/50 | Conventional PCI | N/A |
| 0010b | 66/50 | PCI-X® Mode 1 with parity | N/A |
| 0011b | 100 | PCI-X Mode 1 with parity | N/A |
| 0100b | 133 | PCI-X Mode 1 with parity | N/A |
| 0101b | 66/50 | PCI-X Mode 1 with ECC | N/A |
| 0110b | 100 | PCI-X Mode 1 with ECC | N/A |
| 0111b | 133 | PCI-X Mode 1 with ECCN/A | |
| 1000b | 66/50 | PCI-X Mode 2 ECC | DDR |
| 1001b | 100 | PCI-X Mode 2 ECC | DDR |
| 1010b | 133 | PCI-X Mode 2 ECCDDR | |
| 1011b | 66/50 | PCI-X Mode 2 ECC | QDR |
| 1100b | 100 | PCI-X Mode 2 ECCQDR | |
| 1101b | 133 | PCI-X Mode 2 ECC | QDR |

1011b through 1111b are Reserved.

Notes:
1. See Dev[B,A]:0x48[PSLOW] for nominal speed settings of 33 or 66 MHz running at 25 or 50 MHz.
2. If Dev[B,A];0x48[SHPC_PI_1] is a 1, modes 0101b through 1010b are not valid.

## SHPC Command and Status — SHPC[B,A]:14

For bits [19:16] of this register, the Controller Command Error Code field consists of SHPC[B,A]:14[INVSM_ERR, INVCMD_ERR, MRLO_ERR]. No bits or one bit of the Controller Command

Error Code field may be updated when SHPC[B,A]:16[BSY] transitions from 1 to 0, indicating command completion with an error. If a bit in the Controller Command Error Code field is set, then it remains set until the next 1 to 0 transition of BSY.

For bits [12:0] of this register, writes to SHPC[B,A]:14 are ignored if SHPC[B,A]:16[BSY] = 1.

Default: 0000h Attribute: See Below

| Bits | Description |
|---|---|
| 31:20 | Reserved. |
| 19 | **Invalid Speed/Mode [INVSM_ERR].** Read Only. This bit is set high when one of the following errors occurs:<br>• The target slot specified by SHPC[B,A]:14[TGT] is not capable of running at the current speed or mode when the Slot Operation/Enable command is issued.<br>• A slot on the bus is not capable of running at the current bus speed or mode when the Enable All Slots command is issued.<br>• An enabled slot on the bus segment is not capable of running at the requested bus speed or mode when the Set Bus Segment Speed/Mode command is issued.<br>• The Set Bus Segment Speed/Mode command is issued when the number of slots available at the requested bus speed or mode (specified by SHPC[B,A]:[08, 04]) is greater than zero and less than the number of slots enabled. |
| 18 | **Invalid SHPC Command [INVCMD_ERR].** Read Only. This bit is set high when one of the following errors occurs:<br>• A reserved command code is used.<br>• The target slot specified by SHPC[B,A]:14[TGT] is zero or is greater than the SHPC[B,A]:0C[NSI] for any Slot Operation command.<br>• The target slot specified by SHPC[B,A]:14[TGT] is greater than the number of slots available at the current bus speed or mode (specified by SHPC[B,A]:[08, 04]) when the Slot Operation/Enable command is issued.<br>• The target slot specified by SHPC[B,A]:14[TGT] is enabled when the Slot Operation/Power Only command is issued.<br>• One or more slots on the bus segment are already enabled when the Power Only All Slots or Enable All Slots command is issued.<br>• The Set Bus Segment Speed/Mode command is issued when SHPC[B,A]:[08, 04] indicate no slots are available at the requested speed or mode. |
| 17 | **MRL Open [MRLO_ERR].** Read Only.<br>1 = The MRL of the target slot specified by SHPC[B,A]:14[TGT] was open when the Slot Operation/ Power Only or Slot Operation/Enable command was issued. |
| 16 | **Controller Busy [BSY].** Read Only.<br>1 = An SHPC command (see SHPC[B,A]:14) is in progress. |
| 15:13 | Reserved. |
| 12:8 | **Target Slot [TGT].** Read-Write. Specifies the slot to which SHPC[B,A]:14[CMD] is applied for the Slot Operation command. |
| 7:0 | **SHPC Command Code [CMD].** Read-Write. Specifies the SHPC command to be executed; see Table 7. SHPC Command Codes. |

### Table 7. SHPC Command Codes

| Command Name | CMD[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Slot Operation | 0 | 0 | Attention Indicator | | Power Indicator | | Slot State | |
| Set Bus Segment Speed/Mode 1 | 0 | 1 | 0 | 0 | 0 | Bus Speed/Mode 1 | | |
| Power Only All Slots | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| Enable All Slots | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| Set Bus Segment Speed/ Mode 2 | 0 | 1 | 0 | 1 | Bus Speed Mode 2 | | | |

Decodings for SHPC command code fields are :
- Attention Indicator and Power Indicator specify LED states. 00b = No Change; 01b = On; 10b = Blink; 11b = Off.
- Slot State specifies the command to the slot. 00b = No Change; 01b = Power Only; 10b = Enable Slot; 11b = Disable Slot.
- Bus Speed/Mode 1 specifies the bridge speed and mode, as shown in Table 8.

### Table 8. Mode 1 Bus Speed Encodings

| Encoding | Speed MHz | Mode |
|---|---|---|
| 000b | 33/25 | Conventional PCI with parity |
| 001b | 66/50 | Conventional PCI with parity |
| 010b | 66 | PCI-X® Mode 1 with parity |
| 011b | 100 | PCI-X® Mode 1 with parity |
| 100b | 133 | PCI-X® Mode 1 with parity |

- Bus Speed/Mode 2 specifies the bridge speed, PCI-X mode, and ECC/parity mode, as shown in Table 9. MHz value in the following table is the common clock.
  If Dev[B,A]:0x48[SHPC_PI_1] is 0, Bus Speed/Mode 1 and Bus Speed/Mode 2 are valid.
  If Dev[B,A]:0x48[SHPC_PI_1] is 1, Bus Speed/Mode 1 commands are valid and Bus Speed/Mode 2 commnads are invalid.

### Table 9. Mode 2 Bus Speed Encodings

| Encoding | Speed MHz | PCI-X® Mode | Error Handling | Data Transfer Rate |
|---|---|---|---|---|
| 0000b | 33/25 | Conventional PCI | Parity | SDR |
| 0001b | 66/50 | Conventional PCI | Parity | SDR |
| 0010b | 66/50 | PCI-X® Mode 1 | Parity | SDR |
| 0011b | 100 | PCI-X® Mode 1 | Parity | SDR |
| 0100b | 133 | PCI-X® Mode 1 | Parity | SDR |
| 0101b | 66/50 | PCI-X® Mode 1 | ECC | SDR |

**Table 9. Mode 2 Bus Speed Encodings (Continued)**

| Encoding | Speed MHz | PCI-X® Mode | Error Handling | Data Transfer Rate |
|---|---|---|---|---|
| 0110b | 100 | PCI-X® Mode 1 | ECC | SDR |
| 0111b | 133 | PCI-X® Mode 1 | ECC | SDR |
| 1000b* | 66 | PCI-X® Mode 2 | ECC | DDR |
| 1001b | 100 | PCI-X® Mode 2 | ECC | DDR |
| 1010b | 133 | PCI-X® Mode 2 | ECC | DDR |
| 1011b* | 66 | PCI-X® Mode 2 | ECC | QDR |
| 1100b* | 100 | PCI-X® Mode 2 | ECC | QDR |
| 1101b* | 133 | PCI-X® Mode 2 | ECC | QDR |
| 1110b | Reserved | | | |
| 1111b | Reserved | | | |
| *Not supported. | | | | |

## SHPC Interrupt Locator — SHPC[B,A]:18

Default: 0000 0000h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:5 | Reserved. |
| 4:1 | **Slot Interrupt Pending [IP[4:1]].** Each bit *n* of this field corresponds to slot *n*.<br>1 = A slot status bit capable of generating interrupts is set and the corresponding interrupt mask is 0. Slot status bits capable of generating interrupts are SHPC[B,A]:[30, 2C, 28, 24][CPC_STS, IPF_STS, ABP_STS, MRLSC_STS, CPF_STS]. The corresponding interrupt masks are SHPC[B,A]:[30, 2C, 28, 24][CP_IM, IPF_IM, AB_IM, MRLS_IM, CPF_IM]. |
| 0 | **Command Complete Interrupt Pending [CC_IP].**<br>1 = SHPC[B,A]:20[CC_STS] is 1 and SHPC[B,A]:20[CC_IM] is 0. |

## SHPC SERR Locator — SHPC[B,A]:1C

Default: 0000 0000h — Attribute: Read Only

| Bits | Description |
|---|---|
| 31:5 | Reserved. |
| 4:1 | **Slot SERR Pending [SERRP[4:1]].** Each bit *n* of this field corresponds to slot *n*.<br>1 = A slot status bit capable of generating SERR is set and the corresponding SERR mask is 0. Slot status bits capable of generating SERR are SHPC[B,A]:[30, 2C, 28, 24][MRLSC_STS, CPF_STS]. The corresponding SERR masks are SHPC[B,A]:[30, 2C, 28, 24][MRLS_SERRM, CPF_SERRM]. |
| 0 | **Arbiter SERR Pending [A_SERRP].**<br>1 = SHPC[B,A]:20[ATOUT_STS] is 1 and SHPC[B,A]:20[A_SERRM] is 0. |

## SHPC SERR-INT — SHPC[B,A]:20

The SHPC interrupt shown below either generates an interrupt packet based on the SHPC_INTR IOAPIC entry, or asserts the signal [B,A]_PIRQA_L if the SHPC_INTR RDR[IM] is set and Dev[B,A]:0x04[INTDISABLE] is not set.

```
SHPC_WAKEUP = (SHPC[B,A]:18[IP] != 0000b)
            | ~SHPC[B,A]:20[CC_IM] & SHPC[B,A]:20[CC_STS];
```

The SHPC interrupt shown below is routed to the [B,A]_PIRQA_L pin.

```
SHPC_INTR = ~SHPC[B,A]:20[GIM] & SHPC_WAKEUP;
```

The SHPC system error shown below sets Dev[B,A]:0x1C[RSE] (also see Dev[B,A]:0x3C[SERREN]).

```
SHPC_SERR = ~SHPC[B,A]:20[GSERRM] &
          ( (SHPC[B,A]:1C[SERRP] != 0000b)
          | ~SHPC[B,A]:20[A_SERRM] & SHPC[B,A]:20[ATOUT_STS]);
```

Default: 0000 000Fh — Attribute: See Below

| Bits | Description |
|---|---|
| 31:18 | Reserved. |
| 17 | **Arbiter Timeout Status [ATOUT_STS].** Read. Set by hardware. Write 1 to clear. Set when an arbiter timeout is detected by the SHPC logic. The arbiter timeout occurs when the PCI bus is requested (from the internal arbiter) for a hot-plug operation and it is not granted for $2^{23}$ [B,A]_PCLK cycles. |
| 16 | **Command Completion Status [CC_STS].** Read. Set by hardware. Write 1 to clear. Set when an SHPC[B,A]:16[BSY] transition from 1 to 0 is detected. |
| 15:4 | Reserved. |
| 3 | **Arbiter SERR Mask [A_SERRM].** Read-Write.<br>1 = SERR indication for arbiter timeout is disabled. |
| 2 | **Command Complete Interrupt Mask [CC_IM].** Read-Write.<br>1 = SHPC interrupt generation for command completion is disabled. |

| | |
|---|---|
| 1 | **Global SERR Mask [GSERRM].** Read-Write.<br>1 = SERR indication is disabled. |
| 0 | **Global Interrupt Mask [GIM].** Read-Write.<br>1 = SHPC interrupt generation is disabled. |

## SHPC Logical Slot — SHPC[B,A]:[30,2C,28,24]

The offset for the SHPC LSR (Logical Slot Register) for slot 1 is 24h, for slot 2 is 28h, for slot 3 is 2Ch, and for slot 4 is 30h. The LSR is used instead of SHPC[B,A]:[30, 2C, 28, 24] in the description below. See SHPC[B,A]:20 for information about how these registers may affect interrupts, events, and system errors.

Default: 7F00 3F3Fh — Attribute: See Below

| Bits | Description |
|---|---|
| 31 | Reserved. |
| 30 | **Connected Power Fault SERR Mask [CPF_SERRM].** Read-Write.<br>0 = SERR generation is enabled when LSR[CPF_STS] is set.<br>1 = SERR generation is disabled when LSR[CPF_STS] is set. |
| 29 | **MRL Sensor SERR Mask [MRLS_SERRM].** Read-Write.<br>0 = SERR generation is enabled when LSR[MRLSC_STS] is set.<br>1 = SERR generation is disabled when LSR[MRLSC_STS] is set. |
| 28 | **Connected Power Fault Interrupt Mask [CPF_IM].** Read-Write.<br>0 = Interrupt generation is enabled when LSR[CPF_STS] is set.<br>1 = Interrupt generation is disabled when LSR[CPF_STS] is set. |
| 27 | **MRL Sensor Interrupt Mask [MRLS_IM].** Read-Write.<br>0 = Interrupt generation is enabled when LSR[MRLSC_STS] is set.<br>1 = Interrupt generation is disabled when LSR[MRLSC_STS] is set. |
| 26 | **Attention Button Interrupt Mask [AB_IM].** Read-Write.<br>0 = Interrupt generation is enabled when LSR[ABP_STS] is set.<br>1 = Interrupt generation is disabled when LSR[ABP_STS] is set. |
| 25 | **Isolate Power Fault Interrupt Mask [IPF_IM].** Read-Write.<br>0 = Interrupt generation is enabled when LSR[IPF_STS] is set.<br>1 = Interrupt generation is disabled when LSR[IPF_STS] is set. |
| 24 | **Card Presence Interrupt Mask [CP_IM].** Read-Write.<br>0 = Interrupt generation is enabled when LSR[CPC_STS] is set.<br>1 = Interrupt generation is disabled when LSR[CPC_STS] is set. |
| 23:21 | Reserved. |
| 20 | **Connected Power Fault Status [CPF_STS].** Read. Set by hardware. Write 1 to clear. Set when LSR[PF] changes from 0 to 1 while LSR[SS] = 10b (slot is enabled). |
| 19 | **MRL Sensor Change Status [MRLSC_STS].** Read. Set by hardware. Write 1 to clear. Set when LSR[MRLS] changes its value. |
| 18 | **Attention Button Press Status [ABP_STS].** Read. Set by hardware. Write 1 to clear. Set when LSR[AB] transitions from 0 to 1. |
| 17 | **Isolated Power Fault Status [IPF_STS].** Read. Set by hardware. Write 1 to clear. Set when LSR[PF] changes from 0 to 1 while LSR[SS] ! = 10b (slot is not in the enabled state). |

| | |
|---|---|
| 16 | **Card Presence Change Status [CPC_STS].** Read. Set by hardware. Write 1 to clear. Set when LSR[PRSNT1_2] field changes value. |
| 15 | Reserved. |
| 14:12 | **PCI-X® Capability [PCI-X_CAP].** Read-Only. Reflects the current PCI-X® capability of the add-in card. These bits are not valid if the slot is empty.<br>000b = Conventional PCI<br>001b = 66 MHz PCI-X Mode 1<br>010b = Reserved<br>011b = 133 MHz PCI-X Mode 1<br>100b = PCI-X Mode 2, 266 (DDR data transfer rate. Only valid if Dev[B,A]:0x48[SHPC_PI_1] is a 0.)<br>101b = PCI-X 2, 533 (QDR data transfer rate. Only valid if Dev[B,A]:0x48[SHPC_PI_1] is a 0.) |
| 11:10 | **PRSNT1_L/PRSNT2_L [PRSNT1_2].** Read-Only. Reflects the current debounced state of the PRSNT1_L and PRSNT2_L pins on the slot.<br>00b = Card present, 7.5 W<br>01b = Card present, 25 W<br>10b = Card present, 15 W<br>11b = Slot Empty |
| 9 | **66 MHz Capable [M66_CAP].** Read-Only. This bit is valid only when the slot is occupied and powered.<br>0 = Add-in card is capable of running at 33 MHz conventional mode only.<br>1 = Add-in card is capable of running at 66 MHz conventional mode. |
| 8 | **MRL Sensor [MRLS].** Read-Only. Reflects the current state of the debounced MRL sensor.<br>0 = MRL sensor is closed.<br>1 = MRL sensor is open. |
| 7 | **Attention Button [AB].** Read-Only. Reflects the current state of the debounced attention button.<br>0 = Attention button is released.<br>1 = Attention button is being pressed. |
| 6 | **Power Fault [PF].** Read-Only. Reflects the current state of the power fault latch in the slot power control circuitry. 1 = Power fault (isolated or connected) is detected. |
| 5:4 | **Attention Indicator State [AIS].** Read-Only. Reflects the current state of the attention indicator.<br>00b = Reserved<br>01b = On<br>10b = Blink<br>11b = Off |
| 3:2 | **Power Indicator State [PIS].** Read-Only. Reflects the current state of the power indicator.<br>00b = Reserved<br>01b = On<br>10b = Blink<br>11b = Off |
| 1:0 | **Slot State [SS].** Read-Only. Reflects the current state of the slot.<br>00b = Reserved<br>01b = Powered Only<br>10b = Enabled<br>11b = Disabled |

# Chapter 4 Clocks and Reset

## 4.1 Clocking

REFCLK_[H,L] is required to be running for the AMD-8132™ HyperTransport™ PCI-X®2.0 tunnel to operate. The AMD-8132 tunnel provides [B,A]_PCLK[4:0] as the clocks to the secondary bus devices.

### 4.1.1 Systemboard Requirements

The AMD-8132 tunnel provides:

- The PCI clocks for secondary bus devices, [B,A]_PCLK[4:0].
- A PLL feedback for itself, [B,A]_PLLCLKO to [B,A]_PLLCLKI.

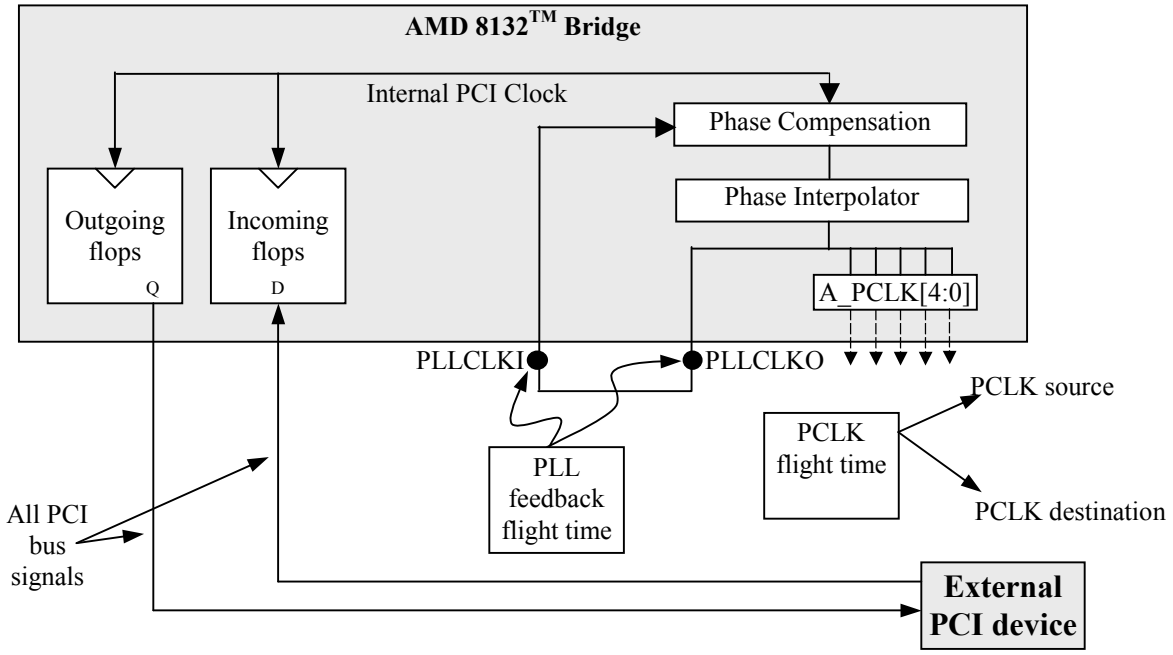
[B,A]_PLLCLKO and [B,A]_PCLK[4:0] run at the specified secondary bus frequency.

The systemboard is required to include a loopback connection from [B,A]_PLLCLKO to [B,A]_PLLCLKI. The length of this connection is required to be approximately the same as the length of the [B,A]_PCLK traces from the AMD-8132 tunnel to the external PCI devices so the flight time of the [B,A]_PCLK signals is the same as the flight time of the PLL feedback.

- The length of the connection from A_PLLCLKO to A_PLLCLKI should be the same as the length of the A_PCLK signals.
- The length of the connection from B_PLLCLKO to B_PLLCLKI should be the same as the length of the B_PCLK signals.

Flight time is defined as the time difference between the rising edge of the clock as observed at the source of the systemboard trace [B,A]_PLLCLKO and [B,A]_ PCLK at the AMD-8132 tunnel, and the rising edge of the clock as observed at the destination of the systemboard trace [B,A]_PLLCLKI at the AMD-8132 tunnel and [B, A]_PCLK at the external device, as shown in Figure 19. The AMD-8132 tunnel is so designed for the purposes of meeting AC timing requirements. If the PCLK flight time matches the PLL feedback flight time, then PCLK as observed at the destination is equivalent to the PCI-defined PCLK signal to the AMD-8132 tunnel. Accordingly, the PLL feedback flight time is required to be the same as any of the PCLK trace flight times (for a bridge), within the skew limits specified by the PCI specifications for PCLK to different devices: 2 ns for conventional PCI 33 MHz; 1 ns for conventional PCI 66 MHz; 0.5 ns for all PCI-X mode frequencies.

**Figure 19. Systemboard Clocking**




## 4.1.2 Clock Gating

Internal clocks may be disabled during power-managed system states such as power-on suspend. It is required that all upstream requests initiated by the AMD-8132 tunnel be suspended while in this state.

To enable clock gating, DevA:0xF0[ICGSMAF] is programmed to the values in which clock gating is enabled. STOP_GRANT cycles and STPCLK deassertion link broadcasts interact to define the window in which the AMD-8132 tunnel is enabled for clock gating during LDTSTOP_L assertions. The system is placed into power-managed states by steps that include a broadcast over the links of the STOP_GRANT cycle that includes the System Management Action Field (SMAF) followed by the assertion of LDTSTOP_L.

When the AMD-8132 tunnel detects the STOP_GRANT broadcast enabled for clock gating, it enables clock gating for the next assertion of LDTSTOP_L. While exiting the power-managed state, the system is required to broadcast a STPCLK deassertion message. The AMD-8132 tunnel uses this message to disable clock gating during LDTSTOP_L assertions. This is important because an LDTSTOP_L assertion is not guaranteed to occur after the STOP_GRANT broadcast is received. The clock gating window must be closed to insure that clock gating does not occur during STOP_GRANT for LDTSTOP_L assertions that are not associated with the power states specified by DevA:0xF0[ICGSMAF]. Only a single LDTSTOP_L assertion may occur during the window. So, to summarize:

STOP_GRANT broadcasts with SMAF fields specified by DevA:0xF0[ICGSMAF] enable the clock gating window and STPCLK deassertion broadcasts disable the window. If LDTSTOP_L is asserted while the clock gating window is enabled, then clock gating occurs.

It is expected that clock gating is only employed during power-on suspend. Therefore, OS and driver software insure that no DMA or interrupt activity occurs. In addition, it is required that there be no host accesses to the bridges or internal registers in progress from the time that LDTSTOP_L is asserted for clock gating until the link reconnects after LDTSTOP_L is deasserted.

# 4.2 Reset and Initialization

## 4.2.1 HyperTransport™ Reset And Initialization

LDTRESET_L and PWROK are both required to be low while power planes to the AMD-8132 tunnel are invalid and for at least 1 millisecond after the power planes are valid. Deassertion of PWROK is a cold reset. After PWROK is brought high, LDTRESET_L is required to stay low for at least 1 additional millisecond. After LDTRESET_L is brought high, the links go through the initialization sequence.

After a cold reset, the AMD-8132 tunnel can be reset by asserting LDTRESET_L while PWROK remains high. This is referred to as a warm reset. LDTRESET_L must be asserted for no less than 1 millisecond during a warm reset.

### 4.2.1.1 LDTREQ_L

LDTREQ_L is an open-drain signal, that can be driven active (low) by any device on the HyperTransport chain.

LDTREQ_L is asserted by the AMD-8132 tunnel whenever a transaction is in progress through it. If the internal arbiter is enabled, LDTREQ_L is also asserted by the AMD-8132 tunnel whenever it sees an active PCI request. If an external arbiter is used, it has the responsibility of asserting LDTREQ_L when a device requests the PCI bus.

### 4.2.1.2 LDTSTOP_L Link Re-Connect Sequence

The LDTSTOP_L signal is used to put the HyperTransport links into a power-down state. This signal can also be used while reprogramming HyperTransport link frequency and width.

Per *HyperTransport™ I/O Link Specification, Rev 2.0*, when LDTSTOP_L is deasserted it may not be detected by the AMD-8132 tunnel until the disconnect sequence is complete. If the disconnect sequence is already complete, then the deassertion of LDTSTOP_L is detected immediately. After the AMD-8132 tunnel detects deassertion of LDTSTOP_L, the following steps occur:

1. If the link transmit signals have been disabled (DevA:0x[C8:C4][LDT3SEN]), then they are enabled immediately and driven to the reset state (L[1,0]_CTLOUT_[H,L]0 deasserted; L[1,0]_CADOUT_[H,L][15:0] asserted).
2. There is a 1 microsecond pause.
3. If the link receive signals have been disabled (DevA:0x[C8:C4][LDT3SEN]), then they are enabled.
4. There is another 1 microsecond pause.
5. The AMD-8132 tunnel may assert L[1,0]_CTLOUT_[H,L]0 at this time. However, if there is a link frequency change, the AMD-8132 tunnel may pause to assure that internal PLLs are stable and then assert L[1,0]_CTLOUT_[H,L]0.

6. The AMD-8132 tunnel starts observing the state of L[1,0]_CTLIN_[H,L]0 and waits for it to assert before starting the next step.
7. Based on the state of DevA:0x[C8:C4][EXTCTL], the AMD-8132 tunnel holds L[1,0]_CTLOUT_[H,L]0 asserted for either a minimum of 16 additional bit times, or for approximately 50 additional microseconds.
8. The AMD-8132 tunnel then deasserts L[1,0]_CTLOUT_[H,L]0 and continues the initialization sequence per the link specification.

When DevA:0xCC[FREQ0] or DevA:0xD0[FREQ1] are changed, the new value for link frequency is not updated until either the start of a warm reset or the link is disconnected through LDTSTOP_L. The internal phase lock loops may need to re-lock as a result of these changes, which may require up to 100 microseconds to complete. Warm resets are required to last at least 1 millisecond, so this is not an issue. However, the link disconnect sequence may be much faster. Consequently, if FREQ0 or FREQ1 are changed prior to an assertion of LDTSTOP_L, then the AMD-8132 tunnel starts a 100 microsecond timer after the AMD-8132 tunnel is fully disconnected. If LDTSTOP_L is deasserted prior to the expiration of the 100 microsecond timer, then the AMD-8132 tunnel holds the links in the reset state (CTL deasserted; CAD asserted) until it expires.

## 4.2.2 PCI/PCI-X® Reset

The AMD-8132 tunnel supplies reset to the PCI/PCI-X buses [B,A]_RESET_L. These signals are asserted any time that LDTRESET_L is asserted and are also asserted if Dev[B,A]:0x3C[SBRST] is asserted, or if required by SHPC commands.

- For buses that are not capable of PCI-X Mode 2 operations, [B,A]_RESET_L is deasserted soon after the deassertion of LDTRESET_L.
- For buses capable of PCI-X Mode 2 operation, the deassertion of [B,A]_RESET_L may be delayed after a cold reset to allow the VIO voltage to stabilize. See section 7.1.4.

The PCI-X initialization pattern is driven onto the PCI/PCI-X bus while [B,A]_RESET_L is asserted.

## 4.2.3 Non-Hot-Plug Initialization

The operational mode (conventional PCI, or PCI-X); ECC or parity mode for PCI-X Mode 1; and frequency of the PCI-X bridges ([B,A]_PCLK[4:0]) are determined after a cold reset by
- the [B,A]_PCIXCAP signals,
- the [B,A]_M66EN signals, and
- by strapping resistors on [B,A]_GNT_L[4,1,0] (the A_ signals specify bridge A and the B_ signals specify bridge B).

For [B,A]_GNT_L[4,1,0]
- To select a 1, a pullup resistor to VDD33 is placed on the signal.
- To select a 0, a pulldown resistor to ground is placed on the signal.

The mode and frequency is determined while PWROK is low and held after PWROK is goes high. The options and associated selects are given in Table 10.

**Table 10. Non-Hot-Plug Operational Modes and Selects**

| GNT_L4 | GNT_L1 | GNT_L0 | PCIXCAP | M66EN | Mode | Frequency Supported | R/G/P |
|---|---|---|---|---|---|---|---|
| 1 | X | 1 | <.11 V33 | 0 | Conventional PCI | 33 MHz | [4:0] |

**Table 10. Non-Hot-Plug Operational Modes and Selects (Continued)**

| GNT_L4 | GNT_L1 | GNT_L0 | PCIXCAP | M66EN | Mode | Frequency Supported | R/G/P |
|---|---|---|---|---|---|---|---|
| 1 | X | 0 | <.11 V33 | 0 | Conventional PCI | 25 MHz | [4:0] |
| 1 | X | 1 | <.11 V33 | 1 | Conventional PCI | 66 MHz | [4:0] |
| 1 | X | 0 | <.11 V33 | 1 | Conventional PCI | 50 MHz | [4:0] |
| 1 | X | 1 | >=.11 V33, <.89 V33 | X | PCI-X® Mode 1 | 66 MHz | [4:0]** |
| 1 | X | 0 | >=.11 V33, <.89 V33 | X | PCI-X® Mode 1 | 50 MHz | [4:0]** |
| 1 | 1 | X | >=.89 V33 | X | PCI-X® Mode 1 | 100 MHz | [4:0]** |
| 1 | 0 | X | >=.89 V33 | X | PCI-X® Mode 1 | 133 MHz | [4:0]** |
| 0 | X | 1 | <.11 V33 | 0 | Conventional PCI | 33 MHz | [0] |
| 0 | X | 0 | <.11 V33 | 0 | Conventional PCI | 25 MHz | [0] |
| 0 | X | 1 | <.11 V33 | 1 | Conventional PCI | 66 MHz | [0] |
| 0 | X | 0 | <.11 V33 | 1 | Conventional PCI | 50 MHz | [0] |
| 0 | 1 | X | >=.11 V33, <.30 V33 | X | PCI-X® Mode 2 | 100 MHz | [0] |
| 0 | 0 | X | >=.11 V33, <.30 V33 | X | PCI-X® Mode 2 | 133 MHz | [0] |
| 0 | 1 | X | >=.30 V33, <.60 V33 | X | PCI-X® Mode 2 Double Data Rate | 100/200 MHz* | [0] |
| 0 | 0 | X | >=.30 V33, <.60 V33 | X | PCI-X® Mode 2 Double Data Rate | 133/266 MHz* | [0] |
| 0 | X | 1 | >=.60 V33, <.89 V33 | X | PCI-X® Mode 1 | 66.67 MHz | [0] |
| 0 | X | 0 | >=.60 V33, <.89 V33 | X | PCI-X® Mode 1 | 50 MHz | [0] |
| 0 | 1 | X | >.89 V33 | X | PCI-X® Mode 1 | 100 MHz | [0] |
| 0 | 0 | X | >.89 V33 | X | PCI-X® Mode 1 | 133 MHz | [0] |

**Notes:**

- *For dual entries (nn/nn MHz), the first value indicates the common clock frequency, the second value indicates the data transfer rate.
- **Only [4,1,0] are available in PCI-X Mode 1 with ECC.
- X means that the state does not matter to the AMD-8132 tunnel.
- The GNT_L[4,1,0] columns show the value latched by the AMD-8132 tunnel while PWROK is low.
- The Supported R/G/P column indicates the sets of REQ_L, GNT_L, and PCLK signals supported by the AMD-8132 tunnel bridge in that mode. There may be other constraints, such as electrical requirements, that further limit the number of external devices supported. For example, in PCI-X Mode 1 at 100 MHz, 5 slots will not work

electrically, but all 5 sets of REQ_L, GNT_L, and PCLK signals are available. In this case the motherboard design can choose from any of the 5 sets of signals, and BIOS should turn off the unused PCLK outputs.

- Up to 5 sets of REQ_L, GNT_L, and PCLK may be functionally active in PCI-X Mode 1. However, 5 slots are only supported electrically if in 33 MHz conventional PCI. If there are 5 slots, M66EN and PCIXCAP should be grounded on the systemboard to the slots so all PCI cards properly initialize.
- If a bridge from the AMD-8132 tunnel supports PCI-X Mode 2 operations, then there must be a single PCI/PCI-X slot. This slot must have the MODE2 pin asserted. SSS_L for this bridge must also be asserted (i.e., the AMD-8132 tunnel must know there is only one slot on this bus). IDSEL for this slot must be connected to [B,A]_GNT_L1 rather than to an AD line (PCI-X Mode 2 operation requires IDSEL lines to be distinct signals, not shared with AD signals). The power supply must be capable of providing 1.5 or 3.3 V to VIO[B,A] and must use [B,A]_REQ_L1 ([B,A]_VIOSEL) and [B,A]_PCLK[1] ([B,A]_VIOEN) to control the VIO[B,A] voltage. See section 7.1.4.
- The state of the straps is reflected in Dev[B,A]:0x60[SCF] and Dev[B,A]:0x40[CPCI66] after a cold reset.
- If the systemboard supports PCI-X mode operation for a bridge, then a pullup resistor to VDD33 must be placed on the bridge PCIXCAP pin. To limit the frequency of a PCI-X-capable bridge to 66 MHz on a systemboard, the systemboard must also include a pulldown resistor from the bridge PCIXCAP pin to ground and must not indicate there is a single slot present (i.e., SSS_L must not be asserted). The strapping options on GNT_L[1] are used to distinguish between systems that support 100MHz and 133 MHz. In either of these two cases, the systemboard should include no pulldown resistors on PCIXCAP.

### 4.2.4 Hot-Plug Initialization

Bridges in hot-plug mode are always placed into 33 MHz conventional PCI mode after LDTRESET_L is asserted. The operational speed and mode are then initialized by software through the following steps:

1. Initialization of Write Once registers in the SHPC[B,A]:XX register block.
2. Optional execution of Power Only All Slots SHPC command.
3. Acquisition of the capabilities and presence information for each slot by observing the RST_L, M66EN, PCIXCAP, PRSNT1_L, and PRSNT2_L signals.
4. Determination of the highest common bus frequency and mode that may be selected.
5. Execution of Set Bus Segment Speed/Mode SHPC command for the selected speed and mode.
6. Execution of Enable All Slots SHPC command.

This sequence is the same when hot-plug single-slot support is selected (Dev[B,A]:0x40[SSS_L]). However, all of the slot signals are forced low until the slot is powered.

# Chapter 5 Error Conditions and Handling

In general, for errors detected by the AMD-8132™ HyperTransport™ PCI-X®2.0 tunnel each detectable error condition sets one or more log bits that are persistent through warm reset and cleared by writing ones to them. The log bits are readable from software and may also be mapped to the various reporting methods listed in this chapter.

## 5.1 HyperTransport™ Interface Errors

### 5.1.1 Sync Flood

Once its link receivers are initialized, if the AMD-8132 tunnel detects sync flooding in either link receiver, it propagates sync flooding out its active transmitters. No enables are required. No logging is performed.

### 5.1.2 CRC Errors

HyperTransport CRC Errors are defined in *HyperTransport™ I/O Link Specification, Rev 2.0*, sections 10.1.1 and 10.1.2. When a CRC error is detected, logging of the error is delayed until L[1:0]_CTLIN for the associated link asserts. If LDT_RESET_L asserts before L[1:0]_CTLIN, the error status is lost. The error is logged by setting the appropriate DevA:0x[C4,C8][9:8] CRCERR bit, based on which link and byte lane detected the error.

The CRCERR bits for each link can be enabled to trigger sync flooding by setting the appropriate DevA:0x[C4,C8][1] CRCFEN bit. The CRCERR bits for both links can be enabled to trigger fatal or nonfatal interrupt assertion by setting the enables located at DevA:0xD4[22] or DevA:0xD4[30], respectively.

### 5.1.3 Protocol Errors

HyperTransport protocol errors are defined in *HyperTransport™ I/O Link Specification, Rev 2.0*, section 10.1.3. In addition to all the conditions listed in the released HyperTransport specification, the AMD-8132 tunnel also detects orphan address extension protocol errors, as defined in *HyperTransport™ I/O Link Errata, Rev 1.05c*.

As required by *HyperTransport™ I/O Link Specification, Rev 2.0*, logging of all protocol errors other than CTL timeout is delayed until L[1:0]_CTLIN for the associated link asserts. If LDT_RESET_L asserts before L[1:0]_CTLIN, the error status is lost. Expiration of the CTL timer results in immediate logging of a protocol error. The error is logged by setting the appropriate DevA:0x[CC,D0][12] Protocol Error bit. The duration of CTL timer is controlled by DevA:0x[CC,D0][15].

The protocol error bits can be enabled to trigger sync flooding by setting DevA:0xD4[16]. The protocol error bits can be enabled to trigger fatal or nonfatal interrupt assertion by setting DevA:0xD4[18] or DevA:0xD4[26] respectively.

With the exception of CTL deassertion during CRC, all protocol errors cause the receiver to lock up and process no more incoming packets from that link if sync flooding is enabled.

### 5.1.4 Receive Buffer Overflow Errors

HyperTransport receive buffer overflow errors are defined in *HyperTransport™ I/O Link Specification, Rev 2.0*, section 10.1.4. The error is logged by setting the appropriate DevA:0x[CC,D0][13] Overflow Error bit. The overflow error bits can be enabled to trigger sync flooding by setting DevA:0xD4[17]. The overflow error bits can also be enabled to trigger fatal or nonfatal interrupt assertion by setting DevA:0xD4[19] or DevA:0xD4[27] respectively. All overflow errors cause the receiver to lock up and process no more incoming packets from that link if sync flooding is enabled.

### 5.1.5 End of Chain (EOC) Errors

End of Chain (EOC) receive buffer overflow errors are defined in *HyperTransport™ I/O Link Specification, Rev 2.0*, section 10.1.5. If the AMD-8132 tunnel receives a packet from a HyperTransport link that the routing rules indicate is to be forwarded to the far link, but the far transmitter is unable to transmit it, the packet is handled as an end of chain packet and dropped. Reasons for the transmitter to drop a packet are:

- The DevA:0x[C4,C8][6] ENDOCH bit for that transmitter is set.
- The DevA:0x[C4,C8][5] INITCPLT bit for that transmitter is clear and DevA:0xC0[28] DOUI is set.
- The packet is a request with an extended address and DevA:0x[C4,C8][15] 64BEn for that transmitter is clear.

All other transmitter conditions that prevent transmission are assumed to be temporary and cause the packets to remain queued for transmission, rather than being dropped.

Other actions taken depend on the type of packet that was dropped:

- Broadcasts, and DIMs with the Silent Drop bit set, are dropped silently. No other action is taken.
- All other posted requests and responses cause the DevA:0x[CC,D0][14] End Of Chain Error bit associated with the transmitter to be set. The EOC error bits can be enabled to trigger fatal or nonfatal interrupt assertion by setting DevA:0xD4[20] or DevA:0xD4[28] respectively.
- Nonposted requests cause the appropriate type of response packet to be generated, with a master abort error status.

### 5.1.6 Atomic Read-Modify-Write Requests

The AMD-8132 tunnel does not support atomic read-modify requests as a target. If an atomic read-modify request is received that targets one of the PCI/PCI-X bridges, the request is dropped and a target abort response returned from that bridge. Read-modify-writes that do not target the AMD-8132 bridges are forwarded through the tunnel normally.

### 5.1.7 Illegal Configuration and I/O Accesses

The AMD-8132 tunnel only supports HyperTransport nonposted reads and writes to its configuration and I/O spaces. These nonposted reads and writes must fall within a 32-bit-aligned block. Posted accesses to configuration or I/O spaces owned by the AMD-8132 tunnel result in undefined behavior. Nonposted reads or writes of greater than 1 DW, or atomic read-modify writes, result in the request being dropped and returning a target abort response. Accesses of greater than 1 DW to memory-mapped registers through AMD-8132 tunnel BARs (APIC or SHPC) result in undefined behavior.

If a legal HyperTransport configuration access is received that targets extended configuration space above the bottom 256 bytes on the PCI/PCI-X bus, but that bus is not in PCI-X Mode 2, then that access is dropped. Logging and response generation are performed as if that request had been issued on the PCI/PCI-X bus and received a master abort.

## 5.1.8 Posted Write Data Errors

If the AMD-8132 tunnel receives a posted write request with the data error bit set that targets either of the PCI/PCI-X bridges, it sets the Dev[B,A]:0x04[31] Detected Parity Error bit in the Status CSR corresponding to that bridge. If the request targets the bus below the bridge (as opposed to an internal register) and the global DevA:0xDC[6] Downstream Post Data Error Disable bit is clear, the data issued on the destination bus is poisoned.

## 5.1.9 Response Match Errors

HyperTransport response match errors are defined in the *HyperTransport™ I/O Link Specification, Rev 2.0*, section 10.1.7. The AMD-8132 implements no checking for response match errors. If a response is received with a UnitId indicating that it belongs to one of the AMD-8132 bridges, but it does not match an outstanding request from that bridge (i.e: SrcTag, Rd/Write, or Count), the resulting behavior is undefined.

## 5.1.10 Error Responses

### 5.1.10.1 Master Aborts

When a master abort response is received from HyperTransport to one of the PCI/PCI-X bridges, the Dev[B,A]:0x04[29] Received Master Abort (RMA) bit is set in the Status CSR corresponding to that bridge. The Dev[B,A]:0x80[19] Primary Signalled Master Abort bit is set in the Misc Bridge Errors CSR:

- If Dev[B,A]:0x84[12] Primary Signalled Master Abort Fatal Enable is set, a fatal interrupt is asserted.
- If Dev[B,A]:0x84[13] Primary Signalled Master Abort Nonfatal Enable is set, a nonfatal interrupt is asserted.

If the secondary bus is in PCI mode, the completion status returned to the delayed request depends on the state of the Dev[B,A]:0x3C[21] Master Abort Response (MARSP) bit in the Bridge Control CSR.

- If MARSP is 0, the operation is allowed to complete normally on the PCI bus. Reads receive the data from the HyperTransport chain, which according to *HyperTransport™ I/O Link Specification, Rev 2.0* should be all 1s.
- If MARSP is 1, a target abort is returned on the PCI bus.

If the secondary bus is in PCI-X mode, a bridge split completion master abort error message is generated (Class 1, index 00).

- If Dev[B,A]:0x84[14] Received Secondary Master Abort Fatal Enable is set, a fatal interrupt is asserted.
- If Dev[B,A]:0x84[15] Received Secondary Master Abort Nonfatal Enable is set, a nonfatal interrupt is asserted.

### 5.1.10.2 Target Aborts

When a target abort response is received from HyperTransport to one of the PCI/PCI-X bridges, the Dev[B,A]:0x04[28] Received Target Abort (RTA) is set in the Status CSR corresponding to that bridge.

- If Dev[B,A]:0x84[8] Signalled Secondary Target Abort Fatal Enable is set, a fatal interrupt is asserted.
- If Dev[B,A]:0x84[9] Signalled Secondary Target Abort Nonfatal Enable is set, a nonfatal interrupt is asserted.

The target abort status is forwarded to the secondary bus. If the secondary bus is in PCI mode, this is done by generating a target abort on that bus. If the secondary bus is in PCI-X mode, a bridge split completion target abort error message is generated (Class 1, index 01).

- If Dev[B,A]:0x84[14] Received Secondary Master Abort Fatal Enable is set, a fatal interrupt is asserted.
- If Dev[B,A]:0x84[15] Received Secondary Master Abort Nonfatal Enable is set, a nonfatal interrupt is asserted.

### 5.1.10.3 Data Errors

When a data error response is received from HyperTransport to one of the PCI/PCI-X bridges, the Dev[B,A]:0x04[24] Master Data Uncorrectable Error (MDPE) bit in the Status CSR corresponding to that bridge is set if the Dev[B,A]:0x04[6] Parity Error Response (PERSP) bit for that bridge is set. Further action depends on the response type.

A RdResponse with data error sets the Dev[B,A]:0x04[31] Detected Parity Error (DPE) bit in the Status CSR corresponding to that bridge. The read data is poisoned when it is returned to the PCI/PCI-X bus.

A TgtDone with data error returns a data error indication on the secondary bus. If the secondary bus is in PCI mode, the data error is indicated by asserting PERR# when the delayed write is reissued by the master and allowed to complete. If the secondary bus is in PCI-X mode, the data error is indicated by issuing a bridge split completion uncorrectable write data error message (Class 1, index 02).

# 5.2 PCI/PCI-X® Interface Errors

## 5.2.1 SERR_L Assertion

Whenever the AMD-8132 tunnel detects the assertion of [B,A]_SERR_L by any device on the PCI/PCI-X bus, or detects [B,A]_SHPC_SERR, it sets the Dev[B,A]:0x1C[30] Received System Error (RSE) bit.

- RSE can be mapped to cause sync flooding by setting the Dev[B,A]:0x3C[17] System Error Enable (SERREN) bit in the Bridge Control CSR.
- RSE can be mapped to fatal/nonfatal error interrupt assertion by setting the Dev[B,A]:0x48[22,21] SERR Fatal/Nonfatal Enable bits.

## 5.2.2 Addressing Errors

### 5.2.2.1 Address/Byte Enable Mismatch

PCI-X MemRdDWORDs and PCI/PCI-X I/O reads and writes are required to have address bits [1:0] match the least-significant asserted byte enable in the request. When the AMD-8132 tunnel is the target of such a request, and the address and byte enables do not match, the AMD-8132 tunnel responds with an immediate target abort.

### 5.2.2.2 Bursts Across Address Range Boundaries

When the starting address of a PCI-X read burst indicates the AMD-8132 tunnel is the target, but the byte count carries the transaction across an address range boundary, the AMD-8132 tunnel splits the transaction and returns read data up to the boundary. It then issues a split completion error message of PCI-X Bridge Error (Class 1), Target Abort (index 01h). Write bursts in all modes and conventional PCI reads don't need to return errors for this case. They simply disconnect at the boundary, allowing the re-issued transaction to master abort if no other device responds. Range boundaries that are checked include:

- top of 64-bit memory address space;
- top of 40-bit memory address space (FD_0000_0000h);
- nonprefetchable memory base, if enabled (Dev[B,A]:0x[D8,20]);
- prefetchable memory base, if enabled (Dev[B,A]:0x[28,24]);
- base of VGA memory space, if enabled (A_0000h).

## 5.2.3 PERR_L Assertion

Whenever the AMD-8132 tunnel detects the assertion of [B,A]_PERR_L by any device on the PCI/PCI-X bus, including itself, it sets the Dev[B,A]:0x80[0] PERR_OBSERVED bit.

- PERR_OBSERVED can be mapped to cause sync flooding by setting the Dev[B,A]:0x48[20] PERR Flood Enable bit.
- PERR_OBSERVED can be mapped to fatal/nonfatal error interrupt assertion by setting the Dev[B,A]:0x48[19,18] PERR Fatal/Nonfatal Enable bits.

Additional action may be taken on [B,A]_PERR_L assertion if it was driven in response to data driven by the AMD-8132 tunnel. The specific action depends on which type of operation the AMD-8132 tunnel was driving, as described in the following subsections.

### 5.2.3.1 PERR_L Assertion on Posted Write Data

If [B,A]_PERR_L is asserted on posted write data from the AMD-8132 tunnel that the AMD-8132 tunnel did not intentionally poison, and the Dev[B,A]:0x3C[16] Uncorrectable Error Response Enable (PEREN) in the Bridge Control CSR is set, the AMD-8132 tunnel sets the Dev[B,A]:0x80[1] DISCARDED_POST bit in the Misc Bridge Errors CSR. If [B,A]_PERR_L is asserted for posted write data that the AMD-8132 tunnel put out poisoned, no additional action is taken.

If the Dev[B,A]:0x48[15] CLEARPCILOG_L bit is set, DISCARDED_POST only pulses high for a single cycle, rather than remaining high. DISCARDED_POST can be mapped to cause sync flooding by clearing Dev[B,A]:0x40[21] PciErrorSerrDisable, or to fatal/nonfatal interrupt assertion by setting Dev[B,A]:0x40[22,23] PciErrorFatalEn/PciErrorNonFatalEn.

#### 5.2.3.2 PERR_L Assertion on Nonposted Write Data

If [B,A]_PERR_L is asserted on nonposted write data from the AMD-8132 tunnel, it sets the Dev[B,A]:0x1C[24] Master Data Uncorrectable Error (MDPE) bit in the Secondary Status CSR if the Dev[B,A]:0x3C[16] Uncorrectable Error Response Enable (PEREN) bit in the Bridge Control CSR is set. When the TgtDone response is returned to HyperTransport, the AMD-8132 tunnel marks it as a data error response if the Dev[B,A]:0x04[6] Parity Error Response (PERSP) bit in the appropriate PCI-X Bridge Status and Command CSR is set, and the global DevA:0xDC[7] Upstream Response Data Error Disable bit is clear.

#### 5.2.3.3 PERR_L Assertion on Read or Split Completion Data

No additional action is taken if [B,A]_PERR_L is asserted on immediate read or split completion data from the AMD-8132 tunnel.

### 5.2.4 Parity/ECC Errors

Depending on bus mode, the AMD-8132 tunnel checks either parity or ECC on all address and attribute phases on the PCI/PCI-X bus and on all data for which it is the target.

In ECC modes, single-bit ECC errors are considered correctable if the secondary Dev[B,A]:0x70[30] Disable Single-Bit-Error Correction bit in the PCI-X ECC Error Control and Status CSR is clear. When a correctable error is detected, correction is performed and the secondary Dev[B,A]:0x70[7] ECC Error Corrected bit is set. The transaction then proceeds normally.

In parity modes, all parity errors are considered uncorrectable. In ECC modes, multi-bit ECC errors are uncorrectable, as are single bit errors if the disable single-bit-error correction bit is set. Detection of uncorrectable errors causes the Dev[B,A]:0x1C[31] Detected Uncorrectable Error (DPE) bit in the Bridge Control CSR to be set. Other actions are taken depending on the type of transaction and location of the error, as listed in the following uncorrectable error subsections.

In ECC modes, all correctable or uncorrectable ECC errors cause the following registers to be updated: Dev[B,A]:0x70[27:8,6:2] PCI-X ECC Control and Status, Dev[B,A]:0x[74,78] PCI-X ECC Addresses, and Dev[B,A]:0x7C PCI-X ECC Attribute.

#### 5.2.4.1 Address/Attribute Phase Uncorrectable Errors

If the AMD-8132 tunnel detects an uncorrectable error in the address or attribute phase of a PCI/PCI-X transaction, it sets the Dev[B,A]:0x80[3] ADDR_OR_ATTR_ERROR bit in the Misc. Bridge Errors CSR. Address decode is not affected by the error. The AMD-8132 tunnel asserts [B,A]_DEVSEL_L normally based on the address it received. However, it does not propagate the transaction to the HyperTransport chain; rather, it drops it and issues a target abort on the PCI/PCI-X bus.

If the Dev[B,A]:0x48[15] CLEARPCILOG_L bit is set, ADDR_OR_ATTR_ERROR only pulses high for a single cycle, rather than remaining high. The combination of ADDR_OR_ATTR_ERROR and Dev[B,A]:0x3C[16] Uncorrectable Error Response Enable (PEREN) in the Bridge Control CSR can be mapped to cause sync flooding by clearing Dev[B,A]:0x40[21] PciErrorSerrDisable, or to fatal/nonfatal interrupt assertion by setting Dev[B,A]:0x40[22,23] PciErrorFatalEn/PciErrorNonFatalEn.

### 5.2.4.2 Posted Write Data Phase Uncorrectable Errors

If the AMD-8132 tunnel detects an uncorrectable error in a data phase of a posted write for which it is the target, it forwards the data to HyperTransport normally but indicates a posted write data error on the packet containing the bad data beat. The AMD-8132 tunnel also asserts [B,A]_PERR_L for the bad beat if [B,A]_PERR_L is enabled.

### 5.2.4.3 Nonposted Write Data Phase Uncorrectable Errors

In conventional PCI mode, inbound nonposted writes are handled as delayed writes. That means data is latched when the master asserts [B,A]_IRDY_L, and the transaction retried (meaning [B,A]_TRDY_L is never asserted) until the operation completes on HyperTransport. Parity is checked on the incoming data at the time it is latched. If an error is detected, and the Dev[B,A]:0x3C[16] Uncorrectable Error Response Enable (PEREN) bit in the Bridge Control CSR is set, [B,A]_TRDY_L is asserted to complete the transaction; [B,A]_PERR_L is also asserted. No new request is queued for transmission to HyperTransport and no outstanding delayed transaction state is affected.

If no parity error is detected on the PCI nonposted write when the data is latched, then it is compared against outstanding delayed transactions. If it matches an outstanding transaction which has completed on the HyperTransport chain, the AMD-8132 tunnel asserts [B,A]_TRDY_L to complete the operation on the PCI bus. When [B,A]_TRDY_L and [B,A]_IRDY_L are both asserted, the parity is checked again. If a parity error is detected and PEREN is set, [B,A]_PERR_L is asserted.

In the PCI-X modes, inbound nonposted writes are handled as split writes. As in conventional PCI mode, the data is latched when [B,A]_IRDY_L is asserted by the master. Normally, the AMD-8132 tunnel would then signal a split response. However, if the latched data contains an uncorrectable error and PEREN is set, the AMD-8132 tunnel asserts [B,A]_TRDY_L to signal normal completion instead, followed by [B,A]_PERR_L.

### 5.2.4.4 Read Data Phase Uncorrectable Errors

The AMD-8132 tunnel handles data phase uncorrectable errors on read data returning to it the same, regardless of whether they are part of a conventional PCI read, PCI-X immediate completion, or PCI-X split completion. If the Dev[B,A]:0x3C[16] Uncorrectable Error Response Enable (PEREN) bit in the appropriate Bridge Control CSR is set, the AMD-8132 tunnel asserts [B,A]_PERR_L, and sets the Dev[B,A]:0x1C[24] Master Data Uncorrectable Error (MDPE) bit in the Secondary Status CSR. The read data is returned to the HyperTransport chain, but with a HyperTransport data error indicated in the response if the global DevA:0xDC[7] Upstream Response Data Error Disable bit is clear.

### 5.2.4.5 Split Completion Message Data Phase Uncorrectable Errors

When the AMD-8132 tunnel detects an uncorrectable error in the data phase of a split completion message targeting it, it sets the Dev[B,A]:0x80[3] SCM_PAR_ERR bit. If the Dev[B,A]:0x3C[16] Uncorrectable Error Response Enable (PEREN) bit in the Bridge Control CSR is set, it asserts [B,A]_PERR_L, sets the Dev[B,A]:0x1C[24] Master Data Uncorrectable Error (MDPE) bit in the Secondary Status CSR, and discards the split completion, generating no response on HyperTransport. This causes the HyperTransport requester to hang, waiting for a response.

If the Dev[B,A]:0x48[15] CLEARPCILOG_L bit is set, SCM_PAR_ERROR only pulses high for a single cycle, rather than remaining high. The combination of SCM_PAR_ERROR and Dev[B,A]:0x3C[16]

Uncorrectable Error Response Enable (PEREN) in the Bridge Control CSR can be mapped to cause sync flooding by clearing Dev[B,A]:0x40[21] PciErrorSerrDisable, or to fatal/nonfatal interrupt assertion by setting Dev[B,A]:0x40[22,23] PciErrorFatalEn/PciErrorNonFatalEn.

### 5.2.5 End of Chain Errors

PCI/PCI-X End of Chain errors occur when a request is received from the PCI/PCI-X bus, and the AMD-8132 tunnel address decode and routing controls are configured to accept that request and send it to a transmitter that is unable to take it, as described in section 5.1.5. In that case, the AMD-8132 tunnel does not assert [B,A]_DEVSEL_L, allowing the request to master abort on the PCI/PCI-X bus. No log bits are set.

### 5.2.6 PCI Discard Timeouts

When the secondary bus is in PCI mode, all inbound nonposted requests are handled as delayed requests. Each delayed request has a discard timer associated with it which starts running when the AMD-8132 tunnel has received a response from HyperTransport and is ready to return it to the PCI bus. The discard timer runs for either 1K or 32K PCI clock cycles, depending on the value of the Dev[B,A]:0x3C[25] Secondary Discard Timer (SDT) bit in the Bridge Control CSR. If the PCI master does not retry the transaction within that time, the contents of the delayed request buffer are flushed, and the Dev[B,A]:0x3C[26] Discard Timer Status [DTS] bit in the Bridge Control CSR is set.

DTS can be mapped to cause sync flooding if the Dev[B,A]:0x3C[27] Discard Timer Sync Flood Enable (DTSE) bit of the Bridge Control CSR is set, and Dev[B,A]:0x40[21] PciErrorSerrDisable is clear. DTS can be mapped to fatal/nonfatal interrupt assertion if DTSE is set, by setting PciErrorFatalEn/PciErrorNonFatalEn (Dev[B,A]:0x40[22,23]).

### 5.2.7 Master Aborts

If a master abort is received for a command issued onto the PCI/PCI-X bus by the AMD-8132 tunnel, the action taken depends on what the command was.

If the command was a posted request, the Dev[B,A]:0x1C[29] Received Master Abort (RMA) bit in the Secondary Status CSR is set. If Dev[B,A]:0x3C[21] Master Abort Response (MARSP) is set or if Dev[B,A]:0x84[16] Discarded Post Log Override is set, the AMD-8132 tunnel also sets the Dev[B,A]:0x80[1] DISCARDED_POST bit in the Misc Bridge Errors CSR. If the Dev[B,A]:0x48[15] CLEARPCILOG_L bit is set, DISCARDED_POST only pulses high for a single cycle, rather than remaining high.

If the command was either a read or write nonposted request, RMA is set. The response generated back to the HyperTransport chain depends on MARSP. If MARSP is 0, a normal response is generated with all 1s data for reads. If MARSP is 1, a target abort response is generated. The Dev[B,A]:0x1C[29] Received Master Abort bit is set:

- If Dev[B,A]:0x84[14] Received Secondary Master Abort Fatal Enable is set, a fatal interrupt is asserted.
- If Dev[B,A]:0x84[15] Received Secondary Master Abort Nonfatal Enable is set, a nonfatal interrupt is asserted.

If the command was a PCI-X split completion, the AMD-8132 tunnel sets the Dev[B,A]:0x60[18] Split Completion Discarded (SCD) bit in the PCI-X Secondary Status CSR. DISCARDED_POST and SCD can both

be mapped to cause sync flooding by clearing Dev[B,A]:0x40[21] PciErrorSerrDisable, or to fatal/nonfatal interrupt assertion by setting Dev[B,A]:0x40[22,23] PciErrorFatalEn/PciErrorNonFatalEn.

If HyperTransport requests to the AMD-8132 tunnel secondary PCI/PCI-X bus are received while that bus is in reset or the bus is disabled for a hot-plug event, the AMD-8132 tunnel responds as if the requests master aborted on the secondary bus. There is one exception: if the AMD-8132 tunnel secondary PCI/PCI-X bus is the system compatibility bus, the AMD-8132 tunnel stalls RdSized or WrSized requests that have the compat bit set until reset deasserts or the bus is re-enabled after a hot-plug event.

## 5.2.8 Target Aborts

If a target abort is received for a command issued onto the PCI/PCI-X bus by the AMD-8132 tunnel, the action taken depends on what the command was.

If the command was a posted request, the AMD-8132 tunnel sets the Dev[B,A]:0x1C[28] Received Target Abort (RTA) bit in the Secondary Status CSR, and the Dev[B,A]:0x80[1] DISCARDED_POST bit in the Misc Bridge Errors CSR. If the Dev[B,A]:0x48[15] CLEARPCILOG_L bit is set, DISCARDED_POST only pulses high for a single cycle, rather than remaining high.

If the command was either a read or write nonposted request, the AMD-8132 tunnel sets RTA and returns a target abort response of the proper type to the HyperTransport chain.

- If Dev[B,A]:0x84[6] Received Target Abort Fatal Enable is set, a fatal interrupt is asserted.
- If 0x84[7] Received Target Abort Nonfatal Enable is set, a nonfatal interrupt is asserted.

If the command was a PCI-X split completion, the AMD-8132 tunnel sets the Dev[B,A]:0x60[18] Split Completion Discarded (SCD) bit in the PCIX Secondary Status CSR.

DISCARDED_POST and SCD can both be mapped to cause sync flooding by clearing Dev[B,A]:0x40[21] PciErrorSerrDisable, or to fatal/nonfatal interrupt assertion by setting Dev[B,A]:0x40[22,23] PciErrorFatalEn/ PciErrorNonFatalEn.

## 5.2.9 Split Completion Error Messages

Split Completion Messages are used to return status without data to split nonposted requests. There are three defined classes of SCM:

- Class 0 - Normal Completion
- Class 1 - PCI-X Bridge Error
- Class 2 - Completer Error

Within each class, an 8-bit message index identifies the specific message.

Class 0 defines only a single message: Normal write completion (index 00h). This is only a legal completion for write requests.

Class 1 defines 3 messages: Master Abort (00h), Target Abort (01h), and Uncorrectable Write Data Error (02h). The AMD-8132 tunnel handles each of these as if it had received the specified status in an immediate response, in terms of both log bit setting and response generation to HyperTransport. Uncorrectable Write Data Error is handled as if the target had asserted PERR# on the data transfer; it is only a legal completion for write requests. In addition, split completion messages of Class 1 Target Abort set the Dev[B,A]:0x84 SCM_Class 1_TargetAbortError bit in the Misc Bridge Errors CSR.

- If Dev[B,A]:0x84[4] SCM_Class1_TargetAbortError_FatalEn is set, assert Fatal interrupt.

- If 0x84[5](SCM_Class1_TargetAbortError_NonFatalEn) is set, assert Nonfatal interrupt.

Class 2 also defines 3 messages: Byte Count out of Range (00h), Uncorrectable Split Write Data Error (01h) and Device-Specific Error (8Xh). Uncorrectable Split Write Data Errors are handled exactly like Class 1 Uncorrectable Write Data Errors, and again are only legal completions for write requests. All Class 2 indices other than 01h cause the Dev[B,A]:0x80[9] CLASS2_SCM_ERR bit in the Misc Bridge Errors CSR to set. If CLASS2_SCM_ERR wasn't already set, the Dev[B,A]:0x80[12:10,8:4] CLASS2_MSG_IDX field is also loaded. They return target aborts to HyperTransport.

- Byte Count Out of Range (00h) returns Target Abort TgtDone to HyperTransport (Err[1:0]=01); sets Signalled Target Abort bit in Status register; sets CLASS2_SCM_ERR and loads CLASS2_MSG_IDX; and sets Byte Count Out of Range Error in Misc Bridge Errors.
  - If 0x84[2](SCM_Class2_ByteCountOutOfRangeError_FatalEn) is set, assert Fatal interrupt.
  - If 0x84[3](SCM_Class2_ByteCountOutOfRangeError_NonFatalEn) is set, assert Nonfatal interrupt.
- Device-Specific Error (8xh) returns Target Abort TgtDone to HyperTransport (Err[1:0]=01); sets Signalled Target Abort bit in Status register; sets CLASS2_SCM_ERR and loads CLASS2_MSG_IDX; and sets Device-Specific Error in Misc Bridge Errors.
  - If 0x84[0](SCM_Class2_DeviceSpecificError_FatalEn) is set, assert Fatal interrupt.
  - If 0x84[1](SCM_Class2_DeviceSpecificError_NonFatalEn) is set, assert Nonfatal interrupt.

All undefined cases including undefined message class, undefined message index for a particular message class, write-specific message index returned to a read request, or read completion returned to a write request, result in target aborts being returned to HyperTransport. No additional logging is performed.

## 5.2.10 Unexpected Split Completions

The AMD-8132 tunnel does not assert DEVSEL# for PCI-X split completions containing its Device ID, unless the completion's tag matches a request which the AMD-8132 tunnel has outstanding. Requests to the AMD-8132 tunnel Device ID which do not match any outstanding request tags are expected to master abort. However, no other checking is performed. A split completion to the AMD-8132 tunnel Device ID with a matching tag but of a type that doesn't match the original request, or with a non-matching byte count, results in undefined behavior.

## 5.2.11 PCI/PCI-X® Busy Time Out

If the PCI/PCI-X bus is not idle (FRAME# or IRDY# is asserted) for 4095 consecutive PCI/PCI-X bus clocks with no data transferred, then the PCI Busy Timeout Error bit in Misc Bridge Errors register will be set.

- If 0x84[10](PciBusyTimeoutError_FatalEn) is set, assert Fatal interrupt.
- If 0x84[11](PciBusyTimeoutError_NonFatalEn) is set, assert Nonfatal interrupt.

# 5.3 AMD-8132™ Tunnel Error Signaling Methods

## 5.3.1 HyperTransport™ Interface

### 5.3.1.1 Sync Flood

Assuming both transmitters are active, the AMD-8132 tunnel always sync floods out both transmitters simultaneously. Sync flood initiation is enabled by the Dev[B,A]:0x04[8] SERR Enable bit in the PCI-X Bridge Status and Command CSR associated with the bridge the error came from. Sync floods caused by errors detected by the HyperTransport tunnel are always associated with bridge A. The AMD-8132 tunnel sets the Dev[B,A]:0x04[30] Signalled System Error bit in the same register when initiating sync flooding.

Sync flood propagation requires no enables and sets no log bits.

### 5.3.1.2 Posted Write Data Errors

The AMD-8132 tunnel signals a posted write data error by setting the Data Error bit in the posted WrSized packet. It also logs this fact by setting the Dev[B,A]:0x04[24] Master Data Uncorrectable Error (MDPE) bit in the PCI-X Bridge Status and Command CSR corresponding to the bridge the posted write came from, if the Dev[B,A]:0x04[6] Parity Error Response (PERSP) bit in the same register is set.

### 5.3.1.3 Error Responses

- **Master Abort.** The AMD-8132 tunnel indicates a master abort in a HyperTransport response by setting Error[1:0] in the response to 11b. The response packets carry the UnitId of PCI-X bridge A.
- **Target Abort.** The AMD-8132 tunnel indicates a target abort in a HyperTransport response by setting Error[1:0] in the response to 01b. Whenever a target abort response is issued, the Dev[B,A]:0x04[27] Signalled Target Abort bit (STA) in the appropriate PCI-X Bridge Status and Command CSR is set.
- **Data Error.** The AMD-8132 tunnel indicates a data error in a HyperTransport response by setting Error[1:0] in the response to 10b. The ability to issue response data errors can be globally disabled by setting the DevA:0xDC[7] Upstream Response Data Error Disable bit in the Tunnel Control CSR.

## 5.3.2 Fatal/Nonfatal Interrupts

For each bridge, the AMD-8132 tunnel has two logical interrupts: fatal and nonfatal. These interrupts can be used to indicate error conditions detected by that bridge. Error conditions detected by the tunnel are always associated with bridge A. Once a fatal or nonfatal interrupt is asserted, it remains asserted until software clears either the log or enable bits generating it.

Logical fatal and nonfatal interrupts can be mapped to HyperTransport interrupt packets through the interrupt redirection registers (RDRs) assigned to each (see section 3.6). If the Interrupt Mask (IM) bit in the RDR is set, indicating that no interrupt packet will be sent for that interrupt, the interrupts are mapped to pins. Fatal interrupt is asserted on [B,A]_PIRQB_L, and nonfatal interrupt on [B,A]_PIRQC_L. Assertion of interrupts on these pins can be blocked by setting the Dev[B,A]:0x04[10] Interrupt Disable (INTDISABLE) bit in the PCI-X Bridge Status and Command CSR. Assertions of the interrupt pins due to fatal/nonfatal interrupts are treated the same as assertions of those pins from external devices; they may result in HyperTransport interrupt packet

generation through the PIRQB/PIRQC RDRs, NIOAIRQB_L/NIOAIRQC_L assertion, or a HyperTransport INTx Virtual Wire Message packet.

## 5.3.3 PCI/PCI-X® Interface

### 5.3.3.1 PERR# Assertion

Assertion of PERR# by the AMD-8132 tunnel is enabled by Dev[B,A]:0x3C[16] Uncorrectable Error Response Enable (PEREN) in the appropriate Bridge Control CSR. This assertion always causes the Dev[B,A]:0x80[0] PERR_OBSERVED bit to be set, which may result in other actions.

### 5.3.3.2 Target Aborts

Whenever the AMD-8132 tunnel signals a target abort on a PCI/PCI-X bus, it sets the Dev[B,A]:0x1C[27] Signalled Target Abort (STA) bit in the appropriate Secondary Status CSR.

### 5.3.3.3 Split Completion Error Messages

The AMD-8132 tunnel is capable of generating one class of split completion error message: PCI-X Bridge Errors (Class 1). It is capable of generating all three message types: Master Abort, Target Abort, and Uncorrectable Write Data Error. When the AMD-8132 tunnel issues a Target Abort message, it sets the Dev[B,A]:0x1C[27] Signalled Target Abort (STA) bit in the appropriate Secondary Status CSR.

### 5.3.3.4 Data Poisoning

Based on bus mode and data width, the AMD-8132 tunnel is capable of appropriately poisoning data it returns to the PCI/PCI-X bus by driving bad parity or ECC as follows:

- Parity, 32-bit: force bad PAR value on all data beats.
- Parity, 64-bit: force bad PAR, PAR64 values on all data beats.
- ECC, 32-bit: 7-bit ECC w/PEL inserted on all beats. For more about PEL, see *PCI-X Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a*.
- ECC, 64-bit: 8-bit ECC w/PED inserted on all beats. For more about PED, see *PCI-X Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a*.

# Chapter 6 Test

Test modes and their encodings for the AMD-8132™ HyperTransport™ PCI-X®2.0 tunnel are given in Table 11.

**Table 11. TMODE[2:0] Encodings**

| Mode | Test | TMODE[2:0] | | |
|---|---|---|---|---|
| | | NIOAIRQD_L | A_PIRQC_L | A_REQ_L0 |
| Functional | 0 | x | x | x |
| Power-Down Mode | 1 | 0 | 0 | 0 |

## 6.1 Power-Down Mode

In power-down mode, all outputs of the AMD-8132 tunnel are placed in their high-impedance state. All input receivers are turned off. All analog circuitry (such as PLLs and phase interpolaters) is turned off.

**Note:** There is also a JTAG command that allows all outputs to be placed in their high impedance state, but which does not turn off input receivers and analog logic.

## 6.2 JTAG

The AMD-8132 tunnel supports JTAG using a standard JTAG port. While in JTAG mode, TEST and STRAPL[1:0] must be low. The PCI-X category 1 signals always have PCI-X Mode 1 electrical characteristics and the VIO voltage level supplied to the AMD-8132 tunnel must be 3.3 volts.

JTAG is controlled by the standard JTAG signals as defined in IEEE 1149.1. TCK is the clock, TRST_L is the reset, TMS is the mode select, TDI is the data input, and TDO is the data output.

There are 5 instructions supported by the AMD-8132 tunnel:

1. BYPASS. Default mode entered any time TRST_L is asserted. In this mode the TDI input is passed to the TDO output with a one-cycle register delay. This allows multiple components to be daisy chained on one JTAG chain.
2. IDCODE. Read the device ID code associated with the AMD-8132 tunnel.
3. HIGHZ. Other than TDO, all outputs of the AMD-8132 tunnel are in the high-impedance state.
4. SAMPLE/PRELOAD. Allows the state of all inputs to the AMD-8132 tunnel to be sampled in the boundary-scan register cells and then read by scanning out the JTAG boundary-scan chain. This mode also allows new values to be scanned into the boundary scan chain for subsequent use by the EXTEST instruction.
5. EXTEST. Drives the outputs of the AMD-8132 tunnel with the values that had previously been scanned into the boundary scan registers (using the SAMPLE/PRELOAD instruction).

# Chapter 7 Electrical Data

## 7.1 Power Requirements

### 7.1.1 Absolute Ratings

The AMD-8132™ HyperTransport™ PCI-X®2.0 tunnel is not designed to operate beyond the parameters shown in the following tables.

**Table 12. Absolute Maximum Ratings**

| Power Plane | Minimum | Maximum | Comments |
|---|---|---|---|
| VDD | -0.5 V | 1.6 V | |
| V33 | -0.5 V | 3.6 V | |
| VIO[B,A] Mode 1 (3.3V) | -0.5 V | 3.6 V | |
| VIO[B,A] Mode 2 (1.5V) | -0.5 V | 1.8 V | |
| VLDT | -0.5 V | 1.7 V | |
| PLL_VDDA[1:2] | -0.5 V | 3.6 V | |

**Table 13. Temperature**

| Temperature | Minimum | Maximum | Comments |
|---|---|---|---|
| $T_{CASE}$ | | 85 C | Operating range with heatsink. |
| $T_{STORAGE}$ | -65 C | 150 C | |

### 7.1.2 Operating Ranges

The AMD-8132 tunnel is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in the following table.

**Table 14. Operating Ranges**

| Parameter | Minimum | Typical | Maximum | Units | Comments |
|---|---|---|---|---|---|
| VDD | 1.14 | 1.2 | 1.26 | V | |
| V33 | 3.135 | 3.3 | 3.465 | V | |
| VIO[B,A] Mode 1 | 3.135 | 3.3 | 3.465 | V | 3.3 V |
| VIO[B,A] Mode 2 | 1.425 | 1.5 | 1.575 | V | 1.5 V |

**Table 14. Operating Ranges (Continued)**

| Parameter | Minimum | Typical | Maximum | Units | Comments |
|---|---|---|---|---|---|
| VIO[B,A] Mode 2 | | | TBD | mV | 1.5 V. Maximum sinusoidal amplitude at frequency range from 50 KHz to 20 MHz. |
| VLDT | 1.14 | 1.2 | 1.26 | V | |
| PLL_VDDA[1:2] | 3.0 | 3.3 | 3.6 | | |
| PLL_VDDA[1:2] Peak-To-Peak | | | 25 | mV | Maximum sinusoidal amplitude at frequency range from 50 KHz to 20 MHz. |

## 7.1.3 Current and Power Consumption

**Table 15. DC Current and Power Consumption**

| Power Plane | Max Current | Max Power |
|---|---|---|
| PLL_VDDA1 (3.3 V) | 6 mA | 20 mW |
| PLL_VDDA2 (3.3 V) | 12 mA | 40 mW |
| V33 (3.3 V) | 500 mA | 1650 mW |
| VDD (1.2 V) | 1100 mA | 1320 mW |
| VIOA<br>• Conventional PCI or PCI-X Mode 1 (3.3 V)<br>• PCI-X Mode 2 (1.5 V) | <br>550 mA<br>1250 mA | <br>1815 mW<br>1875 mW |
| VIOB<br>• Conventional PCI or PCI-X Mode 1 (3.3 V)<br>• PCI-X Mode 2 (1.5 V) | <br>550 mA<br>1250 mA | <br>1815 mW<br>1875 mW |
| VLDT (1.2 V) | 1100 mA | 1320 mW |

Maximum Total Power at nominal supply voltages: 8100 mW

## 7.1.4 Power Plane Sequencing

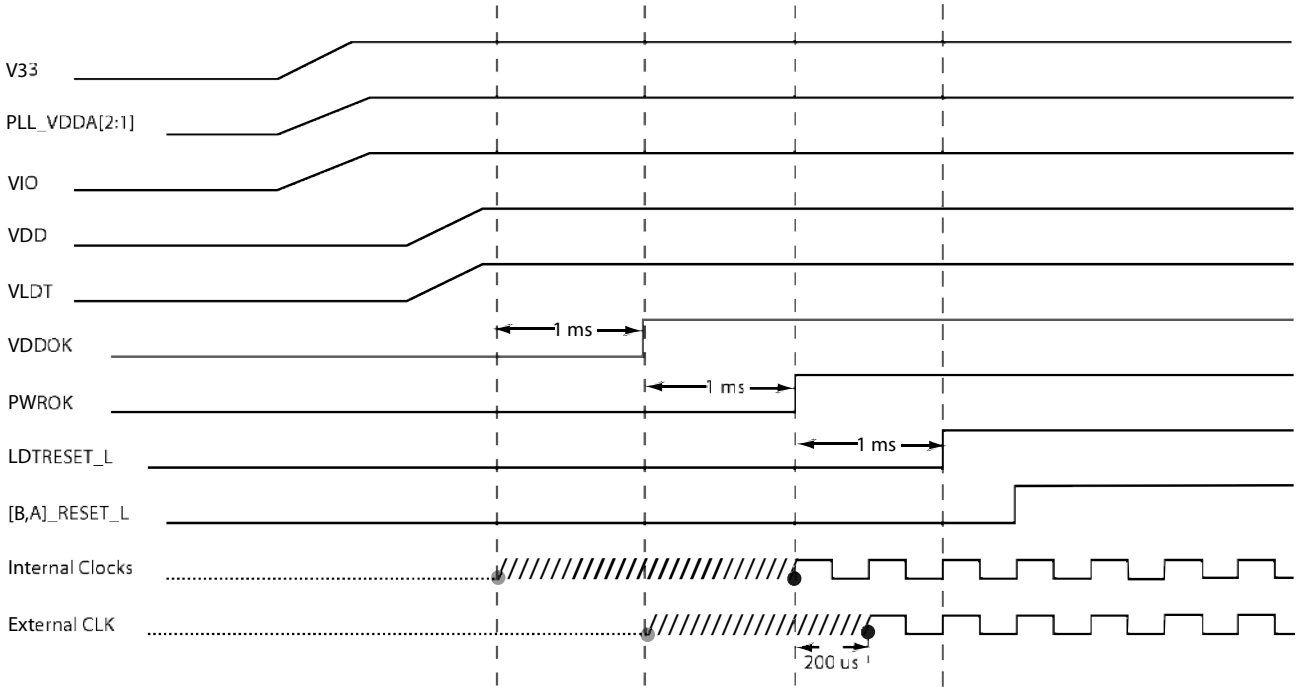
The power planes must be sequenced as follows

1. PLL_VDDA[1:2] can ramp up at the same time as V33, or may be lagged behind by up to 100 milliseconds.
2. VLDT must always be less than V33.
3. VDD must always be less than V33. This power plane can be ramped up simultaneously with VLDT.
4. VDDOK must be deasserted until VDD and VLDT reach their nominal voltage levels.

5. VIO[B,A] must never be above 1.5 volts when the relevant PCI bus is in PCI-X Mode 2. These are hot-plug voltages and may ramp up and down during the appropriate hot-plug initialization/reset sequences. Care must be taken to ensure the plane never switches directly from 3.3 to 1.5 volts as the component can be damaged in the time it takes for the voltage to ramp down.
   - For hot-plug systems capable of running in PCI-X Mode 2, this is accomplished by the TPS2342 using the 5V3VGA/B, VIOGA/B, and/or 15VGA/B signals.
   - For non hot-plug systems capable of running in PCI-X Mode 2, this is accomplished by the two pins [B,A]_VIOSEL, alternate function of [B,A]_REQ_L1, and [B,A]_VIOEN, alternate function of [B,A]_PCLK[1]. The VIO[B,A] power plane should not be powered up until [B,A]_VIOEN is asserted. When the AMD-8132 tunnel is first powered up, [B,A]_VIOEN remains de-asserted until the rising edge of PWROK. At the rising edge of PWROK, the AMD-8132 tunnel determines the operating mode of the PCI buses and drives [B,A]_VIOSEL accordingly. Thereafter, [B,A]_VIOEN is asserted. To ensure that the VIO[B,A] has stabilized, the AMD-8132 tunnel then waits an additional 100 milliseconds before de-asserting [B,A]_RESET_L. This 100 millisecond delay only occurs for buses capable of running in PCI-X Mode 2 and can be overridden at any point by asserting VIO[B,A]_OVERRIDE_DELAY (alternate function of [B,A]_PCLK[4]). VIO[B,A]_OVERRIDE_DELAY should only be asserted if VIO[B,A] is known to be stable. In systems that are not capable of running in PCI-X Mode 2, VIO[B,A] can be ramped to 3.3 volts simultaneously with V33.

The following figures are examples of legal power plane sequencing: Figure 20 for a system that is not Mode 2 capable; Figure 21 for a Mode 2 capable system.

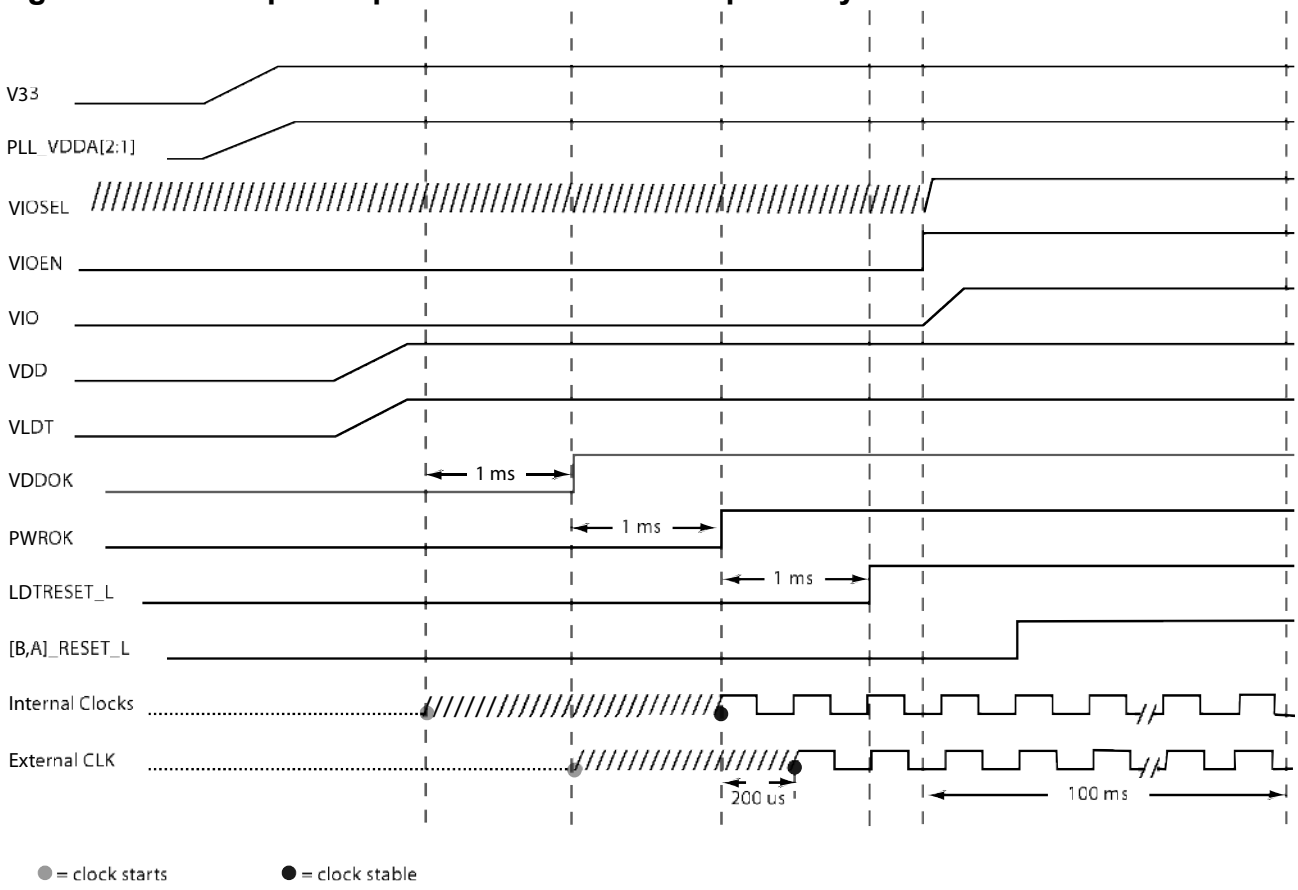
## Figure 20. Example Sequence for A Not Mode 2 Capable System




● = clock starts ● = clock stable

Notes:
1. V33, PLL_VDDA[2:1], VIO, VDD, and VLDT are power plane signals.
2. VDDOK, PWROK, and LDTRESET_L are input signals.
3. [B,A]_RESET_L and the internal/external clocks are output signals.

**Figure 21. Example Sequence for A Mode 2 Capable System**




Notes:
1. V33, PLL_VDDA[2:1], VIO, VDD, and VLDT are power plane signals.
2. VDDOK, PWROK, and LDTRESET_L are input signals.
3. [B,A]_RESET_L, VIOSEL, VIOEN, and the internal/external clocks are output signals.

# 7.2 Input Requirements for REFCLK_[H,L]

## 7.2.1 REFCLK_[H,L]: DC Requirements

**Table 16. REFCLK_[H,L] DC Requirements**

| Symbol | Description | Minimum | Maximum | Units |
|---|---|---|---|---|
| $V_{IH}$ | REFCLK_[H,L] input voltage high. | 0.2 | 0.4 | V |
| $V_{IL}$ | REFCLK_[H,L] input voltage low. | -0.4 | -0.2 | V |

## 7.2.2 REFCLK_[H,L]: AC Requirements

**Table 17. REFCLK_[H,L] AC Requirements**

| Symbol | Description | Minimum | Maximum | Units |
|---|---|---|---|---|
| $F_{REF}$ | REFCLK_[H,L] frequency. | 150 | 200 | MHz |
| $T_{RF}$ | REFCLK_[H,L] rise/fall slew rate. | 2.0 | 10.0 | V/ns |
| $V_{DIFF}$ | Differential voltage measured (single-ended) at the clock test load. | 0.4 | 0.8 | V |
| $V_{\triangle DIFF}$ | Change in differential voltage measured (single-ended) at the clock test load. | -0.05 | 0.05 | V |
| $V_{DIFF}$ Peak-To-Peak | Peak to peak differential. | 0.8 | 1.6 | V |
| $V_{CM}$ | Common mode voltage, measured at the clock test load. | -0.05 | 0.05 | V |
| $V_{\triangle CM}$ | Change in common mode voltage measured at the clock test load. | -0.05 | 0.05 | V |
| $F_{SPREAD}$ | REFCLK_[H,L] spread spectrum frequency change from FREF. | 0 | -0.5 | % |
| $T_D$ | REFCLK_[H,L] duty cycle. | 45 | 55 | % |
| $T_{CJ}$ | REFCLK_[H,L] cycle to cycle jitter. The difference in the period of any two adjacent REFCLK_[H,L] cycles. | 0 | 200 | ps |
| $T_{AJ}$ | REFCLK_[H,L] accumulated jitter. The difference between the clock edge and an ideal clock at the same frequency. | -1000 | 1000 | ps |
| $T_{FS}$ | Frequency stabilization from power-up (cold start). | 0 | 3 | ms |
| $R_{ON}$ | Output impedance differential. | 90 | 110 | ohms |

## 7.2.3 Differential Clock Test Load

A REFCLK_[H,L] clock source that meets the AMD-8132 tunnel signal requirements listed in Table 17 can be characterized using the differential test load shown in Figure 22. The single-ended measurement definitions are shown in Figure 23.

**Figure 22. Differential Test Load**

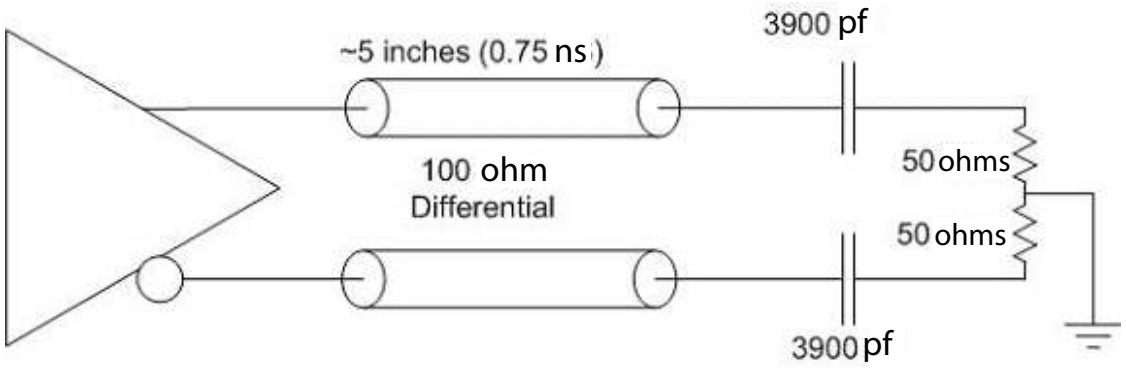
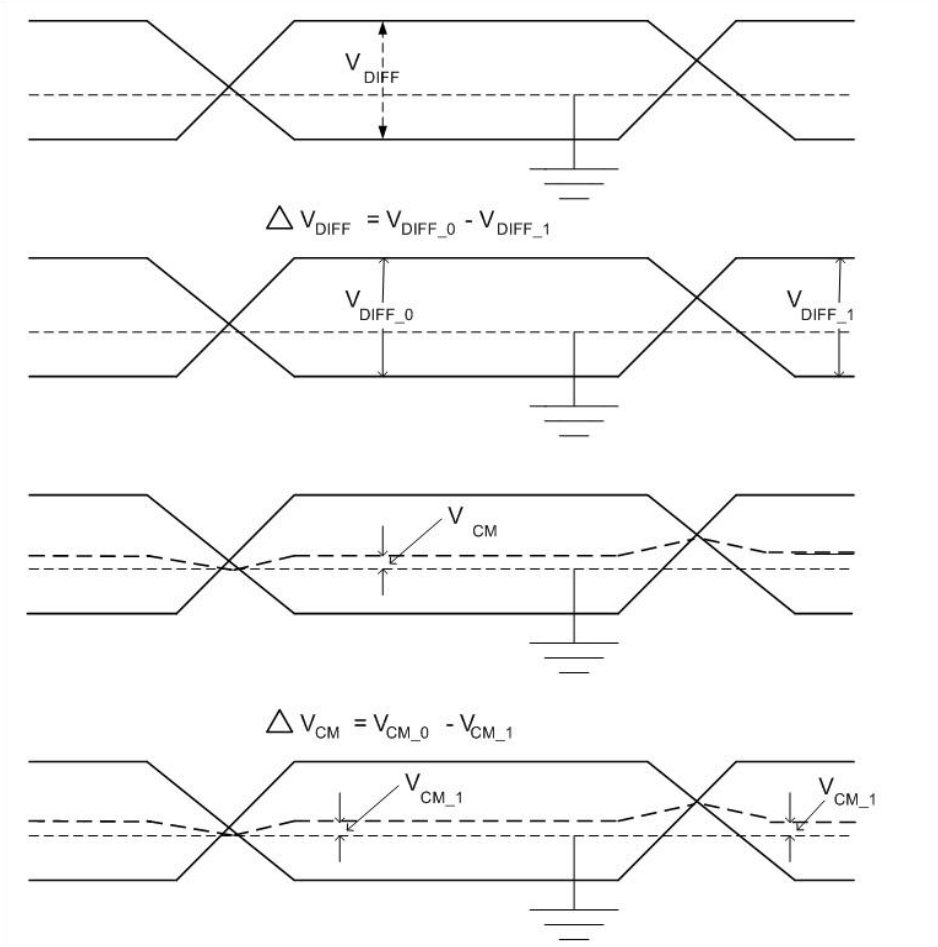



**Figure 23. Single-Ended Measurement Definitions**



# 7.3 3.3 Volt Signals

## 7.3.1 DC Characteristics: Signals on V33 Power Plane

**Table 18. V33: DC Signal Characteristics**

| Symbol | Description | Minimum | Maximum | Units |
|---|---|---|---|---|
| $V_{IH}$ | Input voltage high. | 0.5(V33) | V33 + 0.5 | V |
| $V_{IL}$ | Input voltage low. | -0.5 | 0.35(V33) | V |
| $V_{OH}$ | Output voltage high. | 0.9(V33) | 0.5(V33) | V |
| $V_{OL}$ | Output voltage low. | | 0.1(V33) | V |
| $I_{LI}$ | Input leakage current. | | +/- 10 | uA |
| $C_{IN}$ | Input capacitance. | | 4 | pf |

## 7.3.2 AC Input Requirements: Signals on V33 Power Plane

**Table 19. V33: AC Input Requirements**

| Symbol | Description | Minimum | Maximum | Units |
|---|---|---|---|---|
| $T_{RF}$ | Rise-fall slew rate measured from 0.35(V33) to 0.5(V33). | 1.4 | 4 | V/ns |
| $V_{IH(AC)}$ | Input voltage high. | 0.5(V33) | V33+0.5 | V |
| $V_{IL(AC)}$ | Input voltage low. | -0.5 | 0.35(V33) | V |

# 7.4 Input Requirements for PCIXCAP

## 7.4.1 DC Input Requirements: PCIXCAP

**Table 20. PCIXCAP: DC Input Requirements**

| Symbol | Description | Minimum | Maximum | Units |
|---|---|---|---|---|
| $V_{IH}$ | Input voltage high[1]. | 0.5(V33) | V33+0.5 | V |
| $V_{IL}$ | Input voltage low[1]. | -0.5 | 0.25(V33) | V |
| $I_{LI}$ | Input leakage current. | | +/- 10 | uA |
| $C_{IN}$ | Input capacitance. | | 4 | pf |
| $V_{PCI}$ | [B,A]_PCIXCAP voltage in PCI mode. | -0.5 | 0.05(V33) | V |

**Table 20. PCIXCAP: DC Input Requirements (Continued)**

| Symbol | Description | Minimum | Maximum | Units |
|---|---|---|---|---|
| $V_{PCIX66}$ | [B,A]_PCIXCAP voltage in PCI-X® Mode 1 at 66 MHz. | 0.68(V33) | 0.83(V33) | V |
| $V_{PCIX133}$ | [B,A]_PCIXCAP voltage in PCI-X® Mode 1 at 133 MHz. | 0.95(V33) | V33+0.5 | V |
| $V_{PCIX266}$ | [B,A]_PCIXCAP voltage in PCI-X® Mode 2 at 266 MHz. | 0.43(V33) | 0.55(V33) | V |

**Note:**
1. In hot-plug mode, after reset PCIXCAP is the serial data input from the hot-plug controller.

### 7.4.2 AC Input Requirements: PCIXCAP

**Table 21. PCIXCAP: AC Input Requirements**

| Symbol | Description | Minimum | Maximum | Units |
|---|---|---|---|---|
| $T_{RF}$ | Rise-fall slew rate measured from 0.25(V33) to 0.5(V33). | 1.4 | 4 | V/ns |
| $V_{IH(AC)}$ | Input voltage high[1]. | 0.5(V33) | V33+0.5 | V |
| $V_{IL(AC)}$ | Input voltage low[1]. | -0.5 | 0.25(V33) | V |

**Note:**
1. In hot-plug mode, after reset PCIXCAP is the serial data input from the hot-plug controller.

## 7.5 HyperTransport™ Signal Characteristics

See the *HyperTransport™ I/O Link Specification, Rev 2.0* for the electrical characteristics of the link signals PWROK, LDTREQ_L, LDTRESET, and LDTSTOP_L. Any deviation from this specification is listed in the *AMD-8132™ HyperTransport™ PCI-X®* 2.0 Tunnel *Revision Guide*.

## 7.6 PCI and PCI-X® Signal Characteristics

See *PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification, Rev 2.0a (or higher)* for the electrical characteristics of PCI signals. Any deviation from this specification is listed in the *AMD-8132™ HyperTransport™ PCI-X®* 2.0 Tunnel *Revision Guide*.

# Chapter 8 Package and Pin Designations

## Figure 24. AMD-8132™ Tunnel: Ball Designations

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | | VSS | L0_CTLIN_L0 | VSS | L0_CADIN_L6 | VSS | L0_CADIN_L4 | VSS | L0_CADIN_L3 | VSS | L0_CADIN_L1 | VSS | VLDT | REFCLK_H | VLDT | VSS | L1_CADOUT_H1 | VSS | L1_CADOUT_H3 | VSS | L1_CADOUT_H4 | VSS | L1_CADOUT_H6 | VSS | L1_CTLOUT_H0 | VSS | | | A |
| B | | L0_COMP_PD | NC | L0_CTLIN_H0 | L0_CADIN_L7 | L0_CADIN_H6 | L0_CADIN_L5 | L0_CADIN_H4 | L0_CLKIN_L0 | L0_CADIN_H3 | L0_CADIN_L2 | L0_CADIN_H1 | L0_CADIN_L0 | VLDT | REFCLK_L | VLDT | L1_CADOUT_H0 | L1_CADOUT_L1 | L1_CADOUT_H2 | L1_CADOUT_L3 | L1_CLKOUT_H0 | L1_CADOUT_L4 | L1_CADOUT_H5 | L1_CADOUT_L6 | L1_CADOUT_H7 | L1_CTLOUT_L0 | VSS | L1_COMP_PD | | B |
| C | VSS | VSS | L0_COMP_PU | VDD | L0_CADIN_H7 | VDD | L0_CADIN_H5 | VDD | L0_CLKIN_H0 | VDD | L0_CADIN_H2 | VDD | L0_CADIN_H0 | VLDT | VSS | VLDT | L1_CADOUT_L0 | VDD | L1_CADOUT_L2 | VDD | L1_CLKOUT_L0 | VDD | L1_CADOUT_L5 | VDD | L1_CADOUT_L7 | VDD | L1_COMP_PU | VSS | VSS | C |
| D | L0_CTLOUT_H0 | L0_CTLOUT_L0 | VDD | DIFFOUT_H | VDD | L0_CADIN_L15 | VSS | L0_CADIN_L13 | VSS | L0_CLKIN_L1 | VSS | L0_CADIN_L10 | VSS | L0_CADIN_L8 | VSS | L1_CADOUT_H8 | VSS | L1_CADOUT_H10 | VSS | L1_CLKOUT_H1 | VSS | L1_CADOUT_H13 | VSS | L1_CADOUT_H15 | VDD | VSS | VDD | L1_CTLIN_H0 | L1_CTLIN_L0 | D |
| E | VSS | L0_CADOUT_H7 | L0_CADOUT_L7 | VDD | DIFFOUT_L | L0_CADIN_H15 | L0_CADIN_L14 | L0_CADIN_H13 | L0_CADIN_L12 | L0_CLKIN_H1 | L0_CADIN_L11 | L0_CADIN_H10 | L0_CADIN_L9 | L0_CADIN_H8 | VDD | L1_CADOUT_L8 | L1_CADOUT_H9 | L1_CADOUT_L10 | L1_CADOUT_H11 | L1_CLKOUT_L1 | L1_CADOUT_H12 | L1_CADOUT_L13 | L1_CADOUT_H14 | L1_CADOUT_L15 | VSS | VDD | L1_CADIN_H7 | L1_CADIN_L7 | VSS | E |
| F | L0_CADOUT_H6 | L0_CADOUT_L6 | VDD | L0_CADOUT_H15 | L0_CADOUT_L15 | VDD | L0_CADIN_H14 | VDD | L0_CADIN_H12 | VDD | L0_CADIN_H11 | VDD | L0_CADIN_H9 | VDD | VSS | VDD | L1_CADOUT_L9 | VDD | L1_CADOUT_L11 | VDD | L1_CADOUT_L12 | VDD | L1_CADOUT_L14 | VDD | L1_CADIN_H15 | L1_CADIN_L15 | VDD | L1_CADIN_H6 | L1_CADIN_L6 | F |
| G | VSS | L0_CADOUT_H5 | L0_CADOUT_L5 | VSS | L0_CADOUT_H14 | L0_CADOUT_L14 | VDD | VDDFB_H | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | L1_CADIN_H14 | L1_CADIN_L14 | VSS | L1_CADIN_H5 | L1_CADIN_L5 | VSS | G |
| H | L0_CADOUT_H4 | L0_CADOUT_L4 | VDD | L0_CADOUT_H13 | L0_CADOUT_L13 | VDD | VSS | VDDFB_L | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | L1_CADIN_H13 | L1_CADIN_L13 | VDD | L1_CADIN_H4 | L1_CADIN_L4 | H |
| J | VSS | L0_CLKOUT_H0 | L0_CLKOUT_L0 | VSS | L0_CADOUT_H12 | L0_CADOUT_L12 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | L1_CADIN_H12 | L1_CADIN_L12 | VSS | L1_CLKIN_H0 | L1_CLKIN_L0 | VSS | J |
| K | L0_CADOUT_H3 | L0_CADOUT_L3 | VDD | L0_CLKOUT_H1 | L0_CLKOUT_L1 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | L1_CLKIN_H1 | L1_CLKIN_L1 | VDD | L1_CADIN_H3 | L1_CADIN_L3 | K |
| L | VSS | L0_CADOUT_H2 | L0_CADOUT_L2 | VSS | L0_CADOUT_H11 | L0_CADOUT_L11 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | L1_CADIN_H11 | L1_CADIN_L11 | VSS | L1_CADIN_H2 | L1_CADIN_L2 | VSS | L |
| M | L0_CADOUT_H1 | L0_CADOUT_L1 | VDD | L0_CADOUT_H10 | L0_CADOUT_L10 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | L1_CADIN_H10 | L1_CADIN_L10 | VDD | L1_CADIN_H1 | L1_CADIN_L1 | M |
| N | VSS | L0_CADOUT_H0 | L0_CADOUT_L0 | VSS | L0_CADOUT_H9 | L0_CADOUT_L9 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | L1_CADIN_H9 | L1_CADIN_L9 | VSS | L1_CADIN_H0 | L1_CADIN_L0 | VSS | N |
| P | VLDT | VLDT | VLDT | L0_CADOUT_H8 | L0_CADOUT_L8 | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | L1_CADIN_H8 | L1_CADIN_L8 | VLDT | VLDT | VLDT | P |
| R | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VSS | VSS | VSS | PLL_VDDA1 | PLL_VDDA2 | R |
| T | V33 | V33 | V33 | LDTSTOP_L | LDTREQ_L | LDTRESET_L | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | VDD | VSS | HPSOD | HPSIC | NIOAIRQD_L | V33 | V33 | V33 | T |
| U | TEST | TMS | TDO | TDI | VDDOK | PWROK | B_PLLCLKI | VSS | VIOB | VSS | VIOB | VSS | VIOB | VSS | VSS | VSS | VIOA | VSS | VIOA | VSS | VIOA | VSS | A_PIRQB_L | A_PLLCLKO | STRAPL1 | STRAPL0 | NIOAIRQB_L | NIOAIRQA_L | HPSIL_L | U |
| V | TCK | VSS | B_PCLK2 | VIOB | TRST_L | VSS | B_PLLCLKO | VIOB | VSS | VIOB | VSS | VIOB | VSS | VIOB | VSS | VIOA | VSS | VIOA | VSS | VIOA | VSS | VIOA | A_REQ_L1 | VSS | A_PLLCLKI | VIOA | HPSOC | VSS | NIOAIRQC_L | V |
| W | CMPOVR | B_PCIXCAP | B_PCLK3 | B_PCLK0 | B_AD32 | B_AD33 | B_AD47 | VSS | VIOB | VSS | VIOB | VSS | VIOB | VSS | VSS | VSS | VIOA | VSS | VIOA | VSS | VIOA | VSS | A_ECC5 | A_GNT_L1 | A_RESET_L | A_PCLK1 | A_PCLK4 | A_PCIXCAP | A_COMPAT | W |
| Y | B_PCLK4 | B_PCLK1 | B_AD34 | B_AD35 | B_AD48_CBE_L5 | B_AD46 | B_AD51 | VIOB | VSS | VIOB | VSS | VIOB | VSS | VIOB | VSS | VIOA | VSS | VIOA | VSS | VIOA | VSS | VIOA | A_CBE_L2 | A_ECC4 | A_PCLK3 | A_PIRQC_L | A_PCLK0 | A_PCLK2 | PME_L | Y |
| AA | B_AD36 | VSS | B_AD37 | VIOB | B_AD38 | VSS | B_AD52 | VSS | VIOB | VSS | VIOB | VSS | VIOB | VSS | VSS | VSS | VIOA | VSS | PCIXB_100 | VSS | VIOA | VSS | A_ECC2 | VSS | A_ECC3 | VIOA | A_GNT_L0 | VSS | A_PIRQA_L | AA |
| AB | B_AD39 | B_AD49_CBE_L4 | B_AD40 | B_AD41 | B_AD54 | B_CBE_L7 | B_AD55 | VIOB | VSS | VIOB | VSS | VIOB | VSS | VIOB | VSS | VIOA | VSS | VIOA | PCIXA_100 | VIOA | VDD3FB_H | VIOA | A_AD16 | A_AD17 | A_AD30 | A_AD31 | A_GNT_L4 | A_PIRQD_L | A_REQ_L0 | AB |
| AC | B_AD42 | B_AD43 | B_AD44 | B_AD56 | B_AD57 | B_CBE_L5__AD48 | B_AD50 | B_FRAME_L | B_AD13 | B_AD15 | B_PAR__ECC0 | B_ECC4 | B_ECC5 | B_REQ_L0 | VSS | A_AD49_CBE_L4 | A_AD52 | A_CBE_L7 | A_AD57 | A_IRDY_L | A_REQ64_L__ECC6 | A_ACK64_L__ECC1 | A_PAR__ECC0 | A_AD18 | A_AD19 | A_CBE_L3 | A_AD28 | A_AD29 | A_REQ_L4 | AC |
| AD | B_AD45 | VSS | B_AD58 | VIOB | B_AD59 | VSS | B_DEVSEL_L | B_AD12 | VSS | B_AD14 | B_AD28 | VSS | B_ECC3 | B_PIRQD_L | VSS | A_AD48_CBE_L5 | A_AD47 | VSS | A_AD56 | A_AD51 | VSS | A_AD0 | A_AD14 | VSS | A_AD15 | VIOA | A_AD26 | VSS | A_AD27 | AD |
| AE | B_AD60 | B_AD61 | B_CBE_L6 | B_CBE_L4__AD49 | B_SERR_L | B_IRDY_L | B_AD9 | B_AD11 | B_CBE_L1 | B_AD16 | B_CBE_L2 | B_AD31 | B_ECC2 | B_REQ_L1 | VSS | A_AD32 | A_AD41 | A_AD44 | A_AD53 | A_CBE_L5__AD48 | A_AD50 | A_FRAME_L | A_AD1 | A_AD2 | A_AD4 | A_AD13 | A_AD23 | A_AD24 | A_AD25 | AE |
| AF | B_AD62 | B_AD63 | B_AD53 | VIOB | B_TRDY_L | VIOB | B_AD8 | B_CAL | VIOB | B_AD19 | B_AD27 | VIOB | B_REQ_L4 | B_PIRQA_L | VSS | A_AD33 | A_AD40 | VIOA | A_AD54 | A_AD62 | VIOA | A_CAL | A_PERR_L | VIOA | A_AD5 | VIOA | A_AD12 | A_AD21 | A_AD22 | AF |
| AG | B_PAR64__ECC7 | VSS | B_STOP_L | B_PERR_L | B_AD1 | B_AD3 | B_AD5 | B_AD10 | B_AD20 | B_CBE_L3 | B_AD24 | B_AD30 | B_GNT_L1 | B_GNT_L0 | VSS | A_AD34 | A_AD37 | A_AD43 | A_AD55 | A_CBE_L6 | A_AD61 | A_CBE_L4__AD49 | A_TRDY_L | A_AD3 | A_AD7 | A_AD8 | A_AD10 | VSS | A_AD20 | AG |
| AH | | B_M66EN | VSS | B_ACK64_L__ECC1 | B_CBE_L0 | VSS | B_AD6 | B_AD17 | VSS | B_AD22 | B_AD25 | VSS | B_GNT_L4 | B_PIRQB_L | VSS | A_AD35 | A_AD38 | VSS | A_AD46 | A_AD59 | VSS | A_PAR64__ECC7 | A_DEVSEL_L | VSS | A_AD6 | A_CBE_L1 | VSS | A_AD11 | | AH |
| AJ | | | B_REQ64_L__ECC6 | B_AD0 | B_AD2 | B_AD4 | B_AD7 | B_AD18 | B_AD21 | B_AD23 | B_AD26 | B_AD29 | B_RESET_L | B_PIRQC_L | VSS | A_AD36 | A_AD39 | A_AD42 | A_AD45 | A_AD58 | A_AD60 | A_AD63 | A_M66EN | A_SERR_L | A_STOP_L | A_CBE_L0 | A_AD9 | | | AJ |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | |

The following tables sort the AMD-8132™ HyperTransport™ PCI-X®2.0 tunnel signals. Table 22 -Table 31 sort signals by location. Table 32 - Table 41 sort signals by name.

### Table 22. Signals Sorted by Location A - C

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|---|---|---|---|---|---|
| A3 | VSS | B2 | L0_COMP_PD | C1 | VSS |
| A4 | L0_CTLIN_L0 | B3 | NC | C2 | VSS |
| A5 | VSS | B4 | L0_CTLIN_H0 | C3 | L0_COMP_PU |
| A6 | L0_CADIN_L6 | B5 | L0_CADIN_L7 | C4 | VDD |
| A7 | VSS | B6 | L0_CADIN_H6 | C5 | L0_CADIN_H7 |
| A8 | L0_CADIN_L4 | B7 | L0_CADIN_L5 | C6 | VDD |
| A9 | VSS | B8 | L0_CADIN_H4 | C7 | L0_CADIN_H5 |
| A10 | L0_CADIN_L3 | B9 | L0_CLKIN_L0 | C8 | VDD |
| A11 | VSS | B10 | L0_CADIN_H3 | C9 | L0_CLKIN_H0 |
| A12 | L0_CADIN_L1 | B11 | L0_CADIN_L2 | C10 | VDD |
| A13 | VSS | B12 | L0_CADIN_H1 | C11 | L0_CADIN_H2 |
| A14 | VLDT | B13 | L0_CADIN_L0 | C12 | VDD |
| A15 | REFCLK_H | B14 | VLDT | C13 | L0_CADIN_H0 |
| A16 | VLDT | B15 | REFCLK_L | C14 | VLDT |
| A17 | VSS | B16 | VLDT | C15 | VSS |
| A18 | L1_CADOUT_H1 | B17 | L1_CADOUT_H0 | C16 | VLDT |
| A19 | VSS | B18 | L1_CADOUT_L1 | C17 | L1_CADOUT_L0 |
| A20 | L1_CADOUT_H3 | B19 | L1_CADOUT_H2 | C18 | VDD |
| A21 | VSS | B20 | L1_CADOUT_L3 | C19 | L1_CADOUT_L2 |
| A22 | L1_CADOUT_H4 | B21 | L1_CLKOUT_H0 | C20 | VDD |
| A23 | VSS | B22 | L1_CADOUT_L4 | C21 | L1_CLKOUT_L0 |
| A24 | L1_CADOUT_H6 | B23 | L1_CADOUT_H5 | C22 | VDD |
| A25 | VSS | B24 | L1_CADOUT_L6 | C23 | L1_CADOUT_L5 |
| A26 | L1_CTLOUT_H0 | B25 | L1_CADOUT_H7 | C24 | VDD |
| A27 | VSS | B26 | L1_CTLOUT_L0 | C25 | L1_CADOUT_L7 |
| | | B27 | VSS | C26 | VDD |
| | | B28 | L1_COMP_PD | C27 | L1_COMP_PU |
| | | | | C28 | VSS |
| | | | | C29 | VSS |

**Table 23. Signals Sorted by Location D - F**

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|---|---|---|---|---|---|
| D1 | L0_CTLOUT_H0 | E1 | VSS | F1 | L0_CADOUT_H6 |
| D2 | L0_CTLOUT_L0 | E2 | L0_CADOUT_H7 | F2 | L0_CADOUT_L6 |
| D3 | VDD | E3 | L0_CADOUT_L7 | F3 | VDD |
| D4 | DIFFOUT_H | E4 | VDD | F4 | L0_CADOUT_H15 |
| D5 | VDD | E5 | DIFFOUT_L | F5 | L0_CADOUT_L15 |
| D6 | L0_CADIN_L15 | E6 | L0_CADIN_H15 | F6 | VDD |
| D7 | VSS | E7 | L0_CADIN_L14 | F7 | L0_CADIN_H14 |
| D8 | L0_CADIN_L13 | E8 | L0_CADIN_H13 | F8 | VDD |
| D9 | VSS | E9 | L0_CADIN_L12 | F9 | L0_CADIN_H12 |
| D10 | L0_CLKIN_L1 | E10 | L0_CLKIN_H1 | F10 | VDD |
| D11 | VSS | E11 | L0_CADIN_L11 | F11 | L0_CADIN_H11 |
| D12 | L0_CADIN_L10 | E12 | L0_CADIN_H10 | F12 | VDD |
| D13 | VSS | E13 | L0_CADIN_L9 | F13 | L0_CADIN_H9 |
| D14 | L0_CADIN_L8 | E14 | L0_CADIN_H8 | F14 | VDD |
| D15 | VSS | E15 | VDD | F15 | VSS |
| D16 | L1_CADOUT_H8 | E16 | L1_CADOUT_L8 | F16 | VDD |
| D17 | VSS | E17 | L1_CADOUT_H9 | F17 | L1_CADOUT_L9 |
| D18 | L1_CADOUT_H10 | E18 | L1_CADOUT_L10 | F18 | VDD |
| D19 | VSS | E19 | L1_CADOUT_H11 | F19 | L1_CADOUT_L11 |
| D20 | L1_CLKOUT_H1 | E20 | L1_CLKOUT_L1 | F20 | VDD |
| D21 | VSS | E21 | L1_CADOUT_H12 | F21 | L1_CADOUT_L12 |
| D22 | L1_CADOUT_H13 | E22 | L1_CADOUT_L13 | F22 | VDD |
| D23 | VSS | E23 | L1_CADOUT_H14 | F23 | L1_CADOUT_L14 |
| D24 | L1_CADOUT_H15 | E24 | L1_CADOUT_L15 | F24 | VDD |
| D25 | VDD | E25 | VSS | F25 | L1_CADIN_H15 |
| D26 | VSS | E26 | VDD | F26 | L1_CADIN_L15 |
| D27 | VDD | E27 | L1_CADIN_H7 | F27 | VDD |
| D28 | L1_CTLIN_H0 | E28 | L1_CADIN_L7 | F28 | L1_CADIN_H6 |
| D29 | L1_CTLIN_L0 | E29 | VSS | F29 | L1_CADIN_L6 |

**Table 24. Signals Sorted by Location G - J**

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|---|---|---|---|---|---|
| G1 | VSS | H1 | L0_CADOUT_H4 | J1 | VSS |
| G2 | L0_CADOUT_H5 | H2 | L0_CADOUT_L4 | J2 | L0_CLKOUT_H0 |
| G3 | L0_CADOUT_L5 | H3 | VDD | J3 | L0_CLKOUT_L0 |
| G4 | VSS | H4 | L0_CADOUT_H13 | J4 | VSS |
| G5 | L0_CADOUT_H14 | H5 | L0_CADOUT_L13 | J5 | L0_CADOUT_H12 |
| G6 | L0_CADOUT_L14 | H6 | VDD | J6 | L0_CADOUT_L12 |
| G7 | VDD | H7 | VSS | J7 | VDD |
| G8 | VDDFB_H | H8 | VDDFB_L | J8 | VSS |
| G9 | VDD | H9 | VSS | J9 | VDD |
| G10 | VSS | H10 | VDD | J10 | VSS |
| G11 | VDD | H11 | VSS | J11 | VDD |
| G12 | VSS | H12 | VDD | J12 | VSS |
| G13 | VDD | H13 | VSS | J13 | VDD |
| G14 | VSS | H14 | VDD | J14 | VSS |
| G15 | VDD | H15 | VSS | J15 | VDD |
| G16 | VSS | H16 | VDD | J16 | VSS |
| G17 | VDD | H17 | VSS | J17 | VDD |
| G18 | VSS | H18 | VDD | J18 | VSS |
| G19 | VDD | H19 | VSS | J19 | VDD |
| G20 | VSS | H20 | VDD | J20 | VSS |
| G21 | VDD | H21 | VSS | J21 | VDD |
| G22 | VSS | H22 | VDD | J22 | VSS |
| G23 | VDD | H23 | VSS | J23 | VDD |
| G24 | L1_CADIN_H14 | H24 | VDD | J24 | L1_CADIN_H12 |
| G25 | L1_CADIN_L14 | H25 | L1_CADIN_H13 | J25 | L1_CADIN_L12 |
| G26 | VSS | H26 | L1_CADIN_L13 | J26 | VSS |
| G27 | L1_CADIN_H5 | H27 | VDD | J27 | L1_CLKIN_H0 |
| G28 | L1_CADIN_L5 | H28 | L1_CADIN_H4 | J28 | L1_CLKIN_L0 |
| G29 | VSS | H29 | L1_CADIN_L4 | J29 | VSS |

**Table 25. Signals Sorted by Location K - M**

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|---|---|---|---|---|---|
| K1 | L0_CADOUT_H3 | L1 | VSS | M1 | L0_CADOUT_H1 |
| K2 | L0_CADOUT_L3 | L2 | L0_CADOUT_H2 | M2 | L0_CADOUT_L1 |
| K3 | VDD | L3 | L0_CADOUT_L2 | M3 | VDD |
| K4 | L0_CLKOUT_H1 | L4 | VSS | M4 | L0_CADOUT_H10 |
| K5 | L0_CLKOUT_L1 | L5 | L0_CADOUT_H11 | M5 | L0_CADOUT_L10 |
| K6 | VDD | L6 | L0_CADOUT_L11 | M6 | VDD |
| K7 | VSS | L7 | VDD | M7 | VSS |
| K8 | VDD | L8 | VSS | M8 | VDD |
| K9 | VSS | L9 | VDD | M9 | VSS |
| K10 | VDD | L10 | VSS | M10 | VDD |
| K11 | VSS | L11 | VDD | M11 | VSS |
| K12 | VDD | L12 | VSS | M12 | VDD |
| K13 | VSS | L13 | VDD | M13 | VSS |
| K14 | VDD | L14 | VSS | M14 | VDD |
| K15 | VSS | L15 | VDD | M15 | VSS |
| K16 | VDD | L16 | VSS | M16 | VDD |
| K17 | VSS | L17 | VDD | M17 | VSS |
| K18 | VDD | L18 | VSS | M18 | VDD |
| K19 | VSS | L19 | VDD | M19 | VSS |
| K20 | VDD | L20 | VSS | M20 | VDD |
| K21 | VSS | L21 | VDD | M21 | VSS |
| K22 | VDD | L22 | VSS | M22 | VDD |
| K23 | VSS | L23 | VDD | M23 | VSS |
| K24 | VDD | L24 | L1_CADIN_H11 | M24 | VDD |
| K25 | L1_CLKIN_H1 | L25 | L1_CADIN_L11 | M25 | L1_CADIN_H10 |
| K26 | L1_CLKIN_L1 | L26 | VSS | M26 | L1_CADIN_L10 |
| K27 | VDD | L27 | L1_CADIN_H2 | M27 | VDD |
| K28 | L1_CADIN_H3 | L28 | L1_CADIN_L2 | M28 | L1_CADIN_H1 |
| K29 | L1_CADIN_L3 | L29 | VSS | M29 | L1_CADIN_L1 |

**Table 26. Signals Sorted by Location N - R**

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|---|---|---|---|---|---|
| N1 | VSS | P1 | VLDT | R1 | VSS |
| N2 | L0_CADOUT_H0 | P2 | VLDT | R2 | VSS |
| N3 | L0_CADOUT_L0 | P3 | VLDT | R3 | VSS |
| N4 | VSS | P4 | L0_CADOUT_H8 | R4 | VSS |
| N5 | L0_CADOUT_H9 | P5 | L0_CADOUT_L8 | R5 | VSS |
| N6 | L0_CADOUT_L9 | P6 | VDD | R6 | VSS |
| N7 | VDD | P7 | VSS | R7 | VSS |
| N8 | VSS | P8 | VDD | R8 | VSS |
| N9 | VDD | P9 | VSS | R9 | VDD |
| N10 | VSS | P10 | VDD | R10 | VSS |
| N11 | VDD | P11 | VSS | R11 | VDD |
| N12 | VSS | P12 | VDD | R12 | VSS |
| N13 | VDD | P13 | VSS | R13 | VDD |
| N14 | VSS | P14 | VDD | R14 | VSS |
| N15 | VDD | P15 | VSS | R15 | VDD |
| N16 | VSS | P16 | VDD | R16 | VSS |
| N17 | VDD | P17 | VSS | R17 | VDD |
| N18 | VSS | P18 | VDD | R18 | VSS |
| N19 | VDD | P19 | VSS | R19 | VDD |
| N20 | VSS | P20 | VDD | R20 | VSS |
| N21 | VDD | P21 | VSS | R21 | VDD |
| N22 | VSS | P22 | VDD | R22 | VSS |
| N23 | VDD | P23 | VSS | R23 | VDD |
| N24 | L1_CADIN_H9 | P24 | VDD | R24 | VSS |
| N25 | L1_CADIN_L9 | P25 | L1_CADIN_H8 | R25 | VSS |
| N26 | VSS | P26 | L1_CADIN_L8 | R26 | VSS |
| N27 | L1_CADIN_H0 | P27 | VLDT | R27 | VSS |
| N28 | L1_CADIN_L0 | P28 | VLDT | R28 | PLL_VDDA1 |
| N29 | VSS | P29 | VLDT | R29 | PLL_VDDA2 |

### Table 27. Signals Sorted by LocationT - V

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|---|---|---|---|---|---|
| T1 | V33 | U1 | TEST | V1 | TCK |
| T2 | V33 | U2 | TMS | V2 | VSS |
| T3 | V33 | U3 | TDO | V3 | B_PCLK2 |
| T4 | LDTSTOP_L | U4 | TDI | V4 | VIOB |
| T5 | LDTREQ_L | U5 | VDDOK | V5 | TRST_L |
| T6 | LDTRESET_L | U6 | PWROK | V6 | VSS |
| T7 | VSS | U7 | B_PLLCLKI | V7 | B_PLLCLKO |
| T8 | VDD | U8 | VSS | V8 | VIOB |
| T9 | VSS | U9 | VIOB | V9 | VSS |
| T10 | VDD | U10 | VSS | V10 | VIOB |
| T11 | VSS | U11 | VIOB | V11 | VSS |
| T12 | VDD | U12 | VSS | V12 | VIOB |
| T13 | VSS | U13 | VIOB | V13 | VSS |
| T14 | VDD | U14 | VSS | V14 | VIOB |
| T15 | VSS | U15 | VSS | V15 | VSS |
| T16 | VDD | U16 | VSS | V16 | VIOA |
| T17 | VSS | U17 | VIOA | V17 | VSS |
| T18 | VDD | U18 | VSS | V18 | VIOA |
| T19 | VSS | U19 | VIOA | V19 | VSS |
| T20 | VDD | U20 | VSS | V20 | VIOA |
| T21 | VSS | U21 | VIOA | V21 | VSS |
| T22 | VDD | U22 | VSS | V22 | VIOA |
| T23 | VSS | U23 | A_PIRQB_L | V23 | A_REQ_L1 |
| T24 | HPSOD | U24 | A_PLLCLKO | V24 | VSS |
| T25 | HPSIC | U25 | STRAPL1 | V25 | A_PLLCLKI |
| T26 | NIOAIRQD_L | U26 | STRAPL0 | V26 | VIOA |
| T27 | V33 | U27 | NIOAIRQB_L | V27 | HPSOC |
| T28 | V33 | U28 | NIOAIRQA_L | V28 | VSS |
| T29 | V33 | U29 | HPSIL_L | V29 | NIOAIRQC_L |

**Table 28. Signals Sorted by Location W - AA**

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|---|---|---|---|---|---|
| W1 | CMPOVR | Y1 | B_PCLK4 | AA1 | B_AD36 |
| W2 | B_PCIXCAP | Y2 | B_PCLK1 | AA2 | VSS |
| W3 | B_PCLK3 | Y3 | B_AD34 | AA3 | B_AD37 |
| W4 | B_PCLK0 | Y4 | B_AD35 | AA4 | VIOB |
| W5 | B_AD32 | Y5 | B_AD48__CBE_L5 | AA5 | B_AD38 |
| W6 | B_AD33 | Y6 | B_AD46 | AA6 | VSS |
| W7 | B_AD47 | Y7 | B_AD51 | AA7 | B_AD52 |
| W8 | VSS | Y8 | VIOB | AA8 | VSS |
| W9 | VIOB | Y9 | VSS | AA9 | VIOB |
| W10 | VSS | Y10 | VIOB | AA10 | VSS |
| W11 | VIOB | Y11 | VSS | AA11 | VIOB |
| W12 | VSS | Y12 | VIOB | AA12 | VSS |
| W13 | VIOB | Y13 | VSS | AA13 | VIOB |
| W14 | VSS | Y14 | VIOB | AA14 | VSS |
| W15 | VSS | Y15 | VSS | AA15 | VSS |
| W16 | VSS | Y16 | VIOA | AA16 | VSS |
| W17 | VIOA | Y17 | VSS | AA17 | VIOA |
| W18 | VSS | Y18 | VIOA | AA18 | VSS |
| W19 | VIOA | Y19 | VSS | AA19 | PCIXB_100 |
| W20 | VSS | Y20 | VIOA | AA20 | VSS |
| W21 | VIOA | Y21 | VSS | AA21 | VIOA |
| W22 | VSS | Y22 | VIOA | AA22 | VSS |
| W23 | A_ECC5 | Y23 | A_CBE_L2 | AA23 | A_ECC2 |
| W24 | A_GNT_L1 | Y24 | A_ECC4 | AA24 | VSS |
| W25 | A_RESET_L | Y25 | A_PCLK3 | AA25 | A_ECC3 |
| W26 | A_PCLK1 | Y26 | A_PIRQC_L | AA26 | VIOA |
| W27 | A_PCLK4 | Y27 | A_PCLK0 | AA27 | A_GNT_L0 |
| W28 | A_PCIXCAP | Y28 | A_PCLK2 | AA28 | VSS |
| W29 | A_COMPAT | Y29 | PME_L | AA29 | A_PIRQA_L |

**Table 29. Signals Sorted by Location AB - AD**

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|---|---|---|---|---|---|
| AB1 | B_AD39 | AC1 | B_AD42 | AD1 | B_AD45 |
| AB2 | B_AD49__CBE_L4 | AC2 | B_AD43 | AD2 | VSS |
| AB3 | B_AD40 | AC3 | B_AD44 | AD3 | B_AD58 |
| AB4 | B_AD41 | AC4 | B_AD56 | AD4 | VIOB |
| AB5 | B_AD54 | AC5 | B_AD57 | AD5 | B_AD59 |
| AB6 | B_CBE_L7 | AC6 | B_CBE_L5__AD48 | AD6 | VSS |
| AB7 | B_AD55 | AC7 | B_AD50 | AD7 | B_DEVSEL_L |
| AB8 | VIOB | AC8 | B_FRAME_L | AD8 | B_AD12 |
| AB9 | VSS | AC9 | B_AD13 | AD9 | VSS |
| AB10 | VIOB | AC10 | B_AD15 | AD10 | B_AD14 |
| AB11 | VSS | AC11 | B_PAR__ECC0 | AD11 | B_AD28 |
| AB12 | VIOB | AC12 | B_ECC4 | AD12 | VSS |
| AB13 | VSS | AC13 | B_ECC5 | AD13 | B_ECC3 |
| AB14 | VIOB | AC14 | B_REQ_L0 | AD14 | B_PIRQD_L |
| AB15 | VSS | AC15 | VSS | AD15 | VSS |
| AB16 | VIOA | AC16 | A_AD49__CBE_L4 | AD16 | A_AD48__CBE_L5 |
| AB17 | VSS | AC17 | A_AD52 | AD17 | A_AD47 |
| AB18 | VIOA | AC18 | A_CBE_L7 | AD18 | VSS |
| AB19 | PCIXA_100 | AC19 | A_AD57 | AD19 | A_AD56 |
| AB20 | VIOA | AC20 | A_IRDY_L | AD20 | A_AD51 |
| AB21 | VDD3FB_H | AC21 | A_REQ64_L__ECC6 | AD21 | VSS |
| AB22 | VIOA | AC22 | A_ACK64_L__ECC1 | AD22 | A_AD0 |
| AB23 | A_AD16 | AC23 | A_PAR__ECC0 | AD23 | A_AD14 |
| AB24 | A_AD17 | AC24 | A_AD18 | AD24 | VSS |
| AB25 | A_AD30 | AC25 | A_AD19 | AD25 | A_AD15 |
| AB26 | A_AD31 | AC26 | A_CBE_L3 | AD26 | VIOA |
| AB27 | A_GNT_L4 | AC27 | A_AD28 | AD27 | A_AD26 |
| AB28 | A_PIRQD_L | AC28 | A_AD29 | AD28 | VSS |
| AB29 | A_REQ_L0 | AC29 | A_REQ_L4 | AD29 | A_AD27 |

**Table 30. Signals Sorted by Location AE - AG**

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|---|---|---|---|---|---|
| AE1 | B_AD60 | AF1 | B_AD62 | AG1 | B_PAR64__ECC7 |
| AE2 | B_AD61 | AF2 | B_AD63 | AG2 | VSS |
| AE3 | B_CBE_L6 | AF3 | B_AD53 | AG3 | B_STOP_L |
| AE4 | B_CBE_L4__AD49 | AF4 | VIOB | AG4 | B_PERR_L |
| AE5 | B_SERR_L | AF5 | B_TRDY_L | AG5 | B_AD1 |
| AE6 | B_IRDY_L | AF6 | VIOB | AG6 | B_AD3 |
| AE7 | B_AD9 | AF7 | B_AD8 | AG7 | B_AD5 |
| AE8 | B_AD11 | AF8 | B_CAL | AG8 | B_AD10 |
| AE9 | B_CBE_L1 | AF9 | VIOB | AG9 | B_AD20 |
| AE10 | B_AD16 | AF10 | B_AD19 | AG10 | B_CBE_L3 |
| AE11 | B_CBE_L2 | AF11 | B_AD27 | AG11 | B_AD24 |
| AE12 | B_AD31 | AF12 | VIOB | AG12 | B_AD30 |
| AE13 | B_ECC2 | AF13 | B_REQ_L4 | AG13 | B_GNT_L1 |
| AE14 | B_REQ_L1 | AF14 | B_PIRQA_L | AG14 | B_GNT_L0 |
| AE15 | VSS | AF15 | VSS | AG15 | VSS |
| AE16 | A_AD32 | AF16 | A_AD33 | AG16 | A_AD34 |
| AE17 | A_AD41 | AF17 | A_AD40 | AG17 | A_AD37 |
| AE18 | A_AD44 | AF18 | VIOA | AG18 | A_AD43 |
| AE19 | A_AD53 | AF19 | A_AD54 | AG19 | A_AD55 |
| AE20 | A_CBE_L5__AD48 | AF20 | A_AD62 | AG20 | A_CBE_L6 |
| AE21 | A_AD50 | AF21 | VIOA | AG21 | A_AD61 |
| AE22 | A_FRAME_L | AF22 | A_CAL | AG22 | A_CBE_L4__AD49 |
| AE23 | A_AD1 | AF23 | A_PERR_L | AG23 | A_TRDY_L |
| AE24 | A_AD2 | AF24 | VIOA | AG24 | A_AD3 |
| AE25 | A_AD4 | AF25 | A_AD5 | AG25 | A_AD7 |
| AE26 | A_AD13 | AF26 | VIOA | AG26 | A_AD8 |
| AE27 | A_AD23 | AF27 | A_AD12 | AG27 | A_AD10 |
| AE28 | A_AD24 | AF28 | A_AD21 | AG28 | VSS |
| AE29 | A_AD25 | AF29 | A_AD22 | AG29 | A_AD20 |

**Table 31. Signals Sorted by Location AH - AJ**

| Ball | Signal Name | Ball | Signal Name |
|---|---|---|---|
| AH2 | B_M66EN | AJ3 | B_REQ64_L__ECC6 |
| AH3 | VSS | AJ4 | B_AD0 |
| AH4 | B_ACK64_L__ECC1 | AJ5 | B_AD2 |
| AH5 | B_CBE_L0 | AJ6 | B_AD4 |
| AH6 | VSS | AJ7 | B_AD7 |
| AH7 | B_AD6 | AJ8 | B_AD18 |
| AH8 | B_AD17 | AJ9 | B_AD21 |
| AH9 | VSS | AJ10 | B_AD23 |
| AH10 | B_AD22 | AJ11 | B_AD26 |
| AH11 | B_AD25 | AJ12 | B_AD29 |
| AH12 | VSS | AJ13 | B_RESET_L |
| AH13 | B_GNT_L4 | AJ14 | B_PIRQC_L |
| AH14 | B_PIRQB_L | AJ15 | VSS |
| AH15 | VSS | AJ16 | A_AD36 |
| AH16 | A_AD35 | AJ17 | A_AD39 |
| AH17 | A_AD38 | AJ18 | A_AD42 |
| AH18 | VSS | AJ19 | A_AD45 |
| AH19 | A_AD46 | AJ20 | A_AD58 |
| AH20 | A_AD59 | AJ21 | A_AD60 |
| AH21 | VSS | AJ22 | A_AD63 |
| AH22 | A_PAR64__ECC7 | AJ23 | A_M66EN |
| AH23 | A_DEVSEL_L | AJ24 | A_SERR_L |
| AH24 | VSS | AJ25 | A_STOP_L |
| AH25 | A_AD6 | AJ26 | A_CBE_L0 |
| AH26 | A_CBE_L1 | AJ27 | A_AD9 |
| AH27 | VSS | | |
| AH28 | A_AD11 | | |

**Table 32. Signals Sorted by Name A_A - A_M**

| Pin Name | Pin | Pin Name | Pin | Pin Name | Pin |
|---|---|---|---|---|---|
| A_ACK64_L__ECC1 | AC22 | A_AD30 | AB25 | A_AD61 | AG21 |
| A_AD0 | AD22 | A_AD31 | AB26 | A_AD62 | AF20 |
| A_AD1 | AE23 | A_AD32 | AE16 | A_AD63 | AJ22 |
| A_AD2 | AE24 | A_AD33 | AF16 | A_CAL | AF22 |
| A_AD3 | AG24 | A_AD34 | AG16 | A_CBE_L0 | AJ26 |
| A_AD4 | AE25 | A_AD35 | AH16 | A_CBE_L1 | AH26 |
| A_AD5 | AF25 | A_AD36 | AJ16 | A_CBE_L2 | Y23 |
| A_AD6 | AH25 | A_AD37 | AG17 | A_CBE_L3 | AC26 |
| A_AD7 | AG25 | A_AD38 | AH17 | A_CBE_L4__AD49 | AG22 |
| A_AD8 | AG26 | A_AD39 | AJ17 | A_CBE_L5__AD48 | AE20 |
| A_AD9 | AJ27 | A_AD40 | AF17 | A_CBE_L6 | AG20 |
| A_AD10 | AG27 | A_AD41 | AE17 | A_CBE_L7 | AC18 |
| A_AD11 | AH28 | A_AD42 | AJ18 | A_COMPAT | W29 |
| A_AD12 | AF27 | A_AD43 | AG18 | A_DEVSEL_L | AH23 |
| A_AD13 | AE26 | A_AD44 | AE18 | A_ECC2 | AA23 |
| A_AD14 | AD23 | A_AD45 | AJ19 | A_ECC3 | AA25 |
| A_AD15 | AD25 | A_AD46 | AH19 | A_ECC4 | Y24 |
| A_AD16 | AB23 | A_AD47 | AD17 | A_ECC5 | W23 |
| A_AD17 | AB24 | A_AD48__CBE_L5 | AD16 | A_FRAME_L | AE22 |
| A_AD18 | AC24 | A_AD49__CBE_L4 | AC16 | A_GNT_L0 | AA27 |
| A_AD19 | AC25 | A_AD50 | AE21 | A_GNT_L1 | W24 |
| A_AD20 | AG29 | A_AD51 | AD20 | A_GNT_L4 | AB27 |
| A_AD21 | AF28 | A_AD52 | AC17 | A_IRDY_L | AC20 |
| A_AD22 | AF29 | A_AD53 | AE19 | A_M66EN | AJ23 |
| A_AD23 | AE27 | A_AD54 | AF19 | | |
| A_AD24 | AE28 | A_AD55 | AG19 | | |
| A_AD25 | AE29 | A_AD56 | AD19 | | |
| A_AD26 | AD27 | A_AD57 | AC19 | | |
| A_AD27 | AD29 | A_AD58 | AJ20 | | |
| A_AD28 | AC27 | A_AD59 | AH20 | | |
| A_AD29 | AC28 | A_AD60 | AJ21 | | |

**Table 33. Signals Sorted by Name A_P - B_A**

| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball |
|---|---|---|---|---|---|
| A_PAR__ECC0 | AC23 | B_AD5 | AG7 | B_AD35 | Y4 |
| A_PAR64__ECC7 | AH22 | B_AD6 | AH7 | B_AD36 | AA1 |
| A_PCIXCAP | W28 | B_AD7 | AJ7 | B_AD37 | AA3 |
| A_PCLK0 | Y27 | B_AD8 | AF7 | B_AD38 | AA5 |
| A_PCLK1 | W26 | B_AD9 | AE7 | B_AD39 | AB1 |
| A_PCLK2 | Y28 | B_AD10 | AG8 | B_AD40 | AB3 |
| A_PCLK3 | Y25 | B_AD11 | AE8 | B_AD41 | AB4 |
| A_PCLK4 | W27 | B_AD12 | AD8 | B_AD42 | AC1 |
| A_PERR_L | AF23 | B_AD13 | AC9 | B_AD43 | AC2 |
| A_PIRQA_L | AA29 | B_AD14 | AD10 | B_AD44 | AC3 |
| A_PIRQB_L | U23 | B_AD15 | AC10 | B_AD45 | AD1 |
| A_PIRQC_L | Y26 | B_AD16 | AE10 | B_AD46 | Y6 |
| A_PIRQD_L | AB28 | B_AD17 | AH8 | B_AD47 | W7 |
| A_PLLCLKI | V25 | B_AD18 | AJ8 | B_AD48__CBE_L5 | Y5 |
| A_PLLCLKO | U24 | B_AD19 | AF10 | B_AD49__CBE_L4 | AB2 |
| A_REQ_L0 | AB29 | B_AD20 | AG9 | B_AD50 | AC7 |
| A_REQ_L1 | V23 | B_AD21 | AJ9 | B_AD51 | Y7 |
| A_REQ_L4 | AC29 | B_AD22 | AH10 | B_AD52 | AA7 |
| A_REQ64_L__ECC6 | AC21 | B_AD23 | AJ10 | B_AD53 | AF3 |
| A_RESET_L | W25 | B_AD24 | AG11 | B_AD54 | AB5 |
| A_SERR_L | AJ24 | B_AD25 | AH11 | B_AD55 | AB7 |
| A_STOP_L | AJ25 | B_AD26 | AJ11 | B_AD56 | AC4 |
| A_TRDY_L | AG23 | B_AD27 | AF11 | B_AD57 | AC5 |
| B_ACK64_L__ECC1 | AH4 | B_AD28 | AD11 | B_AD58 | AD3 |
| B_AD0 | AJ4 | B_AD29 | AJ12 | B_AD59 | AD5 |
| B_AD1 | AG5 | B_AD30 | AG12 | B_AD60 | AE1 |
| B_AD2 | AJ5 | B_AD31 | AE12 | B_AD61 | AE2 |
| B_AD3 | AG6 | B_AD32 | W5 | B_AD62 | AF1 |
| B_AD4 | AJ6 | B_AD33 | W6 | B_AD63 | AF2 |
| | | B_AD34 | Y3 | | |

**Table 34. Signals Sorted by Name B_C - L0_CADIN**

| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball |
|---|---|---|---|---|---|
| B_CAL | AF8 | B_PIRQB_L | AH14 | L0_CADIN_H10 | E12 |
| B_CBE_L0 | AH5 | B_PIRQC_L | AJ14 | L0_CADIN_H11 | F11 |
| B_CBE_L1 | AE9 | B_PIRQD_L | AD14 | L0_CADIN_H12 | F9 |
| B_CBE_L2 | AE11 | B_PLLCLKI | U7 | L0_CADIN_H13 | E8 |
| B_CBE_L3 | AG10 | B_PLLCLKO | V7 | L0_CADIN_H14 | F7 |
| B_CBE_L4__AD49 | AE4 | B_REQ_L0 | AC14 | L0_CADIN_H15 | E6 |
| B_CBE_L5__AD48 | AC6 | B_REQ_L1 | AE14 | L0_CADIN_L0 | B13 |
| B_CBE_L6 | AE3 | B_REQ_L4 | AF13 | L0_CADIN_L1 | A12 |
| B_CBE_L7 | AB6 | B_REQ64_L__ECC6 | AJ3 | L0_CADIN_L2 | B11 |
| B_DEVSEL_L | AD7 | B_RESET_L | AJ13 | L0_CADIN_L3 | A10 |
| B_ECC2 | AE13 | B_SERR_L | AE5 | L0_CADIN_L4 | A8 |
| B_ECC3 | AD13 | B_STOP_L | AG3 | L0_CADIN_L5 | B7 |
| B_ECC4 | AC12 | B_TRDY_L | AF5 | L0_CADIN_L6 | A6 |
| B_ECC5 | AC13 | CMPOVR | W1 | L0_CADIN_L7 | B5 |
| B_FRAME_L | AC8 | DIFFOUT_H | D4 | L0_CADIN_L8 | D14 |
| B_GNT_L0 | AG14 | DIFFOUT_L | E5 | L0_CADIN_L9 | E13 |
| B_GNT_L1 | AG13 | HPSIC | T25 | L0_CADIN_L10 | D12 |
| B_GNT_L4 | AH13 | HPSIL_L | U29 | L0_CADIN_L11 | E11 |
| B_IRDY_L | AE6 | HPSOC | V27 | L0_CADIN_L12 | E9 |
| B_M66EN | AH2 | HPSOD | T24 | L0_CADIN_L13 | D8 |
| B_PAR__ECC0 | AC11 | L0_CADIN_H0 | C13 | L0_CADIN_L14 | E7 |
| B_PAR64__ECC7 | AG1 | L0_CADIN_H1 | B12 | L0_CADIN_L15 | D6 |
| B_PCIXCAP | W2 | L0_CADIN_H2 | C11 | | |
| B_PCLK0 | W4 | L0_CADIN_H3 | B10 | | |
| B_PCLK1 | Y2 | L0_CADIN_H4 | B8 | | |
| B_PCLK2 | V3 | L0_CADIN_H5 | C7 | | |
| B_PCLK3 | W3 | L0_CADIN_H6 | B6 | | |
| B_PCLK4 | Y1 | L0_CADIN_H7 | C5 | | |
| B_PERR_L | AG4 | L0_CADIN_H8 | E14 | | |
| B_PIRQA_L | AF14 | L0_CADIN_H9 | F13 | | |

**Table 35. Signals Sorted by Name L0_CADOUT - L1_CADIN**

| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball |
|---|---|---|---|---|---|
| L0_CADOUT_H0 | N2 | L0_CADOUT_L14 | G6 | L1_CADIN_H14 | G24 |
| L0_CADOUT_H1 | M1 | L0_CADOUT_L15 | F5 | L1_CADIN_H15 | F25 |
| L0_CADOUT_H2 | L2 | L0_CLKIN_H0 | C9 | L1_CADIN_L0 | N28 |
| L0_CADOUT_H3 | K1 | L0_CLKIN_H1 | E10 | L1_CADIN_L1 | M29 |
| L0_CADOUT_H4 | H1 | L0_CLKIN_L0 | B9 | L1_CADIN_L2 | L28 |
| L0_CADOUT_H5 | G2 | L0_CLKIN_L1 | D10 | L1_CADIN_L3 | K29 |
| L0_CADOUT_H6 | F1 | L0_CLKOUT_H0 | J2 | L1_CADIN_L4 | H29 |
| L0_CADOUT_H7 | E2 | L0_CLKOUT_H1 | K4 | L1_CADIN_L5 | G28 |
| L0_CADOUT_H8 | P4 | L0_CLKOUT_L0 | J3 | L1_CADIN_L6 | F29 |
| L0_CADOUT_H9 | N5 | L0_CLKOUT_L1 | K5 | L1_CADIN_L7 | E28 |
| L0_CADOUT_H10 | M4 | L0_COMP_PD | B2 | L1_CADIN_L8 | P26 |
| L0_CADOUT_H11 | L5 | L0_COMP_PU | C3 | L1_CADIN_L9 | N25 |
| L0_CADOUT_H12 | J5 | L0_CTLIN_H0 | B4 | L1_CADIN_L10 | M26 |
| L0_CADOUT_H13 | H4 | L0_CTLIN_L0 | A4 | L1_CADIN_L11 | L25 |
| L0_CADOUT_H14 | G5 | L0_CTLOUT_H0 | D1 | L1_CADIN_L12 | J25 |
| L0_CADOUT_H15 | F4 | L0_CTLOUT_L0 | D2 | L1_CADIN_L13 | H26 |
| L0_CADOUT_L0 | N3 | L1_CADIN_H0 | N27 | L1_CADIN_L14 | G25 |
| L0_CADOUT_L1 | M2 | L1_CADIN_H1 | M28 | L1_CADIN_L15 | F26 |
| L0_CADOUT_L2 | L3 | L1_CADIN_H2 | L27 | | |
| L0_CADOUT_L3 | K2 | L1_CADIN_H3 | K28 | | |
| L0_CADOUT_L4 | H2 | L1_CADIN_H4 | H28 | | |
| L0_CADOUT_L5 | G3 | L1_CADIN_H5 | G27 | | |
| L0_CADOUT_L6 | F2 | L1_CADIN_H6 | F28 | | |
| L0_CADOUT_L7 | E3 | L1_CADIN_H7 | E27 | | |
| L0_CADOUT_L8 | P5 | L1_CADIN_H8 | P25 | | |
| L0_CADOUT_L9 | N6 | L1_CADIN_H9 | N24 | | |
| L0_CADOUT_L10 | M5 | L1_CADIN_H10 | M25 | | |
| L0_CADOUT_L11 | L6 | L1_CADIN_H11 | L24 | | |
| L0_CADOUT_L12 | J6 | L1_CADIN_H12 | J24 | | |
| L0_CADOUT_L13 | H5 | L1_CADIN_H13 | H25 | | |

**Table 36. Signals Sorted by Name L1_CADOUT - V33**

| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball |
|---|---|---|---|---|---|
| L1_CADOUT_H0 | B17 | L1_CADOUT_L14 | F23 | REFCLK_H | A15 |
| L1_CADOUT_H1 | A18 | L1_CADOUT_L15 | E24 | REFCLK_L | B15 |
| L1_CADOUT_H2 | B19 | L1_CLKIN_H0 | J27 | VDDOK | U5 |
| L1_CADOUT_H3 | A20 | L1_CLKIN_H1 | K25 | STRAPL0 | U26 |
| L1_CADOUT_H4 | A22 | L1_CLKIN_L0 | J28 | STRAPL1 | U25 |
| L1_CADOUT_H5 | B23 | L1_CLKIN_L1 | K26 | TCK | V1 |
| L1_CADOUT_H6 | A24 | L1_CLKOUT_H0 | B21 | TDI | U4 |
| L1_CADOUT_H7 | B25 | L1_CLKOUT_H1 | D20 | TDO | U3 |
| L1_CADOUT_H8 | D16 | L1_CLKOUT_L0 | C21 | TEST | U1 |
| L1_CADOUT_H9 | E17 | L1_CLKOUT_L1 | E20 | TMS | U2 |
| L1_CADOUT_H10 | D18 | L1_COMP_PD | B28 | TRST_L | V5 |
| L1_CADOUT_H11 | E19 | L1_COMP_PU | C27 | V33 | T1 |
| L1_CADOUT_H12 | E21 | L1_CTLIN_H0 | D28 | V33 | T2 |
| L1_CADOUT_H13 | D22 | L1_CTLIN_L0 | D29 | V33 | T3 |
| L1_CADOUT_H14 | E23 | L1_CTLOUT_H0 | A26 | V33 | T27 |
| L1_CADOUT_H15 | D24 | L1_CTLOUT_L0 | B26 | V33 | T28 |
| L1_CADOUT_L0 | C17 | LDTREQ_L | T5 | V33 | T29 |
| L1_CADOUT_L1 | B18 | LDTRESET_L | T6 | | |
| L1_CADOUT_L2 | C19 | LDTSTOP_L | T4 | | |
| L1_CADOUT_L3 | B20 | NC | B3 | | |
| L1_CADOUT_L4 | B22 | NIOAIRQA_L | U28 | | |
| L1_CADOUT_L5 | C23 | NIOAIRQB_L | U27 | | |
| L1_CADOUT_L6 | B24 | NIOAIRQC_L | V29 | | |
| L1_CADOUT_L7 | C25 | NIOAIRQD_L | T26 | | |
| L1_CADOUT_L8 | E16 | PCIXA_100 | AB19 | | |
| L1_CADOUT_L9 | F17 | PCIXB_100 | AA19 | | |
| L1_CADOUT_L10 | E18 | PLL_VDDA1 | R28 | | |
| L1_CADOUT_L11 | F19 | PLL_VDDA2 | R29 | | |
| L1_CADOUT_L12 | F21 | PME_L | Y29 | | |
| L1_CADOUT_L13 | E22 | PWROK | U6 | | |

**Table 37. Signals Sorted by Name VDD - VDD**

| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball |
|---|---|---|---|---|---|
| VDD | G7 | VDD | G9 | VDD | K8 |
| VDD | C4 | VDD | G11 | VDD | K10 |
| VDD | C6 | VDD | G13 | VDD | K12 |
| VDD | C8 | VDD | G17 | VDD | K14 |
| VDD | C10 | VDD | G19 | VDD | K16 |
| VDD | C12 | VDD | G21 | VDD | K18 |
| VDD | C18 | VDD | G23 | VDD | K20 |
| VDD | C20 | VDD | H3 | VDD | K22 |
| VDD | C22 | VDD | H6 | VDD | K24 |
| VDD | C24 | VDD | H16 | VDD | K27 |
| VDD | C26 | VDD | H10 | VDD | L7 |
| VDD | D3 | VDD | H12 | VDD | L9 |
| VDD | D5 | VDD | E15 | VDD | L11 |
| VDD | D25 | VDD | H14 | VDD | L13 |
| VDD | D27 | VDD | H18 | VDD | L15 |
| VDD | E4 | VDD | H20 | VDD | L17 |
| VDD | E26 | VDD | H22 | VDD | L19 |
| VDD | F3 | VDD | H24 | VDD | L21 |
| VDD | F6 | VDD | H27 | VDD | L23 |
| VDD | F8 | VDD | J7 | VDD | M3 |
| VDD | F10 | VDD | J9 | VDD | M6 |
| VDD | F12 | VDD | J11 | VDD | M8 |
| VDD | F14 | VDD | J13 | VDD | M10 |
| VDD | F16 | VDD | J15 | VDD | M12 |
| VDD | F18 | VDD | J17 | VDD | M14 |
| VDD | F20 | VDD | J19 | VDD | M16 |
| VDD | F22 | VDD | J21 | VDD | M18 |
| VDD | F24 | VDD | J23 | VDD | M20 |
| VDD | F27 | VDD | K3 | VDD | M22 |
| VDD | G15 | VDD | K6 | VDD | M24 |

### Table 38. Signals Sorted by Name VDD - VIOA

| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball |
|---|---|---|---|---|---|
| VDD | M27 | VDD | T12 | VIOA | W19 |
| VDD | N7 | VDD | T14 | VIOA | W21 |
| VDD | N9 | VDD | T16 | VIOA | Y16 |
| VDD | N11 | VDD | T18 | VIOA | Y18 |
| VDD | N13 | VDD | T20 | VIOA | Y20 |
| VDD | N15 | VDD | T22 | VIOA | Y22 |
| VDD | N17 | VDDFB_H | G8 | | |
| VDD | N19 | VDDFB_L | H8 | | |
| VDD | N21 | VDD3FB_H | AB21 | | |
| VDD | N23 | VIOA | AA17 | | |
| VDD | P6 | VIOA | AA21 | | |
| VDD | P8 | VIOA | AA26 | | |
| VDD | P10 | VIOA | AB16 | | |
| VDD | P12 | VIOA | AB18 | | |
| VDD | P14 | VIOA | AB20 | | |
| VDD | P16 | VIOA | AB22 | | |
| VDD | P18 | VIOA | AD26 | | |
| VDD | P20 | VIOA | AF18 | | |
| VDD | P22 | VIOA | AF21 | | |
| VDD | P24 | VIOA | AF24 | | |
| VDD | R9 | VIOA | AF26 | | |
| VDD | R11 | VIOA | U17 | | |
| VDD | R13 | VIOA | U19 | | |
| VDD | R15 | VIOA | U21 | | |
| VDD | R17 | VIOA | V16 | | |
| VDD | R19 | VIOA | V18 | | |
| VDD | R21 | VIOA | V20 | | |
| VDD | R23 | VIOA | V22 | | |
| VDD | T8 | VIOA | V26 | | |
| VDD | T10 | VIOA | W17 | | |

**Table 39. Signals Sorted by Name VIOB - VSS**

| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball |
|---|---|---|---|---|---|
| VIOB | AA4 | VLDT | C14 | VSS | AA15 |
| VIOB | AA9 | VLDT | P1 | VSS | AA16 |
| VIOB | AA11 | VLDT | P2 | VSS | AA18 |
| VIOB | AA13 | VLDT | P3 | VSS | AA20 |
| VIOB | AB8 | VLDT | A16 | VSS | AA22 |
| VIOB | AB10 | VLDT | B16 | VSS | AA24 |
| VIOB | AB12 | VLDT | C16 | VSS | AA28 |
| VIOB | AB14 | VLDT | P27 | VSS | AB9 |
| VIOB | AD4 | VLDT | P28 | VSS | AB11 |
| VIOB | AF4 | VLDT | P29 | VSS | AB13 |
| VIOB | AF6 | VSS | F15 | VSS | AB15 |
| VIOB | AF9 | VSS | H7 | VSS | AB17 |
| VIOB | AF12 | VSS | A3 | VSS | AC15 |
| VIOB | U9 | VSS | A5 | VSS | AD2 |
| VIOB | U11 | VSS | A7 | VSS | AD6 |
| VIOB | U13 | VSS | A9 | VSS | AD9 |
| VIOB | V4 | VSS | A11 | VSS | AD12 |
| VIOB | V8 | VSS | A13 | VSS | AD15 |
| VIOB | V10 | VSS | A17 | VSS | AD18 |
| VIOB | V12 | VSS | A19 | VSS | AD21 |
| VIOB | V14 | VSS | A21 | VSS | AD24 |
| VIOB | W9 | VSS | A23 | VSS | AD28 |
| VIOB | W11 | VSS | A25 | VSS | AE15 |
| VIOB | W13 | VSS | A27 | VSS | AF15 |
| VIOB | Y8 | VSS | AA2 | VSS | AG2 |
| VIOB | Y10 | VSS | AA6 | VSS | AG15 |
| VIOB | Y12 | VSS | AA8 | VSS | AG28 |
| VIOB | Y14 | VSS | AA10 | VSS | AH3 |
| VLDT | A14 | VSS | AA12 | VSS | AH6 |
| VLDT | B14 | VSS | AA14 | VSS | AH9 |

**Table 40. Signals Sorted by Name VSS - VSS**

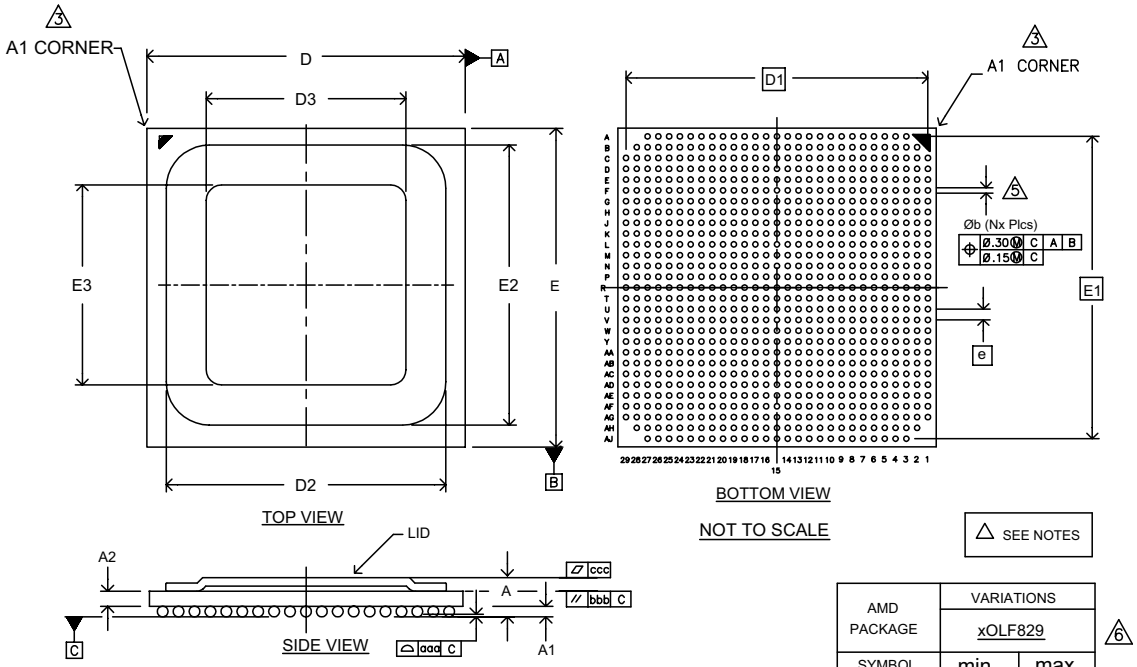
| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball |
|---|---|---|---|---|---|
| VSS | AH12 | VSS | G12 | VSS | K13 |
| VSS | AH15 | VSS | G14 | VSS | K15 |
| VSS | AH18 | VSS | G18 | VSS | K17 |
| VSS | AH21 | VSS | G20 | VSS | K19 |
| VSS | AH24 | VSS | G22 | VSS | K21 |
| VSS | AH27 | VSS | G26 | VSS | K23 |
| VSS | AJ15 | VSS | G29 | VSS | L1 |
| VSS | B27 | VSS | H15 | VSS | L4 |
| VSS | C1 | VSS | H9 | VSS | L8 |
| VSS | C2 | VSS | H11 | VSS | L10 |
| VSS | C15 | VSS | H13 | VSS | L12 |
| VSS | C28 | VSS | H17 | VSS | L14 |
| VSS | C29 | VSS | H19 | VSS | L16 |
| VSS | D7 | VSS | H21 | VSS | L18 |
| VSS | D9 | VSS | H23 | VSS | L20 |
| VSS | D11 | VSS | J1 | VSS | L22 |
| VSS | D13 | VSS | J4 | VSS | L26 |
| VSS | D15 | VSS | J8 | VSS | L29 |
| VSS | D17 | VSS | J10 | VSS | M7 |
| VSS | D19 | VSS | J12 | VSS | M9 |
| VSS | D21 | VSS | J14 | VSS | M11 |
| VSS | D23 | VSS | J16 | VSS | M13 |
| VSS | D26 | VSS | J18 | VSS | M15 |
| VSS | E1 | VSS | J20 | VSS | M17 |
| VSS | E25 | VSS | J22 | VSS | M19 |
| VSS | E29 | VSS | J26 | VSS | M21 |
| VSS | G1 | VSS | J29 | VSS | M23 |
| VSS | G4 | VSS | K7 | VSS | N1 |
| VSS | G16 | VSS | K9 | VSS | N4 |
| VSS | G10 | VSS | K11 | VSS | N8 |

**Table 41. Signals Sorted by Name VSS - VSS**

| Signal Name | Ball | Signal Name | Ball | Signal Name | Ball |
|---|---|---|---|---|---|
| VSS | N10 | VSS | R18 | VSS | V15 |
| VSS | N12 | VSS | R20 | VSS | V17 |
| VSS | N14 | VSS | R22 | VSS | V19 |
| VSS | N16 | VSS | R24 | VSS | V21 |
| VSS | N18 | VSS | R25 | VSS | V24 |
| VSS | N20 | VSS | R26 | VSS | V28 |
| VSS | N22 | VSS | R27 | VSS | W8 |
| VSS | N26 | VSS | T7 | VSS | W10 |
| VSS | N29 | VSS | T9 | VSS | W12 |
| VSS | P7 | VSS | T11 | VSS | W14 |
| VSS | P9 | VSS | T13 | VSS | W15 |
| VSS | P11 | VSS | T15 | VSS | W16 |
| VSS | P13 | VSS | T17 | VSS | W18 |
| VSS | P15 | VSS | T19 | VSS | W20 |
| VSS | P17 | VSS | T21 | VSS | W22 |
| VSS | P19 | VSS | T23 | VSS | Y9 |
| VSS | P21 | VSS | U8 | VSS | Y11 |
| VSS | P23 | VSS | U10 | VSS | Y13 |
| VSS | R1 | VSS | U12 | VSS | Y15 |
| VSS | R2 | VSS | U14 | VSS | Y17 |
| VSS | R3 | VSS | U15 | VSS | Y19 |
| VSS | R4 | VSS | U16 | VSS | Y21 |
| VSS | R5 | VSS | U18 | | |
| VSS | R6 | VSS | U20 | | |
| VSS | R7 | VSS | U22 | | |
| VSS | R8 | VSS | V2 | | |
| VSS | R10 | VSS | V6 | | |
| VSS | R12 | VSS | V9 | | |
| VSS | R14 | VSS | V11 | | |
| VSS | R16 | VSS | V13 | | |

# 8.1 Package Specification

### Figure 25. Package Mechanical Drawing.




| AMD PACKAGE | VARIATIONS | |
|---|---|---|
| | xOLF829 | |
| SYMBOL | min. | max. |
| D/E | 30.8 | 31.2 |
| D1/E1 | 28.00 BSC. | |
| D2/E2 | 27.8 | 28.2 |
| D3/E3 | 22.8 | 23.2 |
| A | 3.25 | 3.56 |
| A1 | 0.40 | 0.60 |
| A2 | 1.00 | 1.20 |
| e | 1.00 BSC | |
| Øb | 0.50 | 0.70 |
| M | 29 | |
| N | 829 | |
| aaa | 0.200 | |
| bbb | 0.250 | |
| ccc | 0.125 | |
| WT (gms) | XXX REF | |

GENERAL NOTES

1. All dimensions are specified in millimeters (mm).
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. This corner is marked with a triangle on both sides of the package identifies ball A1 corner and can be used for handling and orientation purposes.
4. Symbol "M" determines ball matrix size and "N" is number of balls.
5. Dimension "b" is measured at maximum solder ball diameter on a plane parallel to datum C.
6. "x" in front of package variation denotes non-qualified package per AMD 01-002.3.
7. The following features are not shown on drawings:
   a) Marking on die, label on package
   b) Laser elements
   c) Die and passive fudicials

# Appendix A Ordering Part Number