

# SN74ALS233B

## 16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

SCAS253B – MARCH 1990 – REVISED APRIL 1998

- Independent Asynchronous Inputs and Outputs
- 16 Words by 5 Bits
- Data Rates From up to 40 MHz
- Fall-Through Time 14 ns Typ
- 3-State Outputs
- Package Options Include Plastic Small-Outline Package (DW), Plastic Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)

### description

This 80-bit memory uses advanced low-power Schottky technology and features high speed and a fast fall-through time. It is organized as 16 words by 5 bits.

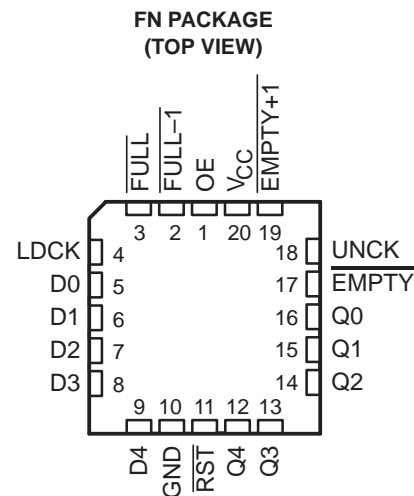
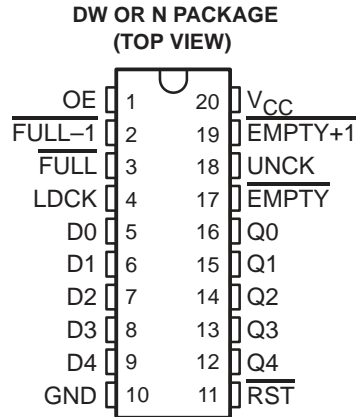
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates up to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the  $\overline{FULL}$ ,  $\overline{EMPTY}$ ,  $\overline{FULL-1}$ , and  $\overline{EMPTY+1}$  output flags. The  $\overline{FULL}$  output is low when the memory is full and high when it is not full. The  $\overline{FULL-1}$  output is low when the memory contains 15 data words. The  $\overline{EMPTY}$  output is low when the memory is empty and high when it is not empty. The  $\overline{EMPTY+1}$  output is low when one word remains in memory.

A low level on the reset ( $\overline{RST}$ ) input resets the internal stack control pointers and also sets  $\overline{EMPTY}$  low and sets  $\overline{FULL}$ ,  $\overline{FULL-1}$ , and  $\overline{EMPTY+1}$  high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a  $\overline{RST}$  pulse or from an empty condition, causes  $\overline{EMPTY}$  to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS233B is characterized for operation from 0°C to 70°C.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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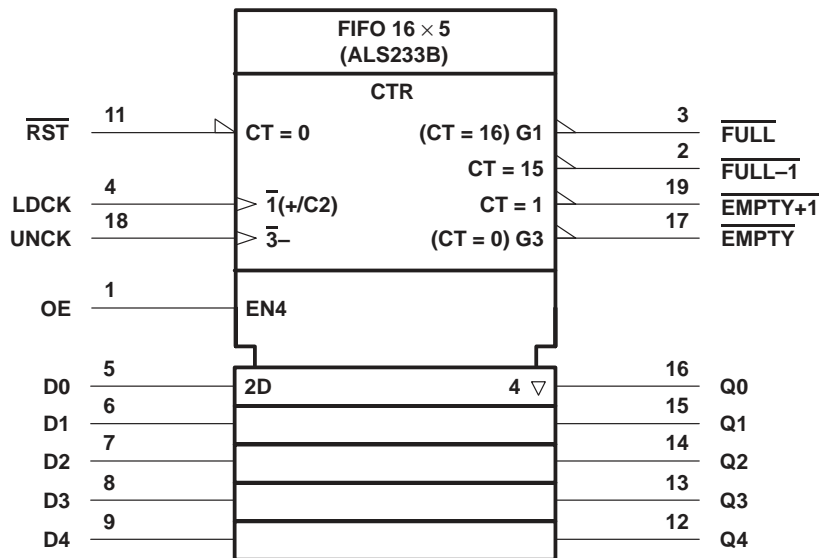
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# SN74ALS233B

## 16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

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### logic symbol†



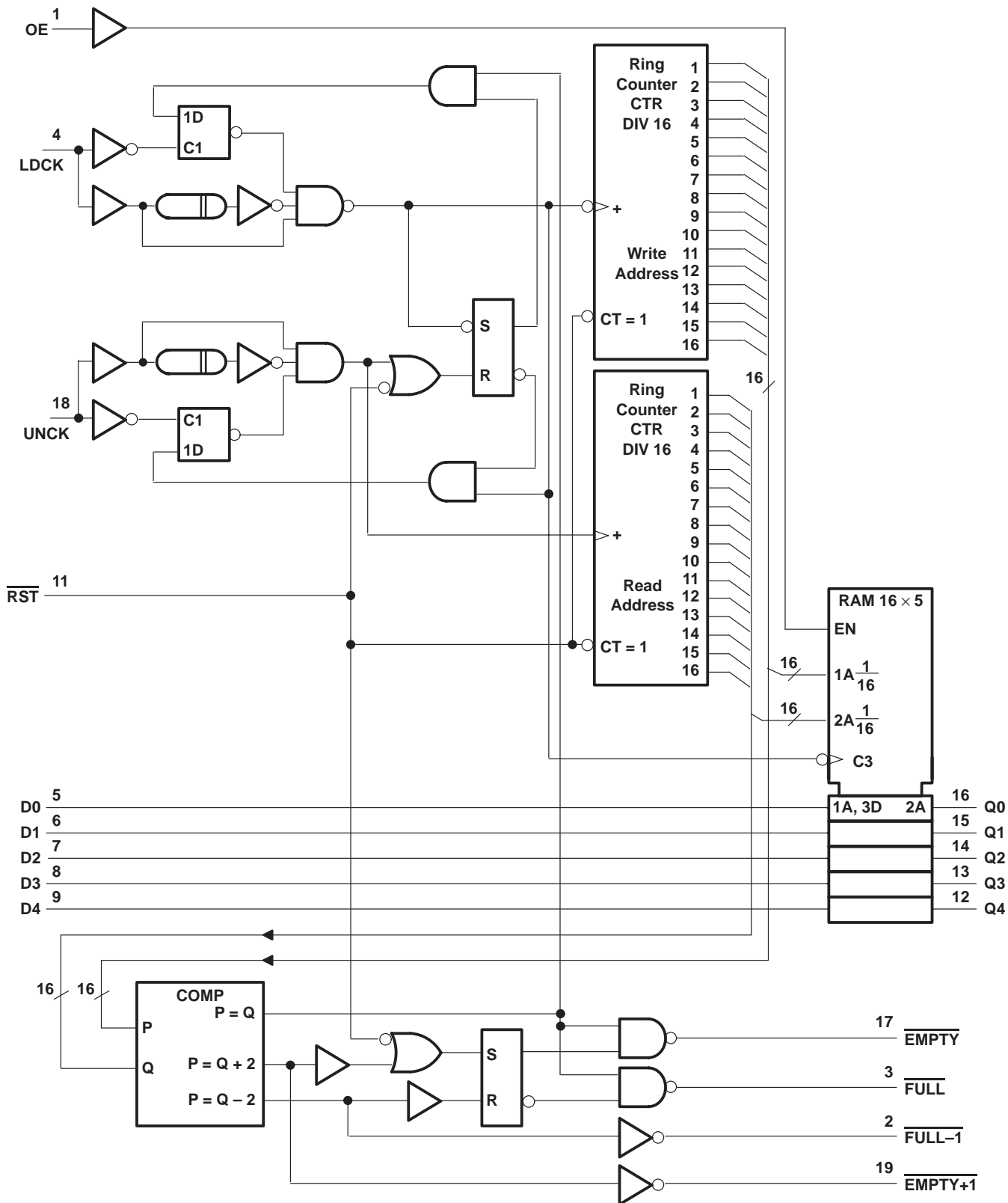
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

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logic diagram (positive logic)

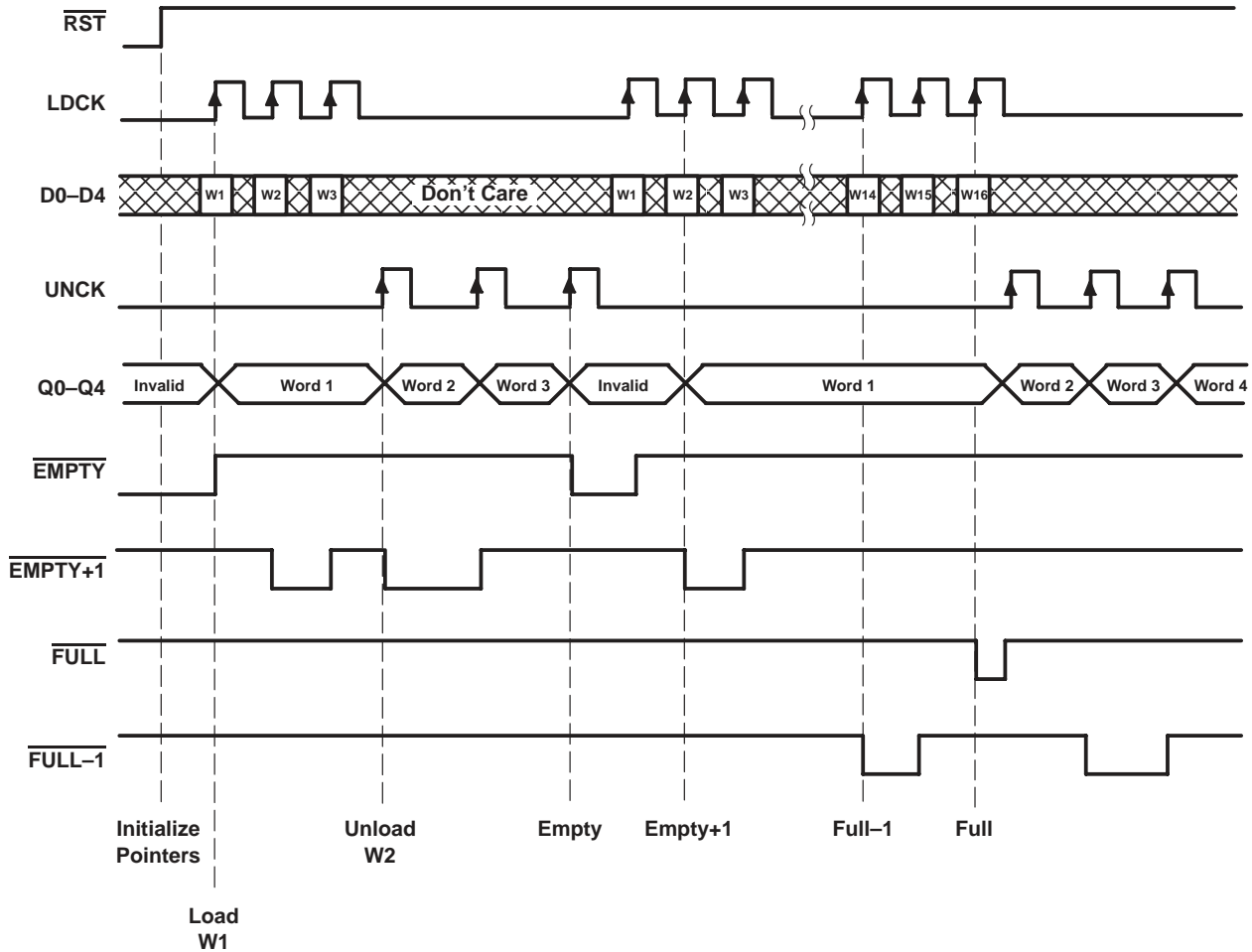


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## 16 × 5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

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### timing diagram



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ .....	7 V
Voltage applied to a disabled 3-state output .....	5.5 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): DW package .....	97°C/W
FN package .....	83°C/W
N package .....	67°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



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### recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>OH</sub>	High-level output current	Q outputs		-1.6	mA
		Status flags		-0.4	
I <sub>OL</sub>	Low-level output current	Q outputs		24	mA
		Status flags		8	
T <sub>A</sub>	Operating free-air temperature	0		70	°C

NOTE 2: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V<sub>IL</sub>, V<sub>IH</sub>, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>	Q outputs	V <sub>CC</sub> = 4.5 V,	I <sub>OH</sub> = -2.6 mA	2.4	3.2		V
	Status flags	V <sub>CC</sub> = 4.5 V to 5.5 V,	I <sub>OH</sub> = -0.4 mA	V <sub>CC</sub> -2			
V <sub>OL</sub>	Q outputs	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 12 mA		0.25	0.4	V
			I <sub>OL</sub> = 24 mA		0.35	0.5	
	Status flags	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 4 mA		0.25	0.4	
			I <sub>OL</sub> = 8 mA		0.35	0.5	
I <sub>OZH</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			20	μA
I <sub>OZL</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.4 V			-20	μA
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V			0.1	mA
I <sub>IH</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20	μA
I <sub>IL</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.4 V			-0.2	mA
I <sub>O‡</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.25 V	-30		-112	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V			88	133	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I<sub>OS</sub>.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

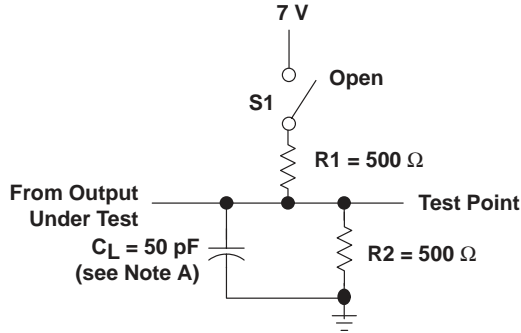
		MIN	NOM	MAX	UNIT
f <sub>clock</sub>	Clock frequency	LDCK		40	MHz
		UNCK		40	
t <sub>w</sub>	Pulse duration	RST <sup>̄</sup> low	18		ns
		LDCK low	15		
		LDCK high	10		
		UNCK low	15		
		UNCK high	10		
t <sub>su</sub>	Setup time	Data before LDCK↑	8		ns
		RST <sup>̄</sup> (inactive) before LDCK↑	5		
		LDCK (inactive) before RST↑	5		
t <sub>h</sub>	Hold time	Data after LDCK↑	5		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f <sub>max</sub>	LDCK, UNCK		40		MHz
t <sub>pd</sub>	LDCK↑	Any Q	6	32	ns
	UNCK↑		6	30	
t <sub>PLH</sub>	LDCK↑	EMPTY <sup>̄</sup>	5	25	ns
t <sub>PHL</sub>	UNCK↑	EMPTY <sup>̄</sup>	6	27	ns
	RST↓		5	25	
t <sub>pd</sub>	LDCK↑	EMPTY+1 <sup>̄</sup>	7	34	ns
	UNCK↑		7	34	
t <sub>PLH</sub>	RST↓	EMPTY+1 <sup>̄</sup>	8	31	ns
t <sub>pd</sub>	LDCK↑	FULL-1 <sup>̄</sup>	9	33	ns
	UNCK↑		8	32	
t <sub>PLH</sub>	RST↓	FULL-1 <sup>̄</sup>	11	32	ns
t <sub>PHL</sub>	LDCK↑	FULL <sup>̄</sup>	6	27	ns
t <sub>PLH</sub>	UNCK↑	FULL <sup>̄</sup>	5	25	ns
	RST↓		9	30	
t <sub>en</sub>	OE↑	Q	2	15	ns
t <sub>dis</sub>	OE↓	Q	1	15	ns

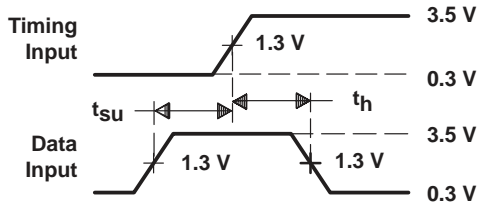


**PARAMETER MEASUREMENT INFORMATION**

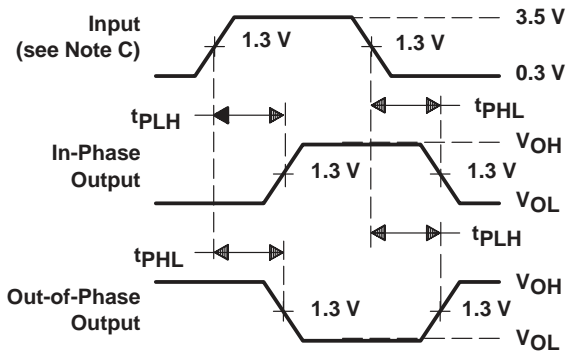


**LOAD CIRCUIT FOR 3-STATE OUTPUTS**

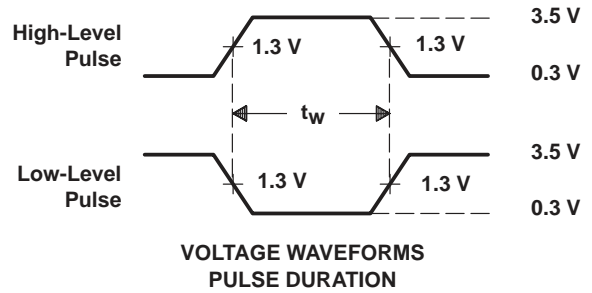
PARAMETER	S1	
$t_{en}$	$t_{PZH}$	Open
	$t_{PZL}$	Closed
$t_{dis}$	$t_{PHZ}$	Open
	$t_{PLZ}$	Closed
$t_{pd}$	$t_{PLH}$	Open
	$t_{PHL}$	Open



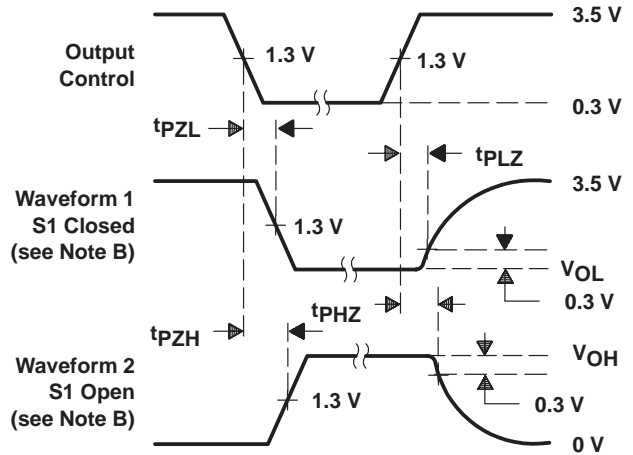
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ALS233BDW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74ALS233BDWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74ALS233BFN	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI
SN74ALS233BN	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



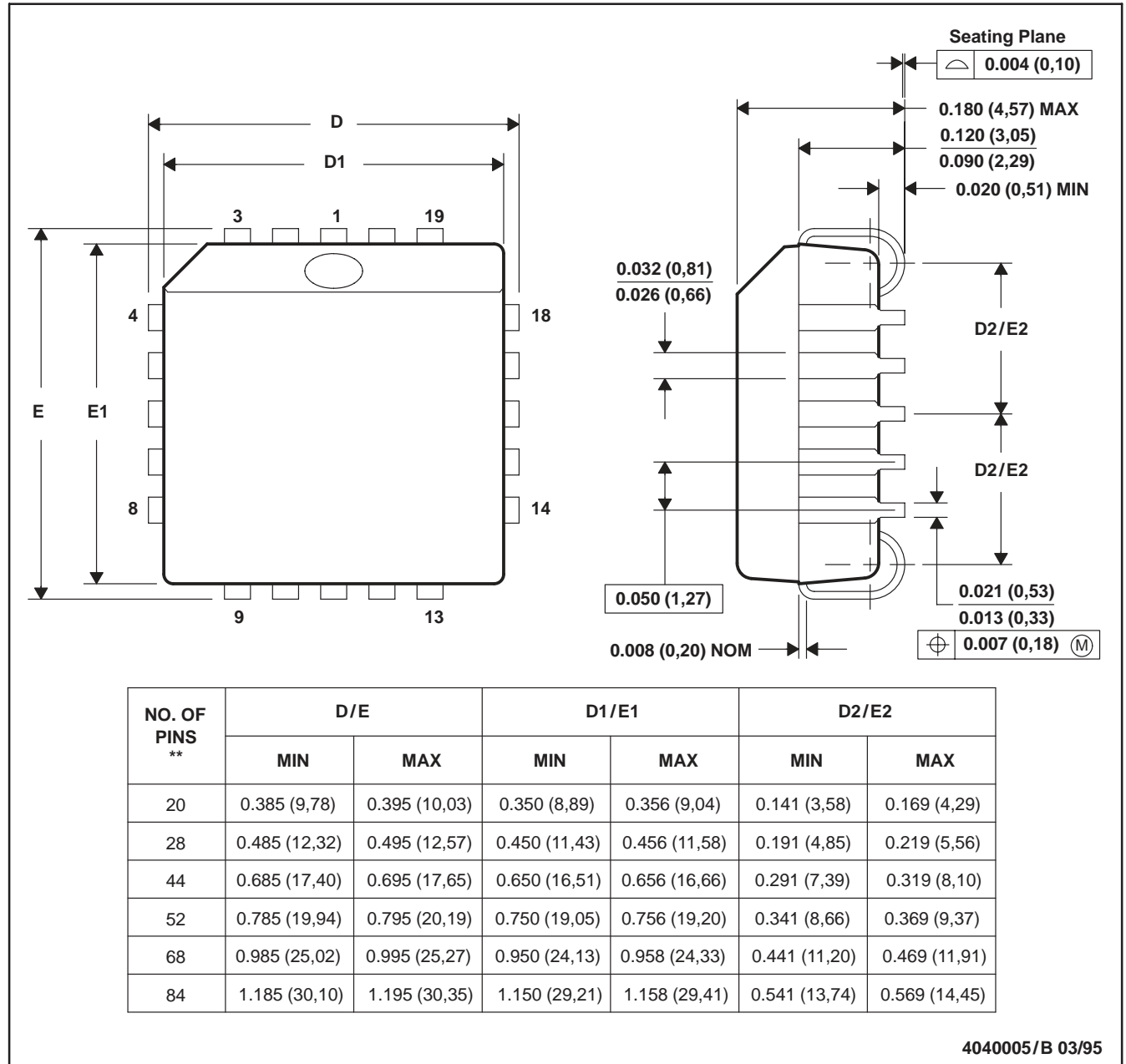
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



FN (S-PQCC-J\*\*)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74ALS233BDW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS233BDWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS233BFN	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS233BN	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

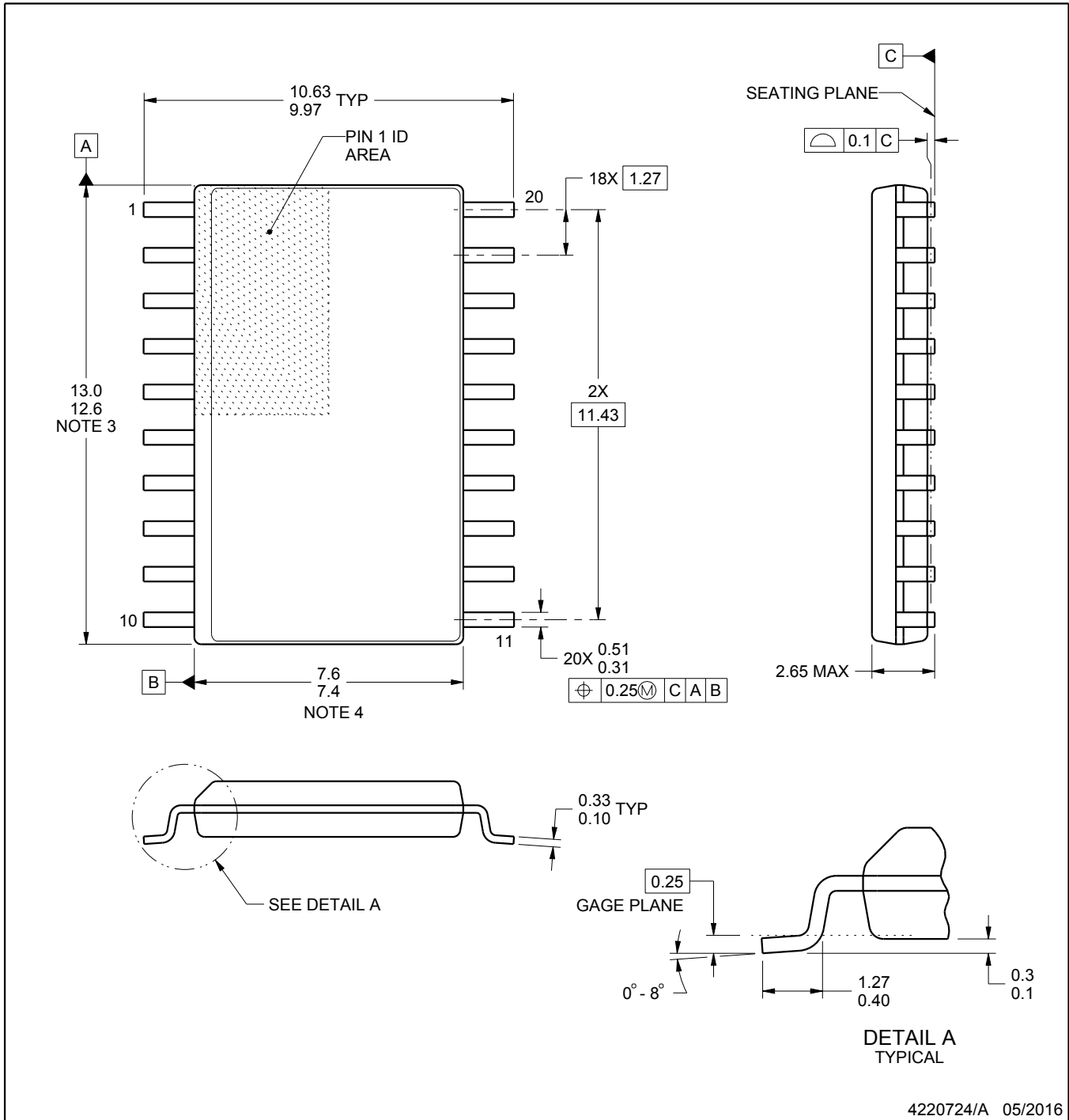
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

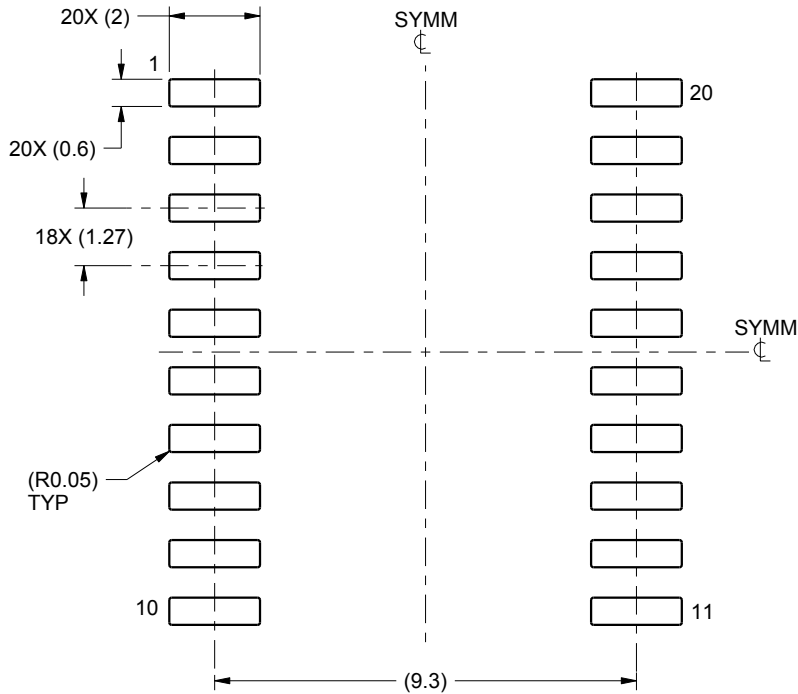
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

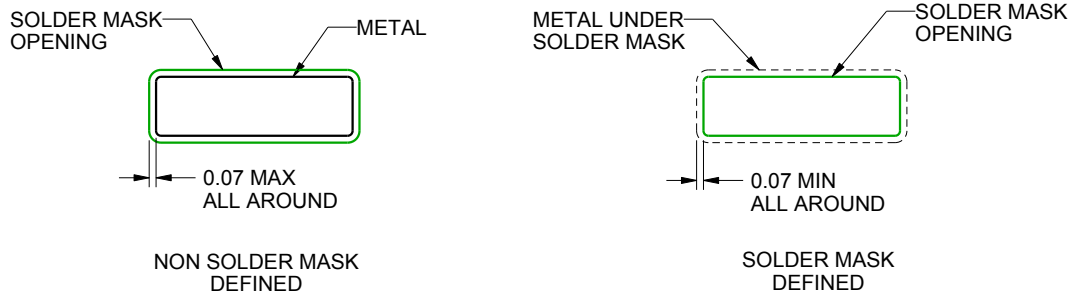
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

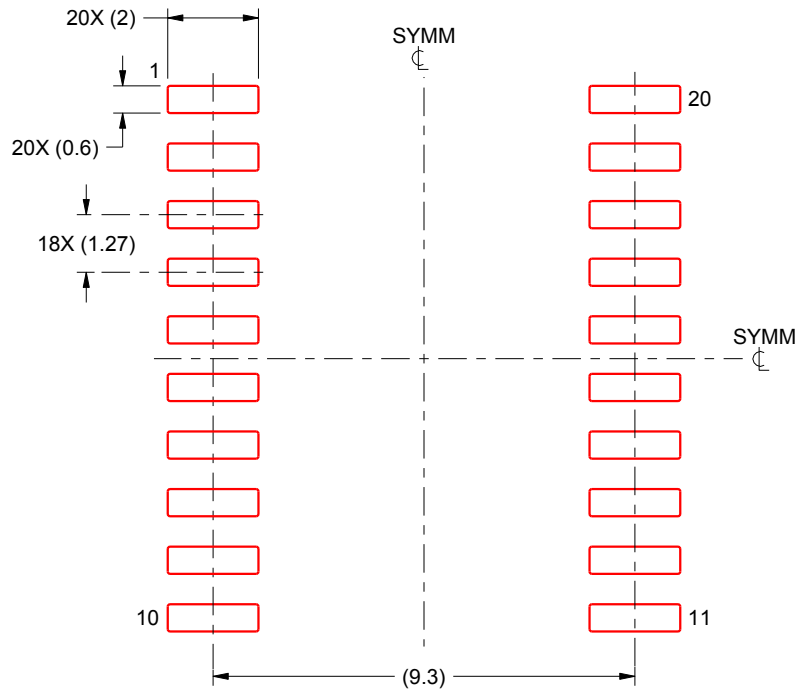
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.





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### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
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