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TRF3705

SLWS223B-AUGUST 2011-REVISED NOVEMBER 2015

TRF3705 300-MHz to 4-GHz Quadrature Modulator

Technical

Documents

1 Features

- High Linearity:
 - Output IP3: 30 dBm at 1850 MHz
- Low Output Noise Floor: -160 dBm/Hz
- 78-dBc Single-Carrier WCDMA ACPR at –10-dBm Channel Power
- Unadjusted Carrier Suppression: -40 dBm
- Unadjusted Sideband Suppression: -45 dBc
- Single Supply: 3.3-V Operation
- 1-bit Gain Step Control
- Fast Power-Up/Power-Down

2 Applications

- Cellular Base Station Transmitter
- CDMA: IS95, UMTS, CDMA2000, TD-SCDMA
- LTE (Long Term Evolution)
- TDMA: GSM, EDGE/UWC-136
- Multicarrier GSM (MC-GSM)
- Wireless MAN Wideband Transceivers

3 Description

The TRF3705 is a low-noise direct quadrature modulator, capable of converting complex modulated signals from baseband or IF directly up to RF. The TRF3705 is a high-performance, superior-linearity device that is ideal to up-convert to RF frequencies of 300 MHz (Note: appropriate matching network is required for optimal performance at 300 MHz) through 4 GHz. The modulator is implemented as a double-balanced mixer.

The RF output block consists of a differential-tosingle-ended converter that is capable of driving a single-ended 50- Ω load. The TRF3705 requires a 0.25-V common-mode voltage for optimum linearity performance. The TRF3705 also provides a fast power-down pin that can be used to reduce power dissipation in TDD applications.

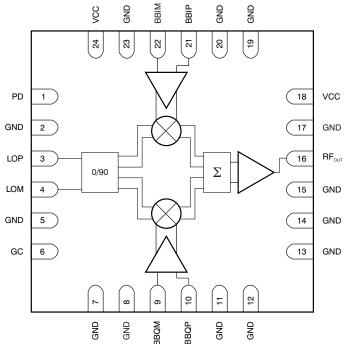
The TRF3705 is available in an RGE-24 VQFN package.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRF3705	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.





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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	hanges from Revision A (October 2011) to Revision B	Page
•	Added the ESD table, Detailed Description, Application and Implementation, Device and Documentation Support, Mechanical, Packaging, and Orderable Information	1
•	Added Note 1 to Figure 65	23
•	Changed the X-axis label of Figure 75 From: Frequency (MHz) To: LO Power (dBm)	28
•	Changed Figure 77	32

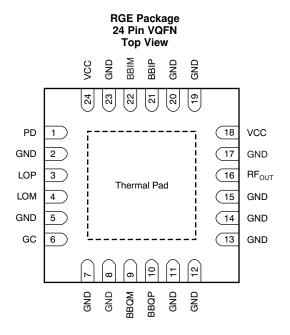
Changes from Original (August 2011) to Revision A

Changed t	he device From: Preview	To: Production
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5 Pin Configuration and Functions



Pin Functions

PIN			DECODIDEION
NO.	NAME	I/O	DESCRIPTION
1	PD	I	Power-down digital input (high = device off)
2	GND	I	Ground
3	LOP	I	Local oscillator input
4	LOM	I	Local oscillator input
5	GND	I	Ground
6	GC	I	Gain control digital input (high = high gain)
7	GND	—	Ground or leave unconnected
8	GND	I	Ground
9	BBQM	I	In-quadrature input
10	BBQP	I	In-quadrature input
11	GND	I	Ground
12	GND	I	Ground
13	GND	I	Ground
14	GND	I	Ground
15	GND	I	Ground
16	RF _{OUT}	0	RF output
17	GND	I	Ground
18	VCC	I	Power supply
19	GND	I	Ground
20	GND	I	Ground
21	BBIP	Ι	In-phase input
22	BBIM	I	In-phase input
23	GND	I	Ground
24	VCC	Ι	Power supply

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

	MIN	МАХ	UNIT
Supply voltage range ⁽²⁾	-0.3	6	V
Digital I/O voltage range	-0.3	$V_{CC} + 0.5$	V
Operating virtual junction temperature range, T _J	-40	150	°C
Operating ambient temperature range, T _A	-40	85	°C
Storage temperature range, T _{stg}	-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 $^{\left(2\right) }$	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V _{CC}	Power-supply voltage	3.15	3.3	3.6	V

6.4 Thermal Information

		TRF3705	
	THERMAL METRIC ⁽¹⁾	RGE (VQFN)	UNIT
		24 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	38.4	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	42.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	16.6	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	6.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.



6.5 Electrical Characteristics: General

Over recommended operating conditions; at power supply = 3.3 V and T_A = +25°C, unless otherwise noted.

	PARAMETERS	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
DC PAR	AMETERS					
		$T_A = +25^{\circ}C$, device on (PD = low)		306		mA
ICC	Total supply current	$T_A = +25^{\circ}C$, device off (PD = high)		35		μA
LO INPL	Л					
	LO low frequency			300		MHz
f _{LO}	LO high frequency			4000		MHz
	LO input power		-10	0	+15	dBm
BASEBA	AND INPUTS					
V _{CM}	I and Q input dc common-mode voltage			0.25	0.5	V
BW	1-dB input frequency bandwidth			1000		MHz
7	1	Resistance		8		kΩ
ZI	Input impedance	Parallel capacitance		4.6		pF
POWER	ON/OFF					
	Turn on time	PD = low to 90% final output power		0.2		μs
	Turn off time	PD = high to initial output power -30 dB		0.2		μs
DIGITAL	INTERFACE					
V _{IH}	PD high-level input voltage		2			V
VIL	PD low-level input voltage				0.8	V

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6.6 Electrical Characteristics

	PARAMETERS	TEST CONDITIONS	MIN TYP MAX	UNIT
i _{lo} = 400 l	MHz			
G	Voltago gain	Output RMS voltage over input I (or Q) RMS voltage, GC set low	-4.7	dB
G	Voltage gain	Output RMS voltage over input I (or Q) RMS voltage, GC set high	-1.9	dB
D	2.1.1	GC set low	-0.7	dBm
Pout	Output power	GC set high	2.1	dBm
	2 · · · · · · · · · · ·	GC set low	8.5	dBm
P1dB	Output compression point	GC set high	9.1	dBm
Do	0.1.1.100	f _{BB1} = 4.5 MHz; f _{BB2} = 5.5 MHz; GC set low	26	dBm
P3	Output IP3	f _{BB1} = 4.5 MHz; f _{BB2} = 5.5 MHz; GC set high	25.4	dBm
D 0	0.1.170	Measured at f _{LO} + (f _{BB1} ± f _{BB2}), GC set low	60.2	dBm
P2	Output IP2	Measured at f _{LO} + (f _{BB1} ± f _{BB2}), GC set high	61.9	dBm
SBS	Unadjusted sideband suppression		-57.4	dBc
CF		Measured at LO frequency	-51.6	dBm
	Unadjusted carrier feedthrough	Measured at 2 x LO	-50	dBm
		Measured at 3 x LO	-49	dBm
	Output noise floor	DC only to BB inputs; 10-MHz offset from LO	-166.7	dBm/Hz
HD2 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V _{PP} each at f_{LO} ±(2 x f_{BB})	-67	dBc
HD3 _{BB}	Baseband harmonics	Measured with \pm 1-MHz tone at 0.5 V _{PP} each at f _{LO} \pm (3 x f _{BB})	-64	dBc
f _{LO} = 750 l	MHz			
-	Voltage gain	Output RMS voltage over input I (or Q) RMS voltage, GC set low	0.2	dB
G		Output RMS voltage over input I (or Q) RMS voltage, GC set high	3.0	dB
_	2.1.1	GC set low	4.2	dBm
ООТ	Output power	GC set high	7	dBm
	2 · · · · · · · · ·	GC set low	13.3	dBm
P1dB	Output compression point	GC set high	13.9	dBm
		f _{BB1} = 4.5 MHz; f _{BB2} = 5.5 MHz; GC set low	31.5	dBm
P3	Output IP3	f _{BB1} = 4.5 MHz; f _{BB2} = 5.5 MHz; GC set high	30.8	dBm
D.a.	0.1.170	Measured at f _{LO} + (f _{BB1} ± f _{BB2}), GC set low	73.6	dBm
P2	Output IP2	Measured at f _{LO} + (f _{BB1} ± f _{BB2}), GC set high	80.5	dBm
SBS	Unadjusted sideband suppression		-45.2	dBc
		Measured at LO frequency	-45.7	dBm
CF	Unadjusted carrier feedthrough	Measured at 2 x LO	-46	dBm
		Measured at 3 x LO	-53.5	dBm
	Output noise floor	DC only to BB inputs; 10-MHz offset from LO	-159.9	dBm/Hz
HD2 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V_{PP} each at f_{LO} ±(2 x $f_{BB})$	-70	dBc
HD3 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V_{PP} each at f_{LO} ±(3 x f_{BB})	-66	dBc



Electrical Characteristics (continued)

	PARAMETERS	TEST CONDITIONS	MIN TYP MAX	UNIT
f _{LO} = 900 l	MHz			
0	Valtage gein	Output RMS voltage over input I (or Q) RMS voltage, GC set low	0.3	dB
G	Voltage gain	Output RMS voltage over input I (or Q) RMS voltage, GC set high	3.1	dB
-	2	GC set low	4.3	dBm
Pout	Output power	GC set high	7.1	dBm
	Output commencies activit	GC set low	13.2	dBm
P1dB	Output compression point	GC set high	13.7	dBm
Do	0.1.1.100	f _{BB1} = 4.5 MHz; f _{BB2} = 5.5 MHz; GC set low	31.7	dBm
IP3	Output IP3	f_{BB1} = 4.5 MHz; f_{BB2} = 5.5 MHz; GC set high	30.9	dBm
DO		Measured at f_{LO} + ($f_{BB1} \pm f_{BB2}$), GC set low	71.5	dBm
IP2	Output IP2	Measured at f _{LO} + (f _{BB1} ± f _{BB2}), GC set high	75.3	dBm
SBS	Unadjusted sideband suppression		-43.8	dBc
		Measured at LO frequency	-48.5	dBm
CF	Unadjusted carrier feedthrough	Measured at 2 x LO	-53	dBm
		Measured at 3 x LO	50	dBm
	Output noise floor	DC only to BB inputs; 10-MHz offset from LO	-157.9	dBm/H:
HD2 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V _{PP} each at $f_{LO} \pm (2 \times f_{BB})$	-80	dBc
HD3 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V_{PP} each at f_{LO} ±(3 \times $f_{BB})$	-65	dBc
f _{LO} = 1840	MHz			1
•	•	Output RMS voltage over input I (or Q) RMS voltage, GC set low	-0.1	dB
G	Voltage gain	Output RMS voltage over input I (or Q) RMS voltage, GC set high	2.5	dB
D	0.1.1	GC set low	3.9	dBm
P _{OUT}	Output power	GC set high	6.5	dBm
	2 · · · · · · · · · · · · · · · · · · ·	GC set low	13.2	dBm
P1dB	Output compression point	GC set high	13.6	dBm
	0.1.1.100	f _{BB1} = 4.5 MHz; f _{BB2} = 5.5 MHz; GC set low	32.1	dBm
IP3	Output IP3	f_{BB1} = 4.5 MHz; f_{BB2} = 5.5 MHz; GC set high	30.3	dBm
		Measured at f_{LO} + ($f_{BB1} \pm f_{BB2}$), GC set low	60.8	dBm
IP2	Output IP2	Measured at f_{LO} + ($f_{BB1}\pm f_{BB2}$), GC set high	62	dBm
SBS	Unadjusted sideband suppression		-43.4	dBc
		Measured at LO frequency	-42.4	dBm
CF	Unadjusted carrier feedthrough	Measured at 2 x LO	-41	dBm
		Measured at 3 x LO	-53	dBm
	Output noise floor	DC only to BB inputs; 10-MHz offset from LO	-158.8	dBm/H
HD2 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V_{PP} each at f_{LO} ±(2 x $f_{BB})$	-69	dBc
HD3 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V _{PP} each at f_{LO} ±(3 × f_{BB})	-80	dBc

Electrical Characteristics (continued)

	PARAMETERS	TEST CONDITIONS	MIN TYP MAX	UNIT
f _{LO} = 2140	MHz			
0	Voltoro roin	Output RMS voltage over input I (or Q) RMS voltage, GC set low	0.1	dB
G	Voltage gain	Output RMS voltage over input I (or Q) RMS voltage, GC set high	2.9	dB
D	Output nower	GC set low	4.1	dBm
Pout	Output power	GC set high	6.9	dBm
	Output commencies activit	GC set low	13.1	dBm
P1dB	Output compression point	GC set high	13.5	dBm
		f_{BB1} = 4.5 MHz; f_{BB2} = 5.5 MHz; GC set low	28.6	dBm
P3 Output IP3		$f_{BB1} = 4.5 \text{ MHz}; f_{BB2} = 5.5 \text{ MHz}; \text{GC set high}$	27.6	dBm
	Output ID0	Measured at f_{LO} + ($f_{BB1} \pm f_{BB2}$), GC set low	65.5	dBm
IP2	Output IP2	Measured at f_{LO} + ($f_{BB1}\pm f_{BB2}$), GC set high	68.2	dBm
SBS	Unadjusted sideband suppression		-45.6	dBc
		Measured at LO frequency	-39.3	dBm
CF	Unadjusted carrier feedthrough	Measured at 2 x LO	-37	dBm
		Measured at 3 x LO	-46	dBm
	Output noise floor	DC only to BB inputs; 10-MHz offset from LO	-160.0	dBm/H
HD2 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V_{PP} each at f_{LO} ±(2 x $f_{BB})$	-61	dBc
HD3 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V_{PP} each at f_{LO} ±(3 x $f_{BB})$	-60	dBc
f _{LO} = 2600	MHz	1		
0	-	Output RMS voltage over input I (or Q) RMS voltage, GC set low	-0.8	dB
G	Voltage gain	Output RMS voltage over input I (or Q) RMS voltage, GC set high	2	dB
D		GC set low	3.2	dBm
P _{OUT}	Output power	GC set high	5.6	dBm
	Output commencies activit	GC set low	12.5	dBm
P1dB	Output compression point	GC set high	12.8	dBm
		f_{BB1} = 4.5 MHz; f_{BB2} = 5.5 MHz; GC set low	28	dBm
IP3	Output IP3	$Ff_{BB1} = 4.5 \text{ MHz}; f_{BB2} = 5.5 \text{ MHz}; GC \text{ set high}$	27.2	dBm
		Measured at f _{LO} + (f _{BB1} ± f _{BB2}), GC set low	67.9	dBm
IP2	Output IP2	Measured at f _{LO} + (f _{BB1} ± f _{BB2}), GC set high	66.4	dBm
SBS	Unadjusted sideband suppression		-52.9	dBm
		Measured at LO frequency	-37.8	dBm
CF	Unadjusted carrier feedthrough	Measured at 2 x LO	-41	dBm
		Measured at 3 x LO	-42	dBm
	Output noise floor	DC only to BB inputs; 10-MHz offset from LO	-160.6	dBm/H
HD2 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V_{PP} each at f_{LO} ±(2 x $f_{BB})$	-67	dBc
HD3 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V _{PP} each at f_{LO} ±(3 x f_{BB})	-59	dBc



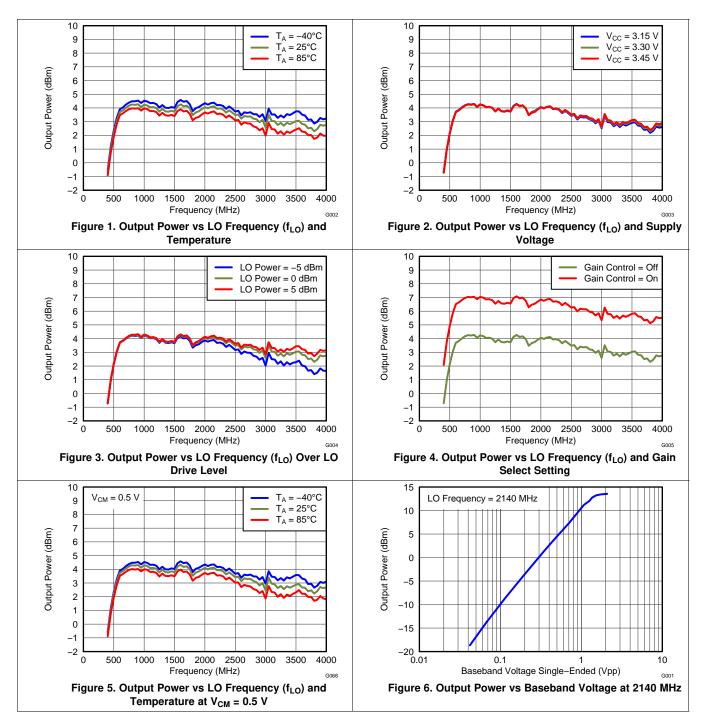
Electrical Characteristics (continued)

	PARAMETERS	TEST CONDITIONS	MIN TYP	MAX	UNIT
f _{LO} = 3500) MHz	·			
0	Vellere seis	Output RMS voltage over input I (or Q) RMS voltage, GC set low	-1		dB
G Voltage gain	Output RMS voltage over input I (or Q) RMS voltage, GC set high	1.8		dB	
D		GC set low	3		dBm
P _{OUT}	Output power	GC set high	5.8		dBm
P1dB	Output compression point	GC set low	12.1		dBm
PIUB	P1dB Output compression point	GC set high	12.3		dBm
	P3 Output IP3	f_{BB1} = 4.5 MHz; f_{BB2} = 5.5 MHz; GC set low	23.8		dBm
123	Output IP3	f_{BB1} = 4.5 MHz; f_{BB2} = 5.5 MHz; GC set high	25.3		dBm
IP2	Output IP2	Measured at f_{LO} + ($f_{BB1} \pm f_{BB2}$), GC set low	47.8		dBm
IP2	Output IP2	Measured at f_{LO} + ($f_{BB1}\pm f_{BB2}$), GC set high	48.6		dBm
SBS	Unadjusted sideband suppression		-45.2		dBm
		Measured at LO frequency	-31.6		dBm
CF	Unadjusted carrier feedthrough	Measured at 2 x LO	-30		dBm
		Measured at 3 x LO	-53		dBm
	Output noise floor	DC only to BB inputs; 10-MHz offset from LO	-160.6		dBm/Hz
HD2 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V_{PP} each at f_{LO} ±(2 x $f_{BB})$	-54		dBc
HD3 _{BB}	Baseband harmonics	Measured with ±1-MHz tone at 0.5 V_{PP} each at f_{LO} ±(3 x $f_{BB})$	-50		dBc

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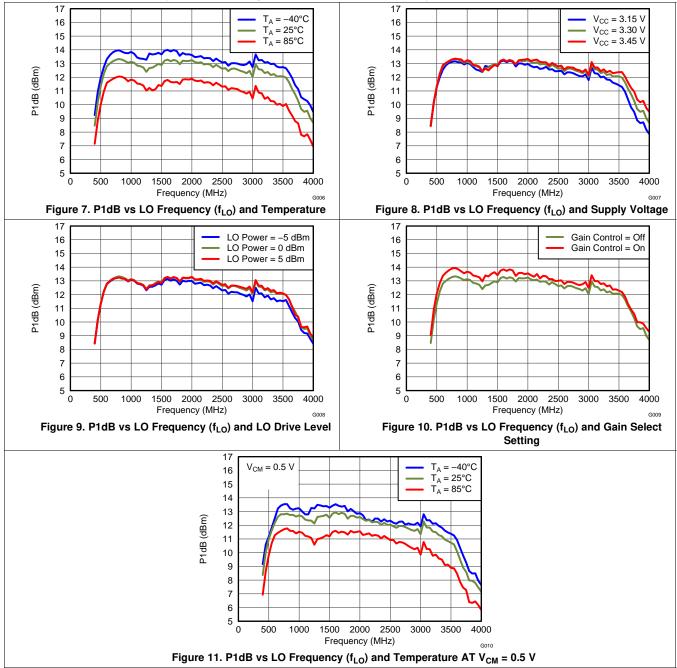
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6.7 Typical Characteristics: Single-Tone Baseband



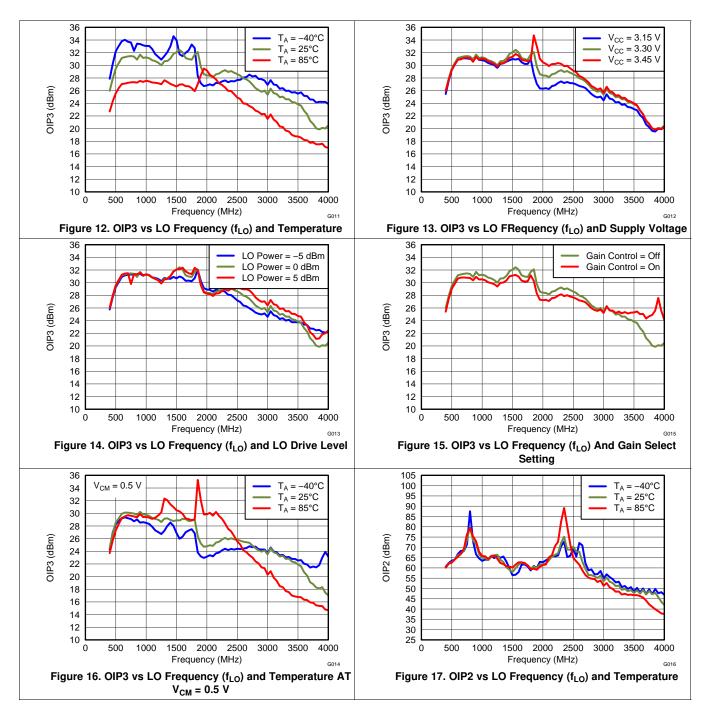


Typical Characteristics: Single-Tone Baseband (continued)



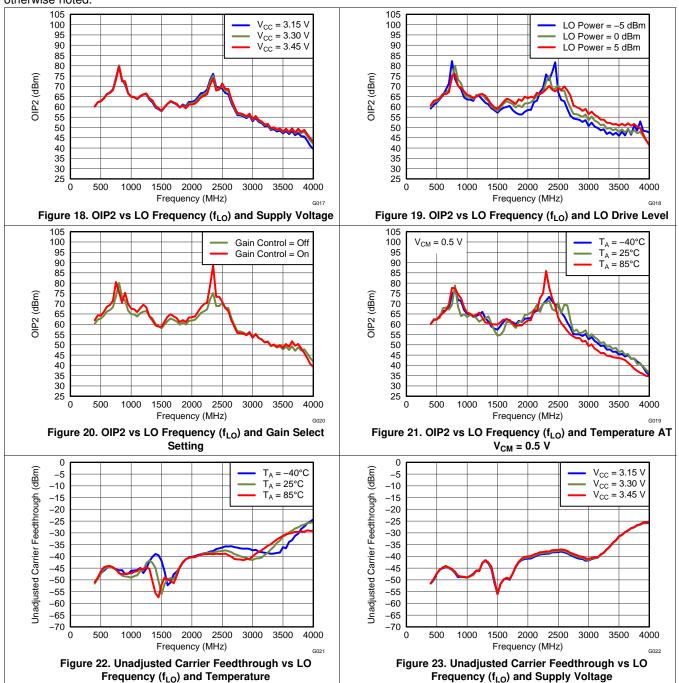


6.8 Typical Characteristics: Two-Tone Baseband



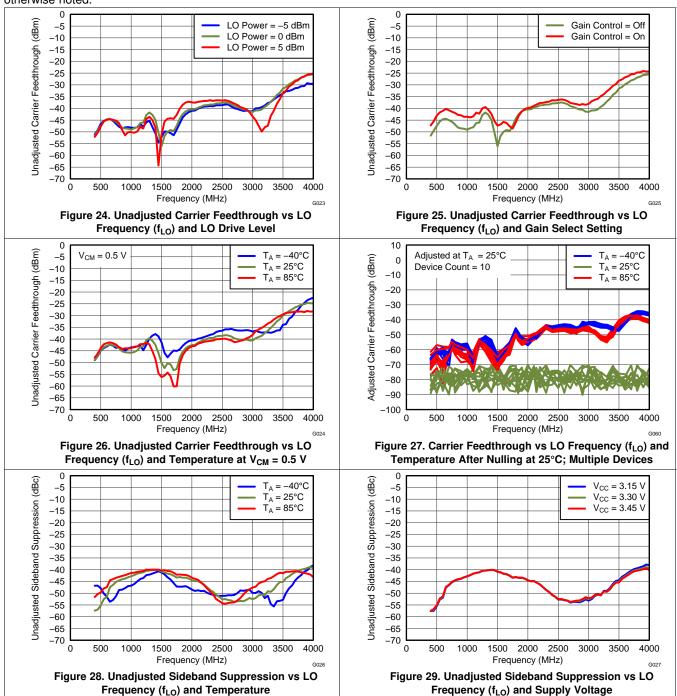


Typical Characteristics: Two-Tone Baseband (continued)



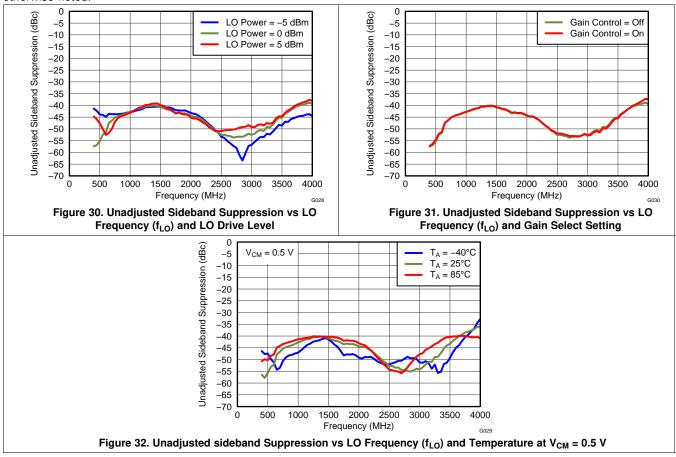


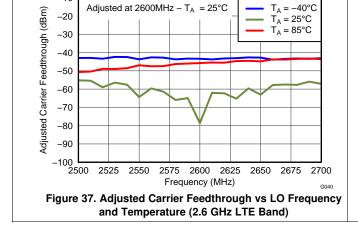
Typical Characteristics: Two-Tone Baseband (continued)

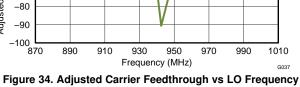




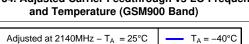
Typical Characteristics: Two-Tone Baseband (continued)







Adjusted at 942.5MHz – $T_A = 25^{\circ}C$



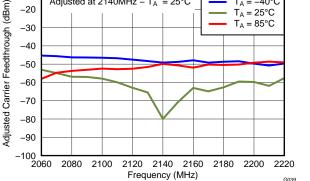
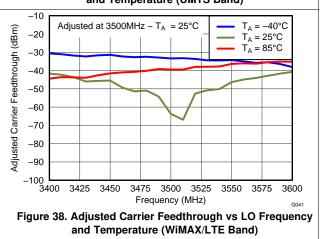


Figure 36. Adjusted carrier Feedthrough vs LO Frequency and Temperature (UMTS Band)



Adjusted at 748MHz - T_A = 25°C

-10

-20

-30

-40

-50

-60

-70

-80

-90

-100

-10

-20

-30

-50

-60

-80

-90

-10

-100 -1880

1900

1920

1940

1960

Frequency (MHz)

Figure 35. Adjusted Carrier Feedthrough vs LO Frequency and Temperature (PCS Band)

1980

2000

(dBm)

Feedthrough -40

Adjusted Carrier -70

680

700

720

Adjusted at 1960MHz - T_A = 25°C

740

(dBm)

Adjusted Carrier Feedthrough

6.9 Typical Characteristics: Two-Tone Baseband, Mid-Band Calibration

780

760

Frequency (MHz)

Figure 33. Adjusted Carrier Feedthrough vs LO Frequency

and Temperature (750 LTE Band)

V_{CC} = 3.3 V; T_A = 25°C; LO = 0 dBm, single-ended drive (LOP); I/Q frequency (f_{BB}) = 4.5 MHz, 5.5 MHz; baseband I/Q amplitude = 0.5-V_{PP}/tone differential sine waves in quadrature with V_{CM} = 0.25 V; and broadband output match, unless otherwise noted. Single point adjustment mid-band.

 $T_A = -40^{\circ}C$

 $T_A = 25^{\circ}C$

 $T_A = 85^{\circ}C$

800

 $T_A = -40^{\circ}C$

 $T_A = 25^{\circ}C$

 $T_A = 85^{\circ}C$

2020

2040

C036

820

-10

-20

-30

-40

-50

-60

-70

-10

Adjusted Carrier Feedthrough (dBm)

 $T_A = -40^{\circ}C$

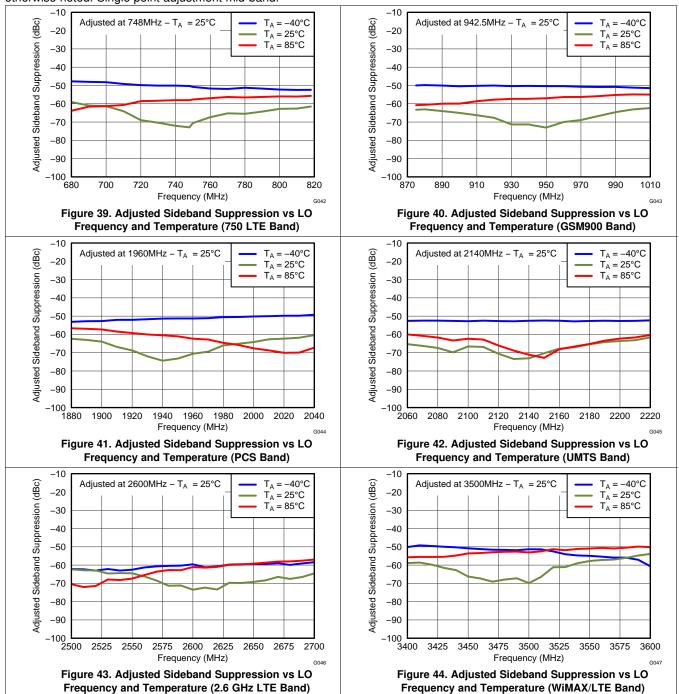
 $T_A = 25^{\circ}C$

 $T_A = 85^{\circ}C$

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Typical Characteristics: Two-Tone Baseband, Mid-Band Calibration (continued)

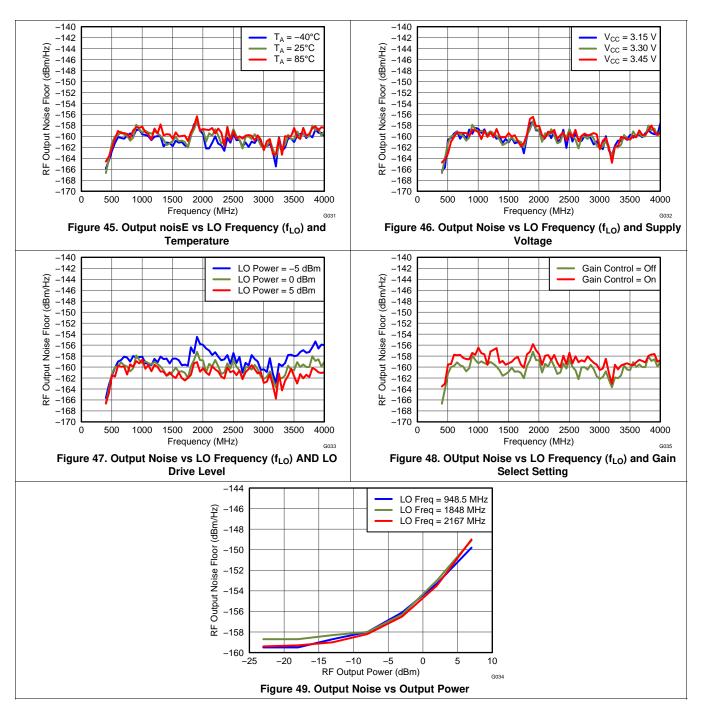


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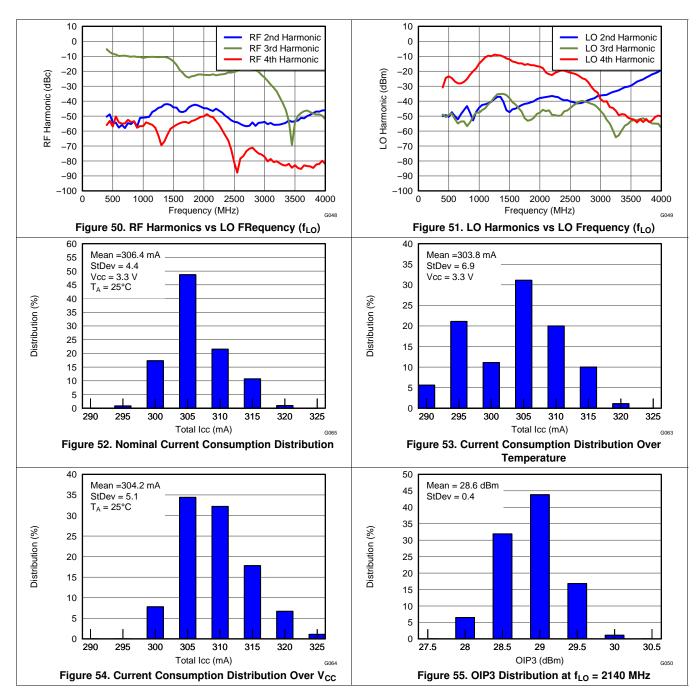
6.10 Typical Characteristics: No Baseband

 V_{CC} = 3.3 V; T_A = 25°C; LO = 0 dBm, single-ended drive (LOP); and input baseband ports terminated in 50 Ω , unless otherwise noted.



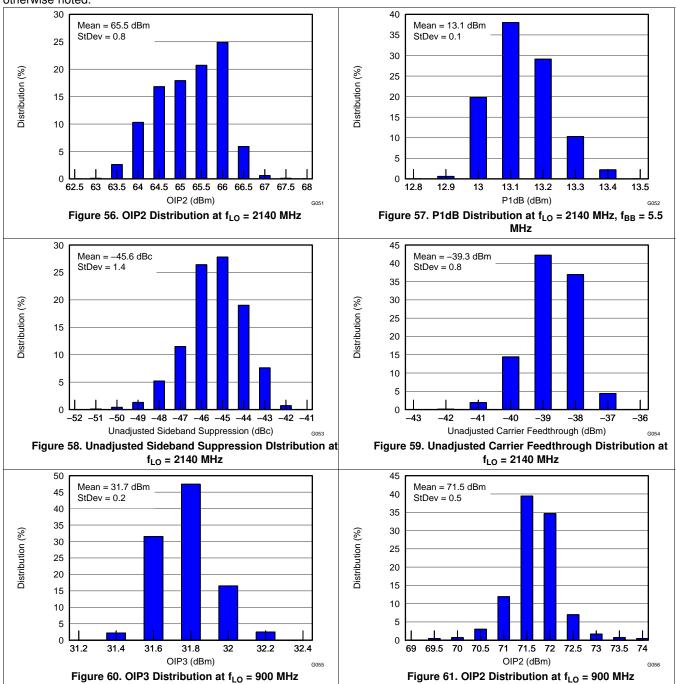


6.11 Typical Characteristics: Two-Tone Baseband



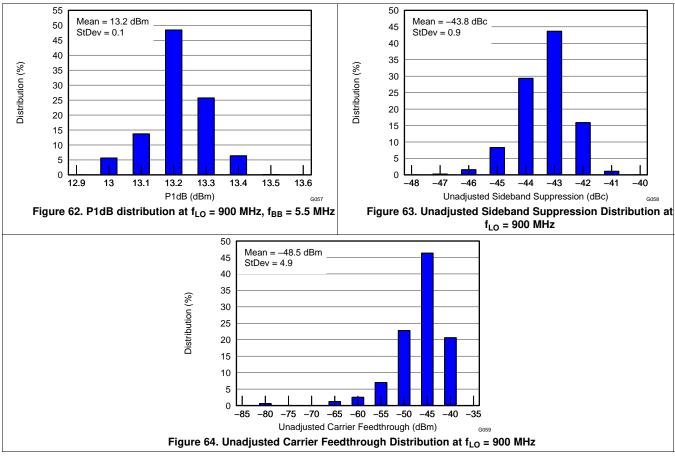


Typical Characteristics: Two-Tone Baseband (continued)





Typical Characteristics: Two-Tone Baseband (continued)



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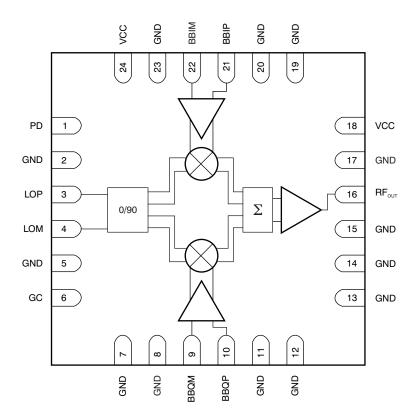
7 Detailed Description

7.1 Overview

TRF3705 is a low-noise direct quadrature modulator with high linearity, capable of converting complex modulated signals from baseband or IF directly to RF. With high-performance and superior-linearity, TRF3705 is an ideal device to up-convert to RF frequencies of 300 MHz through 4 GHz. With appropriate matching network, optimal performance can be obtained. The modulator is implemented as a double-balanced mixer.

TRF3705 has a RF output block which consists of a differential-to-single-ended converter that is capable of directly driving a single-ended 50- Ω load. The TRF3705 requires a 0.25-V common-mode voltage for optimal linearity performance. With a fast power-down pin, TRF3705 can be used to reduce power dissipation in TDD application

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Gain Control Feature

TRF3705 has a specific GC pin which is used for gain control. The GC pin is gain control digital input which is internally pulled down. When driving low or left open, modulator is in low gain mode. With driving high externally, the modulator is in high gain mode. This 1 bit gain step control feature offers a typical 3-dB gain increase in high gain mode. If power optimization is desired, driving this pin low can easily put the modulator into low gain mode.

7.4 Device Functional Modes

7.4.1 Power Down Mode

TRF3705 features a PD pin to power down the modulator. The PD pin is internally pulled down. When the powerdown digital input pin is driven high, the device is off. This feature provides a fast power-down which can be used to reduce power dissipation in time division duplexing applications.



8 Application and Implementation

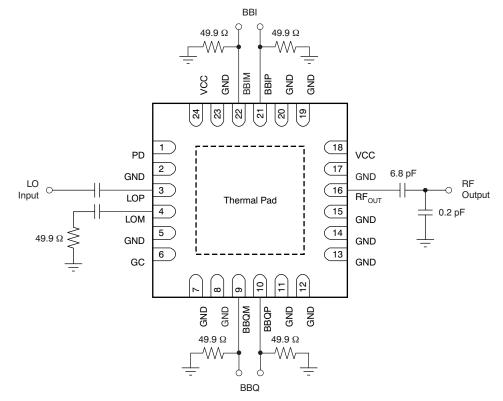
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TRF3705 is a quadrature modulator for up-converting the in-phase (I) and the quadrature-phase (Q) signals to radio frequency (RF) in the transmit chain. Typically, the device is used between the digital-to-analog converter (DAC) and the RF power amplifier.

8.2 Typical Application



(1) Pin 1 (PD) and Pin 6 (GC) are internally pulled down.

Figure 65. Typical Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters shown in Table 1.

NAME	NAME PIN NO DESCRIPTION										
BBQM	9	Base-band in-quadrature input: negative terminal. Input impedance is 8 K Ω //4.6 pF. Optimal linearity is obtained if V _{CM} is 0.25 V. Normally terminated in 50 Ω									
BBQP	10	Base-band in-quadrature input: positive terminal. Input impedance is 8 K Ω //4.6 pF. Optimal linearity is obtained if V _{CM} is 0.25 V. Normally terminated in 50 Ω									
LOP	3	Local oscillator input: positive terminal. This is preferred port when driving single ended. Normally AC coupled and terminated in 50 Ω									
LOM	4	Local oscillator input: negative terminal. When driving LO single-ended, normally AC coupled and terminated in 50 Ω .									
RFOUT	16	RF output. Normally using optimal matching circuits to match RF output to 50 Ω. Normally AC coupled.									
GC	6	Gain control digital input. Internally pulled down. When driving high, get 3 dB gain increase of RF output.									
PD	1	Power down digital input. Internally pulled down. When driving high, the modulator is off.									
VCC	18,24	3.3-V power supply. Can be tied together and source from a single clean supply. Each pin should be properly RF bypassed and decoupled.									

Table 1. Pin Termination Requirements and Limitations

8.2.2 Detailed Design Procedure

8.2.2.1 Baseband Inputs

The baseband inputs consist of the in-phase signal (I) and the Quadrature-phase signal (Q). The I and Q lines are differential lines that are driven in quadrature. The nominal drive level is 1-V_{PP} differential on each branch.

The baseband lines are nominally biased at 0.25-V common-mode voltage (V_{CM}); however, the device can operate with a V_{CM} in the range of 0 V to 0.5 V. The baseband input lines are normally terminated in 50 Ω , though it is possible to modify this value if necessary to match to an external filter load impedance requirement.

8.2.2.2 LO Input

The LO inputs can be driven either single-ended or differentially. There is no significant performance difference between either option with the exception of the sideband suppression. If driven single-ended, either input can be used, but LOP (pin 3) is recommended for best broadband performance of sideband suppression. When driving in single-ended configuration, simply ac-couple the unused port and terminate in 50 Ω . The comparison of the sideband suppression performance is shown in Figure 71 for driving the LO single-ended from either pin and for driving the LO input differentially.

8.2.2.3 RF Output

The RF output must be ac-coupled and can drive a 50- Ω load. The suggested output match provides the best broadband performance across the frequency range of the device. It is possible to modify the output match to optimize performance within a selected band if needed. The optimized matching circuits are to match the RF output impedances to 50 Ω .

Figure 72 shows a slightly better OIP3 performance at the frequency above 1850 MHz with an 0.2-pF matching capacitor.



8.2.2.4 350-MHz Operation

A different matching circuit, as shown in Figure 66, could also be applied to improve the performance for the frequency from 300 MHz to 400 MHz.

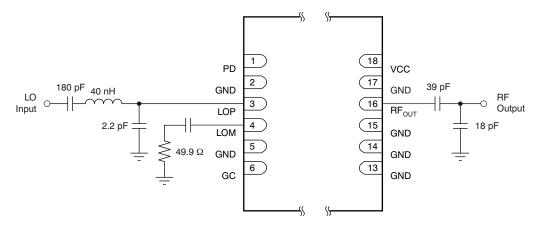


Figure 66. Matching Components for Operation Centered at 350 MHz

Figure 73 and Figure 74 show a slight improvement in OIP3 performance at frequencies above 1850 MHz with an 0.2-pF matching capacitor.

8.2.2.5 DAC to Modulator Interface Network

For optimum linearity and dynamic range, a digital-to-analog converter (DAC) can interface directly with the TRF3705 modulator. It is imperative that the common-mode voltage of the DAC and the modulator baseband inputs be properly maintained. With the proper interface network, the common-mode voltage of the DAC can be translated to the proper common-mode voltage of the modulator. The TRF3705 common-mode voltage is typically 0.25 V, and is ideally suited to interface with the DAC3482/3484 (DAC348x) family because the common-mode voltages of both devices are the same; there is no translation network required. The interface network is shown in Figure 67.

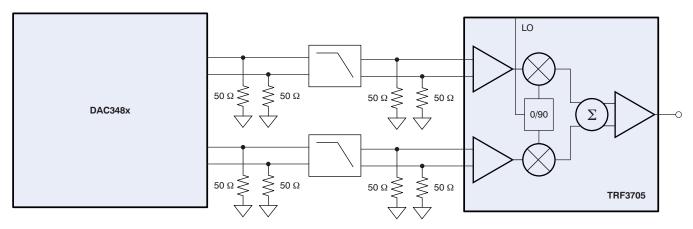


Figure 67. DAC348x Interface with the TRF3705 Modulator

The DAC348x requires a load resistor of 25 Ω per branch to maintain its optimum voltage swing of 1-V_{PP} differential with a 20-mA max current setting. The load of the DAC is separated into two parallel 50- Ω resistors placed on the input and output side of the low-pass filter. This configuration provides the proper resistive load to the DAC while also providing a convenient 50- Ω source and load termination for the filter.



SLWS223B-AUGUST 2011-REVISED NOVEMBER 2015

8.2.2.6 DAC348x with TRF3705 Modulator Performance

The combination of the DAC348x driving the TRF3705 modulator yields excellent system parameters suitable for high-performance applications. As an example, the following sections illustrate the typical modulated adjacent channel power ratio (ACPR) for common telecom standards and bands. These measurements were taken on the DAC348x evaluation board.

8.2.2.6.1 WCDMA

The adjacent channel power ratio (ACPR) performance using a single-carrier WCDMA signal in the UMTS band is shown in Figure 68.

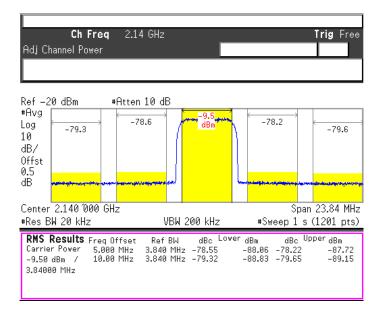


Figure 68. Single-Carrier WCDMA ACPR, IF = 30 MHz, LO Frequency = 2110 MHz

A marginal improvement in OIP3 and output noise performance can be observed by increasing the LO drive power, resulting in slightly improved ACPR performance. The ACPR performance versus LO drive level is plotted in Figure 75 across common frequencies to illustrate the amount of improvement that is possible.



8.2.2.6.2 LTE

ACPR performance using a 10 MHz LTE signal in the 700-MHz band is shown in Figure 69.

Adj Cł	Ch Freq nannel Power	748 MHz			Trig Free
Ref -2 #Avg Log 10 dB/ 0ffst 0.5 dB	0 dBm	#Atten 8 dB	-8.8 dBm	-77.3	-77.7
#Res B RMS I Carrie	dBm / 20.00	lffset Ref Bk I MHz 9.015 M		#Sweep 1 s	Span 50 MH: s (1201 pts) Jpper dBm -86.13 -86.54

Figure 69. 10 MHz LTE ACPR, IF = 30 MHz, LO Frequency = 718 MHz

8.2.2.6.3 MC-GSM

ACPR performance using a four-carrier MC-GSM signal in the 1800-MHz band is shown in Figure 70.

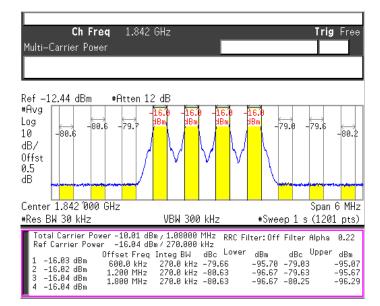
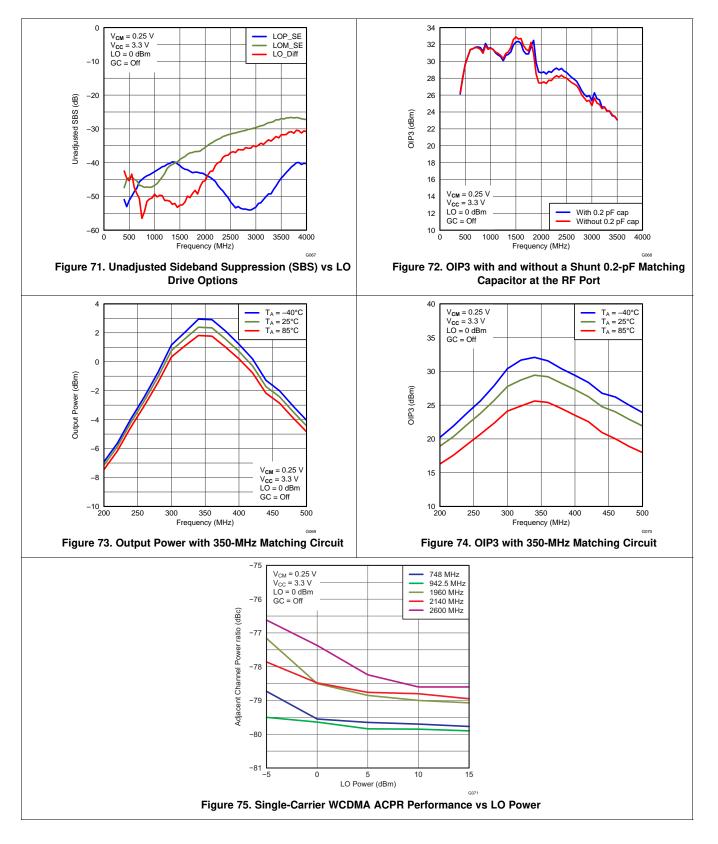


Figure 70. Four-Carrier MC-GSM, IF = 30 MHz ACPR, LO Frequency = 1812 MHz



8.2.3 Application Curves





9 Power Supply Recommendations

The TRF3705 is powered by supplying a nominal 3.3 V to pins 18 and 24. These supplies can be tied together and sourced from a single clean supply. Proper RF bypassing should be placed close to each power supply pin.

Ground pin connections should have at least one ground via close to each ground pin to minimize ground inductance. The PowerPAD[™] must be tied to ground, preferably with the recommended ground via pattern to provide a good thermal conduction path to the alternate side of the board and to provide a good RF ground for the device. (Refer to *Layout Guidelines* for additional information.)



10 Layout

Populated RoHS-compliant evaluation boards are available for testing the TRF3705 as a stand-alone device. Contact your local TI representative for information on ordering these evaluation modules, or see the TRF3705 product folder on the TI website. In addition, the TRF3705 can be evaluated with the DAC348x (quad/dual 16-bit, 1.25GSPS) EVM driving the baseband inputs through a seamless interface at 0.25V common-mode voltage.

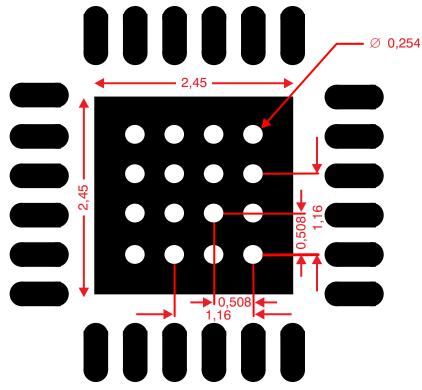
10.1 Layout Guidelines

The TRF3705 device is fitted with a ground slug on the back of the package that must be soldered to the printed circuit board (PCB) ground with adequate ground vias to ensure a good thermal and electrical connection. The recommended via pattern and ground pad dimensions are shown in Figure 76. The recommended via diameter is 10 mils (0.10 in or 0,25 mm). The ground pins of the device can be directly tied to the ground slug pad for a low-inductance path to ground. Additional ground vias may be added if space allows.

Decoupling capacitors at each of the supply pins are strongly recommended. The value of these capacitors should be chosen to provide a low-impedance RF path to ground at the frequency of operation. Typically, the value of these capacitors is approximately 10 pF or lower.

The device exhibits symmetry with respect to the quadrature input paths. It is recommended that the PCB layout maintain this symmetry in order to ensure that the quadrature balance of the device is not impaired. The I/Q input traces should be routed as differential pairs and the respective lengths all kept equal to each other. On the RF traces, maintain proper trace widths to keep the characteristic impedance of the RF traces at a nominal 50 Ω .

10.2 Layout Example



Note: Dimensions are in millimeters (mm).

Figure 76. PCB Ground Via Layout Guide



11 Device and Documentation Support

11.1 Device Support

11.1.1 Definition of Specifications

11.1.1.1 Carrier Feedthrough

This specification measures the power of the local oscillator component that is present at the output spectrum of the modulator. The performance depends on the dc offset balance within the baseband input lines. Ideally, if all of the baseband lines were perfectly matched, the carrier (that is, the LO) would be naturally suppressed; however, small dc offset imbalances within the device allow some of the LO component to feed through to the output. This parameter is expressed as an absolute power in dBm, and is independent of the RF output power and the injected LO input power.

It is possible to adjust the baseband dc offset balance to suppress the output carrier component. Devices such as the DAC348x DAC family have dc offset adjustment capabilities specifically for this function. The Adjusted Carrier Feedthrough graphs (see Figure 33 through Figure 38) optimize the performance at the center of the band at room temperature. Then, with the adjusted dc offset values held constant, the parameter is measured over the frequency band and across the temperature extremes. The typical performance plots provide an indication of how well the adjusted carrier suppression can be maintained over frequency and temperature with only one calibration point.

11.1.1.2 Sideband Suppression

This specification measures the suppression of the undesired sideband at the output of the modulator relative to the desired sideband. If the amplitude and phase within the I and Q branch of the modulator were perfectly matched, the undesired sideband (or image) would be naturally suppressed. Amplitude and phase imbalance in the I and Q branches result in the increase of the undesired sideband. This parameter is measured in dBc relative to the desired sideband.

It is possible to adjust the relative amplitude and phase balance within the baseband lines to suppress the unwanted sideband. Devices such as the DAC348x DAC family have amplitude and phase adjustment control specifically for this function. The Adjusted Sideband Suppression graphs (refer to Figure 39 through Figure 44) optimize the performance at the center of the band at room temperature. Then, with the adjusted amplitude and phase values held constant, the parameter is measured over the frequency band and across the temperature extremes. The performance plots provide an indication of how well the adjusted sideband suppression can be maintained over frequency and temperature with only one calibration point.

11.1.1.3 Output Noise

The output noise specifies the absolute noise power density that is output from the RF_{OUT} pin (pin 16). This parameter is expressed in dBm/Hz. This parameter, in conjunction with the OIP3 specification, indicates the dynamic range of the device. In general, at high output signal levels the performance is limited by the linearity of the device; at low output levels, on the other hand, the performance is limited by noise. As a result of the higher gain and output power of the TRF3705 compared to earlier devices, it is expected that the noise density is slightly higher as well. With its increased gain and high OIP3 performance, the overall dynamic range of the TRF3705 is maintained at exceptional levels.

11.1.1.4 Definition of Terms

A simulated output spectrum with two tones is shown in Figure 77, with definitions of various terms used in this data sheet.



Device Support (continued)

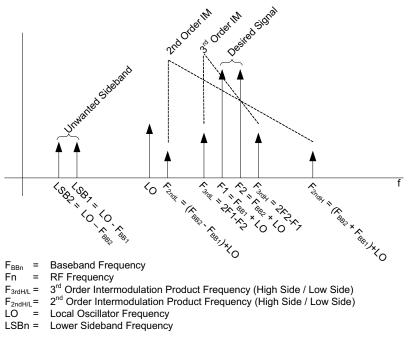


Figure 77. Graphical Illustration of Common Terms

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E[™] Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help

solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

11.4 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF3705IRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	(6) NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TRF3705 IRGE	Samples
TRF3705IRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TRF3705 IRGE	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

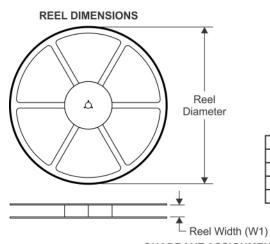
10-Dec-2020

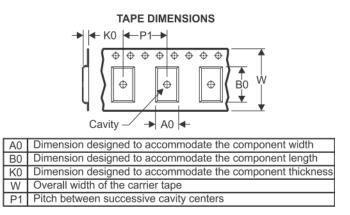
PACKAGE MATERIALS INFORMATION

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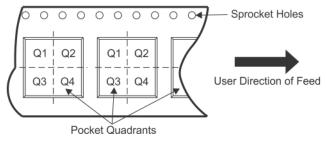
Texas Instruments

TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF3705IRGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TRF3705IRGET	VQFN	RGE	24	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

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PACKAGE MATERIALS INFORMATION

3-Aug-2017



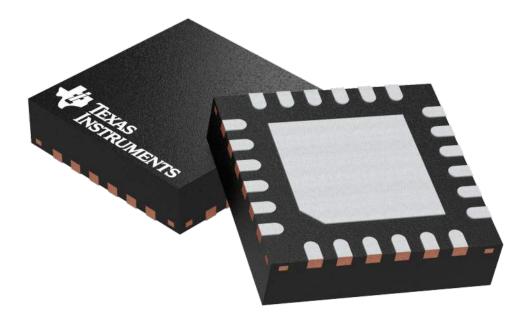
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF3705IRGER	VQFN	RGE	24	3000	367.0	367.0	38.0
TRF3705IRGET	VQFN	RGE	24	250	367.0	367.0	38.0

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



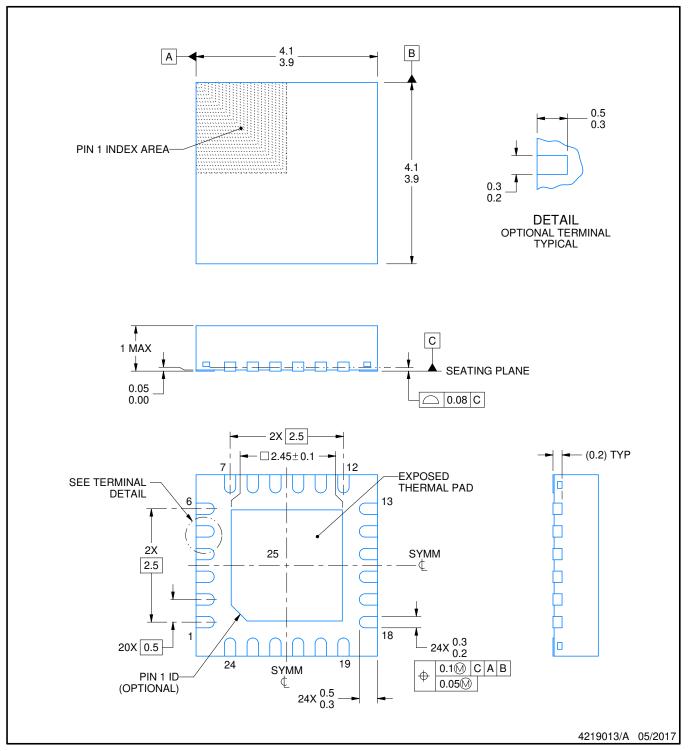
RGE0024B



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M. 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

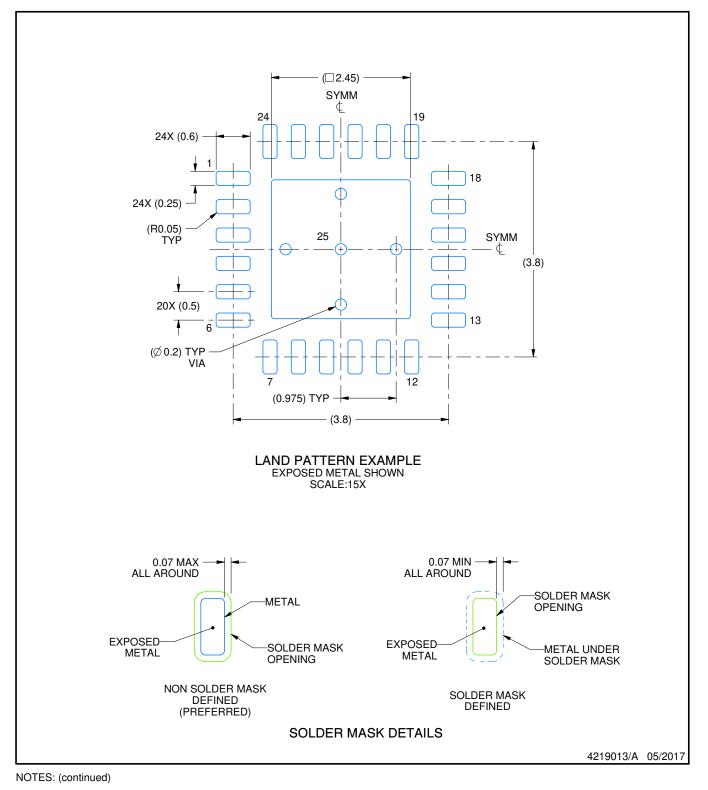


RGE0024B

EXAMPLE BOARD LAYOUT

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



 This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

 Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

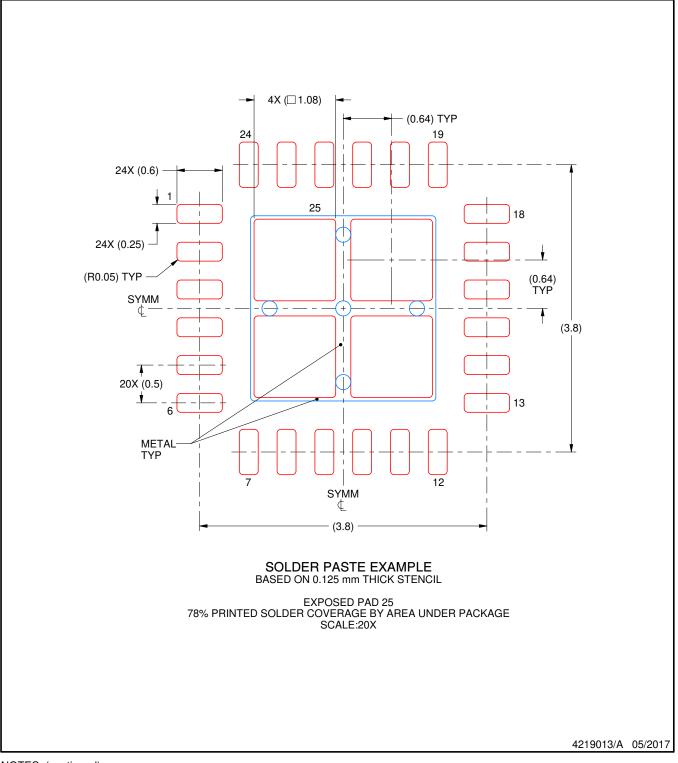


RGE0024B

EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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