

N-channel 30 V, 0.0027 Ω typ., 23 A STripFET™ H7 Power MOSFET plus monolithic Schottky in a PowerFLAT™ 3.3 x 3.3

Datasheet - production data

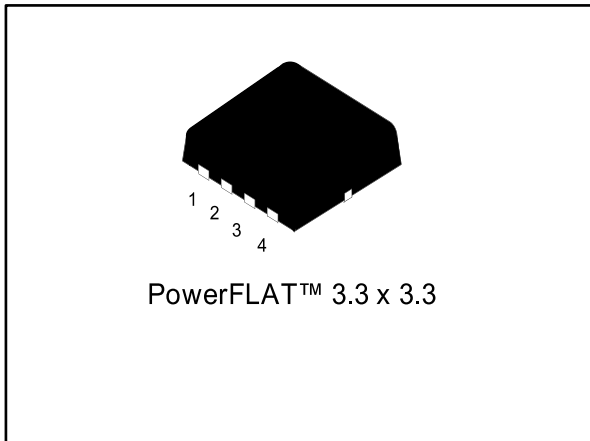


Figure 1: Internal schematic diagram

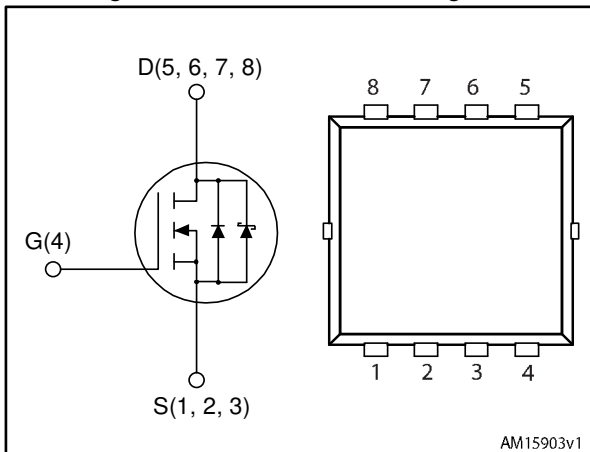


Table 1: Device summary

Order code	Marking	Package	Packing
STL23NS3LLH7	23NS3	PowerFLAT™ 3.3 x 3.3	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STL23NS3LLH7	30 V	0.0037 Ω	23 A

- Very low on-resistance
- Very low Q_g
- High avalanche ruggedness
- Embedded Schottky diode

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes the STripFET H7 technology with a trench gate structure combined with extremely low on-resistance. The device also offers ultra-low capacitances for higher switching frequency operations.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	23	A
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	14.3	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	92	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	92	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	57.5	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	368	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	2.9	W
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature		

Notes:

⁽¹⁾This value is rated according to R_{thj-c} .

⁽²⁾Pulse width limited by safe operating area.

⁽³⁾This value is rated according to $R_{thj-pcb}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	42.8	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case max	2.5	$^\circ\text{C/W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2oz Cu, $t < 10$ sec.

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ $V_{DS} = 24\text{ V}$			500	μA
I_{GSS}	Gate-body leakage current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 1\text{ mA}$	1.2		2.3	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 11.5\text{ A}$		0.0027	0.0037	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 11.5\text{ A}$		0.004	0.005	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 15\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2100	-	pF
C_{oss}	Output capacitance		-	850	-	pF
C_{rss}	Reverse transfer capacitance		-	60	-	pF
Q_g	Total gate charge	$V_{DD} = 10\text{ V}$, $I_D = 23\text{ A}$, $V_{GS} = 4.5\text{ V}$ (see Figure 13: "Gate charge test circuit")	-	13.7	-	nC
Q_{gs}	Gate-source charge		-	7.5	-	nC
Q_{gd}	Gate-drain charge		-	3.3	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$, $I_D = 11.5\text{ A}$, $R_G = 3\text{ }\Omega$, $V_{GS} = 4.5\text{ V}$	-	10	-	ns
t_r	Rise time		-	33	-	ns
$t_{d(off)}$	Turn-off delay time		-	22	-	ns
t_f	Fall time		-	7.5	-	ns

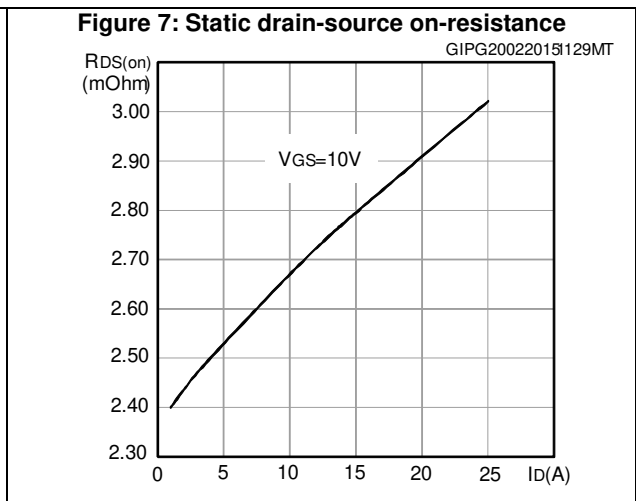
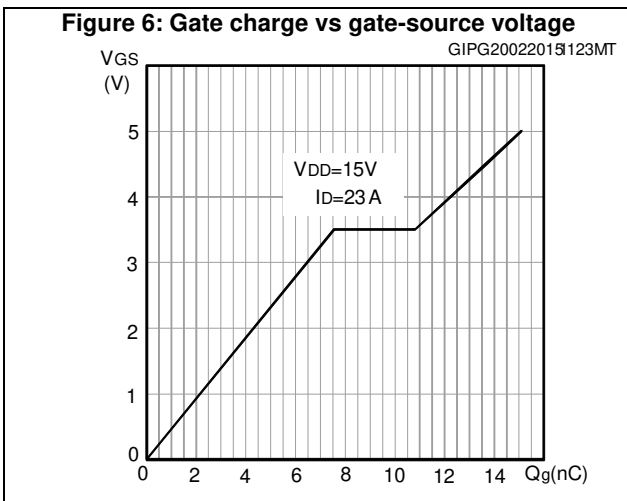
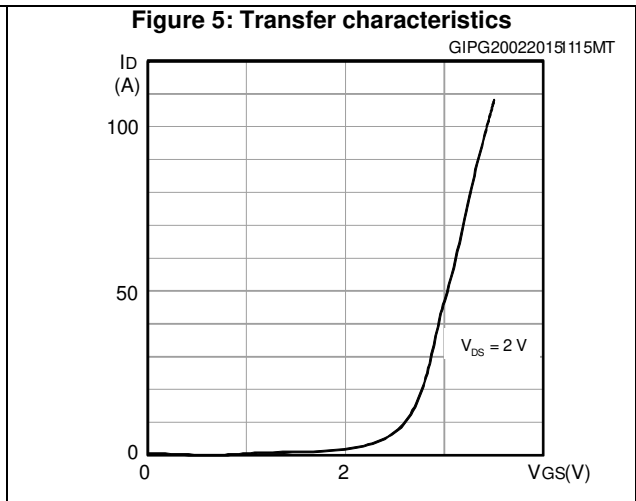
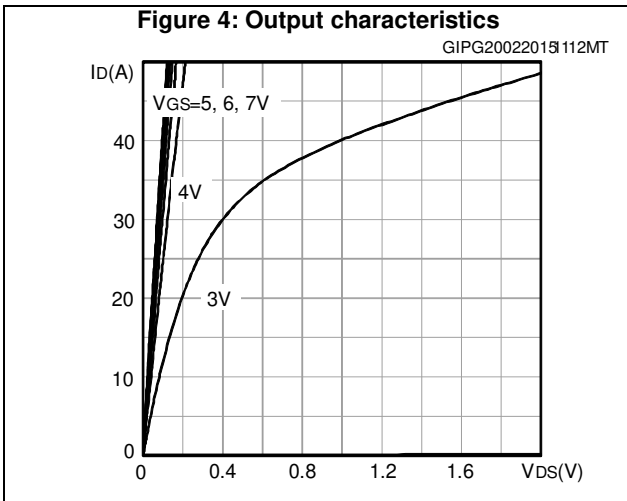
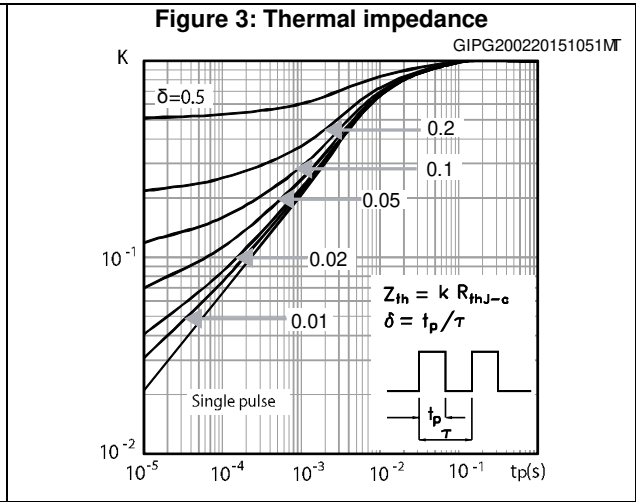
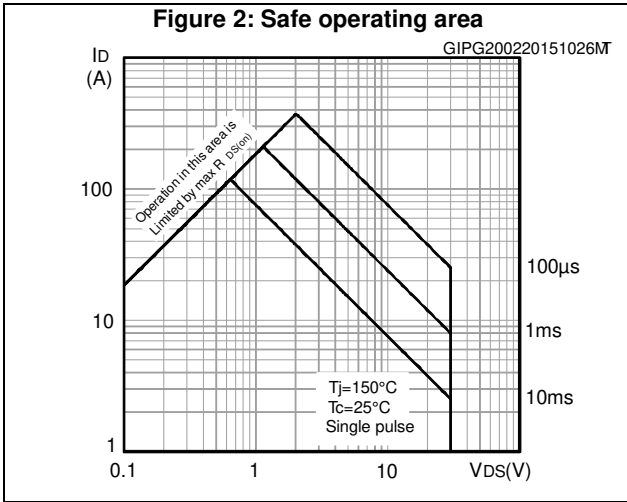
Table 7: Source drain diode

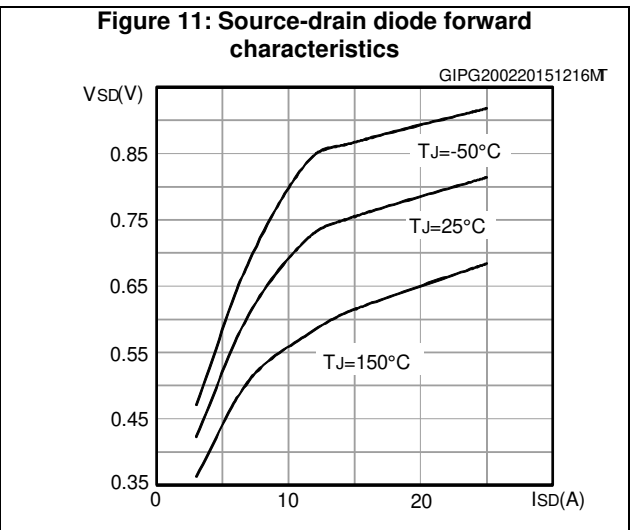
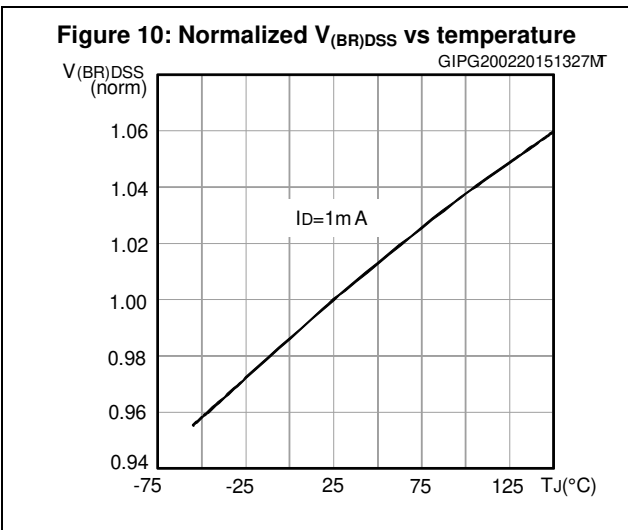
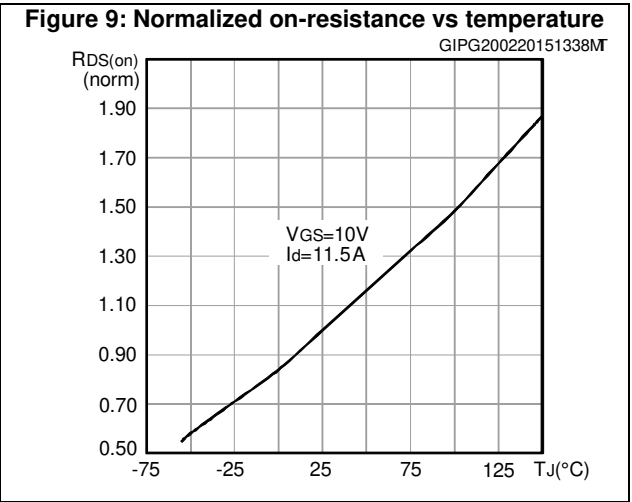
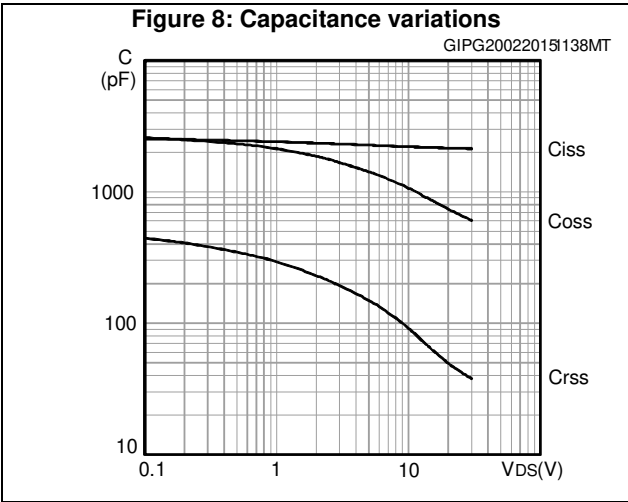
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 2 \text{ A}$, $V_{GS} = 0$	-	0.4	0.7	V
t_{rr}	Reverse recovery time	$I_{SD} = 2 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{GS} = 0 \text{ V}$	-	31.2		ns
Q_{rr}	Reverse recovery charge		-	18.7		nC
I_{RRM}	Reverse recovery current		-	1.2		A

Notes:

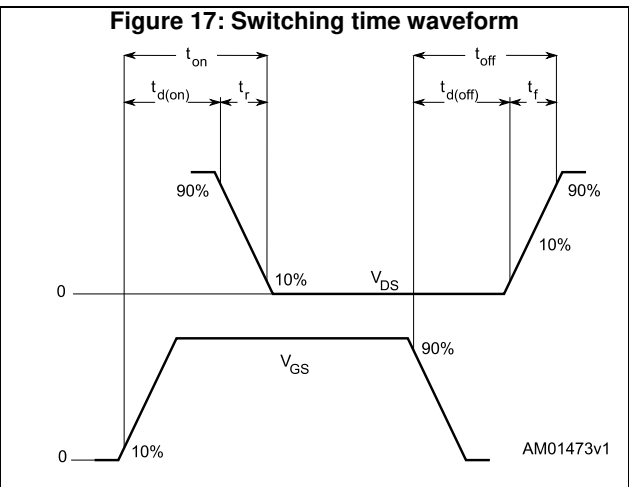
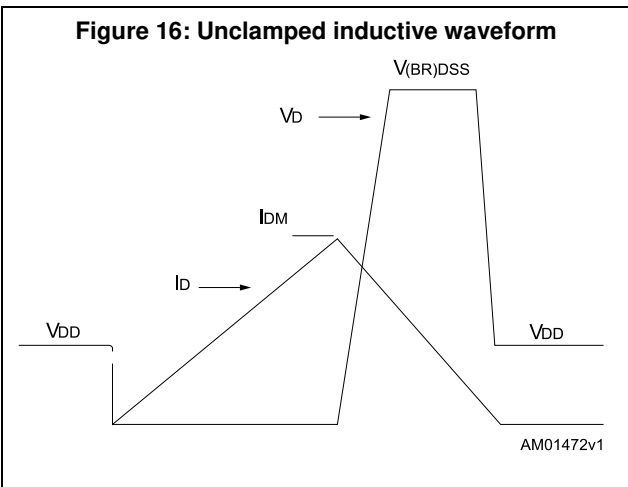
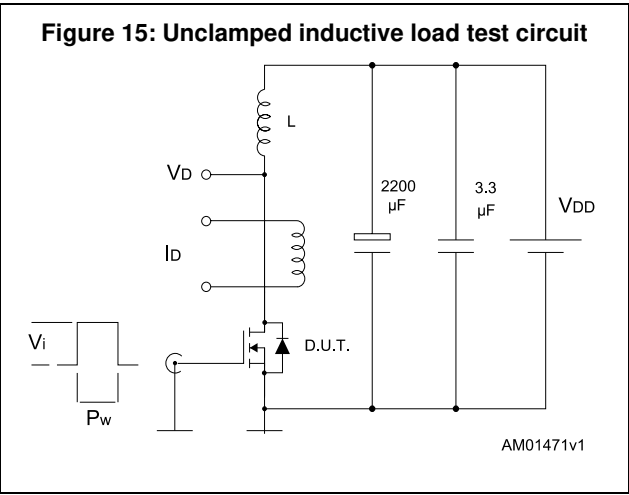
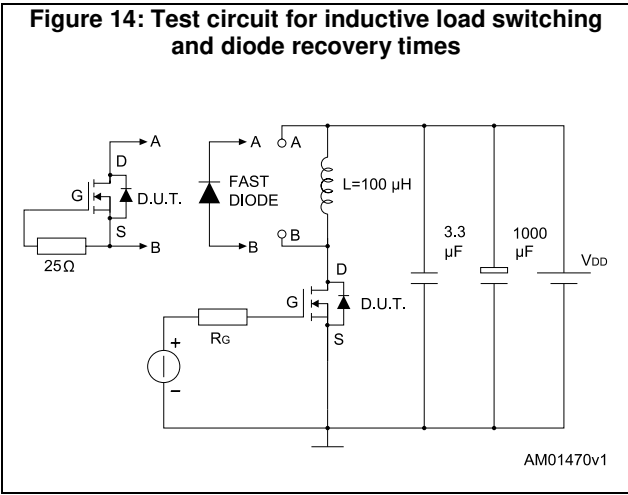
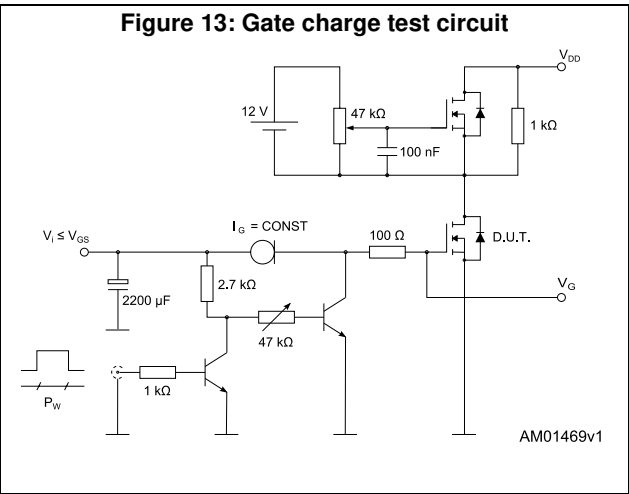
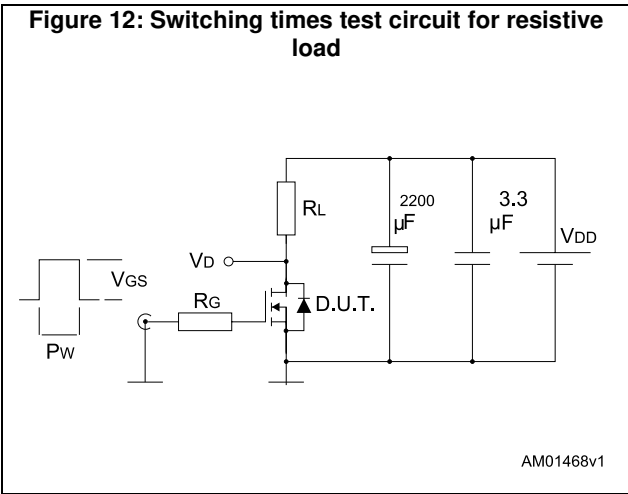
⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)





3 Test circuits



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 PowerFlat 3.3 x 3.3 package information

Figure 18: PowerFLAT™ 3.3 x 3.3 package outline

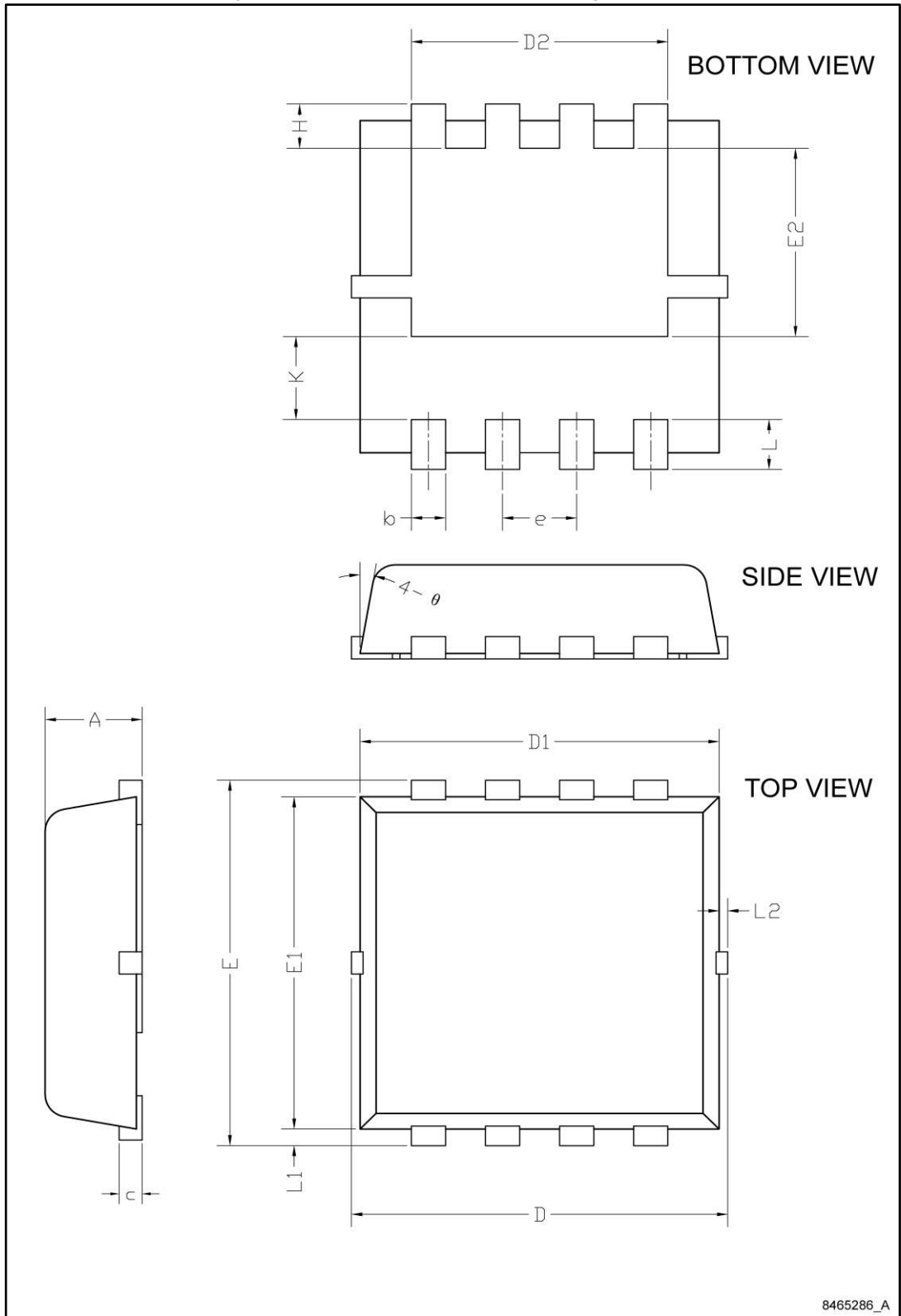
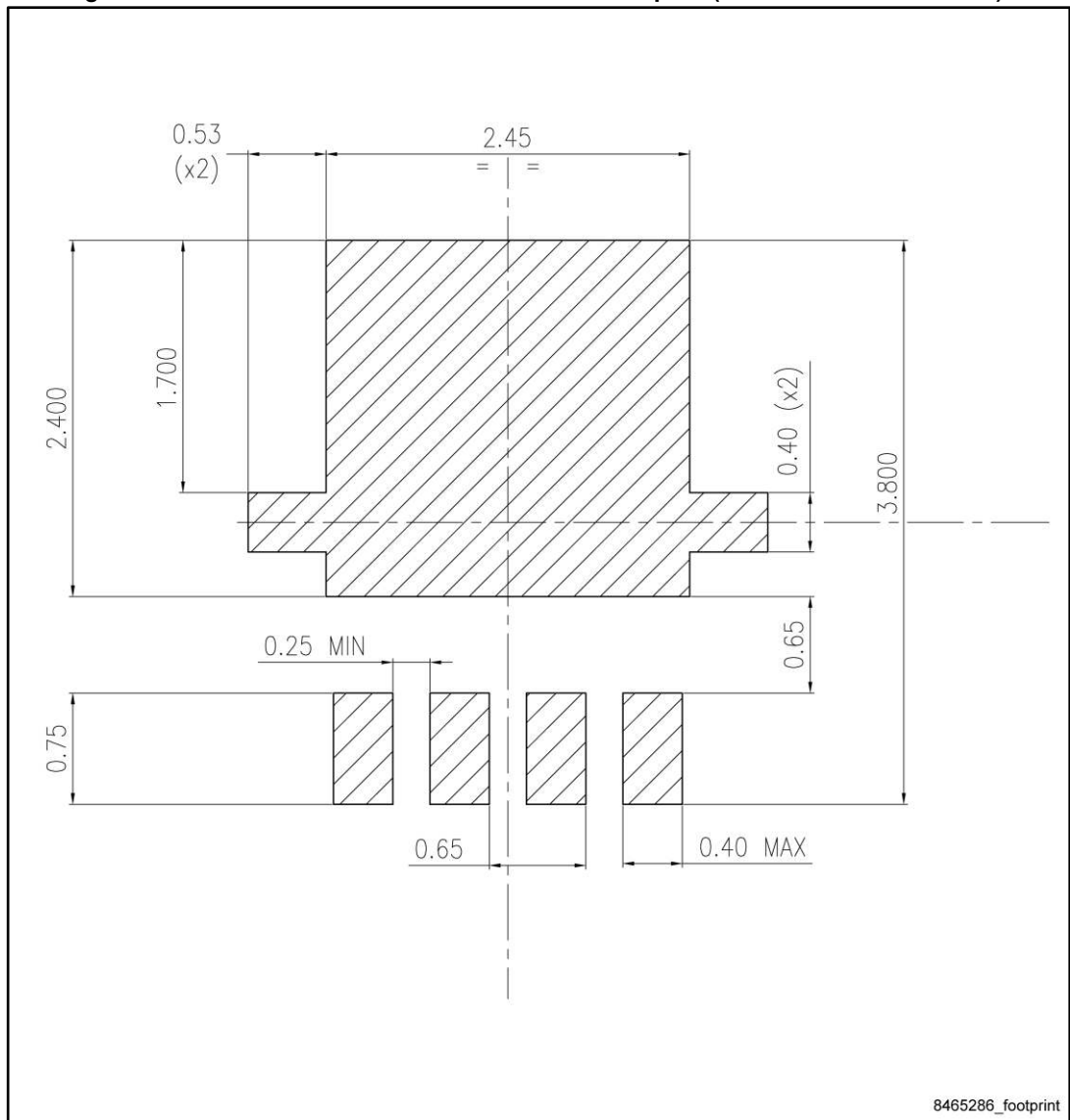


Table 8: PowerFLAT™ 3.3 x 3.3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
θ	8°	10°	12°

Figure 19: PowerFLAT™ 3.3 x 3.3 recommended footprint (dimension in millimeters)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
31-Jul-2013	1	First release.
27-Mar-2015	2	Updated title and features in cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "On /off states"</i> and <i>Table 7: "Source drain diode"</i> . Added <i>Section 2.1: "Electrical characteristics (curves)"</i> . Minor text changes.
07-May-2015	3	Document status promoted from preliminary data to production data. Minor text changes.

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