19-3103; Rev 0; 12/07

EVALUATION KIT AVAILABLE

Multirate CDR with Integrated Serializer/Deserializer for GPON and BPON ONT Applications

MAX3886

General Description

The MAX3886 2.488Gbps/1.244Gbps/622Mbps CDR with SerDes (serializer/deserializer) is designed specifically for low-cost optical network terminal (ONT) applications in Gigabit passive optical network (GPON) and broadband passive optical network (BPON) fiber-to-the-home (FTTH) systems. It provides G.984- and G.983-compliant clock and data recovery (CDR) for the continuous downstream data signal, with an integrated 4-bit SerDes that has LVDS parallel interfaces and CML serial interfaces.

The SerDes uses the recovered downstream clock for upstream serialization (loopback clock), providing optimum PON operation. The CDR frequency reference can be provided by a low-cost 19.44MHz SMD-type crystal or external LVCMOS source, and excellent jitter tolerance supports applications requiring FEC. An integrated burst-enable signal path also simplifies high-performance upstream burst timing.

This 3.3V IC is housed in a 8mm x 8mm, 56-lead thin QFN package and operates from -40°C to +85°C.

Applications

BPON/GPON Optical Network Terminal (ONT)

Features

- **2.488Gbps, 1.244Gbps, and 622Mbps Clock and Data Recovery**
- **Meets G.984 and G.983 Jitter Requirements**
- **4-Bit Serializer and 4-Bit Deserializer with Loop-Timed Serialization**
- **CML Serial I/O, LVDS Parallel I/O**
- **Integrated Reference Oscillator Uses 19.44MHz SMD Crystal**
- **Integrated Upstream Burst-Enable Signal Path**

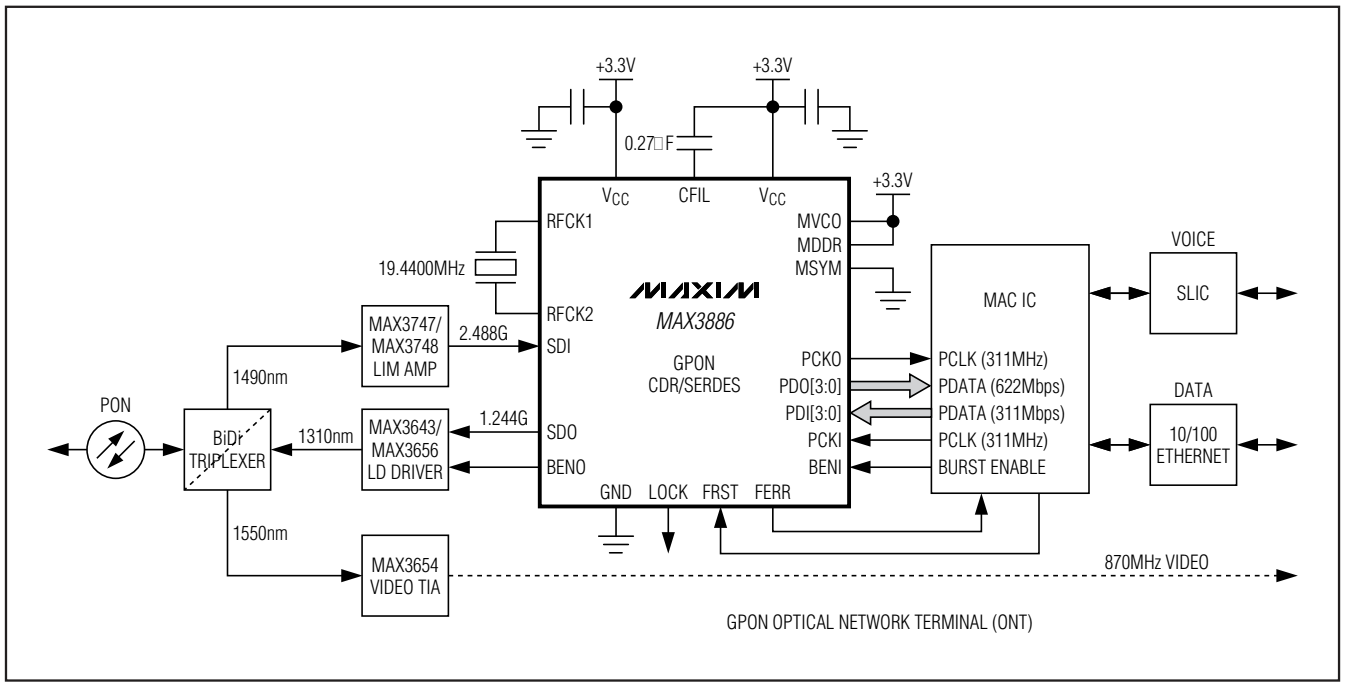
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3886ETN+	-40°C to +85°C	56 TQFN (8mm x 8mm)	T5688-2

+Denotes a lead-free package.

Pin Configuration appears at end of data sheet.

Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{CC}).....-0.3V to +4.0V
CML Input Voltage Range (SDI±).....-0.3V to (V_{CC} + 0.3V)
CML Output Current (SDO±, BENO±).....±22mA
LVDS Input Voltage Range
(PCKI±, PDI[3:0]±, BENI±).....-0.3V to (V_{CC} + 0.3V)
LVDS Output Voltage Range
(RCKO±, PDO[3:0]±, PCKO±).....-0.3V to (V_{CC} + 0.3V)
LVCMOS Input Voltage Range
(MSYM, MDDR, FRST).....-0.3V to (V_{CC} + 0.3V)
Three-State Input Voltage Range
(MVCO).....-0.3V to (V_{CC} + 0.3V)
LVCMOS Output Voltage Range
(LOCK, FERR) .....-0.3V to (V_{CC} + 0.3V)
Voltage Range at CFIL, RFCK1,
RFCK2, TP1, TP2, TP3, TP4 .....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
56-Pin TQFN (derate 47.6mW/°C above 70°C).....3808mW
Operating Junction Temperature Range.....-55°C to +150°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Temperature	T_A		-40		+85	°C
Power-Supply Voltage	V_{CC}		3.0		3.6	V
Downstream/Upstream Data Rates				See Table 2		Gbps
Reference Frequency		Internal or external oscillator		19.4400		MHz
Crystal Accuracy		Includes aging, temperature, and other contributors			±250	ppm
Crystal ESR		Fundamental type, AT-strip cut	10		60	Ω
Crystal Drive					100	µW
Crystal Load Capacitance		On-chip parallel capacitance		18		pF
Reference Clock Input Duty Cycle		When driven by an LVCMOS clock source	40		60	%

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A= +25°C, unless otherwise noted. LVDS outputs terminated 100Ω differential, CML inputs terminated 100Ω differential, CML outputs terminated 100Ω differential.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}			240	310	mA
CDR/DESERIALIZER SPECIFICATIONS						
Serial Input Data Rate	Rate	MVCO = 1		2488.32		Mbps
		MVCO = open		1244.16		
		MVCO = 0		622.08		
CDR CID Immunity		BER ≤ 10^{-10} (Note 2)		> 100		Bits
CDR Sinusoidal Jitter Tolerance	f > f_C	BER ≤ 10^{-10} (Note 3)	0.3	0.7		UI_{P-P}
SDI to SDO Jitter Transfer		(Notes 4, 5)			0.1	dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A= +25°C, unless otherwise noted. LVDS outputs terminated 100Ω differential, CML inputs terminated 100Ω differential, CML outputs terminated 100Ω differential.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDI to SDO Jitter Transfer Bandwidth		(Notes 3, 4)			f_C	MHz
Parallel Clock Output Random Jitter		(Note 6)		< 0.5		mUI_{RMS}
Parallel-Output Clock to Data Time	t_{CK-Q}	Figure 1	-80		+80	ps
Parallel Clock and Data-Output Rise/Fall Time	t_r, t_f	20% to 80%			300	ps
Parallel-Clock Output Duty Cycle			45		55	%
Parallel-Clock Output Frequency				See Table 2		MHz
Parallel-Data Output Channel-to-Channel Skew					100	ps
CDR Acquisition Time (After Startup)				2		ms
Reference-Output Clock Frequency				See Table 2		MHz
SERIALIZER SPECIFICATIONS						
Parallel-Input Clock Frequency				See Table 2		MHz
Serial-Output Data Rate				See Table 2		Mbps
Parallel-Data Input-Setup Time	t_{SU}	Figure 1	170			ps
Parallel-Data Input-Hold Time	t_{HD}	Figure 1	300			ps
Serial-Data Output Rise/Fall Time	t_r, t_f	20% to 80%			160	ps
Serial-Data Output Random Jitter		(Notes 5, 6)			4	mUI_{RMS}
Serial-Data Output Deterministic Jitter		(Notes 2, 5)			47	mUI_{P-P}
Burst Enable to Serial Data MSB Time	t_{B-MSB}	Figure 2	-50		+50	ps
Minimum Pulse Width of FIFO Reset		UI is PCKO period		4		UI
Tolerated Drift Between PCKI and PCKO After FIFO Reset		UI is PCKO period		±1		UI
I/O SPECIFICATIONS						
CML Differential Input Voltage	V_{IN}		200		1600	mV_{P-P}
CML Input Common-Mode Range			V_{CC} - 1.49	V_{CC} - 1.32	V_{CC} - V_{IN}/4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A= +25°C, unless otherwise noted. LVDS outputs terminated 100Ω differential, CML inputs terminated 100Ω differential, CML outputs terminated 100Ω differential.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CML Differential Output			640	800	1000	mV_{P-P}
CML Differential Output Resistance			80	100	120	Ω
LVDS Input Voltage Range			0		2400	mV
LVDS Differential Input Range		(Note 5)	±100		±600	mV
LVDS Differential Input Resistance			80	100	120	Ω
LVDS Output Voltage High					1475	mV
LVDS Output Voltage Low			925			mV
LVDS Output Differential Voltage	V_{OD}	Figure 3	250		400	mV
LVDS Output Offset Voltage	V_{OS}	$V_{OS} = (V_{OUT+} + V_{OUT-})/2$, Figure 3	1125		1275	mV
LVDS Output Change in V_{OD}	$\lvert\Delta V_{OD}\rvert$	Between “0” and “1”			25	mV
LVDS Output Change in V_{OS}	$\lvert\Delta V_{OS}\rvert$	Between “0” and “1”			25	mV
LVDS Differential Output Resistance			80	100	140	Ω
LVCMOS Input Voltage Low	V_{IL}				0.8	V
LVCMOS Input Voltage High	V_{IH}		2.0			V
LVCMOS Input Current		$V_{IH} = V_{CC}$ or V_{IL} = ground	-10		+10	µA
Three-State Input Current		MVCO input, $V_{IH} = V_{CC}$ or V_{IL} = ground	-50		+50	µA
LVCMOS Output Voltage Low	V_{OL}	I_{OL} = 100µA			0.2	V
LVCMOS Output Voltage High	V_{OH}	I_{OH} = -100µA	V_{CC} - 0.2			V

Note 1: With a 19.4400MHz SMD AT-strip crystal at RFCK1 and RFCK2.

Note 2: Pattern is 16 x 2^7 - 1 PRBS, 100 CIDs, 16 x 2^7 - 1 PRBS inverted, 100 CIDs inverted.

Note 3: For 622Mbps operation, f_C = 500kHz.
For 1.244Gbps operation, f_C = 1MHz.
For 2.488Gbps operation, f_C = 2MHz.

Note 4: Jitter transfer from SDI to SDO, with parallel side looped back. Defined as:

$$\text{Jitter transfer} = \left[\frac{\text{jitter on upstream signal UI}}{\text{jitter on downstream signal UI}} \times \frac{\text{downstream bit rate}}{\text{upstream bit rate}}\right]$$

Note 5: Guaranteed by design and characterization.

Note 6: For 2.488Gbps operation, measurement bandwidth = 8kHz to 20MHz.
For 1.244Gbps operation, measurement bandwidth = 4kHz to 10MHz.
For 622Mbps operation, measurement bandwidth = 2kHz to 5MHz.
For 155Mbps operation, measurement bandwidth = 0.5kHz to 1.3MHz.

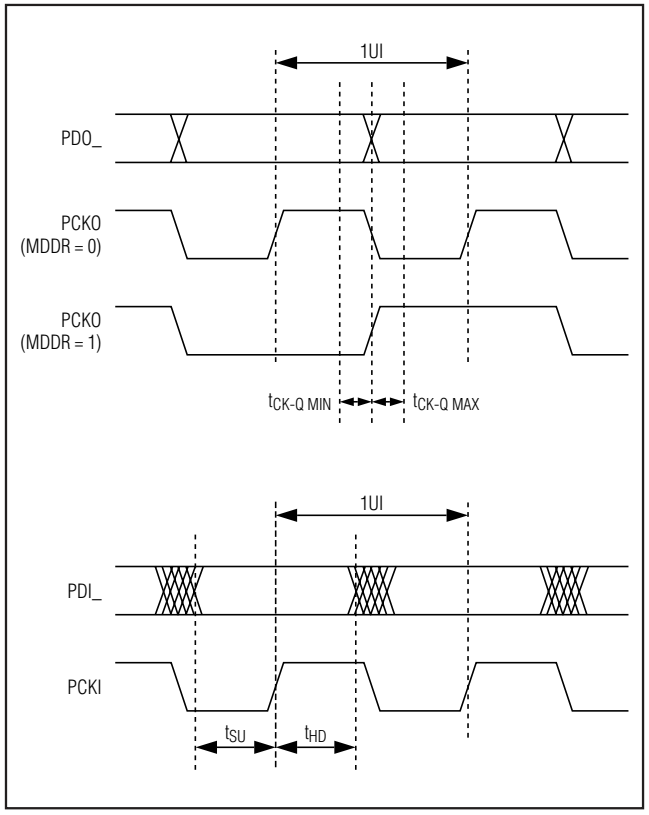


Figure 1. Parallel Interface Timing Diagrams

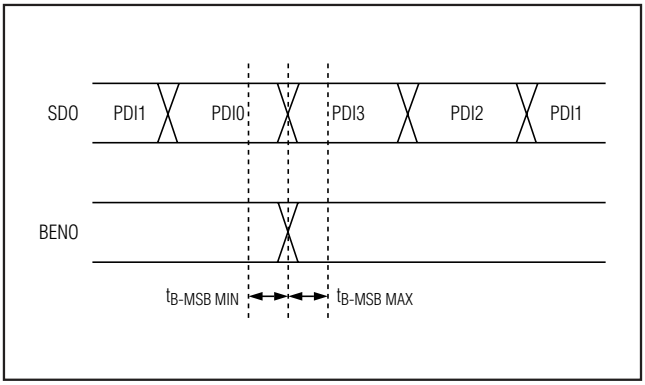


Figure 2. Burst-Enable Timing

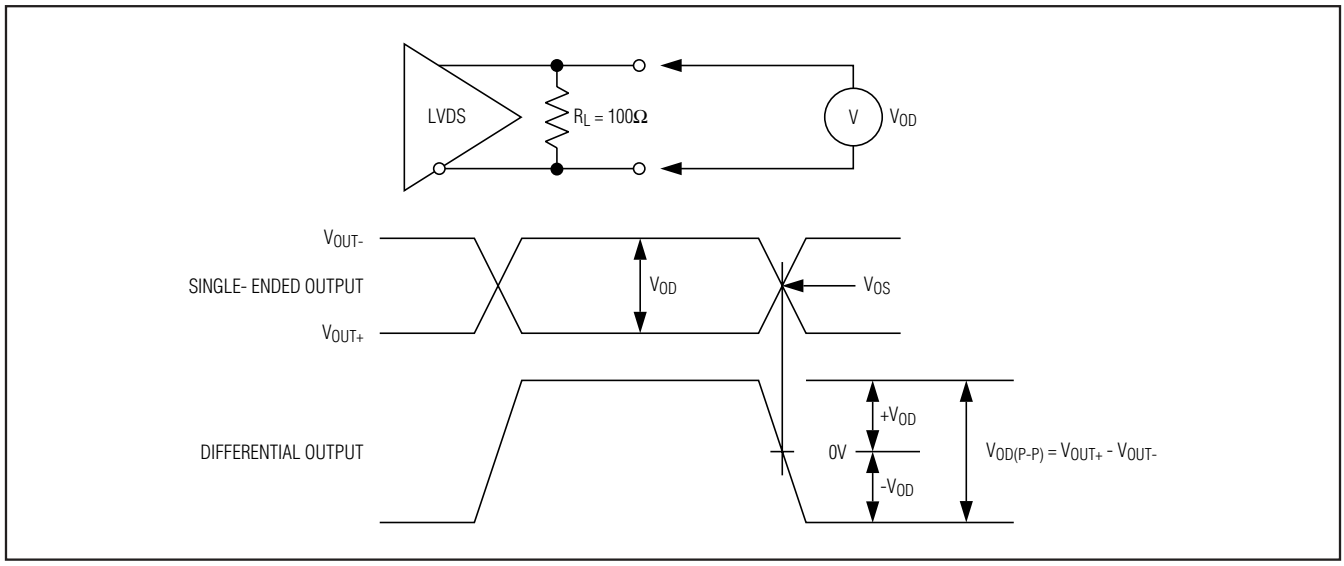


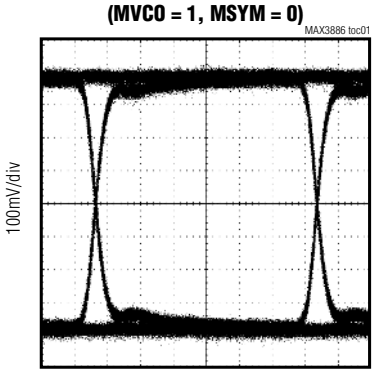
Figure 3. Definition of LVDS Output Levels

Multirate CDR with Integrated Serializer/Deserializer for GPON and BPON ONT Applications

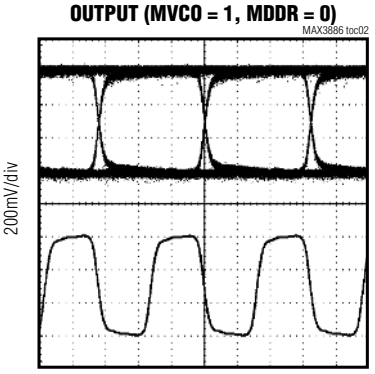
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

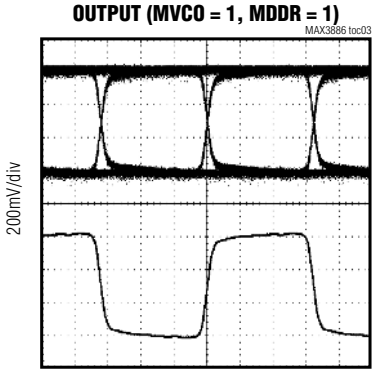
1.244Gbps SERIAL DATA OUTPUT (MVCO = 1, MSYM = 0)



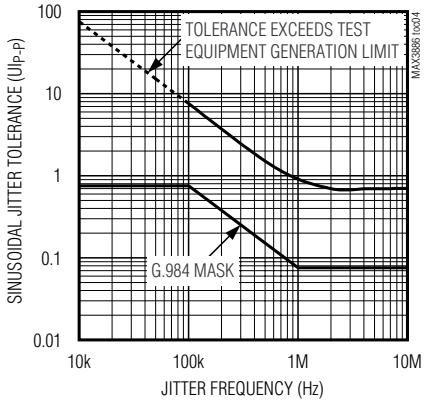
622Mbps PARALLEL DATA AND CLOCK OUTPUT (MVCO = 1, MDDR = 0)



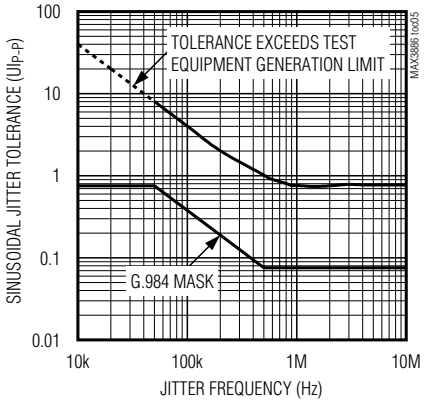
622Mbps PARALLEL DATA AND CLOCK OUTPUT (MVCO = 1, MDDR = 1)



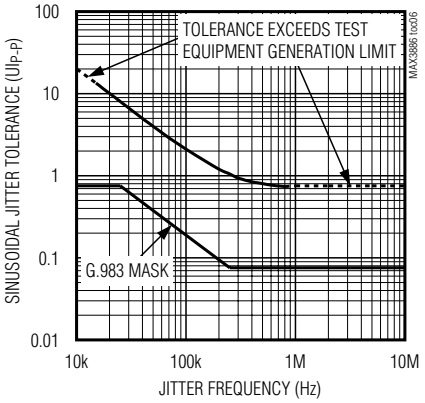
2.488Gbps JITTER TOLERANCE



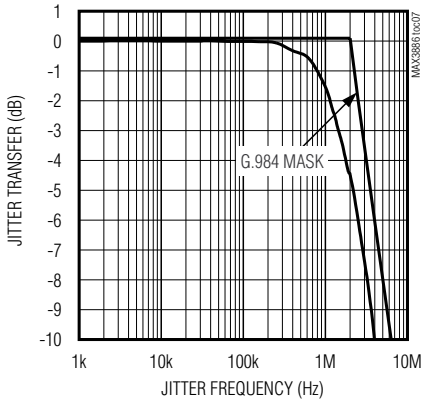
1.244Gbps JITTER TOLERANCE



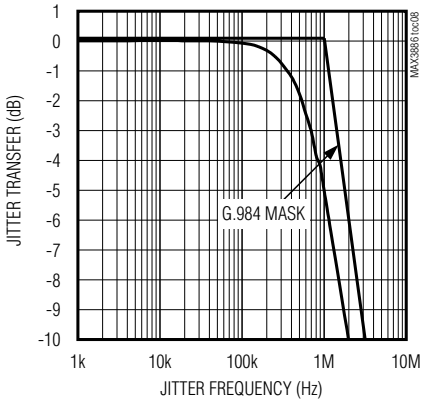
622Mbps JITTER TOLERANCE



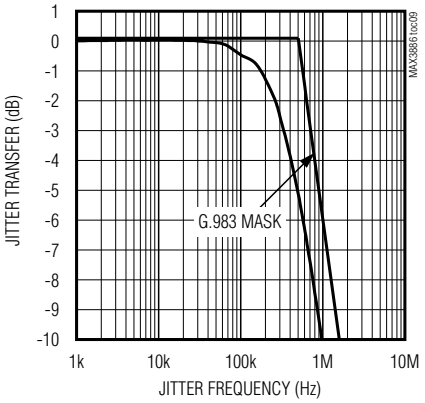
SDI TO SDO JITTER TRANSFER (SDI = 2.488Gbps)



SDI TO SDO JITTER TRANSFER (SDI = 1.244Gbps)



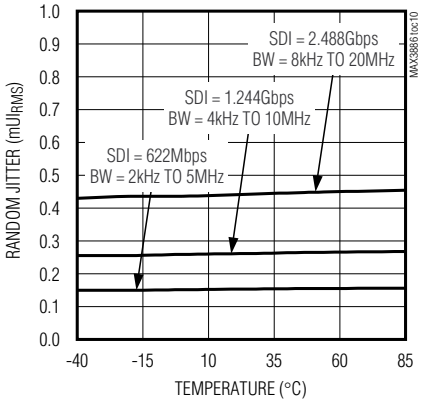
SDI TO SDO JITTER TRANSFER (SDI = 622Mbps)



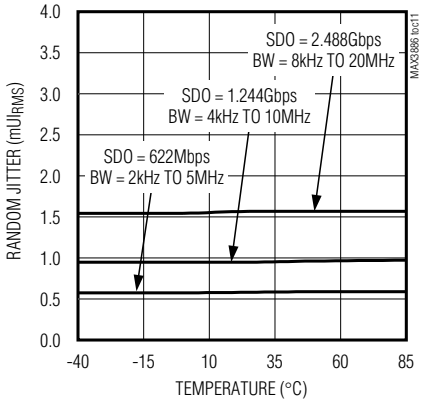
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

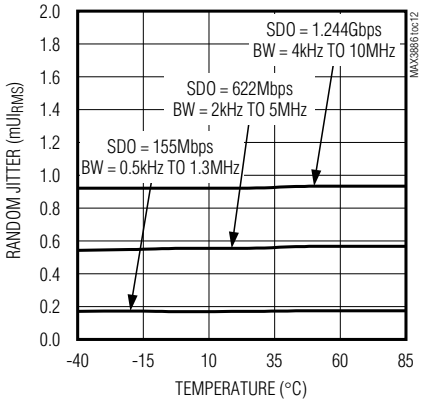
PARALLEL CLOCK OUTPUT RANDOM JITTER vs. TEMPERATURE



SDO RANDOM JITTER vs. TEMPERATURE (SYMMETRIC, MSYM = 1)



SDO RANDOM JITTER vs. TEMPERATURE (ASYMMETRIC, MSYM = 0)



Pin Description

PIN	NAME	FUNCTION
1, 14, 15, 29, 42, 43, 56	GND	Supply Ground
2	TP1	Test Pin, Reserved. Connect to GND for normal operation.
3, 6, 12, 28, 46, 53	V_{CC}	+3.3V Supply Voltage
4	SDI+	Positive Serial Data Input, CML or LVPECL
5	SDI-	Negative Serial Data Input, CML or LVPECL
7	BENO-	Negative Burst-Enable Output, CML
8	BENO+	Positive Burst-Enable Output, CML
9	TP2	Test Pin, Reserved. Connect to V_{CC} for normal operation.
10	SDO-	Negative Serial Data Output, CML
11	SDO+	Positive Serial Data Output, CML
13	TP3	Test Pin, Reserved. Connect to GND for normal operation.
16	PCKI+	Positive Parallel Clock Input, LVDS
17	PCKI-	Negative Parallel Clock Input, LVDS
18	PDI3+	Positive Parallel Data Input 3, LVDS, MSB (First Serial Bit Out)
19	PDI3-	Negative Parallel Data Input 3, LVDS, MSB (First Serial Bit Out)
20	PDI2+	Positive Parallel Data Input 2, LVDS
21	PDI2-	Negative Parallel Data Input 2, LVDS
22	PDI1+	Positive Parallel Data Input 1, LVDS

Pin Description (continued)

PIN	NAME	FUNCTION
23	PDI1-	Negative Parallel Data Input 1, LVDS
24	PDI0+	Positive Parallel Data Input 0, LVDS, LSB (Last Serial Bit Out)
25	PDI0-	Negative Parallel Data Input 0, LVDS, LSB (Last Serial Bit Out)
26	BENI+	Positive Burst Enable Input, LVDS
27	BENI-	Negative Burst Enable Input, LVDS
30	RCKO+	Positive Parallel Rate Reference Clock Output, LVDS
31	RCKO-	Negative Parallel Rate Reference Clock Output, LVDS
32	PDO3+	Positive Parallel Data Output 3, LVDS, MSB (First Serial Bit In)
33	PDO3-	Negative Parallel Data Output 3, LVDS, MSB (First Serial Bit In)
34	PDO2+	Positive Parallel Data Output 2, LVDS
35	PDO2-	Negative Parallel Data Output 2, LVDS
36	PDO1+	Positive Parallel Data Output 1, LVDS
37	PDO1-	Negative Parallel Data Output 1, LVDS
38	PDO0+	Positive Parallel Data Output 0, LVDS, LSB (Last Serial Bit In)
39	PDO0-	Negative Parallel Data Output 0, LVDS, LSB (Last Serial Bit In)
40	PCKO+	Positive Parallel Clock Output, LVDS; Rate/4 or Rate/8, depending on value of MDDR pin. See Figure 1 for timing diagram.
41	PCKO-	Negative Parallel Clock Output, LVDS; Rate/4 or Rate/8, depending on value of MDDR pin. See Figure 1 for timing diagram.
44	FERR	FIFO Error Output, LVCMOS. A high output indicates when the FIFO read and write clocks attempt to access the same register. Normally connected to MAC IC.
45	FRST	FIFO Reset Input, LVCMOS. A high input resets the FIFO. Normally connected to MAC IC.
47	RFCK2	Reference Clock Crystal Input. A 19.4400MHz crystal must be connected between RFCK1 and RFCK2; or a 19.4400MHz LVCMOS clock source (capable of driving up to 10pF load) can be connected through a 10pF ±10% series capacitor to RFCK1, RFCK2 unconnected.
48	RFCK1	Reference Clock Crystal Input. See Pin 47.
49	MDDR	Dual Data Rate Select Input, LVCMOS. A high input selects dual data rate (DDR) parallel clock output. See Figure 1 for timing diagram.
50	MSYM	Symmetric Select Input, LVCMOS. A high input selects symmetric operation, a low input selects asymmetric operation. See Table 2.
51	MVCO	VCO Rate Select Input, Three-State. See Table 2.
52	LOCK	PLL Lock Detector Output, LVCMOS. A high output indicates the PLL is in lock, this output can chatter when no valid input signal is present.
54	CFIL	PLL Filter Capacitor Connection. Connect a 0.27µF ceramic capacitor (±10%, 10V, X7R-type) between pin 54 and pin 53.
55	TP4	Test Pin, Reserved. Connect to V_{CC} for normal operation.
—	EP	Exposed Paddle. Connect to thermal and electrical ground.

Detailed Description

The MAX3886 CDR/SerDes provides 2.488Gbps/1.244Gbps/622Mbps clock and data recovery, plus 1:4 deserializer for continuous downstream data and 1:4 serializer for burst upstream data (Figure 4). Specifically designed for GPON and BPON ONT applications, the serializer uses the recovered downstream clock to serialize the upstream serial data (loop-timed serialization). The upstream rate can be configured to be either equal to the downstream rate (symmetric operation) or a submultiple of the downstream rate (asymmetric operation). A low-cost 19.4400MHz SMD-type crystal or external LVCMOS source serves as the CDR frequency reference, providing robust frequency acquisition and lock detection.

A parallel rate reference clock output, derived from the recovered downstream signal, is provided for use by the MAC layer IC, and an integrated FIFO is provided to deal with phase variation between the serializer and MAC layer IC. Once the FIFO has been initialized, the serializer tolerates up to one parallel UI phase difference between the read and write clocks. The FIFO circuitry includes an error output that indicates when the FIFO attempts to read and write from the same location. An integrated burst-enable signal path also includes the FIFO to simplify upstream burst timing.

The deserializer parallel output clock can optionally be configured for dual data rate (DDR) operation. The high-speed CML-format serial-data interfaces are compatible with Maxim burst-mode laser drivers and both CML and LVPECL limiting amplifiers. The parallel data interfaces are LVDS format for compatibility with FPGAs or ASICs.

Serial Input Clock/Data Recovery

Clock and data recovery is provided by a phase-locked loop (PLL) with selectable 2.488GHz/1.244GHz/622MHz operation. The operating frequency is controlled by the three-state MVCO input. A phase detector and filter generate error voltage proportional to the phase difference between the internal VCO and the input data, and feedback in the PLL drives the error voltage to zero, aligning the recovered clock to the center of the input data for retiming.

A frequency detector assists the PLL to “pull in” to the serial data and generates the lock indicator signal on the LOCK pin. When no valid input signal is present, the LOCK output can oscillate (chatter) as the PLL hunts for the input signal.

The PLL VCO and integrated loop filter implement a second-order transfer function, with loop bandwidth dependent on the VCO rate selected (e.g., 1.5MHz for 2.488Gbps). An external filter capacitor, connected between CFIL and V_{CC} sets the damping factor of the PLL. All jitter specifications are based on an external 0.27µF capacitor. Modifying the value of CFIL changes jitter peaking, acquisition time, and loop stability but not loop bandwidth.

PLL Reference Clock Oscillator

An integrated oscillator provides a reference clock signal for robust CDR acquisition and lock detection. This oscillator requires a 19.4400MHz crystal connected between RFCK1 and RFCK2, or an external LVCMOS 19.4400MHz clock source can be used. See the *Applications Information* section for important information about crystal selection and how to connect an external clock source.

Deserializer and Parallel Output

The downstream data is deserialized, producing four parallel LVDS outputs, PDO[3:0]±. The first serial data bit received on the SDI input is the most significant bit (MSB), which is routed to the parallel output PDO3. The LVDS parallel output clock, PCKO, can be configured for either full rate or half rate operation, as shown in the timing diagrams of Figure 1. The PCKO rate is controlled using the LVCMOS MDDR input. Set the MDDR pin to logic high to clock out parallel data on each edge of the PCKO clock.

Parallel Input, FIFO, and Serializer

Parallel data presented at the four LVDS data inputs PDI[3:0]± is latched into the input register using the LVDS parallel input clock PCKI and clocked out of the ONT SerDes using the recovered serial clock. The parallel data bit PDI3 is the MSB and the first bit out of the serial SDO output. For GPON and BPON ONT applications, the clock multiplier unit (CMU) frequency synthesizer normally incorporated in SONET serializers is eliminated, improving PON performance. Asymmetric operation is configured using the LVCMOS MSYM input (see Table 2). The parallel clock is also output on the LVDS RCKO pins for use, if needed, by the MAC layer.

The serializer’s 4-bit-long FIFO accommodates phase variation between RCKO and PCKI. PCKI provides the FIFO write clock and the internal RCKO is the read clock (loading the 4:1 serializer); this arrangement allows the phase relationship between these two clocks to vary ±1UI. In the event that valid read and write clocks attempt to access the same FIFO address, this error condition is indicated on the LVCMOS FERR output. To initiate the FIFO or clear an error condition, the LVCMOS FRST input must be asserted high for at least 4UI while valid clocks are present.

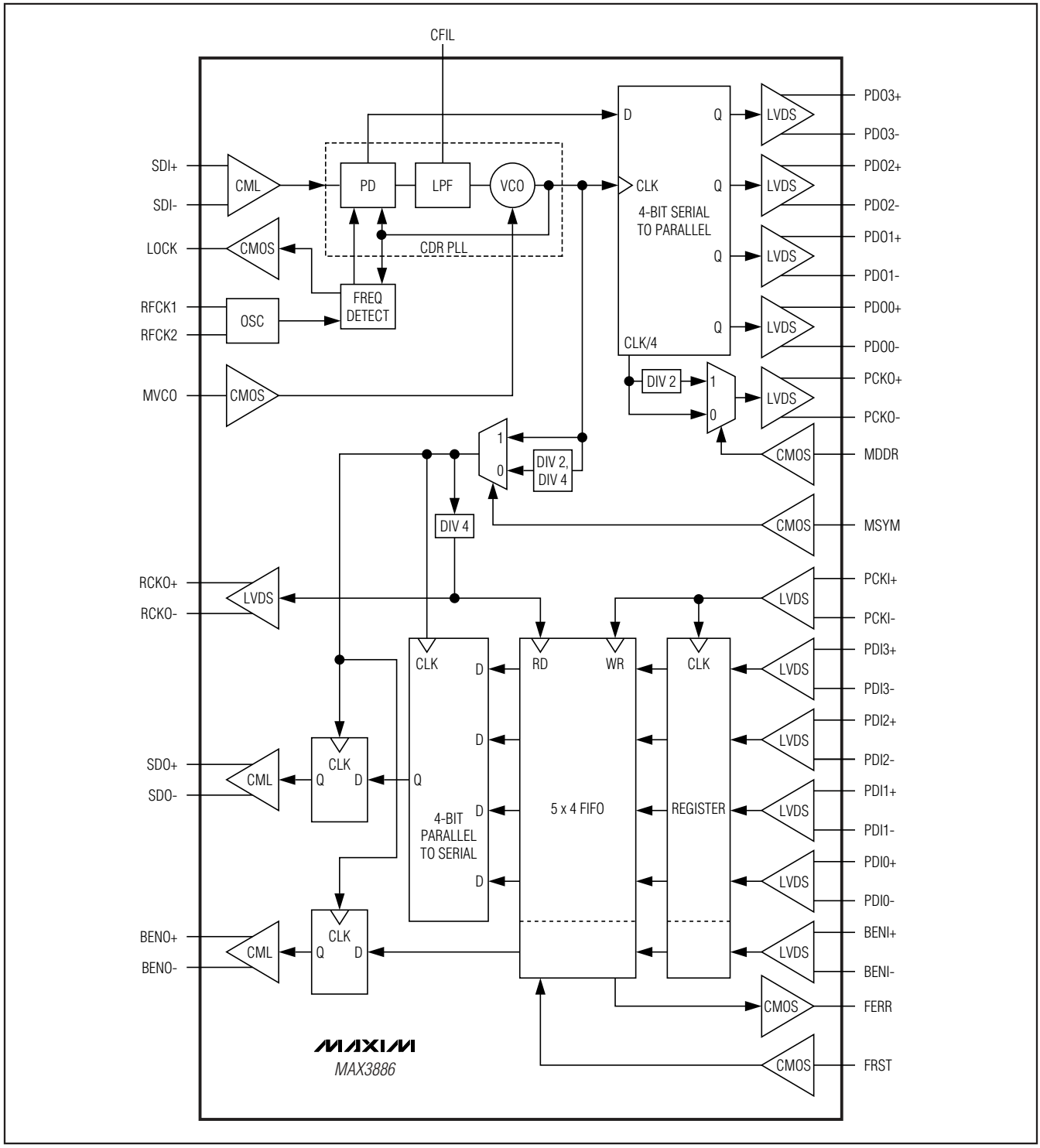


Figure 4. Functional Diagram

Burst-Enable Signal Processing

To minimize PON overhead, it is important that the laser driver burst-enable (BEN) signal correspond accurately with the beginning of the serial data burst. This is supported in the MAX3886 by the BENI LVDS input and associated signal path. The LVDS burst-enable signal from the MAC layer IC is passed through the same FIFO as the parallel data and output on the BENO CML output, which ensures that the laser driver's burst enable matches the beginning of the associated serial MSB. If FRST or FERR are high, the BENO output is forced low to prevent the laser driver from transmitting erroneous data. The parallel data setup and hold timing requirements also apply to the burst-enable signal.

Lock Detector Output

The lock detector operates by comparing a divided-down version of the VCO output to the reference clock. The LOCK output pin indicates lock (high) when the frequency difference between the reference clock and the CDR VCO is less than 250ppm, within the "pullin" range of the PLL. The LOCK output indicates out-of-lock (low) when the frequency difference between the reference clock and the CDR VCO becomes more than 500ppm. When valid input data is present, this provides a stable lock indication.

At power-up, the CDR takes approximately 50ms (if valid NRZ data is present) for initial acquisition while the internal reference oscillator, the PLL, and the frequency detector reach their operating conditions. During this startup period, the LOCK status output may provide false indication of a lock condition. Once the PLL and frequency detector are initialized, the nominal time for reacquisition of an NRZ input is 2ms.

When valid NRZ input data is not present, the lock detector may produce a chattering LOCK indicator output while the PLL searches for the input frequency. If needed, an external digital filter can be used to mask this chattering.

Table 1. Lock Detector Output

CDR INPUT	LOCK OUTPUT
Valid NRZ data	1
No CDR input	0/1 (chatter)

Control Input Summary

Table 2 summarizes the clock and data rates as controlled by MVCO, MSYM, and MDDR.

Table 2. Clock and Data Rate Controls

MVCO	MSYM	MDDR	Rx			Tx			
			SDI RATE (Mbps)	PDO RATE (Mbps)	PCKO (MHz)	SDO RATE (Mbps)	PDI RATE (Mbps)	PCKI (MHz)	RCKO (MHz)
0	0	0	622	155	155	155	39	39	39
0	0	1	622	155	78	155	39	39	39
0	1	0	622	155	155	622	155	155	155
0	1	1	622	155	78	622	155	155	155
Open	0	0	1244	311	311	622	155	155	155
Open	0	1	1244	311	155	622	155	155	155
Open	1	0	1244	311	311	1244	311	311	311
Open	1	1	1244	311	155	1244	311	311	311
1	0	0	2488	622	622	1244	311	311	311
1	0	1	2488	622	311	1244	311	311	311
1	1	0	2488	622	622	2488	622	622	622
1	1	1	2488	622	311	2488	622	622	622

Multirate CDR with Integrated Serializer/Deserializer for GPON and BPON ONT Applications

Applications Information

Interfacing to the CDR/SerDes

The MAX3886 has CML, LVDS, and LVCMOS inputs and outputs. The high-speed CML (LVPECL-compatible) inputs, SDI±, are biased to V_{CC} - 1.3V with an on-chip high-impedance network (Figure 5). Figures 6 and 7 provide examples of DC-coupled and AC-coupled termination networks that can be used to connect the limiting amplifier outputs (CML or LVPECL) to the SDI± inputs. The two high-speed CML outputs, SDO± and BENO±, have internal 50Ω back terminations to V_{CC} (Figure 8) and should be terminated with 50Ω to V_{CC} or 100Ω differential at the laser driver inputs (Figure 9). The burst SDO and BENO outputs must be DC-coupled to the laser driver for proper operation. SDO can be AC-coupled if a continuous serial signal is provided between bursts (with gating provided by the laser driver BEN input).

The LVDS outputs (PDO[3:0]±, PCKO±, RCKO±) require 100Ω differential termination for proper operation. The LVDS inputs (PDI[3:0]±, PCKI±) are internally terminated with 100Ω differential resistance, eliminating the need for external termination when connected to an LVDS output (Figure 10).

Equivalent circuits for the three-state input (MVCO), LVCMOS inputs (MSYM, MDDR, FRST), and LVCMOS outputs (LOCK, FERR) are given in Figure 11, Figure 12, and Figure 13. For more information on interfacing to Maxim's high-speed I/O circuits, refer to Application Note HFAN-01.0: *Introduction to LVDS, PECL, and CML*.

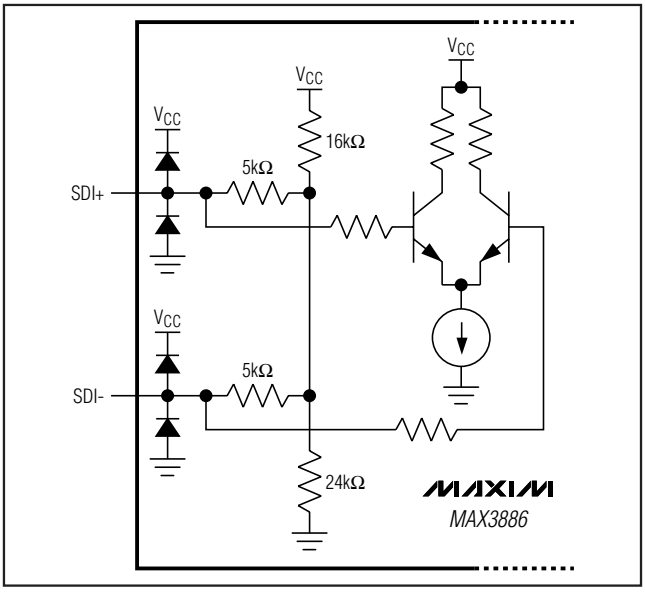


Figure 5. CML (LVPECL-Compatible) Input

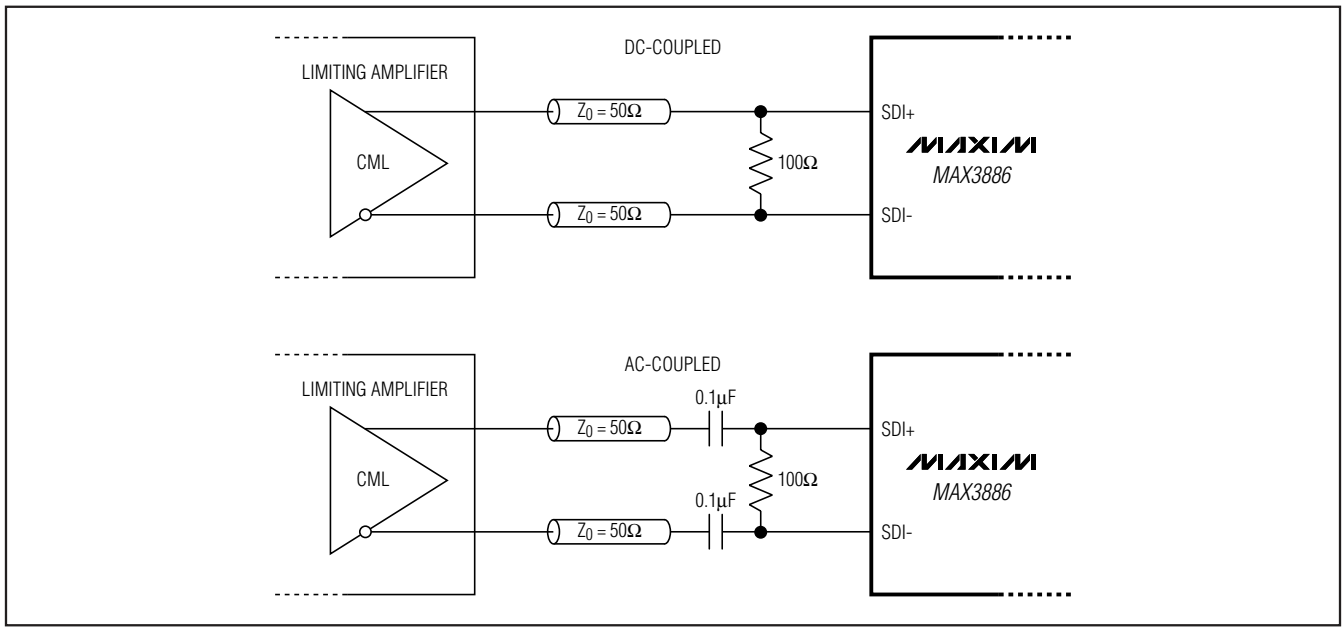


Figure 6. Interface to Limiting Amplifier (CML Outputs)

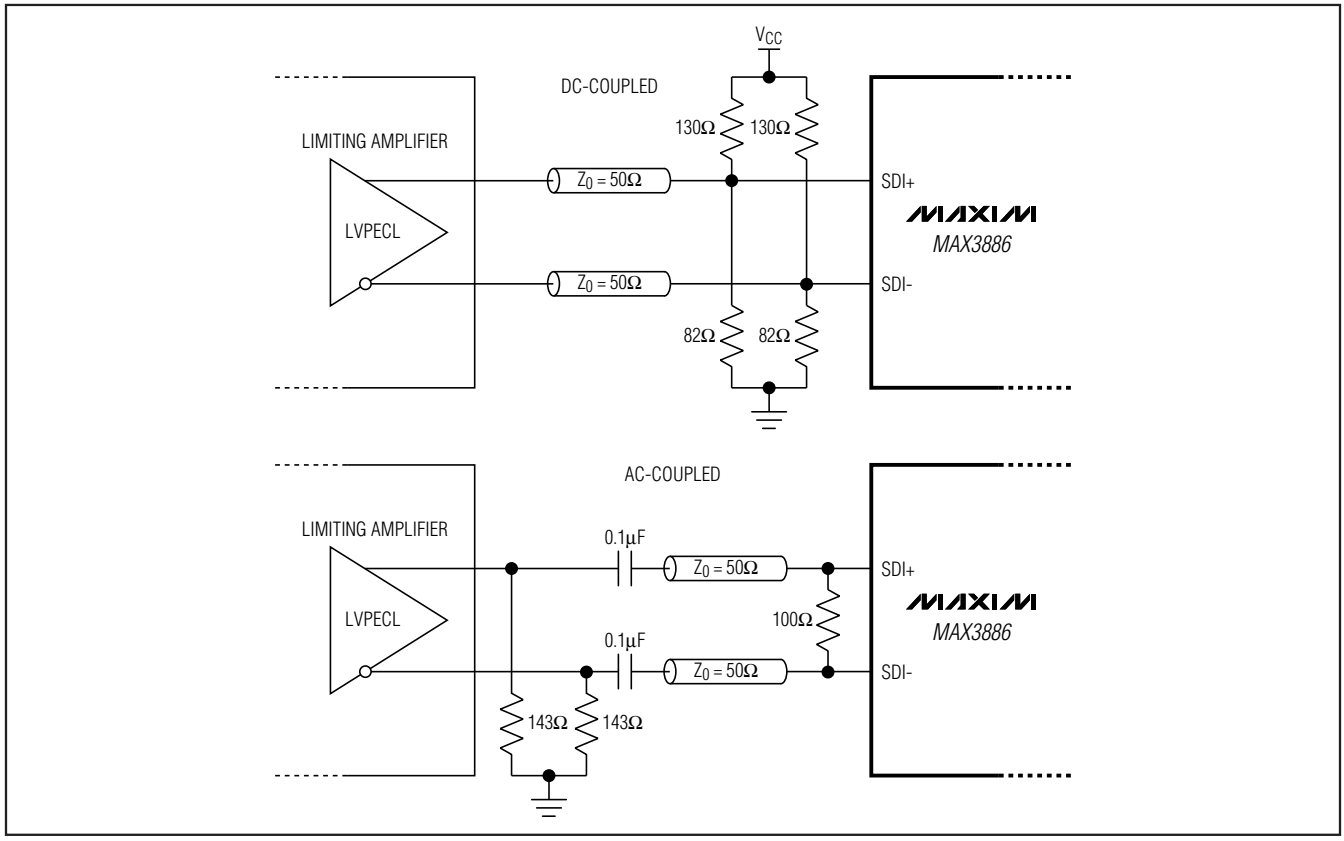


Figure 7. Interface to Limiting Amplifier (LVPECL Outputs)

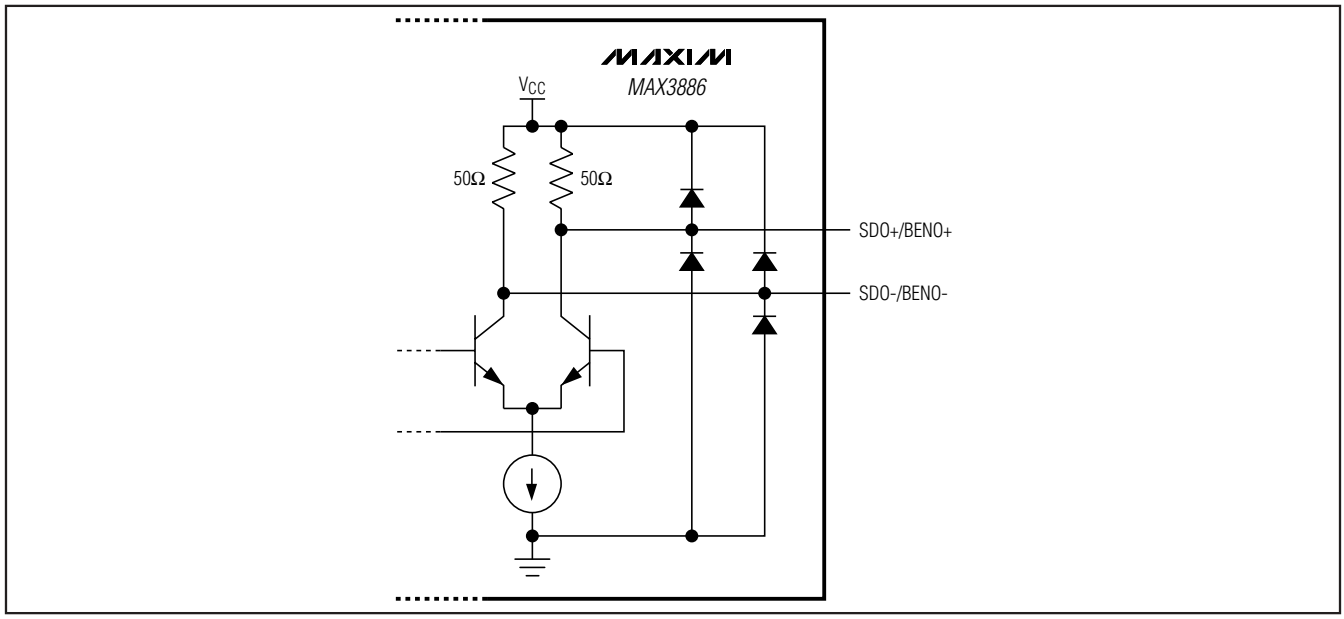


Figure 8. CML Outputs

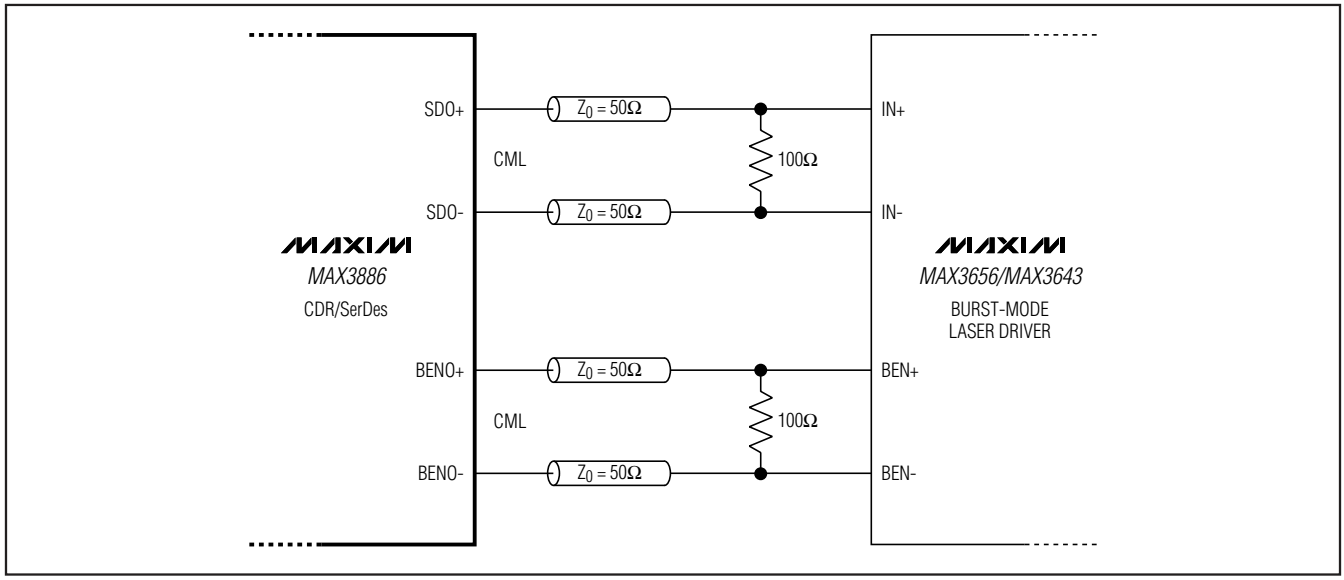


Figure 9. Interface to Laser Driver

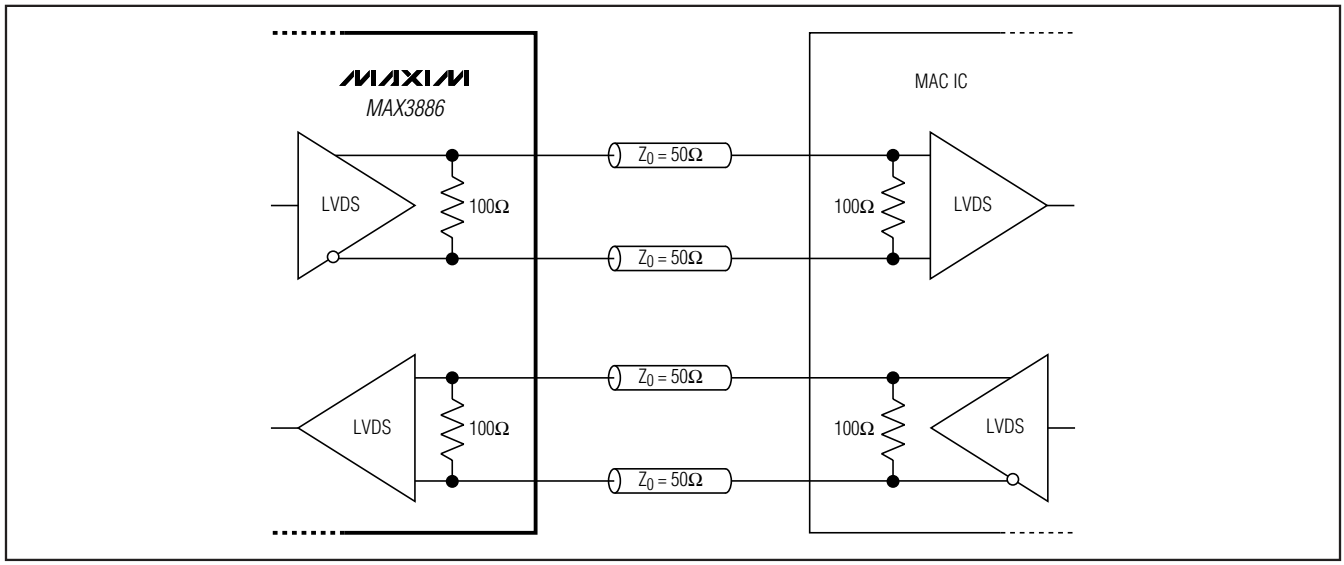


Figure 10. LVDS Interface

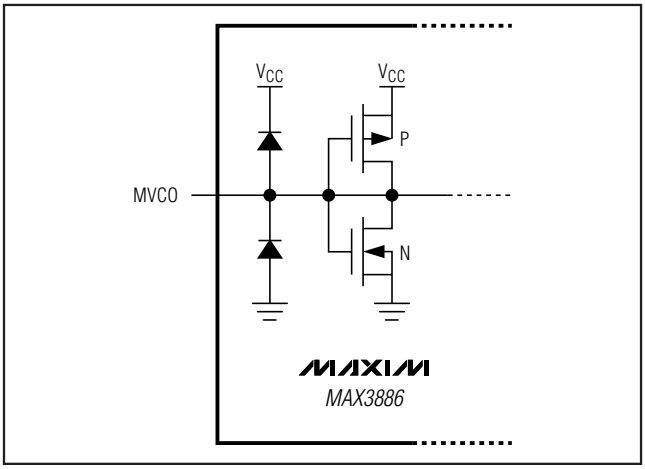


Figure 11. Three-State Input (MVCO)

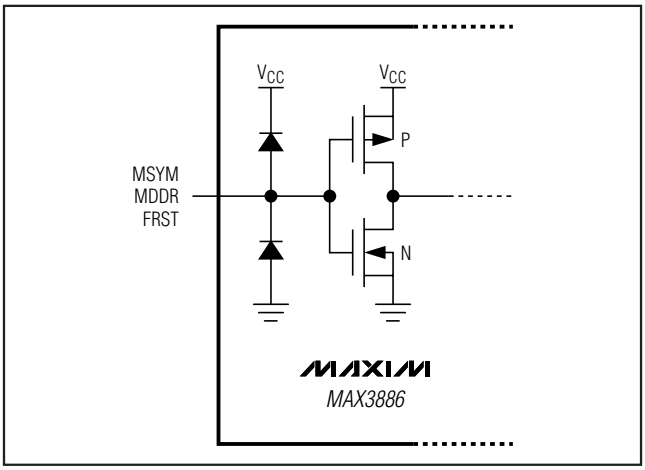


Figure 12. LVCMOS Inputs

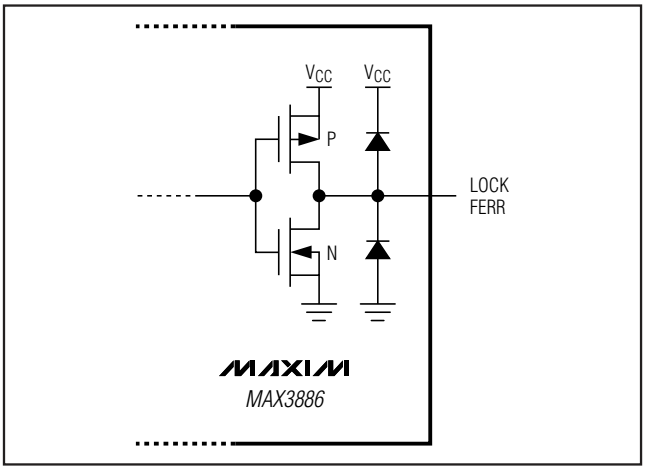


Figure 13. LVCMOS Outputs

FIFO Control Signals

A valid input at FRST is required to initialize the FIFO after the relationship between PCKO or RCKO and PCKI has stabilized prior to operating the serializer, or after the FERR output has indicated that the FIFO has overflowed or underflowed due to the phase difference between PCKO or RCKO and PCKI exceeding its capacity. The MAC IC provides the control signal for FRST. FERR should not be directly connected to FRST.

If the PCKI signal is interrupted between bursts, the FIFO must be reset before the beginning of each burst while valid clocks are present. If a continuous PCKI signal is provided between bursts, the FIFO maintains the correct FIFO counter values as long as the phase relationship does not change.

Reference Clock Oscillator

The integrated reference oscillator requires a parallel resonant 19.4400MHz AT-strip cut crystal connected between pins RFCK1 and RFCK2. It has 18pF nominal (15pF to 21pF) of on-chip crystal load capacitance; any frequency error due to mismatch to the rated crystal load capacitance must be included in the budget for the difference between reference clock frequency and input data rate. Take care that the wiring capacitances at the nodes RFCK1 and RFCK2 are controlled (typically no more than 2pF) to ensure proper operation.

To drive the reference clock with an external 19.4400MHz LVCMOS clock source, connect it to RFCK1 through a 10pF ±10% series capacitor and leave RFCK2 open. The LVCMOS clock source must be capable of driving a 10pF load.

To ensure proper acquisition, the maximum difference between the downstream data rate (divided down to 19.4400MHz) and 19.4400MHz clock should be 500ppm, including 57ppm required by the CDR itself. Table 3 shows a typical budget.

Table 3. Typical Frequency Budget

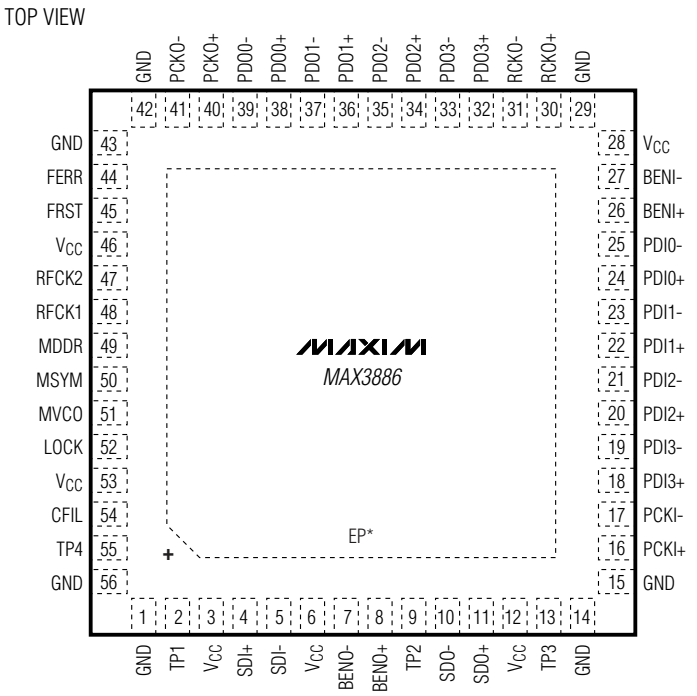
DESCRIPTION	Δf (±ppm)	NOTES
Downstream Data Rate	50	G.983, G.984
Crystal Load Capacitance	63	e.g., 21ppm/pF Δ from 18pF
Crystal Tolerance	75	
Crystal Temperature Stability	100	
Crystal Aging	50	
CDR Operation	57	
Total	395	Total is less than 500ppm

Power Supply and Ground Connection

The MAX3886 has six V_{CC} connection pads, and installation of a bypass capacitor at each V_{CC} pad is recommended. All six V_{CC} connections should be driven from the same source to eliminate the possibility of independent power-supply sequencing. Pin 53 provides current directly to the internal VCO stage; excessive supply noise at this node can result in increased jitter.

The 56-pin TQFN package features an exposed pad (EP) that provides a low resistance thermal path for heat removal from the IC and must be connected to the circuit board ground plane for proper operation. The EP also provides essential electrical ground connectivity.

Pin Configuration



THIN QFN
(8mm × 8mm × 0.8mm)

* THE EXPOSED PAD OF THE THIN QFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL AND ELECTRICAL OPERATION.

Chip Information

TRANSISTOR COUNT: 10,684

PROCESS: SiGe BiCMOS

Package Information

(For the latest package outline information, go to **www.maxim-ic.com/packages**.)

PACKAGE TYPE	DOCUMENT NO.
56 Thin QFN	**21-0135**