Ultra Flat, High Gain Wideband DVGA with addressable function

500MHz - 8000MHz

Device Features

- Integrate AMP1 + DSA + AMP2 Functionality
- 500 - 8000MHz Broadband Performance
- Wide VDD Range
  AMP1 & AMP2 : 4.0V to 5.25V
  DSA : 2.7V to 5.5V
- Low Current : 215mA @ 5V, 110mA @ 4V
- High Gain
  41.5dB @ 1.9GHz, 40.5dB @ 3.5GHz (VDD=5V)
  39.9dB @ 1.9GHz, 39.0dB @ 3.5GHz (VDD=4V)
- High OP1dB
  21.3dBm @ 1.9GHz, 21.2dBm @ 3.5GHz (VDD=5V)
  19.1dBm @ 1.9GHz, 19.5dBm @ 3.5GHz (VDD=4V)
- High OIP3
  36.3dBm @ 1.9GHz, 35.6dBm @ 3.5GHz (VDD=5V)
  31.3dBm @ 1.9GHz, 32.8dBm @ 3.5GHz (VDD=4V)
- Excellent Noise Figure
  1.5dB @ 1.9GHz, 1.8dB @ 3.5GHz (ATT=0dB)
  3.2dB @ 1.9GHz, 3.4dB @ 3.5GHz (ATT=15.75dB)
- Attenuation Range : Up to 31.75dB / 0.25dB step
- Safe attenuation state transitions
- Excellent attenuation accuracy
  ±(0.25 + 3% x ATT) @ 1.9GHz
  ±(0.25 + 5% x ATT) @ 3.5GHz
- Programming modes
  Serial mode only to minimize Control line
- 2bit Addressable function
  LE/DATA/CLK can be shared up to 4EA Chips
- Lead-free/RoHS2-compliant 32-lead 5mm x 5mm x 0.9mm QFN SMT package

32-lead 5mm x 5mm x 0.9mm QFN

Figure 1. Package Type

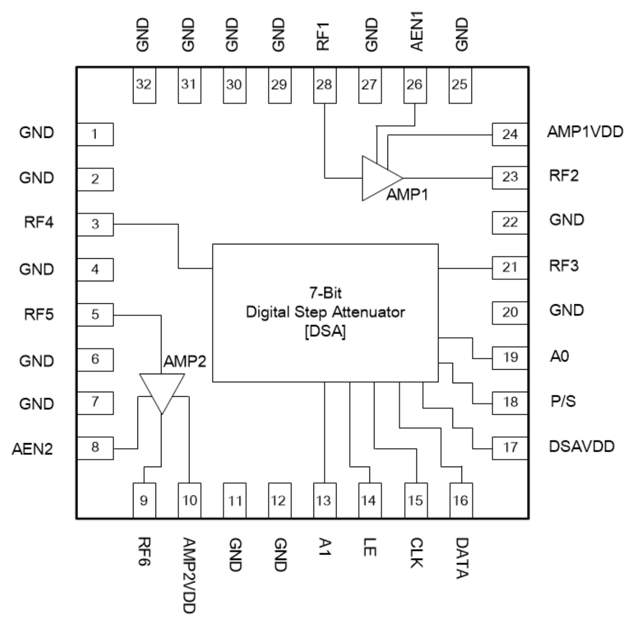


Figure 2. Functional Block Diagram

Product Description

The BVA2762 is a wideband flat high gain and high linearity DVGA (Digitally controlled variable gain amplifier) operating from 500MHz to 8GHz.

The BVA2762 integrates a high performance digital step attenuator (DSA) and two high linearity, broadband gain block amplifier operating voltage 4.0V to 5.25V DC within AMP enable control using the small package (5x5mm QFN package).

Both DSA and gain block amplifiers in BVA2762 are internally matched to 50 Ohms and It is easy to use with minimum external matching components required.

The BVA2762 can control 7bit attenuation to 0.25dB step up to 31.75dB and initialize to the maximum attenuation setting on power-up until next programming word is inputted.
In addition, Internal DSA has a 2-bit addressable function, so it can share up to 4 DSA's Latch Enable (LE), DATA and CLOCK(CLK) pin. This has the advantage of reducing the number of IO pins when using multiple DSA or DVGA chip with addressable function.

The BVA2762 is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless application.

Application

- 5G/4G/3G Wireless infrastructure and other high performance RF application
- Microwave and Satellite Radio
- General purpose Wireless

Table 1. Electrical Specifications [1] @ VDD = 5V

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			500		8000	MHz
Gain [2]		ATT = 0dB @ 3500MHz		40.5		dB
Attenuation Control range		0.25dB Step		0 - 31.75		dB
Attenuation Step				0.25		dB
Attenuation Accuracy	0.5GHz - 1GHz	Any bit or bit combination			±(0.25 + 2% of ATT setting)	dB
	1GHz - 2GHz				±(0.25 + 3% of ATT setting)	
	2GHz - 3GHz				±(0.25 + 3% of ATT setting)	
	3GHz - 4GHz				±(0.25 + 5% of ATT setting)	
	4GHz - 6GHz				±(0.25 + 5% of ATT setting)	
	6GHz - 8GHz				±(0.25 + 5% of ATT setting)	
Input Return loss	0.5GHz - 2GHz	ATT = 0dB		-15		dB
	2GHz - 4GHz			-12		
	4GHz - 6GHz			-13		
	6GHz - 8GHz			-14		
Output Return loss	0.5GHz - 2GHz	ATT = 0dB		-15		dB
	2GHz - 4GHz			-12		
	4GHz - 6GHz			-10		
	6GHz - 8GHz			-10		
Output Power for 1dB Compression		ATT = 0dB @ 3500MHz		21.2		dBm
Output Third Order Intercept Point [3]		ATT = 0dB @ 3500MHz		35.6		dBm
Noise Figure		ATT = 0dB @ 3500MHz		1.8		dB
DSA Switching time		50% CTRL to 90% or 10% RF		500	800	ns
AMP Switching time		50% CTRL to 90% or 10% RF		150		ns
Maximum Spurious level		Measured @ RF3, RF4 ports		< -145		dBm
Impedance				50		Ω

1. Device performance _ measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+5.0V, measure on Evaluation Board (AMP1 + DSA + AMP2)
2. Gain data has PCB & Connectors insertion loss de-embedded
3. OIP3 _ measured with two tones at an output of 5dBm per tone separated by 1MHz.

Table 2. Electrical Specifications [1] @ VDD = 4V

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			500		8000	MHz
Gain [2]		ATT = 0dB @ 3500MHz		39		dB
Attenuation Control range		0.25dB Step		0 - 31.75		dB
Attenuation Step				0.25		dB
Attenuation Accuracy	0.5GHz - 1GHz	Any bit or bit combination			±(0.25 + 2% of ATT setting)	dB
	1GHz - 2GHz				±(0.25 + 3% of ATT setting)	
	2GHz - 3GHz				±(0.25 + 3% of ATT setting)	
	3GHz - 4GHz				±(0.25 + 5% of ATT setting)	
	4GHz - 6GHz				±(0.25 + 5% of ATT setting)	
	6GHz - 8GHz				±(0.25 + 5% of ATT setting)	
Input Return loss	0.5GHz - 2GHz	ATT = 0dB		-14		dB
	2GHz - 4GHz			-13		
	4GHz - 6GHz			-14		
	6GHz - 8GHz			-14		
Output Return loss	0.5GHz - 2GHz	ATT = 0dB		-15		dB
	2GHz - 4GHz			-12		
	4GHz - 6GHz			-10		
	6GHz - 8GHz			-10		
Output Power for 1dB Compression		ATT = 0dB @ 3500MHz		19.5		dBm
Output Third Order Intercept Point [3]		ATT = 0dB @ 3500MHz		32.8		dBm
Noise Figure		ATT = 0dB @ 3500MHz		1.8		dB
DSA Switching time		50% CTRL to 90% or 10% RF		500	800	ns
AMP Switching time		50% CTRL to 90% or 10% RF		150		ns
Maximum Spurious level		Measured @ DSA RF3, RF4 ports		< -145		dBm
Impedance				50		Ω

1. Device performance _ measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+4.0V, measure on Evaluation Board (AMP1 + DSA + AMP2)
2. Gain data has PCB & Connectors insertion loss de-embedded
3. OIP3 _ measured with two tones at an output of 5dBm per tone separated by 1MHz.

Table 3. Typical RF Performance (VDD = 5.0V)[1]

Parameter	Frequency								Unit
	900[3]	1800[4]	2140[4]	2650[4]	3500[5]	4650[5]	6300[6]	7200[6]	MHz
Gain[7]	42.0	41.6	41.4	41.0	40.5	40.5	38.5	38.6	dB
S11	-26.4	-10.0	-9.5	-13.2	-10.1	-20.7	-16.3	-15.1	dB
S22	-16.4	-18.4	-26.6	-28.3	-13.5	-7.7	-8.5	-11.8	dB
OIP3[8]@ ATT=0dB	36.7	36.7	35.1	35.4	35.6	36.5	34.0	33.6	dBm
OIP3[8]@ ATT=15.75dB	36.2	35.1	34.6	33.8	33.3	32.8	31.6	31.8	dBm
P1dB	20.6	21.2	21.5	21.8	21.2	19.0	18.6	17.2	dBm
Noise Figure	1.5	1.5	1.5	1.5	1.8	2.0	2.3	2.8	dB

Table 4. Typical RF Performance (VDD = 4.0V)[2]

Parameter	Frequency								Unit
	900[3]	1800[4]	2140[4]	2650[4]	3500[5]	4650[5]	6300[6]	7200[6]	MHz
Gain[7]	40.4	40.0	39.7	39.6	39.0	39.1	37.1	36.9	dB
S11	-21.5	-8.0	-7.7	-11.1	-9.8	-16.5	-15.6	-11.6	dB
S22	-18.7	-20.0	-19.2	-22.0	-13.0	-9.9	-10.5	-13.8	dB
OIP3[8]@ ATT=0dB	31.6	31.5	30.2	31.4	32.8	34.0	33.0	31.8	dBm
OIP3[8]@ ATT=15.75dB	30.1	29.9	29.2	28.8	31.6	31.6	30.2	28.2	dBm
P1dB	18.8	19.2	19.0	19.8	19.5	17.6	17.1	15.8	dBm
Noise Figure	1.5	1.5	1.5	1.5	1.8	2.0	2.3	2.9	dB

1. Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+5.0V, 50 Ω system. (AMP1 + DSA + AMP2)
2. Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+4.0V, 50 Ω system. (AMP1 + DSA + AMP2)
3. 900MHz measured with application circuit refer to table 11.
4. 1800MHz, 2140MHz, 2650MHz measured with application circuit refer to table 14.
5. 3500MHz, 4650MHz measured with application circuit refer to table 17.
6. 6300MHz, 7200MHz measured with application circuit refer to table 20.
7. Gain data has PCB & Connectors insertion loss de-embedded.
8. OIP3 measured with two tones at an output of 5dBm per tone separated by 1MHz

Table 5. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage	AMP1 / AMP2			5.5	V
	DSA			5.5	V
Supply Current	AMP1 / AMP2			180	mA
	DSA			1000	uA
Digital input voltage	AMP Control Pin (AEN1, AEN2)	-0.3		5.25	V
	DSA Control Pin (LE, DATA, CLK, P/S, A0, A1)	-0.3		3.6	V
Maximum input power	AMP1 / AMP2			15	dBm
	DSA			30	dBm
Storage Temperature		-55		150	℃
Junction Temperature			150		℃

Operation of this device above any of these parameters may result in permanent damage.

Table 6. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	AMP1 + DSA + AMP2	500		8000	MHz
Supply Voltage, VDD	AMP1 & AMP2 VDD	4	5	5.25	V
	DSA VDD	2.7		5.5	V
Current, IDD	AMP1 ON, AMP2 OFF @ VDD=5V		108		mA
	AMP1 ON, AMP2 OFF @ VDD=4V		55		mA
	AMP2 ON, AMP1 OFF @ VDD=5V		108		mA
	AMP2 ON, AMP1 OFF @ VDD=4V		55		mA
	AMP1 + AMP2 ON @ VDD=5V		215		mA
	AMP1 + AMP2 ON @ VDD=4V		110		mA
	AMP1 OFF + AMP2 OFF		5		mA
	DSA		200		uA
AMP Control Voltage [AEN1, AEN2]	AMP ON	0		0.6	V
	AMP OFF	1.17		VDD	V
AEN1 & AEN2 pin Current	AMP OFF		150		uA
DSA Control Voltage	Digital Input High	1.17		3.6	V
	Digital Input Low	-0.3		0.6	V
DSA Control pin Current	Digital Input High			20	uA
Operating Temperature	AMP1 + DSA + AMP2	-40		105	℃

Specifications are not guaranteed over all recommended operating conditions.

Figure 3. Pin Configuration (Top View)

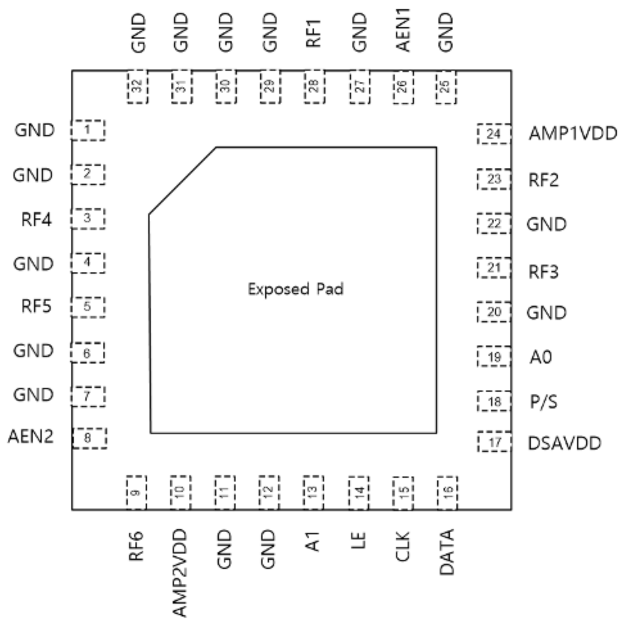


Table 7. Pin Description

Pin	Pin name	Description
3	RF4	DSA output port (Attenuator RF Output) This pin should be connected to RF5(Pin 5) with DC blocking capacitor.
5	RF5	AMP2 RF Input
8	AEN2	AMP2 Enable input. Amplifier is enabled when this pin is set to Low .
9	RF6	AMP2 RF Output This pin is a final RF output port. (AMP + DSA + AMP structure)
10	AMP2VDD	AMP2 DC power supply input
13	A1	Address bit A1 connection.
14	LE	Latch Enable input
15	CLK	Serial interface clock input
16	DATA	Serial interface data input
17	DSAVDD	DSA Power Supply input
18	P/S	Serial Mode Select. This pin have to be set to HIGH.
19	A0	Address bit A0 connection.
21	RF3	DSA input port (Attenuator RF Input)
23	RF2	AMP1 RF Output This pin should be connected to RF3(Pin 21) with DC blocking capacitor.
24	AMP1VDD	AMP1 DC power supply input
26	AEN1	AMP1 Enable input. Amplifier is enabled when this pin is set to Low .
28	RF1	AMP1 input port This pin is a main RF input port. (AMP + DSA + AMP structure)
1, 2, 4, 6, 7, 11, 12, 20, 22, 25, 27, 29, 30, 31, 32	GND	Ground, These pins must be connected to ground

Programming Options

The BVA2762 is programmed to operate only in serial mode.
It operates in serial mode when the P/S pin is High, and when P/S pin is low, the internal DSA is fixed as Max attenuation(31.75dB), so the P/S pin must be set to High to use the serial mode.

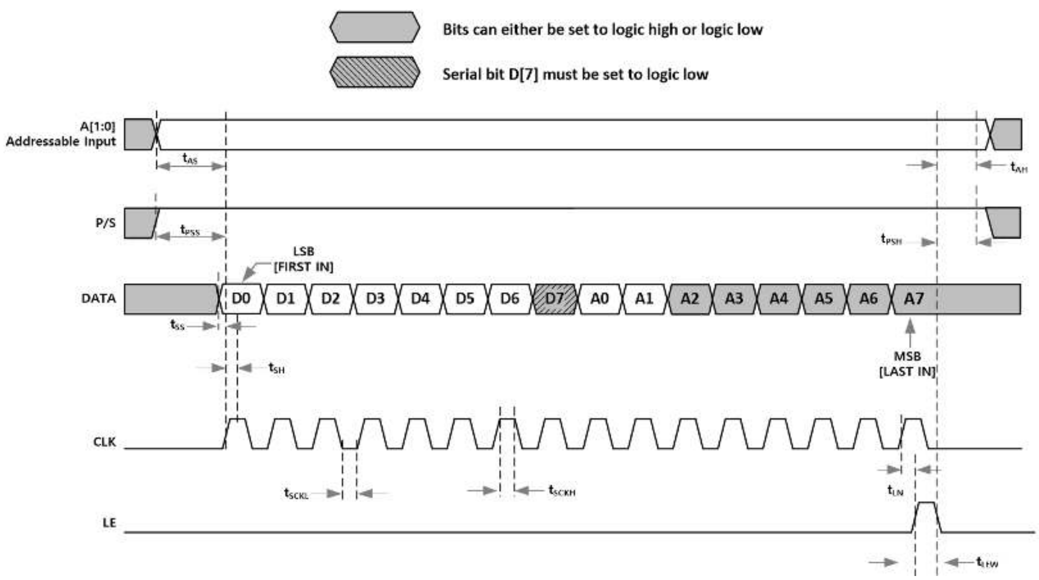
Serial Control Mode

The serial interface is a 7-bit shift register to shift in the data LSB (D0) first. It is controlled by three CMOS-compatible signals: DATA, CLK, and Latch Enable (LE).

Table 8. Truth Table for Serial Control Word

Digital Control Input								Attenuation
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	state (dB)
LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	0
LOW	LOW	LOW	LOW	LOW	LOW	LOW	**HIGH**	0.25
LOW	LOW	LOW	LOW	LOW	LOW	**HIGH**	LOW	0.5
LOW	LOW	LOW	LOW	LOW	**HIGH**	LOW	LOW	1.0
LOW	LOW	LOW	LOW	**HIGH**	LOW	LOW	LOW	2.0
LOW	LOW	LOW	**HIGH**	LOW	LOW	LOW	LOW	4.0
LOW	LOW	**HIGH**	LOW	LOW	LOW	LOW	LOW	8.0
LOW	**HIGH**	LOW	LOW	LOW	LOW	LOW	LOW	16.0
LOW	**HIGH**	**HIGH**	**HIGH**	**HIGH**	**HIGH**	**HIGH**	**HIGH**	31.75

Figure 4. Serial Mode Timing Diagram



The serial interface is a 16-bit shift register made up of two words. The first 8-bit word is the Attenuation word, which controls the DSA state.

The second word is the address word, which uses only 2 of 8-bits that must match the hard wired A0-A1 programming in order to change the DSA state. If no external connections are made to A0–A1 then internally they will default to 00 due to internal pull down resistors.

If these 2 external preset address bits are not matched with the SPI loaded address bits then the current attenuator state will remain unchanged.

This allows up to 4 serial-controlled devices to be used on a single board, which share a common DATA, CLK and LE. **(Figure 5)**

Table 9. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{CLK}	Serial data clock frequency			10	MHz
t_{AS}	Address setup time	100			ns
t_{AH}	Address hold time	100			ns
t_{PSS}	P/S setup time	100			ns
t_{PSH}	P/S hold time	100			ns
t_{SS}	Serial Data setup time	10			ns
t_{SH}	Serial Data hold time	10			ns
t_{SCKH}	Serial clock high time	30			ns
t_{SCKL}	Serial clock low time	30			ns
t_{LN}	LE setup time	10			ns
t_{LEW}	Minimum LE pulse width	30			ns

Figure 5. Multi Device Addressing Scheme using SPI

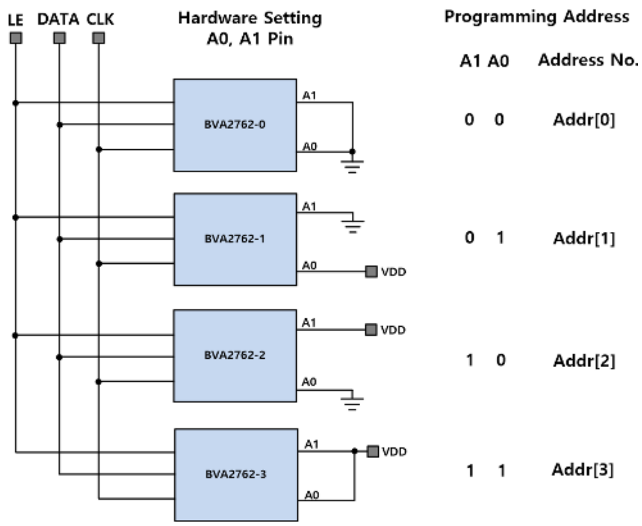


Table 10. Truth Table for Address Control Word

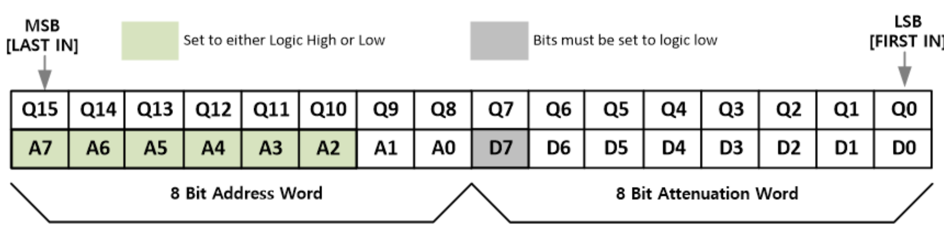
Address Digital Control Input								Address Setting	Addr No.
A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)		
X	X	X	X	X	X	LOW	LOW	00	Addr[0]
X	X	X	X	X	X	LOW	**HIGH**	01	Addr[1]
X	X	X	X	X	X	**HIGH**	LOW	10	Addr[2]
X	X	X	X	X	X	**HIGH**	**HIGH**	11	Addr[3]

Serial Register Map

The BVA2762 can be programmed via the serial control on the rising edge of Latch Enable (LE) which loads the last 8-bits attenuation word and 8-bits address word in the SHIFT Register. Data is clocked in LSB(D0) first.

The shift register must be loaded while LE is kept LOW to prevent changing the attenuation value during data is inputted.

Figure 6. Serial Register Map



The serial register consist of 16 bits as shown in Figure 6. First 8 bits from LSB are Attenuation word, 8 bits after that are Address word.
The Attenuation word is DSA attenuation control bit and the Address word is static logical bit determined by A0 and A1 digital inputs.
The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four because of 0.25dB step up to 31.75dB (total 127 Attenuation state), then convert to binary.

For example, to program attenuation 15.75dB state of Addr[3] BVA2762 :

Attenuation State	Address state
4 x 15.75 = 63	Digital input of A1, A0 pin = 11
63 -> 00111111	A7 - A0 : xxxxxx11

Serial Data Input : xxxxxx1100111111

x	x	x	x	x	x	1	1	0	0	1	1	1	1	1	1
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

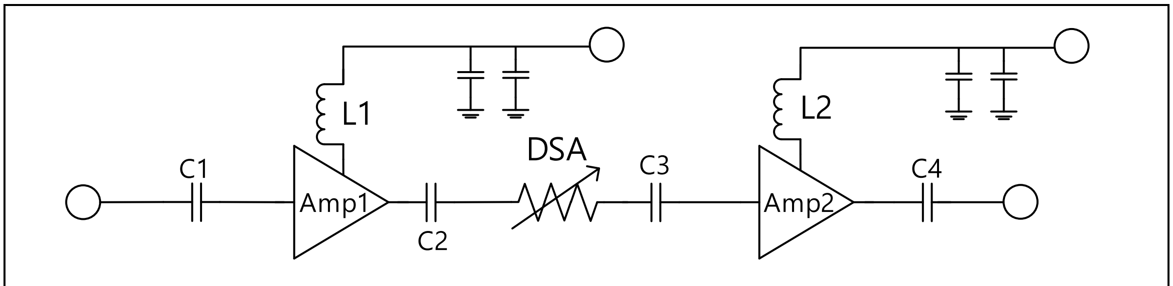
Power-Up state Settings

The BVA2762 will always initialize to the minimum Gain state (Max Attenuation = 31.75dB) on power-up and will remain in this setting until the user latches in the next programming word.

Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit : 500 ~ 1100MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Table 11. 500 ~ 1100MHz RF Application Circuit



BOM	L1	L2	C1	C2	C3	C4						
	56nH	56nH	100pF	100pF	100pF	100pF						

This value can be changed little by little according to the frequency band and bandwidth.

Table 12. Typical IF Performance @ VDD = 5V

Parameter	Frequency			Unit
	500	700	900	MHz
Gain[1]	40.5	41.7	42.0	dB
S11	-12.0	-21.5	-26.4	dB
S22	-11.0	-17.9	-16.4	dB
OIP3[2]@ ATT=0dB	37.5	37.0	36.7	dBm
OIP3[2]@ ATT=15.75dB	37.1	36.9	36.2	dBm
P1dB	18.8	19.8	20.6	dBm
Noise Figure	1.5	1.5	1.5	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 5dBm per tone separated by 1MHz.

Table 13. Typical IF Performance @ VDD = 4V

Parameter	Frequency			Unit
	500	700	900	MHz
Gain[1]	39.3	40.3	40.4	dB
S11	-13.5	-23.4	-21.5	dB
S22	-12.7	-19.9	-18.7	dB
OIP3[2]@ ATT=0dB	31.3	31.8	31.6	dBm
OIP3[2]@ ATT=15.75dB	30.6	30.6	30.1	dBm
P1dB	17.1	18.1	18.8	dBm
Noise Figure	1.5	1.5	1.5	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 5dBm per tone separated by 1MHz.

Figure 7. Gain vs. Frequency @ VDD = 5V
over Temperature

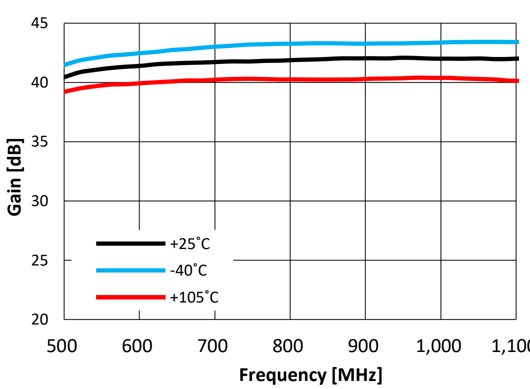
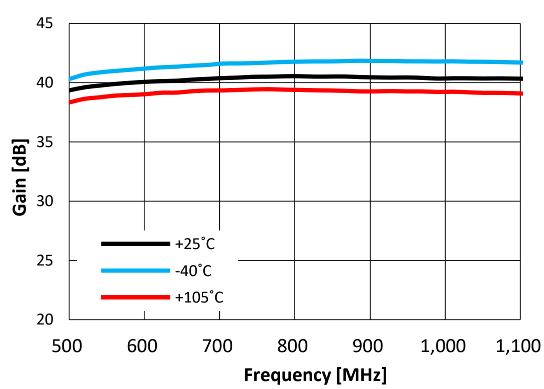


Figure 8. Gain vs. Frequency @ VDD = 4V
over Temperature



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit : 500 ~ 1100MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Figure 9. Gain vs. Frequency
over Major Attenuation States

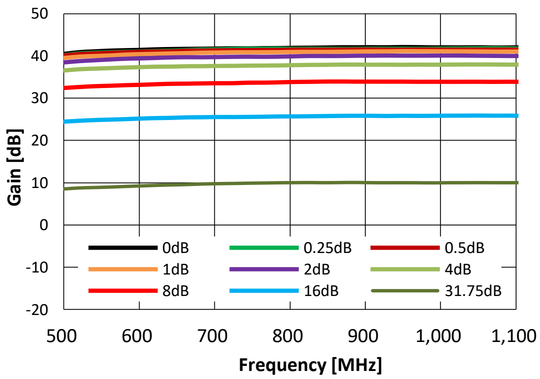


Figure 10. Gain vs. Frequency vs VDD
Max Gain States

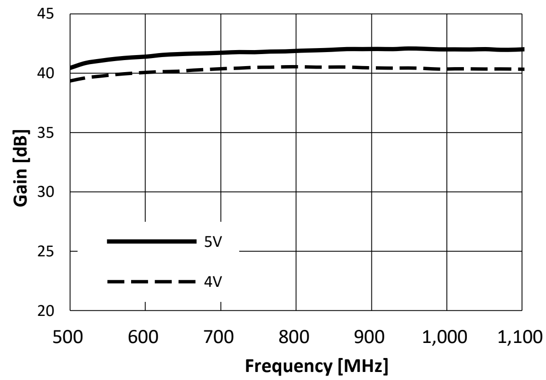


Figure 11. Input Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

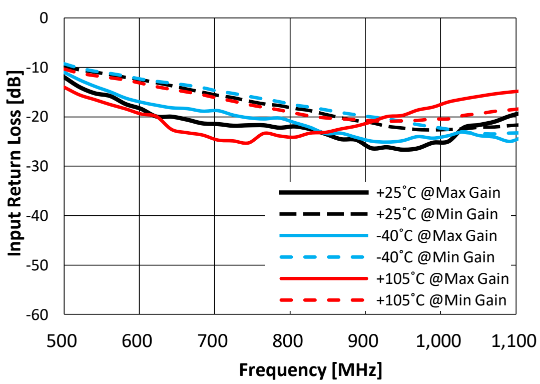
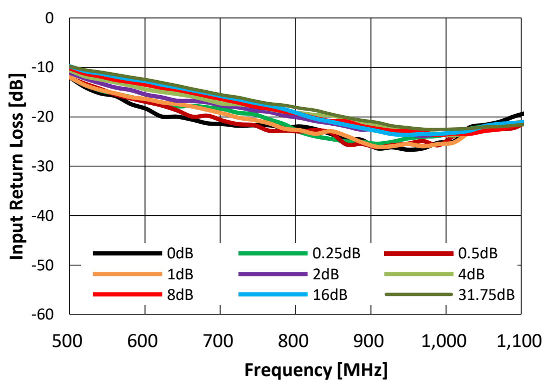


Figure 12. Input Return Loss vs. Frequency
Over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 13. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

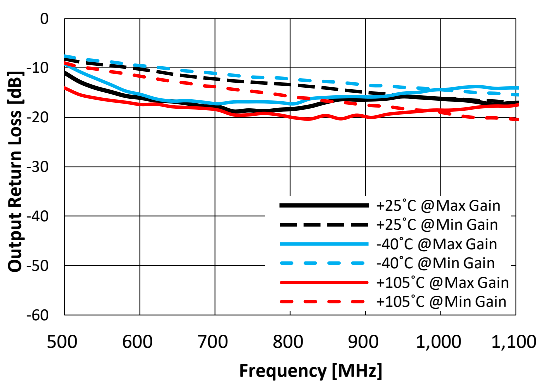
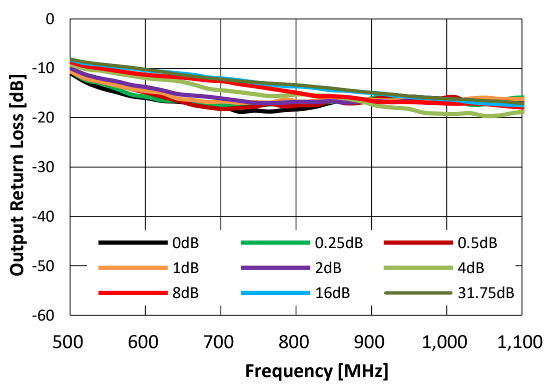


Figure 14. Output Return Loss vs. Frequency
over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit : 500 ~ 1100MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Figure 15. OIP3 vs. Frequency vs. VDD
Over Temperature (Max Gain State)

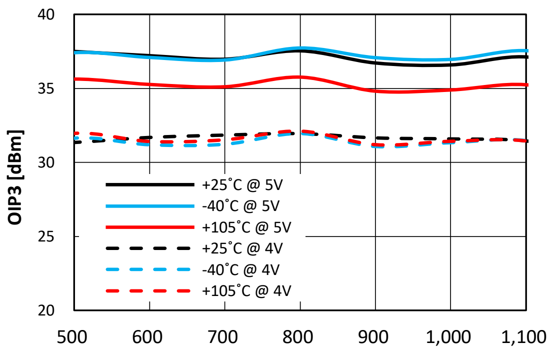


Figure 16. OIP3 vs. Frequency vs VDD
(15.75dB Attenuation State)

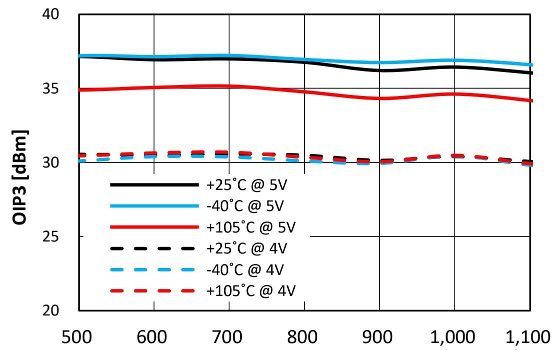


Figure 17. P1dB vs. Frequency vs VDD
Over Temperature (Max Gain State)

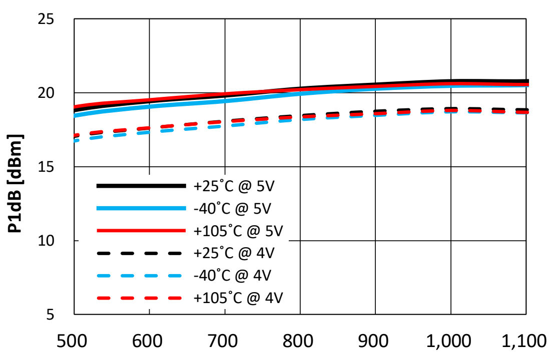


Figure 18. Noise Figure vs. Frequency @ VDD = 5V
Over Temperature (Max Gain State)

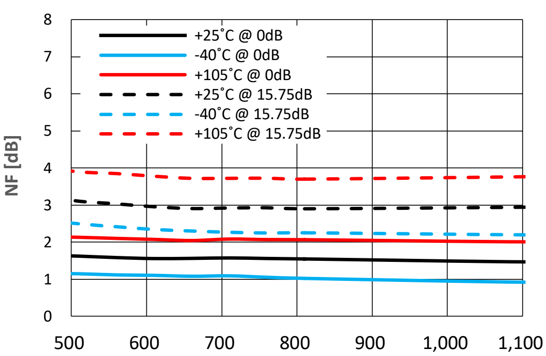
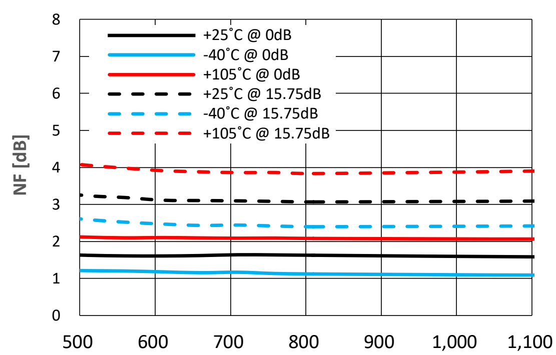


Figure 19. Noise Figure vs. Frequency @ VDD = 4V
Over Temperature (Max Gain State)



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit : 500 ~ 1100MHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 11

Figure 20. Attenuation Error vs Frequency
over Major Attenuation Steps

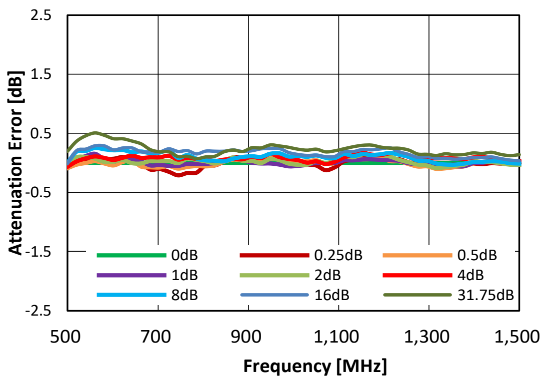


Figure 21. Attenuation Error vs Attenuation Setting
over Major Frequency

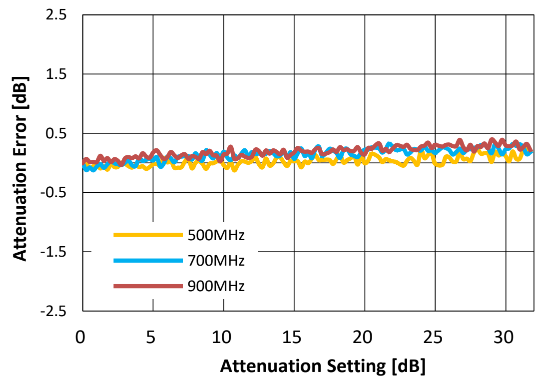


Figure 22. Attenuation Error at 500MHz vs Temperature
Over All Attenuation States

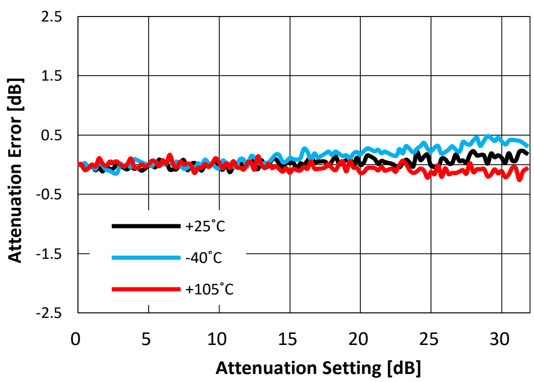


Figure 23. Attenuation Error at 700MHz vs Temperature
Over All Attenuation States

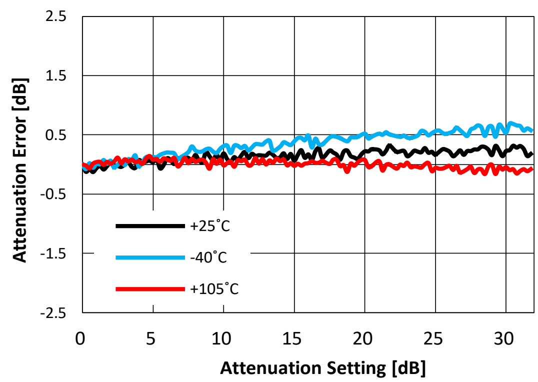
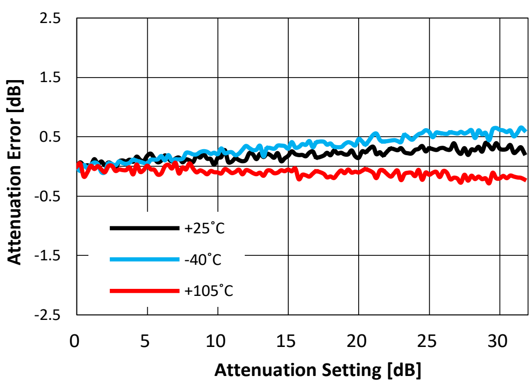


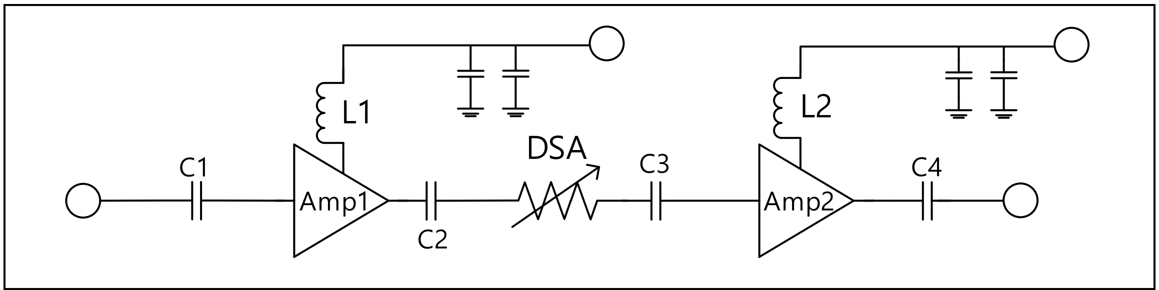
Figure 24. Attenuation Error at 900MHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:1.7~ 2.7GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 14

Table 14. 1.7 ~ 2.7GHz RF Application Circuit



BOM	L1	L2	C1	C2	C3	C4						
	6.2nH	6.2nH	20pF	20pF	20pF	20pF						

This value can be changed little by little according to the frequency band and bandwidth.

Table 15. Typical RF Performance @ VDD = 5V

Parameter	Frequency			Unit
	1800	2140	2650	MHz
Gain[1]	41.6	41.4	41.0	dB
S11	-10.0	-9.5	-13.2	dB
S22	-18.4	-26.6	-28.3	dB
OIP3[2]@ ATT=0dB	36.7	35.1	35.4	dBm
OIP3[2]@ ATT=15.75dB	35.1	34.6	33.8	dBm
P1dB	21.2	21.5	21.8	dBm
Noise Figure	1.5	1.5	1.5	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 5dBm per tone separated by 1MHz.

Table 16. Typical RF Performance @ VDD = 4V

Parameter	Frequency			Unit
	1800	2140	2650	MHz
Gain[1]	40.0	39.7	39.6	dB
S11	-8.0	-7.7	-11.1	dB
S22	-20.0	-19.2	-22.0	dB
OIP3[2]@ ATT=0dB	31.5	30.2	31.4	dBm
OIP3[2]@ ATT=15.75dB	29.9	29.2	28.8	dBm
P1dB	19.2	19.0	19.8	dBm
Noise Figure	1.5	1.5	1.5	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 5dBm per tone separated by 1MHz.

Figure 25. Gain vs. Frequency @ VDD = 5V
over Temperature

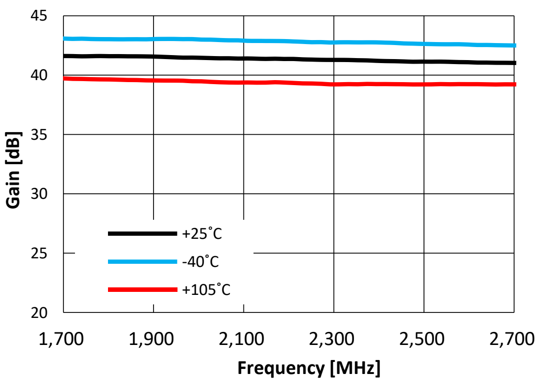
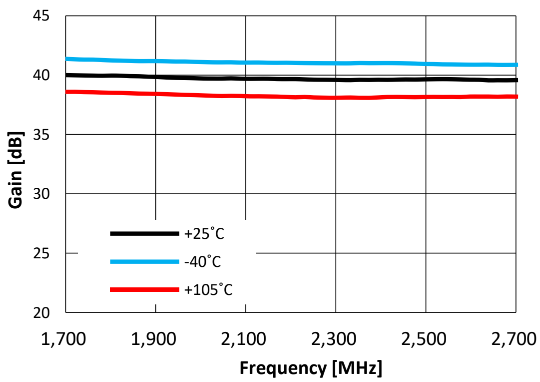


Figure 26. Gain vs. Frequency @ VDD = 4V
over Temperature



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:1.7 ~ 2.7GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 14

Figure 27. Gain vs. Frequency
over Major Attenuation States

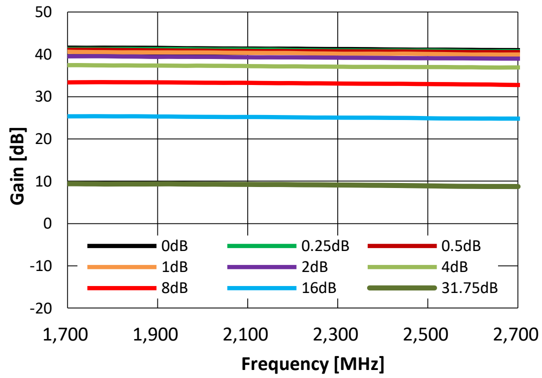


Figure 28. Gain vs. Frequency vs VDD
Max Gain States

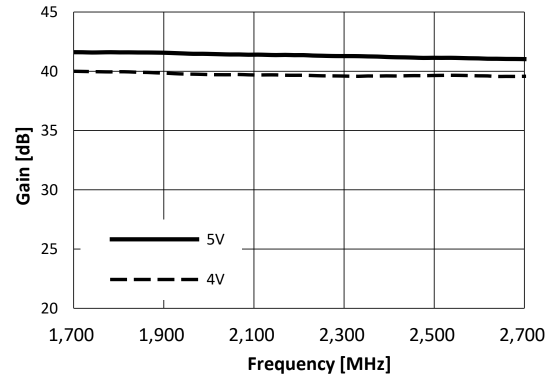


Figure 29. Input Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

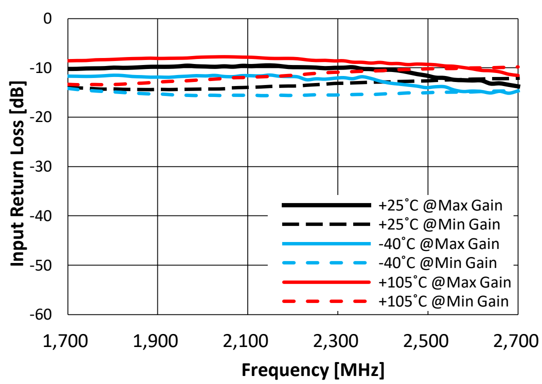
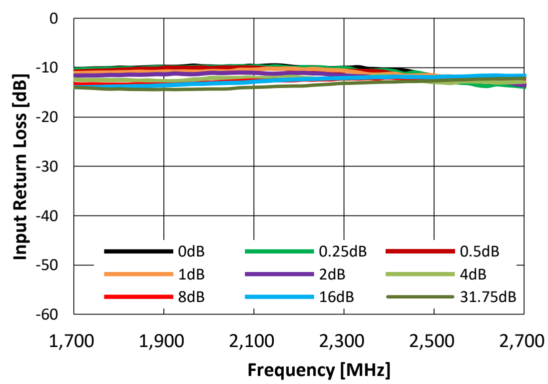


Figure 30. Input Return Loss vs. Frequency
Over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 31. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

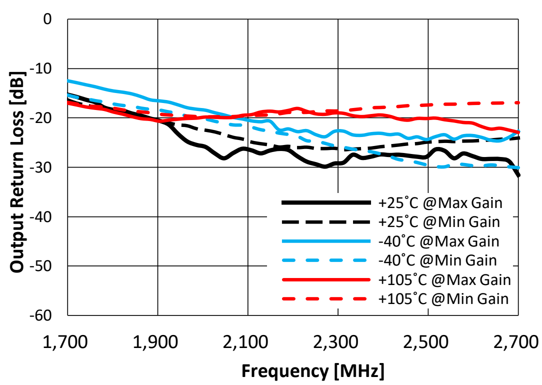
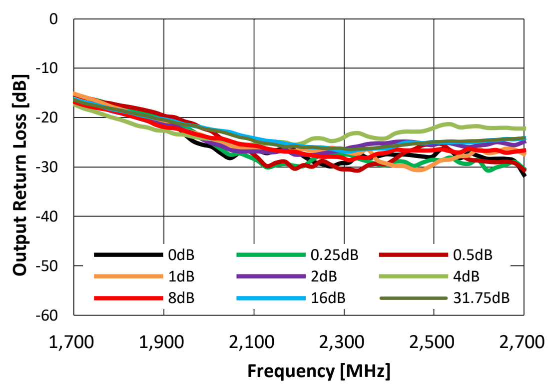


Figure 32. Output Return Loss vs. Frequency
over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:1.7 ~ 2.7GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 14

Figure 33. OIP3 vs. Frequency vs. VDD
Over Temperature (Max Gain State)

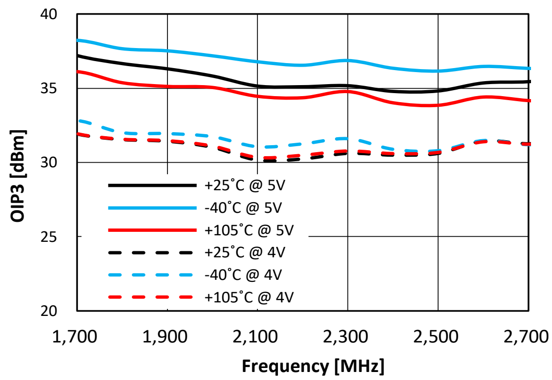


Figure 34. OIP3 vs. Frequency vs. VDD
(15.75dB Attenuation State)

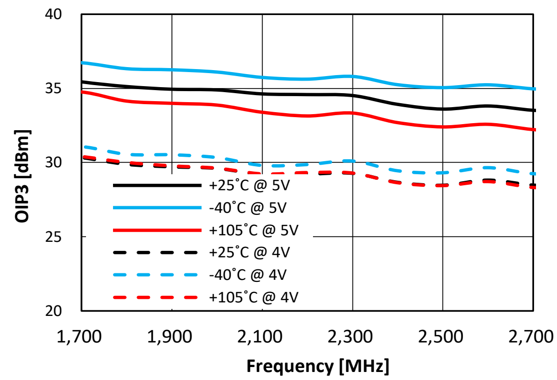


Figure 35. P1dB vs. Frequency vs. VDD
Over Temperature (Max Gain State)

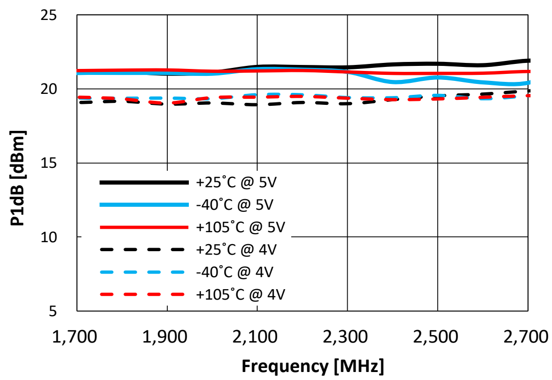


Figure 36. Noise Figure vs. Frequency @ VDD = 5V
Over Temperature

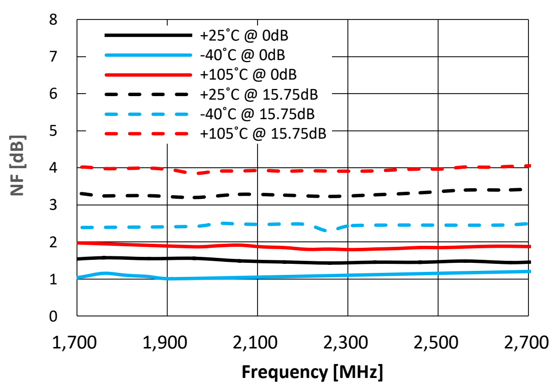
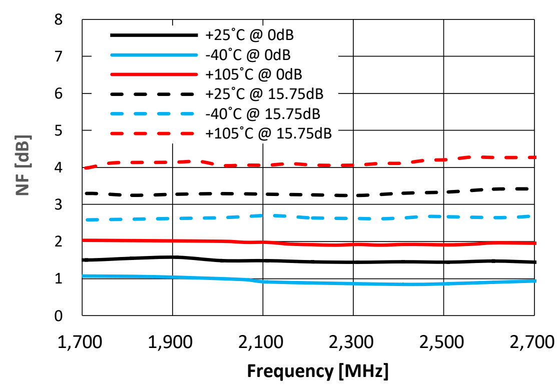


Figure 37. Noise Figure vs. Frequency @ VDD = 4V
Over Temperature



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:1.7 ~ 2.7GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 14

Figure 38. Attenuation Error vs Frequency
over Major Attenuation Steps

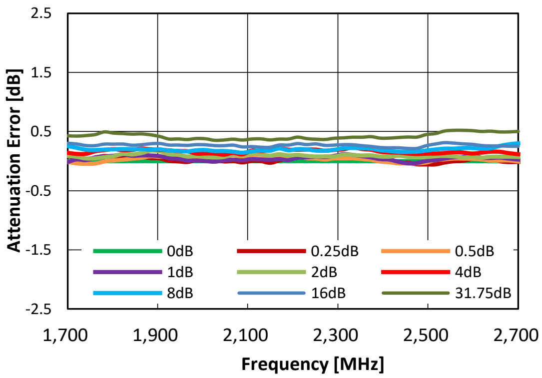


Figure 39. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

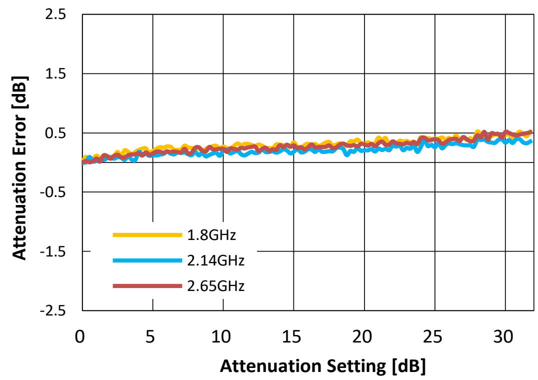


Figure 40. Attenuation Error at 1.8GHz vs Temperature
Over All Attenuation States

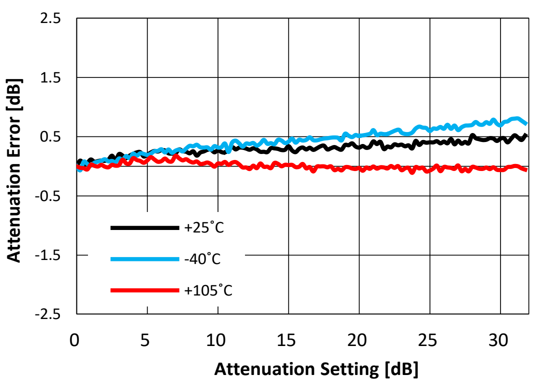


Figure 41. Attenuation Error at 2.14GHz vs Temperature
Over All Attenuation States

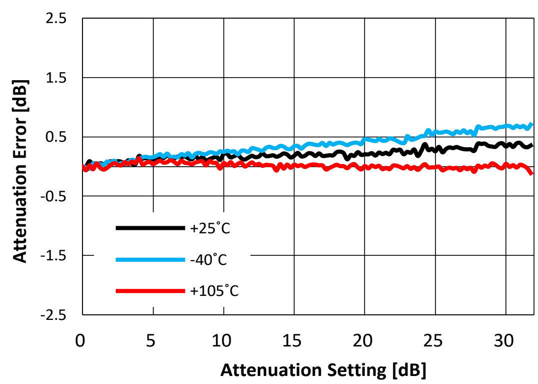
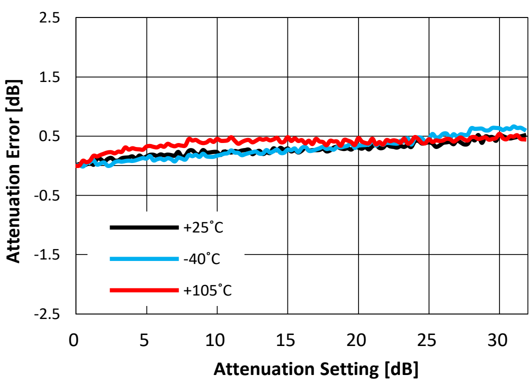


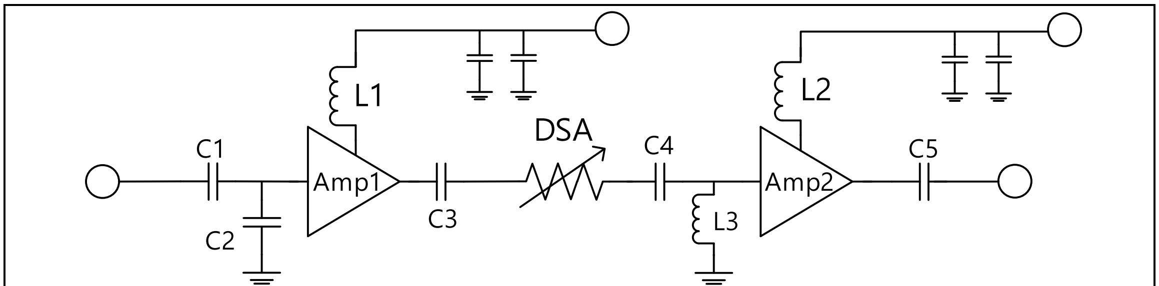
Figure 42. Attenuation Error at 2.65GHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:3 ~ 5GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 17

Table 17. 3 ~ 5GHz RF Application Circuit



BOM	L1	L2	L3	C1	C2	C3	C4	C5				
	1.5nH	3.3nH	2.7nH	10pF	0.2pF	10pF	10pF	10pF				

This value can be changed little by little according to the frequency band and bandwidth.

Table 18. Typical RF Performance @ VDD = 5V

Parameter	Frequency			Unit
	3500	3900	4650	MHz
Gain[1]	40.5	40.5	40.5	dB
S11	-10.1	-13.1	-20.7	dB
S22	-13.5	-12.0	-7.7	dB
OIP3[2]**@ ATT=0dB**	35.6	35.2	36.5	dBm
OIP3[2]**@ ATT=15.75dB**	33.3	32.9	32.8	dBm
P1dB	21.2	20.2	19.0	dBm
Noise Figure	1.8	1.9	2.0	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 5dBm per tone separated by 1MHz.

Table 19. Typical RF Performance @ VDD = 4V

Parameter	Frequency			Unit
	3500	3900	4650	MHz
Gain[1]	39.0	39.1	39.1	dB
S11	-9.8	-11.2	-16.5	dB
S22	-13.0	-13.0	-9.9	dB
OIP3[2]**@ ATT=0dB**	32.8	33.1	34.0	dBm
OIP3[2]**@ ATT=15.75dB**	31.6	31.4	31.6	dBm
P1dB	19.5	19.1	17.6	dBm
Noise Figure	1.8	1.9	2.0	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 5dBm per tone separated by 1MHz.

Figure 43. Gain vs. Frequency @ VDD = 5V
over Temperature

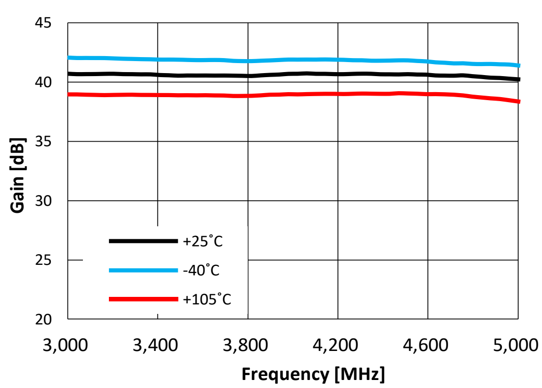
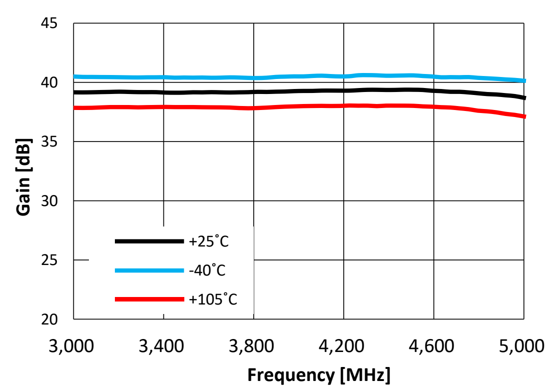


Figure 44. Gain vs. Frequency @ VDD = 4V
over Temperature



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:3 ~ 5GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 17

Figure 45. Gain vs. Frequency
over Major Attenuation States

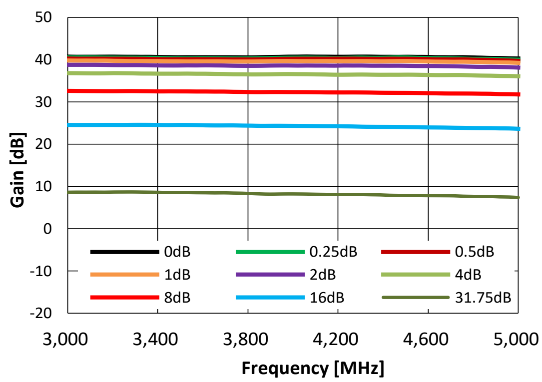


Figure 46. Gain vs. Frequency vs VDD
Max Gain States

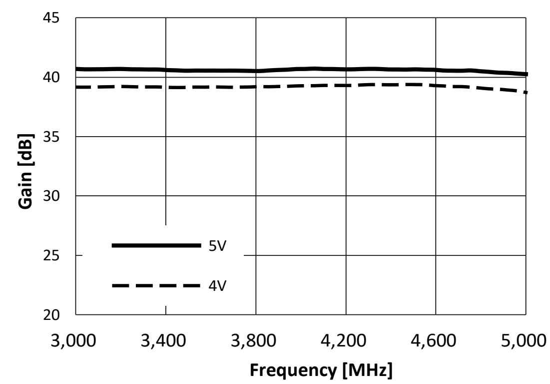
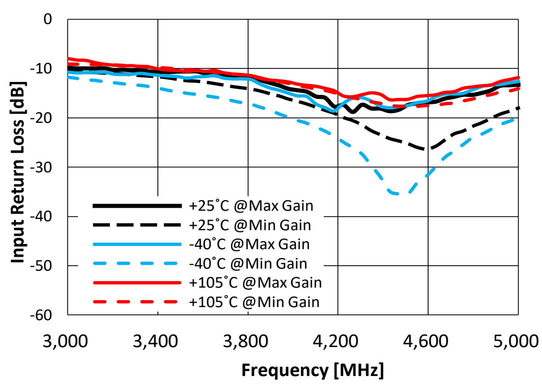


Figure 47. Input Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 48. Input Return Loss vs. Frequency
Over Major Attenuation States

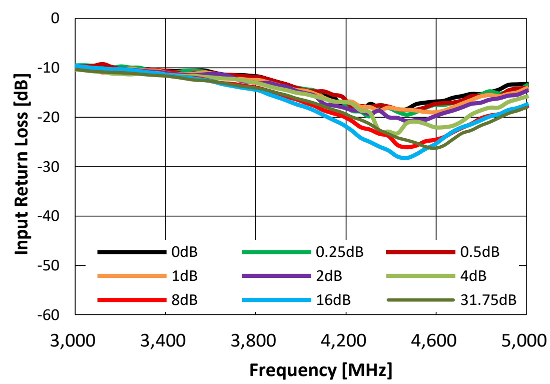
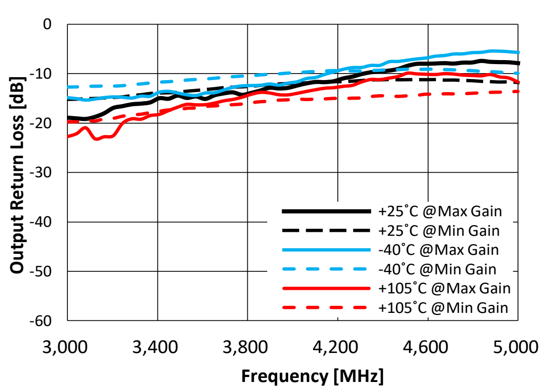
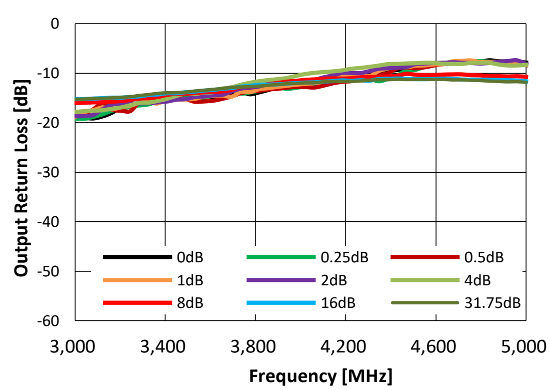


Figure 49. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 50. Output Return Loss vs. Frequency
over Major Attenuation States



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:3 ~ 5GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 17

Figure 51. OIP3 vs. Frequency vs. VDD
Over Temperature (Max Gain State)

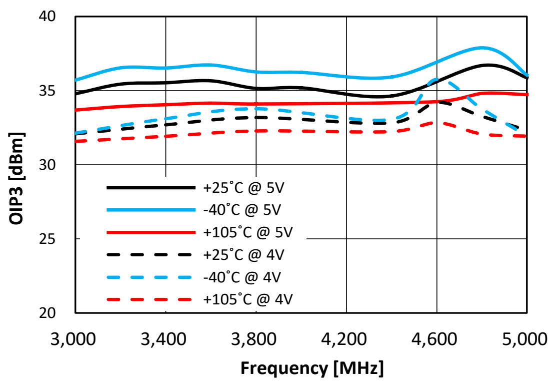


Figure 52. OIP3 vs. Frequency vs. VDD
Over Temperature (15.75dB Attenuation State)

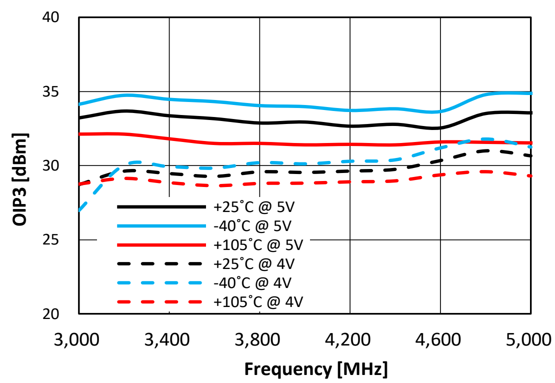


Figure 53. P1dB vs. Frequency vs. VDD
Over Temperature (Max Gain State)

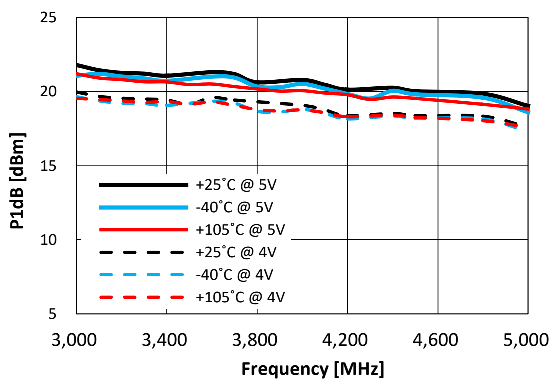


Figure 54. Noise Figure vs. Frequency @ VDD = 5V
Over Temperature

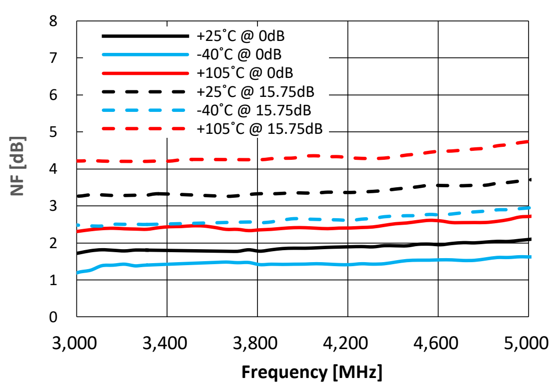
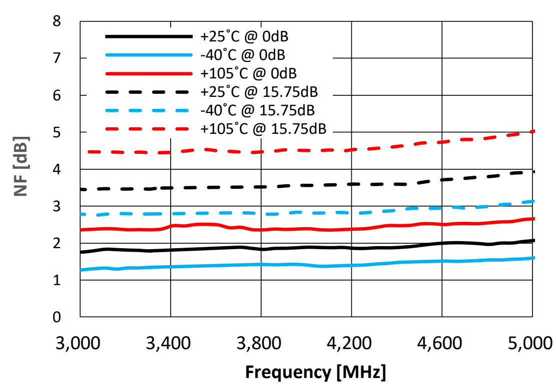


Figure 55. Noise Figure vs. Frequency @ VDD = 4V
Over Temperature



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:3~ 5GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 17

Figure 56. Attenuation Error vs Frequency
over Major Attenuation Steps

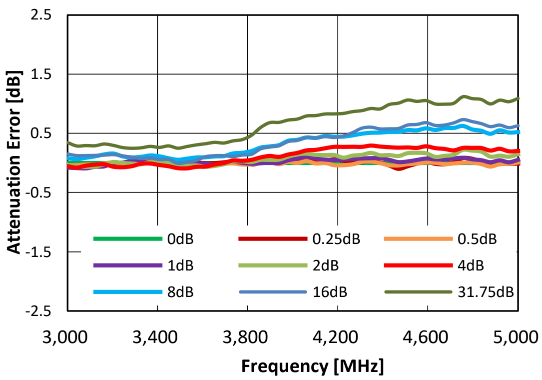


Figure 57. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

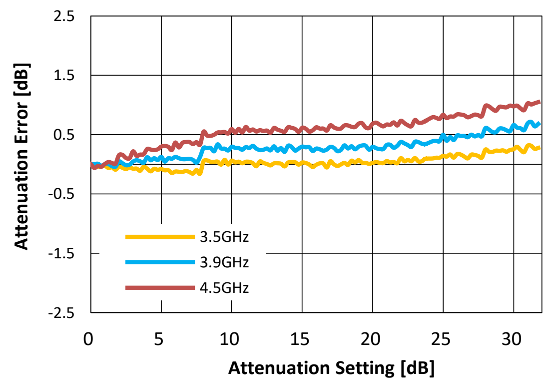


Figure 58. Attenuation Error at 3.5GHz vs Temperature
Over All Attenuation States

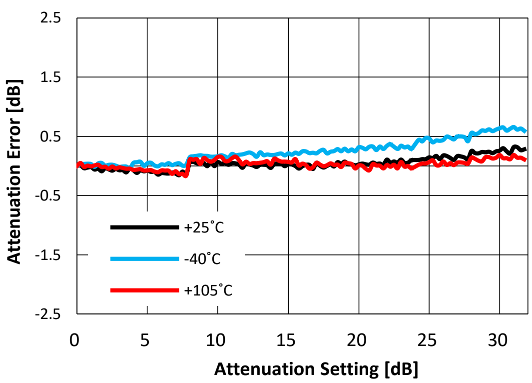


Figure 59. Attenuation Error at 3.9GHz vs Temperature
Over All Attenuation States

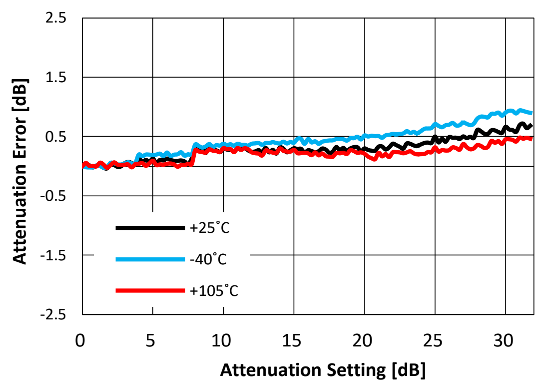
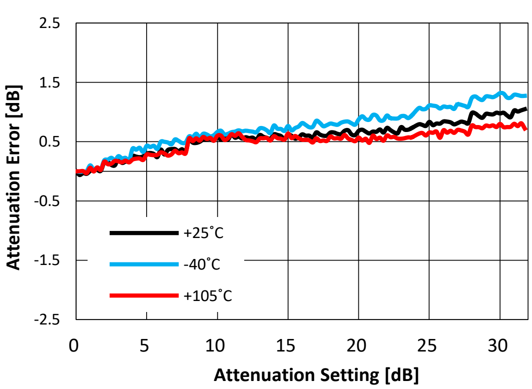


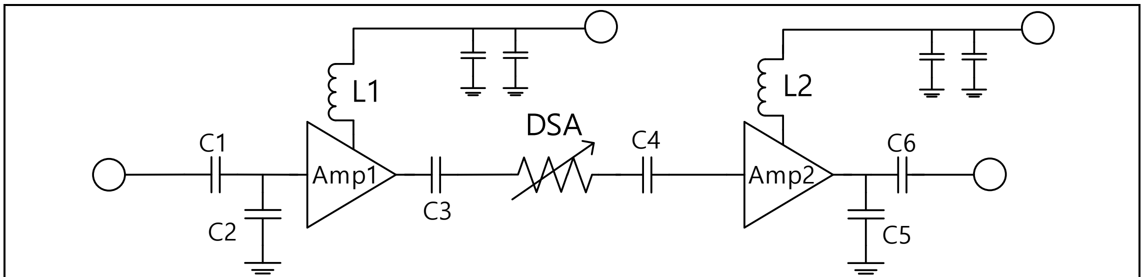
Figure 60. Attenuation Error at 4.65GHz vs Temperature
Over All Attenuation States



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:6 ~ 7.5GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 20

Table 20. 6 ~ 7.5GHz RF Application Circuit



BOM	L1	L2	C1	C2	C3	C4	C5	C6				
	1nH	1nH	10pF	0.3pF	10pF	0.5pF	0.3pF	1pF				

This value can be changed little by little according to the frequency band and bandwidth.
The Capacitor locations(C1, C6) also can be changed according to the frequency band and bandwidth.

Table 21. Typical RF Performance @ VDD = 5V

Parameter	Frequency			Unit
	6300	6800	7200	MHz
Gain[1]	38.5	38.2	38.6	dB
S11	-16.3	-17.2	-15.1	dB
S22	-8.5	-11.7	-11.8	dB
OIP3[2]**@ ATT=0dB**	34.0	33.8	33.6	dBm
OIP3[2]**@ ATT=15.75dB**	31.6	31.7	31.8	dBm
P1dB	18.6	17.5	17.2	dBm
Noise Figure	2.3	2.5	2.8	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 5dBm per tone separated by 1MHz.

Table 22. Typical RF Performance @ VDD = 4V

Parameter	Frequency			Unit
	6300	6800	7200	MHz
Gain[1]	37.1	36.6	36.9	dB
S11	-15.6	-14.4	-11.6	dB
S22	-10.5	-13.6	-13.8	dB
OIP3[2]**@ ATT=0dB**	33.0	32.1	31.8	dBm
OIP3[2]**@ ATT=15.75dB**	30.2	29.4	28.2	dBm
P1dB	17.1	16.1	15.8	dBm
Noise Figure	2.3	2.6	2.9	dB

1. Gain data has PCB & Connectors insertion loss de-embedded
2. OIP3 _ measured with two tones at an output of 5dBm per tone separated by 1MHz.

Figure 61. Gain vs. Frequency @ VDD = 5V
over Temperature

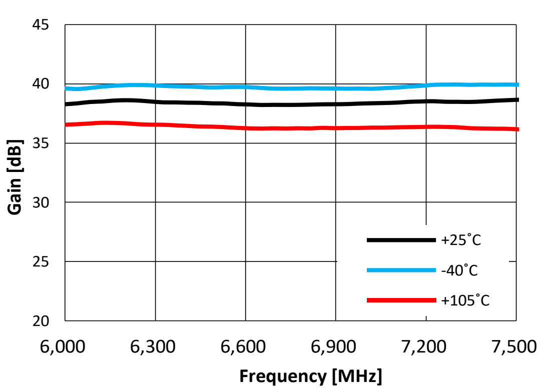
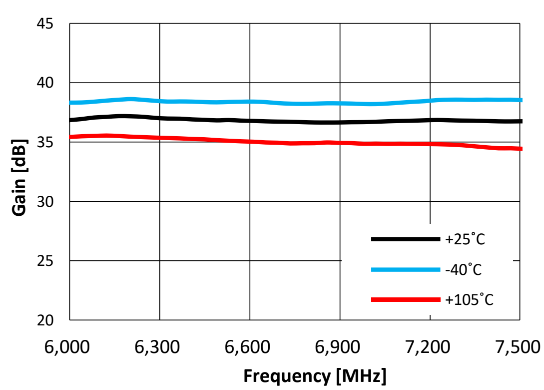


Figure 62. Gain vs. Frequency @ VDD = 4V
over Temperature



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:6 ~ 7.5GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 20

Figure 63. Gain vs. Frequency
over Major Attenuation States

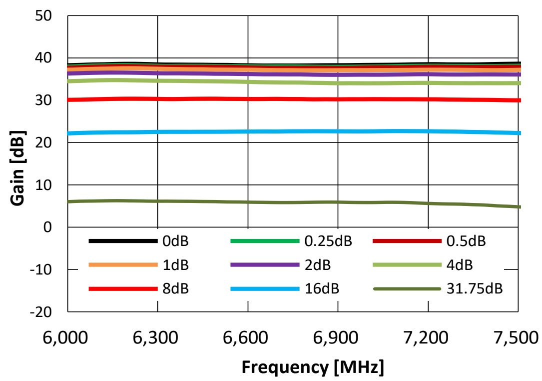


Figure 64. Gain vs. Frequency vs VDD
Max Gain States

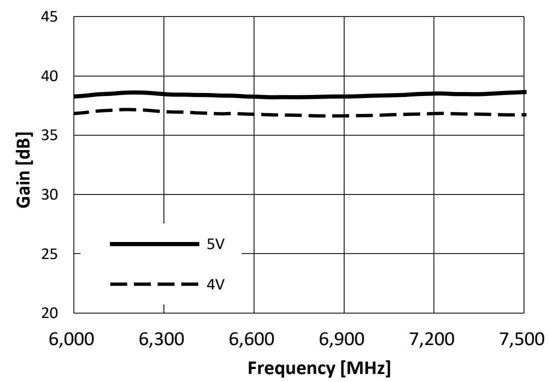


Figure 65. Input Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

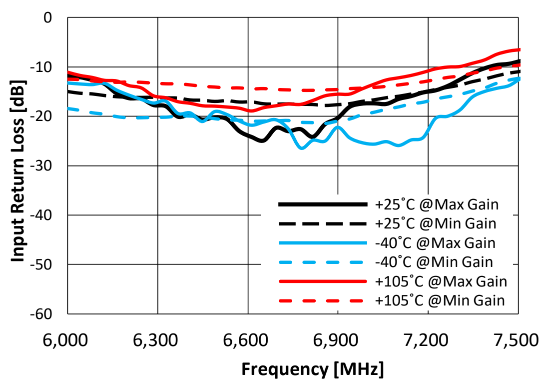
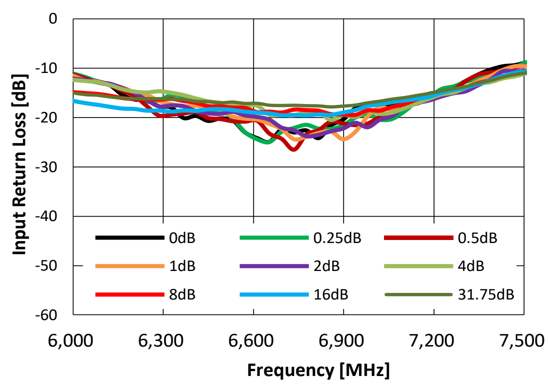


Figure 66. Input Return Loss vs. Frequency
Over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Figure 67. Output Return Loss vs. Frequency
over Temperature (Min[1] / Max Gain State)

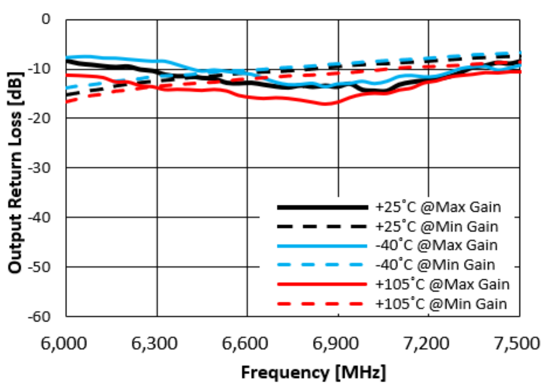
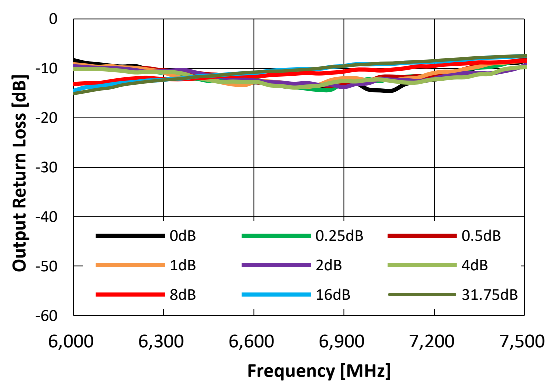


Figure 68. Output Return Loss vs. Frequency
over Major Attenuation States



1.Min Gain was measured in the state is set with attenuation 31.75dB.

Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:6~ 7.5GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 20

Figure 69. OIP3 vs. Frequency vs. VDD
Over Temperature (Max Gain State)

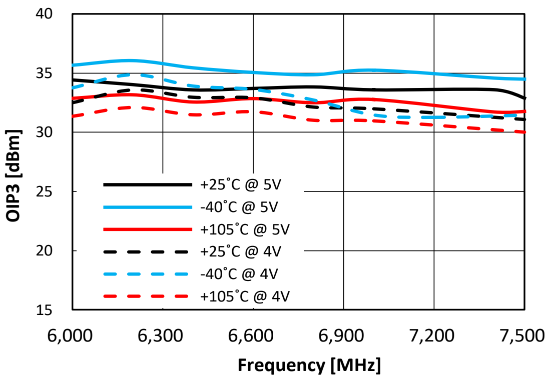


Figure 70. OIP3 vs. Frequency vs. VDD
(15.75dB Attenuation State)

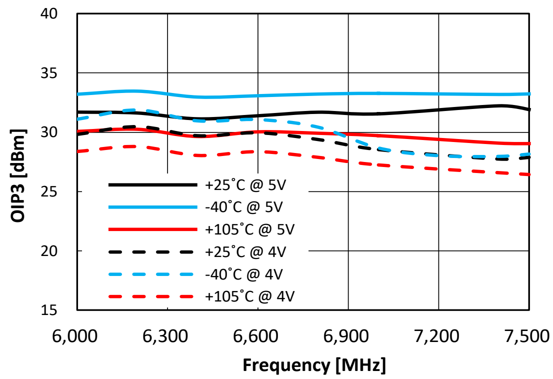


Figure 71. P1dB vs. Frequency vs. VDD
Over Temperature (Max Gain State)

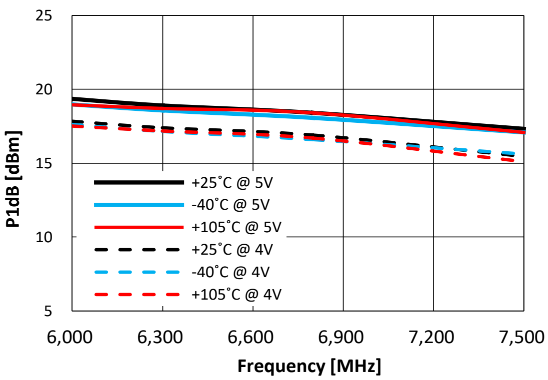


Figure 72. Noise Figure vs. Frequency @ VDD = 5V
Over Temperature

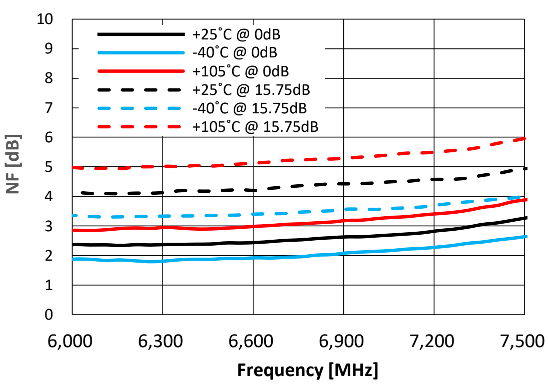
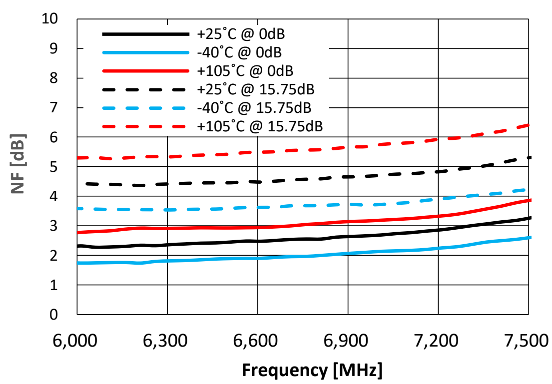


Figure 73. Noise Figure vs. Frequency @ VDD = 4V
Over Temperature



Typical RF Performance Plot - BVA2762 EVK - PCB (Application Circuit:6~ 7.5GHz)

Typical Performance Data @ 25°C and VDD = 5V unless otherwise noted and Application Circuit refer to Table 20

Figure 74. Attenuation Error vs Frequency
over Major Attenuation Steps

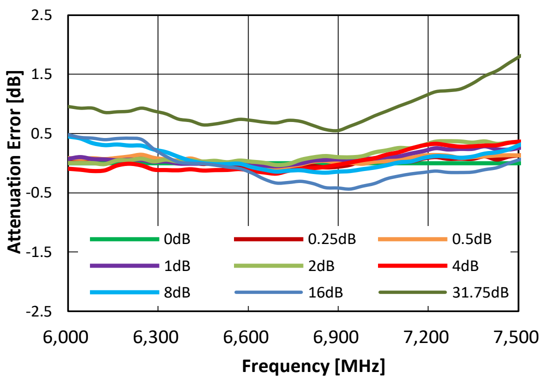


Figure 75. Attenuation Error vs Attenuation Setting
over Major Frequency (Max Gain State)

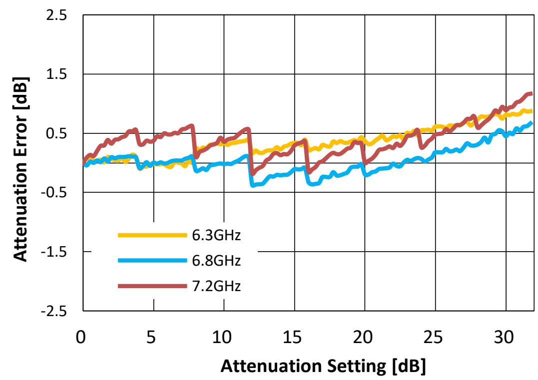


Figure 76. Attenuation Error at 6.3GHz vs Temperature
Over All Attenuation States

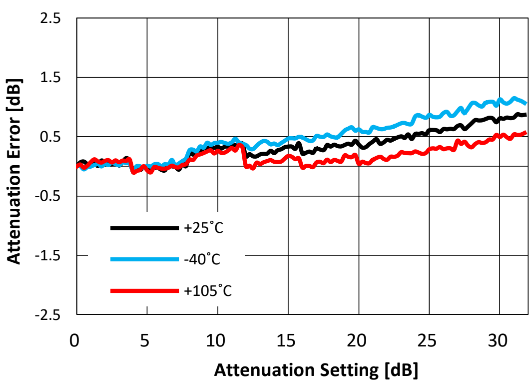


Figure 77. Attenuation Error at 6.8GHz vs Temperature
Over All Attenuation States

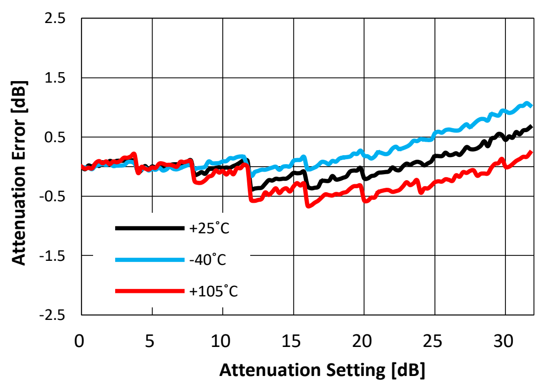


Figure 78. Attenuation Error at 7.2GHz vs Temperature
Over All Attenuation States

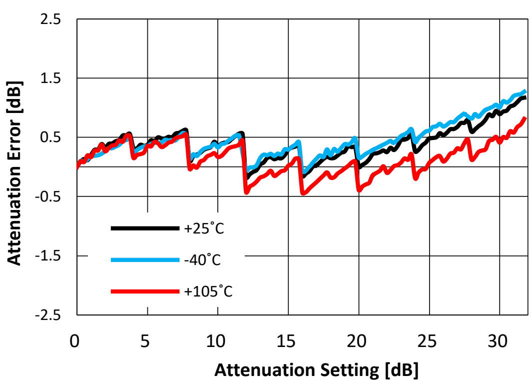


Figure 79. Evaluation Board Schematic

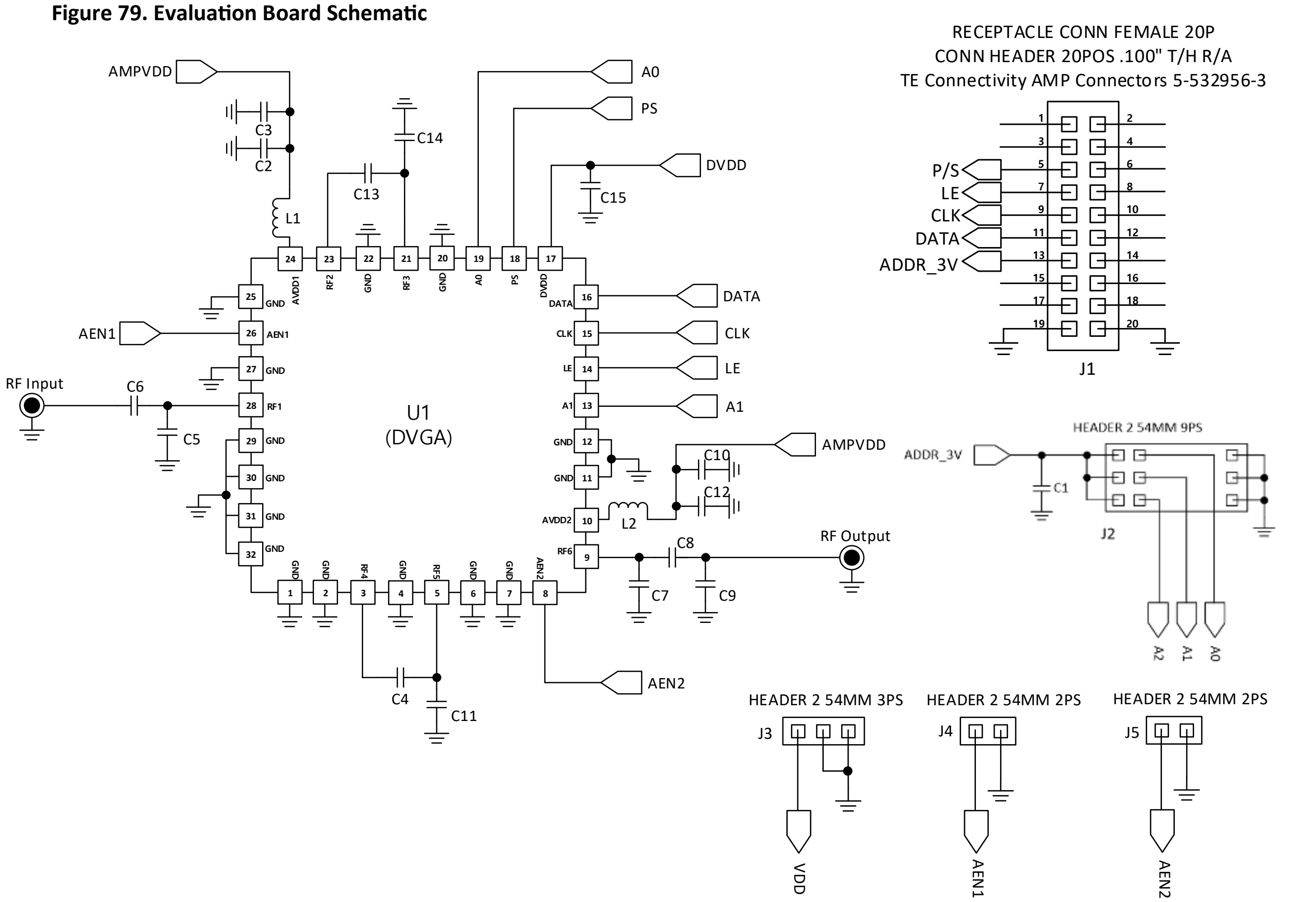
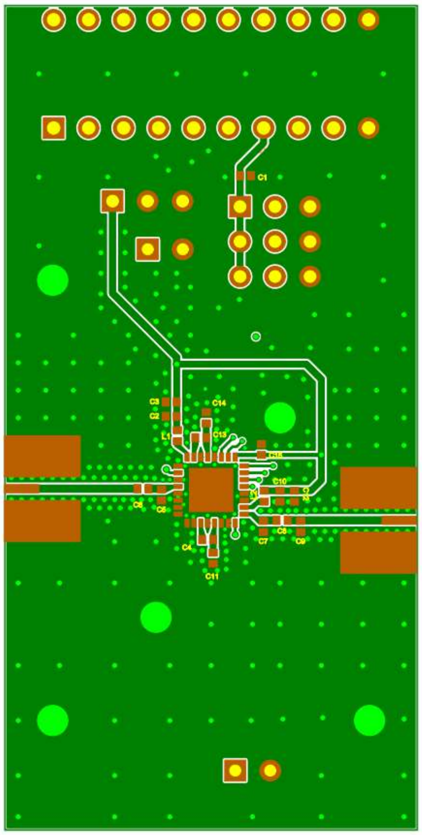


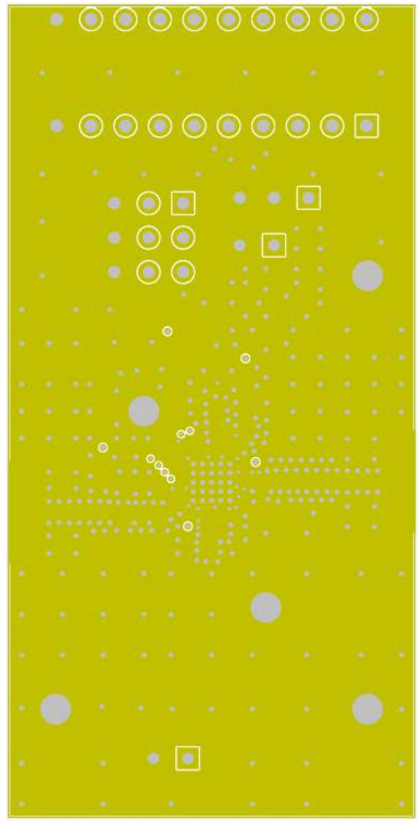
Table 23. Application Circuit

Application Circuit Values Example					
Frequency band		500MHz ~ 1.1GHz	1.7GHz ~ 2.7GHz	3GHz ~ 5GHz	6GHz ~ 7.5GHz
AMP1 Matching	L1	**56nH**	**6.2nH**	**1.5nH**	**1nH**
	C5	NC	NC	**0.2pF**	**0.3pF**
	C6	**100pF**	**20pF**	**10pF**	**10pF**
	C13	**100pF**	**20pF**	**10pF**	**10pF**
	C14	NC	NC	NC	NC
AMP2 Matching	L2	**56nH**	**6.2nH**	**3.3nH**	**1nH**
	C7	NC	NC	NC	**0.3pF**
	C8	**100pF**	**20pF**	**10pF**	**1pF**
	C9	NC	NC	NC	NC
	C4	**100pF**	**20pF**	**10pF**	**0.5pF**
	C11	NC	NC	**2.7nH**	NC

Figure 80. Evaluation Board PCB



[Top view]



[Bottom view]

Table 24. Bill of Material - Evaluation Board

No.	Part Number	Qty	Description	REMARK
1	L1, L2	2	Inductor 0402	Refer to Table 23
2	C1, C3, C12, C15	4	Capacitor 0402 100nF	
3	C2, C10	2	Capacitor 0402 100pF	
4	C4, C5, C6, C7, C8, C9, C11, C13, C14	9	Capacitor 0402	Refer to Table 23
5	J1	1	20pin Receptacle connector	2.54mm, female
6	J2	1	3pin Header	2.54mm, male
7	J3	1	3pin x 3 Header array	2.54mm, male
8	J4, J5	2	2pin Header	2.54mm, male
9	J6, J7	2	SMA_END_LAUNCH	RF SMA Connector

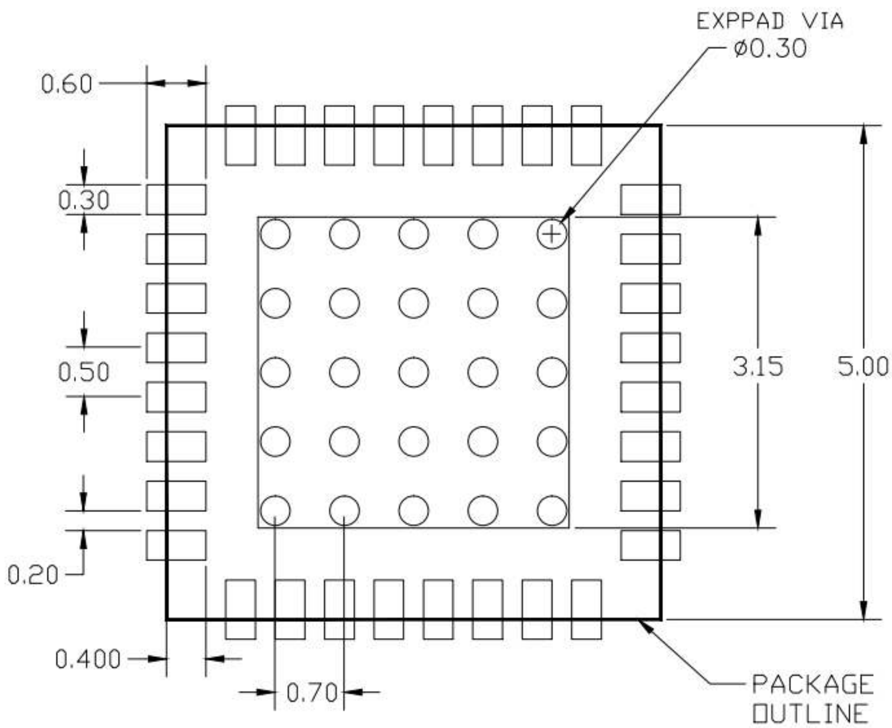


Figure 81. Suggested PCB Land Pattern and PAD Layout

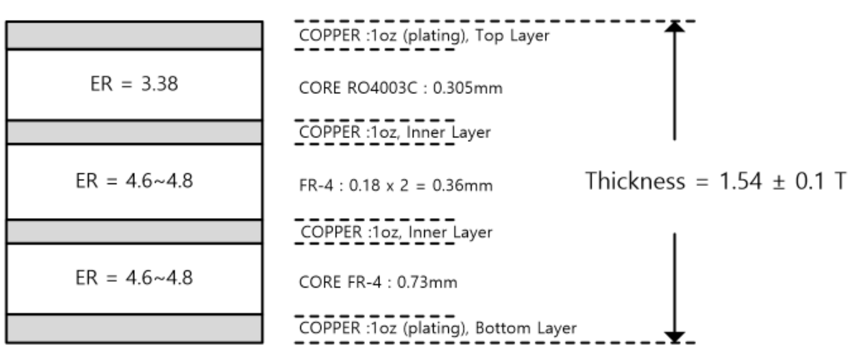
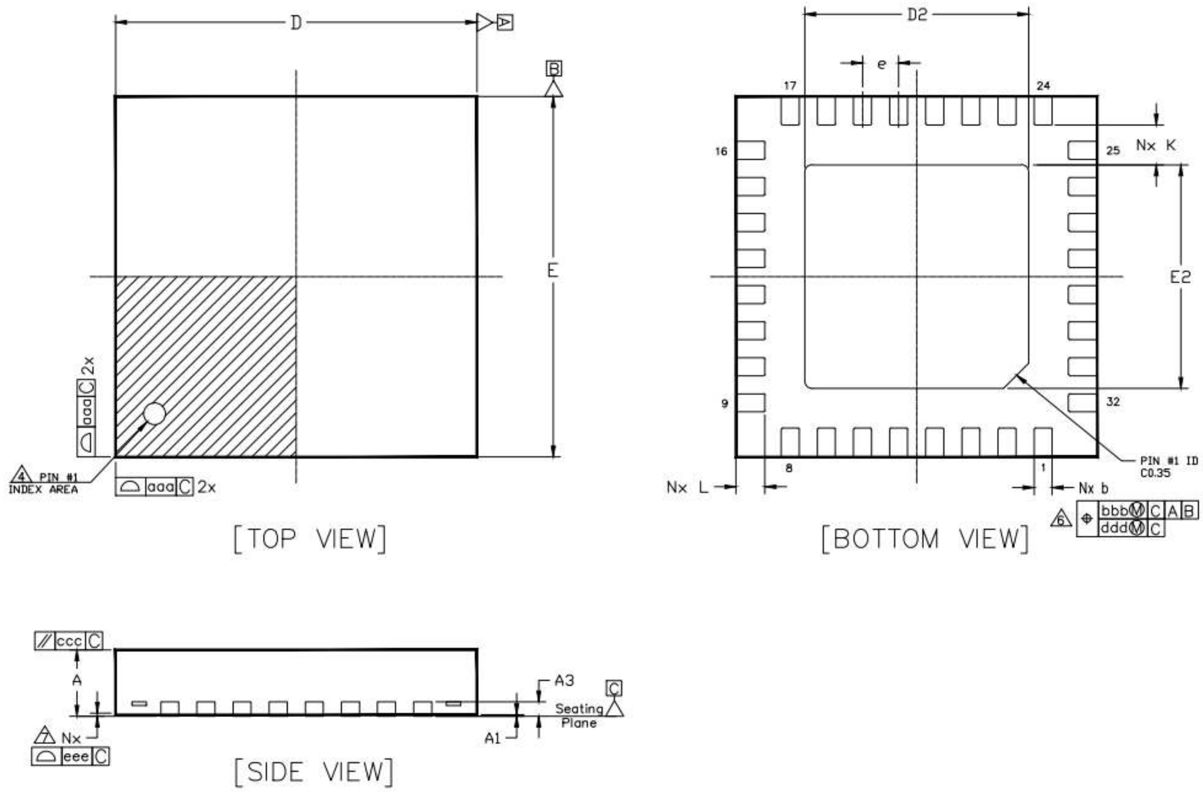


Figure 82. Evaluation Board PCB Layer Information

Figure 83. Package Outline Dimension

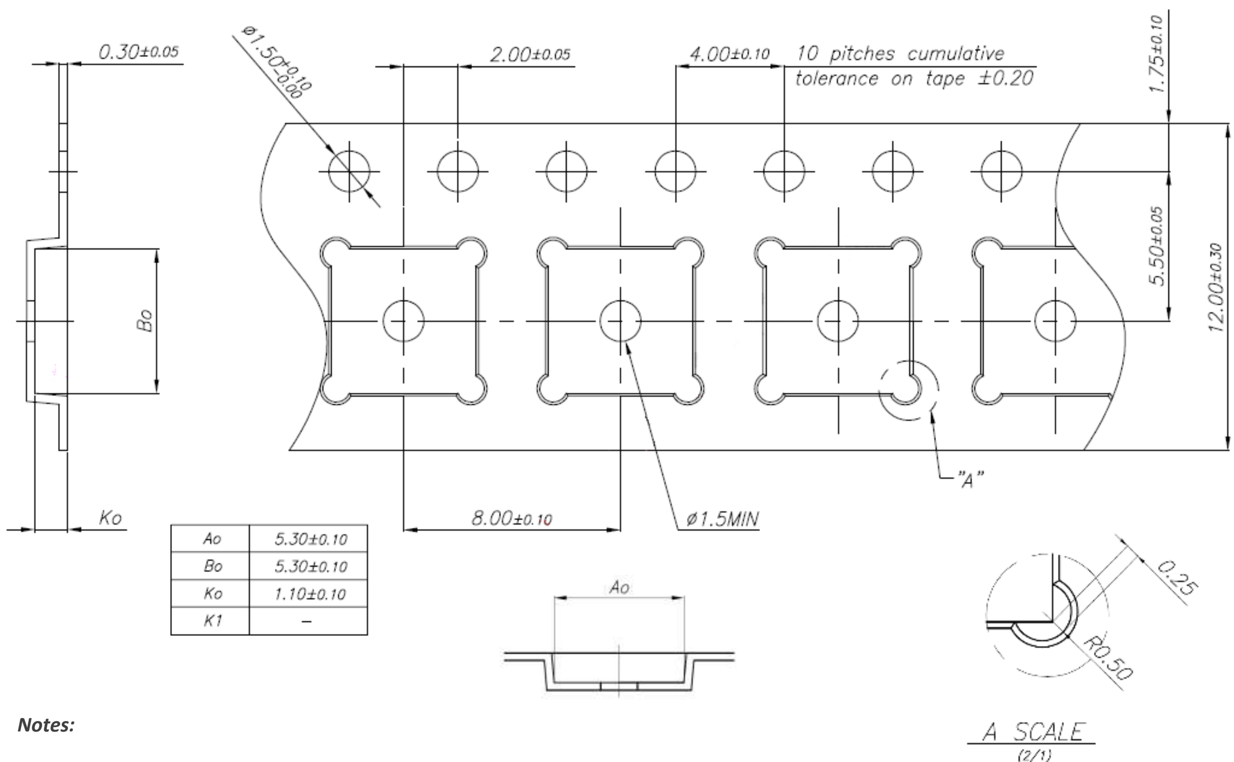


NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5–2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals each D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.3mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

Dimension Table (Notes 1,2)				
Symbol Thickness	Min	Nominal	Max	Note
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref.	---	
b	0.15	0.25	0.30	6
D		5.00 BSC		
E		5.00 BSC		
e		0.50 BSC		
D2	3.05	3.10	3.15	
E2	3.05	3.10	3.15	
K	0.2	---	---	
L	0.30	0.40	0.50	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		32		3
ND		8		5
NE		8		5

Figure 84. Tape & Reel



Ao	5.30±0.10
Bo	5.30±0.10
Ko	1.10±0.10
K1	–

Notes:

1. ***10 sprocket hole pitch cumulative tolerance 0.2/-0.2***
2. ***Camber not to exceed 1mm in 250mm.***
3. ***Material : Black conductive Polystyrene.***
4. ***Ao and Bo measured on a plane 0.3mm above the bottom of the pocket***
5. ***Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.***
6. ***Pocket center position relative to sprocket hole center measured as true position center of pocket, not pocket hole center.***
7. ***Pocket center and pocket hole center must be same position.***

Packaging information:	
Tape Width	12mm
Reel Size	7"
Device Cavity Pitch	8mm
Devices Per Reel	1K

Figure 85. Package Marking

Marking information:	
BVA2762	Device Name
YY	Year
WW	Work Week
XX	Wafer Run Number

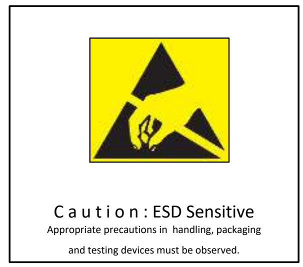
Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating:	Class 1C
Value:	±1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JS-001-2017
MSL Rating:	**Level 1 at +260°C convection reflow**
Standard:	JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

2	**N**	**9**	**6**	**F**