

### FEATURES

- White LED driver based on inductive boost converter
- Integrated 40 V MOSFET with 1.5 A peak current limit
- Input voltage range: 6 V to 21 V
- Maximum output adjustable up to 36 V
- 600 kHz to 1 MHz adjustable operating frequency
- Typical 39 V fixed overvoltage protection (OVP)
- Built-in soft start for boost converter
- Drives up to 4 LED current strings
- LED current adjustable up to 25 mA for each channel
- Headroom control to maximize efficiency
- Fixed LED dimming frequency: 8 kHz
- LED open fault protection
- Brightness control with PWM input
- Dimming controls
  - 4-channel operation: 90 degree phase shift between channels
  - 3-channel operation: 120 degree phase shift between channels
- General
  - Thermal shutdown
  - Undervoltage lockout
  - 14-lead, 4 mm × 3 mm LFCSP

### APPLICATIONS

Notebook PCs, UMPCs, and monitor displays

### GENERAL DESCRIPTION

The **ADD5207** is a white LED driver for backlight applications based on high efficiency, current mode, step-up converter technology. It is designed with a 0.15 Ω, 1.5 A internal switch and a pin-adjustable operating frequency between 600 kHz and 1 MHz.

The **ADD5207** contains four regulated current sources for uniform LED brightness. Each current source can drive up to 25 mA and the LED-driving current is pin adjustable by an external resistor. The **ADD5207** drives up to four parallel strings of multiple series-connected LEDs with a ±1.5% current matching between strings.

The **ADD5207** provides phase shift PWM brightness control methods. LED dimming control is achieved through the PWM input. The device includes an 8 kHz LED-dimming oscillator for driving each current source. The **ADD5207** operates over an input voltage range of 6 V to 21 V, but the device can function with a voltage as low as 5.6 V.

The **ADD5207** also has multiple safety protection features to prevent damage during fault conditions. If any LED is open, the device automatically disables the faulty current source. The internal soft start circuit prevents a high inrush current during startup. Thermal shutdown protection prevents thermal damage.

The **ADD5207** is available in a low profile, thermally enhanced, 4 mm × 3 mm × 0.75 mm, 14-lead, RoHS-compliant lead frame chip scale package (LFCSP) and is specified over the industrial temperature range of -25°C to +85°C.

### TYPICAL APPLICATION CIRCUIT

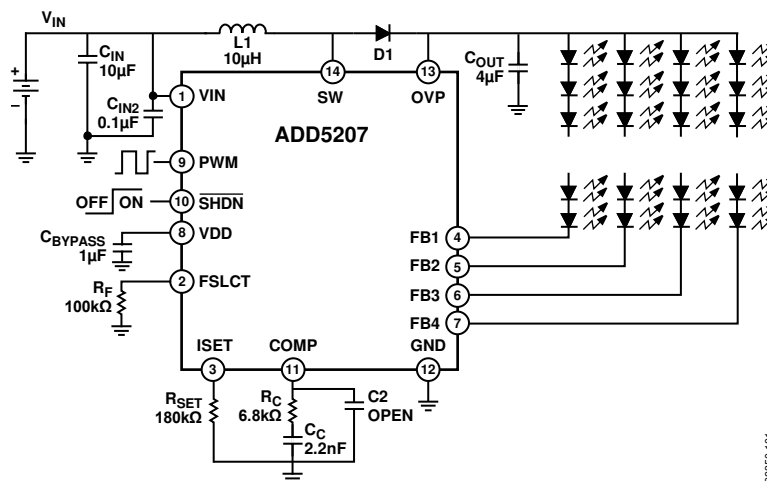


Figure 1.

### Rev. A

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## TABLE OF CONTENTS

Features .....	1	Typical Performance Characteristics .....	9
Applications.....	1	Theory of Operation .....	11
General Description .....	1	Current Mode, Step-Up Switching Regulator Operation .....	11
Typical Application Circuit .....	1	Internal 3.3 V Regulator .....	11
Revision History .....	2	Boost Converter Switching Frequency.....	11
Functional Block Diagram .....	3	Dimming Frequency ( $f_{PWM}$ ) .....	11
Specifications.....	4	Current Source.....	11
Step-Up Switching Regulator Specifications.....	4	PWM Dimming Mode .....	11
LED Current Regulation Specifications .....	5	Safety Features .....	11
General Specifications .....	6	External Component Selection Guide.....	12
Absolute Maximum Ratings.....	7	Layout Guidelines.....	13
Thermal Resistance .....	7	Typical Application Circuits .....	15
ESD Caution.....	7	Outline Dimensions .....	16
Pin Configuration and Function Descriptions.....	8	Ordering Guide .....	16

## REVISION HISTORY

### 2/12—Rev. Sp0 to Rev. A

Replaced Block Diagram with Typical Application Circuit.....	1
Changes to Features Section and General Description Section .	1
Changes to Current Mode, Step-Up Switching Regulator Operation Section, Boost Converter Switching Frequency Section, PWM Dimming Mode Section, Phase Shift PWM Dimming Section, and Safety Features Section.....	11

Changes to Overvoltage Protection (OVP) Section .....	11
Changes to Open-Loop Protection (OLP) Section, Undervoltage Lockout (UVLO) Section, and Thermal Protection Section .....	12
Changes to Layout Guidelines Section .....	13

### 7/09—Revision Sp0: Initial Version

# FUNCTIONAL BLOCK DIAGRAM

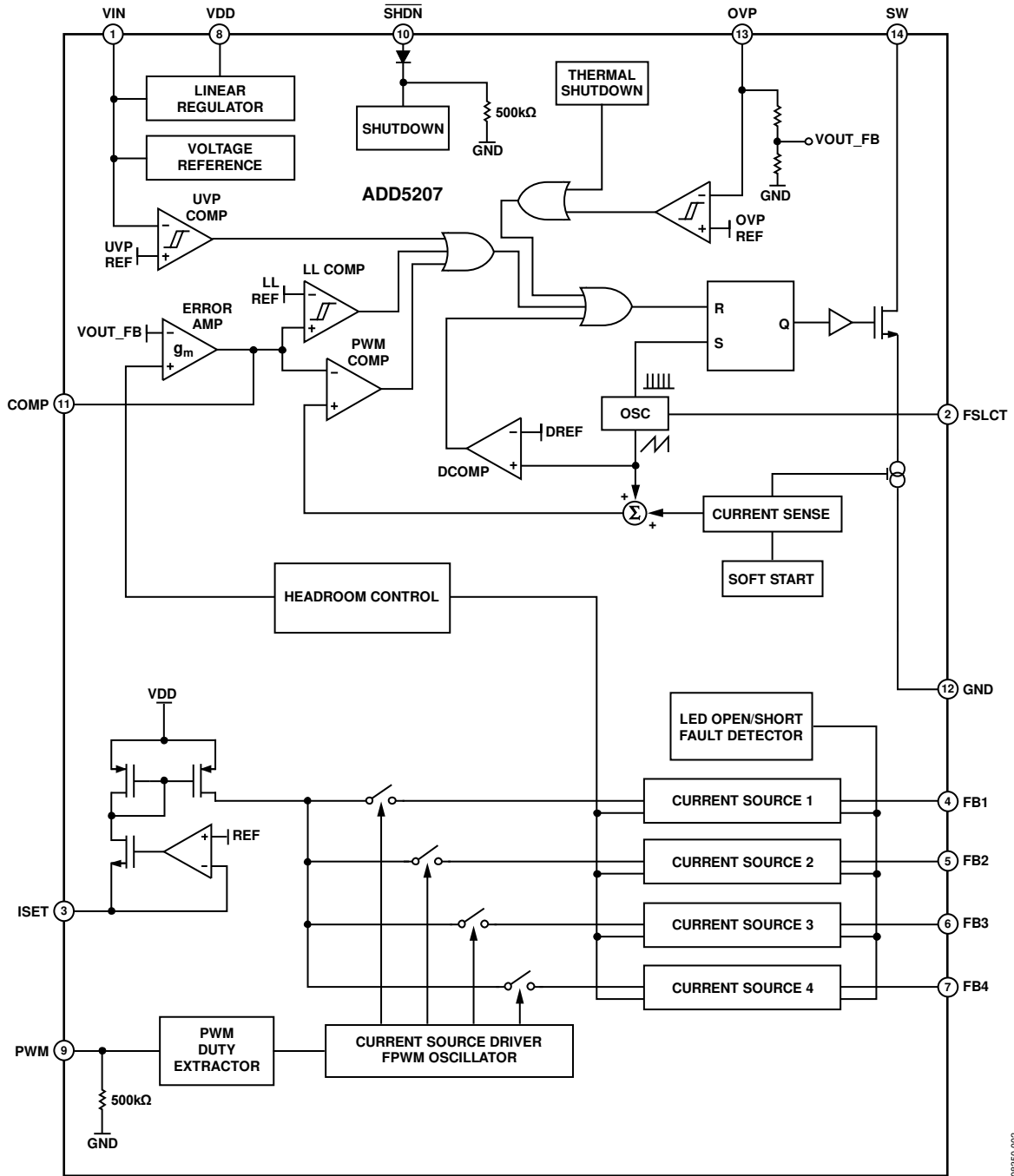


Figure 2. Functional Block Diagram

08350-002

## SPECIFICATIONS

### STEP-UP SWITCHING REGULATOR SPECIFICATIONS

$V_{IN} = 12\text{ V}$ ,  $\overline{\text{SHDN}} = \text{high}$ ,  $T_A = -25^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Input Voltage Range	$V_{IN}$		6		21	V
BOOST OUTPUT						
Output Voltage	$V_{OUT}$				36	V
SWITCH						
On Resistance	$R_{DS(ON)}$	$V_{IN} = 12\text{ V}$ , $I_{SW} = 100\text{ mA}$		150	300	m $\Omega$
Leakage Current	$I_{LKG}$				1	$\mu\text{A}$
Peak Current Limit	$I_{CL}$	Duty cycle (D) = $D_{MAX}$	1.5			A
OSCILLATOR						
Switching Frequency	$f_{SW}$	$R_F = 97\text{ k}\Omega$	800	1000	1200	kHz
Maximum Duty Cycle	$D_{MAX}$	$R_F = 97\text{ k}\Omega$	84	90		%
SOFT START						
Soft Start Time	$t_{SS}$			1.1		ms
OVERVOLTAGE PROTECTION						
Overvoltage Rising Threshold on OVP Pin	$V_{OVPR}$		36.5	39	40	V
Overvoltage Hysteresis on OVP Pin	$V_{OVPR\_HYS}$		0.1	0.7	1.4	V

**LED CURRENT REGULATION SPECIFICATIONS**

$V_{IN} = 12\text{ V}$ ,  $\overline{\text{SHDN}} = \text{high}$ ,  $T_A = -25^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .

**Table 2.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>CURRENT SOURCE</b>						
ISET Pin Voltage	$V_{SET}$	$6\text{ V} \leq V_{IN} \leq 21\text{ V}$	1.14	1.18	1.22	V
Adjustable LED Current <sup>1</sup>	$I_{LED}$		0		25	mA
Constant Current Sink of 20 mA <sup>2</sup>	$I_{LED20}$	$R_{SET} = 180\text{ k}\Omega$	19.4	20	20.6	mA
Minimum Headroom Voltage <sup>2</sup>	$V_{HR20}$	$R_{SET} = 180\text{ k}\Omega$		0.66	0.9	V
Current Matching Between Strings <sup>2</sup>		$R_{SET} = 180\text{ k}\Omega$	-1.5		+1.5	%
LED Current Accuracy <sup>2</sup>		$R_{SET} = 180\text{ k}\Omega$	-3		+3	%
Current Source Leakage Current					1	$\mu\text{A}$
<b>FPWM GENERATOR</b>						
Dimming Frequency	$f_{PWM}$		6.8	8.0	9.2	kHz
<b>LED FAULT DETECTION</b>						
Open Fault Delay <sup>1</sup>	$t_{D\_OPENFAULT}$				6.5	$\mu\text{s}$

<sup>1</sup> This electrical specification is guaranteed by design.

<sup>2</sup> Tested at  $T_A = +25^\circ\text{C}$ .

**GENERAL SPECIFICATIONS**

$V_{IN} = 12\text{ V}$ ,  $\overline{\text{SHDN}} = \text{high}$ ,  $T_A = -25^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ .

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Input Voltage Range	$V_{IN}$		6		21	V
Quiescent Current	$I_Q$	$6\text{ V} \leq V_{IN} \leq 21\text{ V}$ , $\overline{\text{SHDN}} = \text{high}$		3.5	7	mA
Shutdown Supply Current	$I_{SD}$	$6\text{ V} \leq V_{IN} \leq 21\text{ V}$ , $\overline{\text{SHDN}} = \text{low}$			2	$\mu\text{A}$
VDD REGULATOR						
VDD Regulated Output	$V_{VDD\_REG}$	$6\text{ V} \leq V_{IN} \leq 21\text{ V}$	3.1	3.3	3.5	V
PWM INPUT						
PWM Voltage High	$V_{PWM\_HIGH}$		2.0		5.5	V
PWM Voltage Low	$V_{PWM\_LOW}$				0.8	V
PWM Input Range			100		10,000	Hz
THERMAL SHUTDOWN						
Thermal Shutdown Threshold <sup>1</sup>	$T_{SD}$			160		$^\circ\text{C}$
Thermal Shutdown Hysteresis <sup>1</sup>	$T_{SDHYS}$			30		$^\circ\text{C}$
UVLO						
$V_{IN}$ Falling Threshold	$V_{UVLOF}$	$V_{IN}$ falling	4	4.2		V
$V_{IN}$ Rising Threshold	$V_{UVLOR}$	$V_{IN}$ rising		5.0	5.6	V
SHDN CONTROL						
Input Voltage High	$V_{IH}$		2.5		5.5	V
Input Voltage Low	$V_{IL}$				0.5	V
$\overline{\text{SHDN}}$ Pin Input Current	$I_{\overline{\text{SHDN}}}$	$\overline{\text{SHDN}} = 3.3\text{ V}$		6		$\mu\text{A}$

<sup>1</sup> This electrical specification is guaranteed by design.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 4.

Parameter	Rating
VIN	-0.3 V to +23 V
SW	-0.3 V to +40 V
SHDN, PWM	-0.3 V to +6 V
ISSET, FSLCT, COMP	-0.3 V to +3.5 V
VDD	-0.3 V to +3.7 V
FB1, FB2, FB3, FB4	-0.3 V to +40 V
OVP	-0.3 V to +40 V
Maximum Junction Temperature ( $T_J$ max)	150°C
Operating Temperature Range ( $T_A$ )	-25°C to +85°C
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Reflow Peak Temperature (20 sec to 40 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

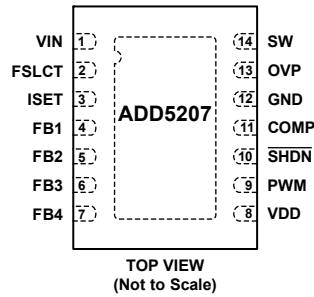
Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
14-Lead LFCSP	33.24	2.42	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
 1. CONNECT THE EXPOSED PADDLE TO GROUND.

08350-003

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Supply Input. Must be locally bypassed with a capacitor to ground.
2	FSLCT	Frequency Select. A resistor from this pin to ground sets the boost switching frequency from 600 kHz to 1 MHz.
3	ISET	Full-Scale LED Current Set. A resistor from this pin to ground sets the LED current up to 25 mA.
4	FB1	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin.
5	FB2	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin.
6	FB3	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin.
7	FB4	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin. If unused, connect FB4 to GND.
8	VDD	Internal Linear Regulator Output. This regulator provides power to the <a href="#">ADD5207</a> .
9	PWM	PWM Signal Input.
10	SHDN	Shutdown Control for PWM Input Operation Mode. Active low.
11	COMP	Compensation for the Boost Converter. Two capacitors and a resistor are connected in series between ground and this pin for stable operation.
12	GND	Ground.
13	OVP	Overshoot Protection. The boost converter output is connected to this pin directly.
14	SW	Drain Connection of the Internal Power FET.
	EP	Exposed Paddle. Connect the exposed paddle to ground.



### TYPICAL PERFORMANCE CHARACTERISTICS

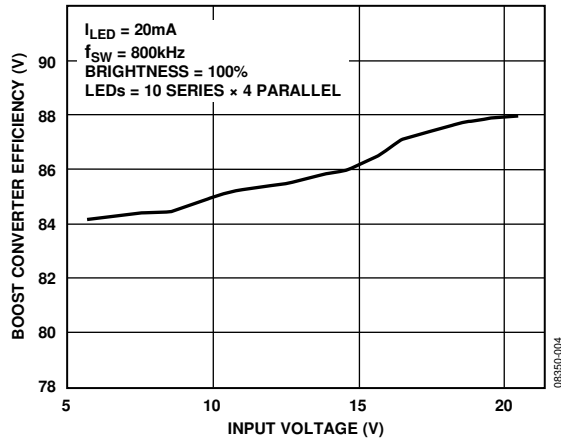


Figure 4. Boost Converter Efficiency vs. Input Voltage

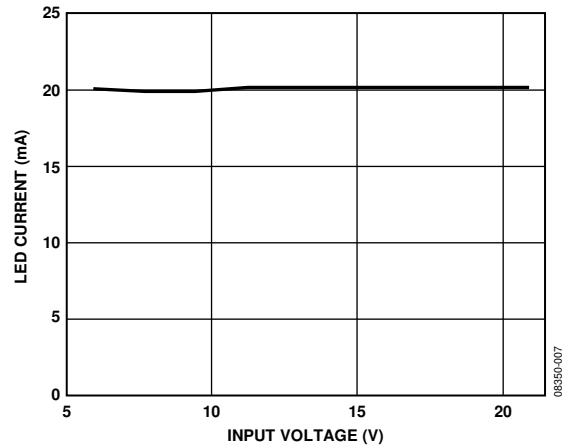


Figure 7. LED Current vs. Input Voltage ( $I_{LED} = 20\text{ mA}$ )

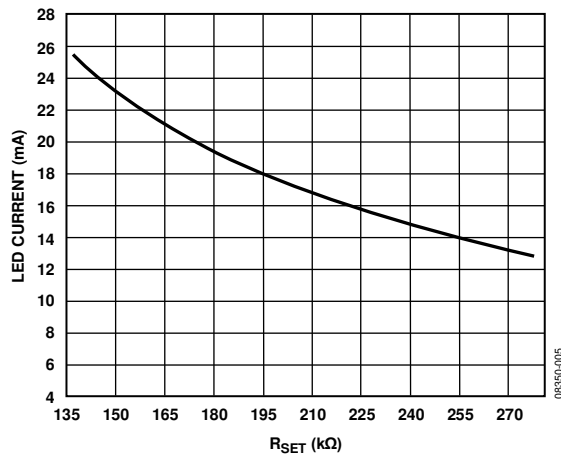


Figure 5. LED Current vs.  $R_{SET}$

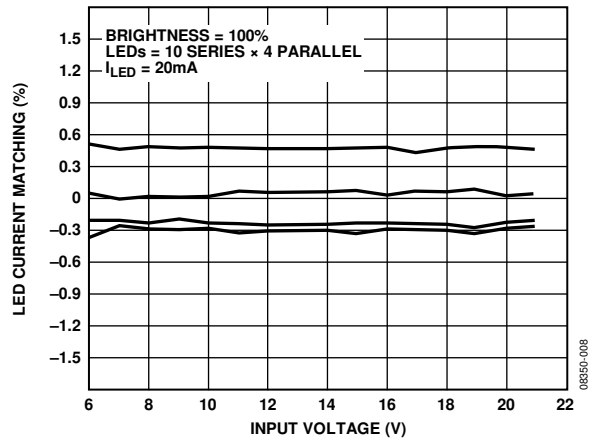


Figure 8. LED Current Matching vs. Input Voltage

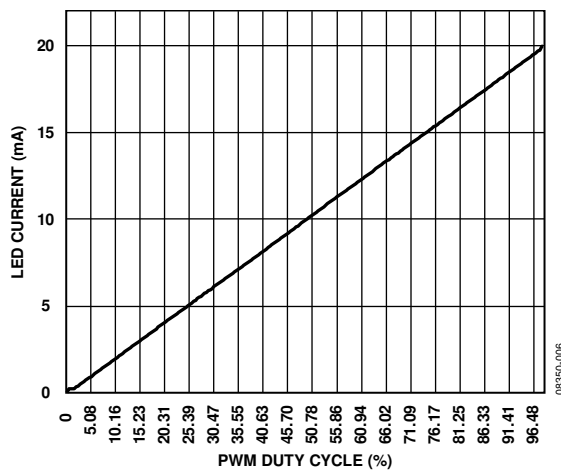


Figure 6. LED Current vs. PWM Input Duty Cycle

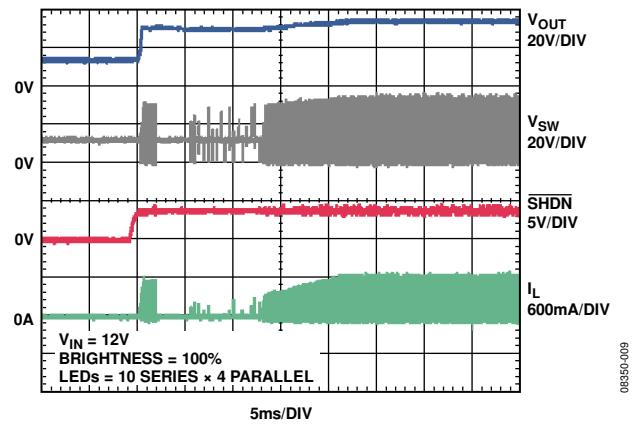


Figure 9. Start-Up Waveforms (Brightness = 100%)

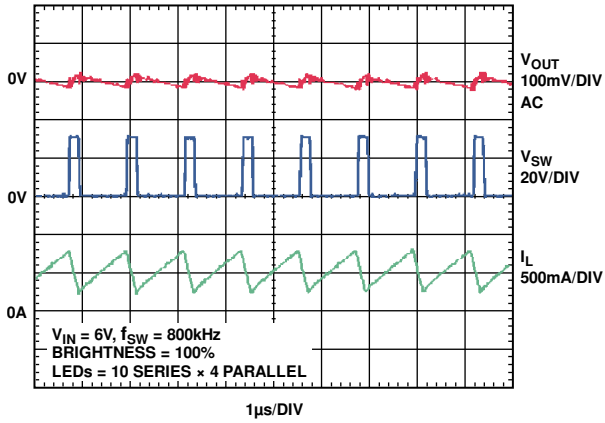


Figure 10. Switching Waveforms ( $V_{IN} = 6\text{ V}$ )

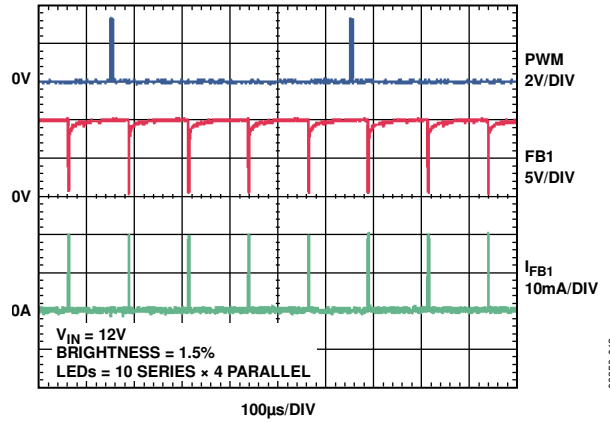


Figure 12. LED Current Waveforms (Brightness = 1.5%)

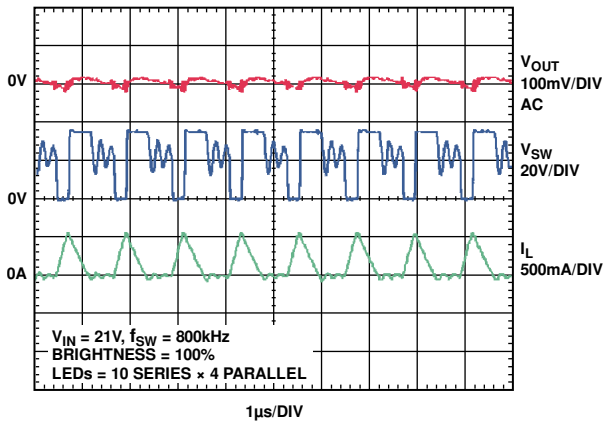


Figure 11. Switching Waveforms ( $V_{IN} = 21\text{ V}$ )

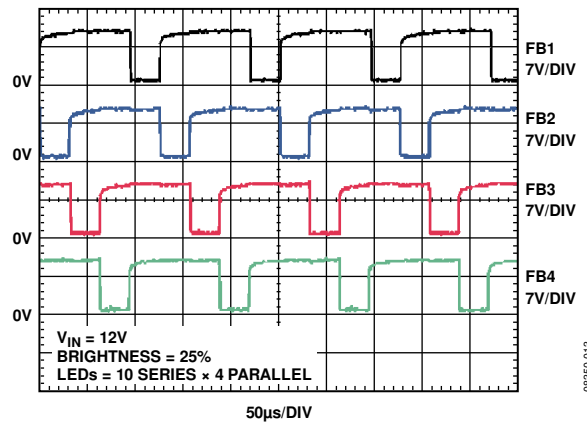


Figure 13. LED FBx Waveforms (Brightness = 25%)

08350-010

08350-012

08350-011

08350-013

## THEORY OF OPERATION

### CURRENT MODE, STEP-UP SWITCHING REGULATOR OPERATION

The **ADD5207** uses a current mode PWM boost regulator to generate the minimum voltage needed to drive the LED string at the programmed LED current. The current mode regulation system allows a fast transient response while maintaining a stable output voltage. By selecting the proper resistor-capacitor network from COMP to GND, the regulator response is optimized for a wide range of input voltages, output voltages, and load conditions. The **ADD5207** can provide a 36 V maximum output voltage and drive up to 10 LEDs (3.4 V/25 mA type of LEDs) for each channel.

### INTERNAL 3.3 V REGULATOR

The **ADD5207** contains a 3.3 V linear regulator that is used for biasing internal circuitry. The internal regulator requires a 1  $\mu$ F bypass capacitor. Place this bypass capacitor between Pin VDD (Pin 8) and GND, as close as possible to Pin VDD.

### BOOST CONVERTER SWITCHING FREQUENCY

The **ADD5207** boost converter switching frequency is user adjustable, between 600 kHz to 1 MHz, by using an external resistor,  $R_F$ . A frequency of 600 kHz is recommended to optimize the regulator for high efficiency, and a frequency of 1 MHz is recommended to minimize the size of external components.

See Figure 14 for considerations when selecting a switching frequency and an adjustment resistor ( $R_F$ ).

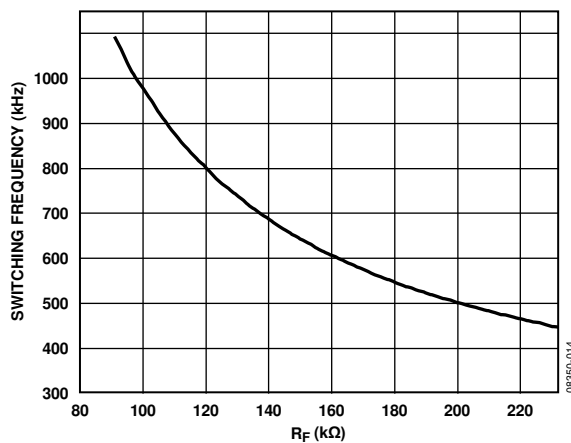


Figure 14. Switching Frequency vs.  $R_F$

### DIMMING FREQUENCY ( $f_{PWM}$ )

The **ADD5207** contains an internal oscillator to generate the PWM dimming signal for LED brightness control. The LED dimming frequency ( $f_{PWM}$ ) is fixed at 8 kHz internally.

### CURRENT SOURCE

The **ADD5207** contains four current sources to provide accurate current sinking for each LED string. String-to-string tolerance is kept within  $\pm 1.5\%$  at 20 mA. Each LED string current is adjusted up to 25 mA using an external resistor.

The **ADD5207** contains an LED open fault protection circuit for each channel. If the headroom voltage of the current source remains below 150 mV while the boost converter output reaches the OVP level, the **ADD5207** recognizes that the current source has an open-load fault for the current source, and the current source is disabled.

If an application requires three LED strings, each LED string should be connected using FB1 to FB3. The unused FB4 pin should be tied to GND.

The **ADD5207** contains hysteresis to prevent the LED current change that is caused by a  $\pm 0.195\%$  jitter of the PWM input.

### Programming the LED Current

As shown in the Figure 2, the **ADD5207** has an LED current set pin (ISET). A resistor ( $R_{SET}$ ) from this pin to ground adjusts the LED current up to 25 mA. LED current level can be set with following equation:

$$I_{LED} = \frac{3600}{R_{SET}} (A)$$

### PWM DIMMING MODE

The **ADD5207** supports 8-bit resolution to control brightness. However, each current source has a minimum on time requirement for LED current regulation such that the dimming is in the range of 1.5% to 100%. Accordingly, even when the PWM input duty cycle is more than 0% and less than 1.5%, the LED duty cycle is held at 1.5%.

### Phase Shift PWM Dimming

There is a phase delay between each current source channel that is programmed by the number of current sources in operation. If the application requires four separate LED strings, each string has a 90 degree phase delay between channels. If three LED strings are connected at the FB1 to FB3 pins (FB4 = GND), each string has a 120 degree phase delay.

### SAFETY FEATURES

The **ADD5207** contains several safety features to provide stable and reliable operation.

#### Soft Start

The **ADD5207** contains an internal soft start function to reduce inrush current at startup. The soft start time is typically 1.1 ms.

#### Overvoltage Protection (OVP)

The **ADD5207** contains OVP circuits to prevent boost converter damage if the output voltage becomes excessive for any reason. To keep a safe output level, the integrated OVP circuit monitors

the output voltage. When the OVP pin voltage reaches the OVP rising threshold, the boost converter stops switching, which causes the output voltage to drop. When the OVP pin voltage drops below the OVP falling threshold, the boost converter begins switching again, causing the output to rise. There is about 0.8 V hysteresis between the rising and falling thresholds. The OVP level is fixed at 39 V (typical).

### Open-Load Protection (OLP)

The [ADD5207](#) contains a headroom control circuit to minimize power loss at each current source. Therefore, the minimum feedback voltage is achieved by regulating the output voltage of the boost converter. If any LED string is open circuit during normal operation, the current source headroom voltage ( $V_{HR}$ ) is pulled to GND. In this condition, OLP is activated if  $V_{HR}$  is less than 150 mV until the boost converter output voltage rises up to the OVP level.

### Undervoltage Lockout (UVLO)

An undervoltage lockout circuit is included with built-in hysteresis. The [ADD5207](#) turns on when  $V_{IN}$  rises above 5.0 V (typical) and shuts down when  $V_{IN}$  falls below 4.2 V (typical).

### Thermal Protection

Thermal overload protection prevents excessive power dissipation from overheating and damaging the [ADD5207](#). When the junction temperature ( $T_j$ ) exceeds 160°C, a thermal sensor immediately activates the fault protection, which shuts down the device and allows it to cool. The device self-starts when the junction temperature ( $T_j$ ) of the die falls below 130°C.

## EXTERNAL COMPONENT SELECTION GUIDE

### Inductor Selection

The inductor is an integral part of the step-up converter. It stores energy during the switch's on time and transfers that energy to the output through the output diode during the switch's off time. An inductor in the range of 4.7  $\mu$ H to 22  $\mu$ H is recommended. In general, lower inductance values result in higher saturation current and lower series resistance for a given physical size. However, lower inductance results in higher peak current, which can lead to reduced efficiency and greater input and/or output ripple and noise. Peak-to-peak inductor ripple current at close to 30% of the maximum dc input current typically yields an optimal compromise.

The input ( $V_{IN}$ ) and output ( $V_{OUT}$ ) voltages determine the switch duty cycle (D), which, in turn, is used to determine the inductor ripple current.

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Use the duty cycle and switching frequency ( $f_{sw}$ ) to determine the on time.

$$t_{ON} = \frac{D}{f_{sw}}$$

The inductor ripple current ( $\Delta I_L$ ) in a steady state is:

$$\Delta I_L = \frac{V_{IN} \times t_{ON}}{L}$$

Solve for the inductance value (L):

$$L = \frac{V_{IN} \times t_{ON}}{\Delta I_L}$$

Make sure that the peak inductor current (that is, the maximum input current plus half of the inductor ripple current) is less than the rated saturation current of the inductor. In addition, ensure that the maximum rated rms current of the inductor is greater than the maximum dc input current to the regulator.

For duty cycles greater than 50% that occur with input voltages greater than half the output voltage, slope compensation is required to maintain stability of the current mode regulator. The inherent open-loop stability causes subharmonic instability when the duty ratio is greater than 50%. To avoid subharmonic instability, the slope of the inductor current should be less than half of the compensation slope.

Inductor manufacturers include: Coilcraft, Inc., Sumida Corporation, and Toko.

### Input and Output Capacitor Selection

The [ADD5207](#) requires input and output bypass capacitors to supply transient currents while maintaining a constant input and output voltage. Use a low effective series resistance (ESR) 10  $\mu$ F or greater capacitor for the input capacitor to prevent noise at the [ADD5207](#) input. Place the input between  $V_{IN}$  and GND, as close as possible to the [ADD5207](#). Ceramic capacitors are preferred because of their low ESR characteristics. Alternatively, use a high value, medium ESR capacitor in parallel with a 0.1  $\mu$ F low ESR capacitor as close as possible to the [ADD5207](#).

The output capacitor maintains the output voltage and supplies current to the load while the [ADD5207](#) switch is on. The value and characteristics of the output capacitor greatly affect the output voltage ripple and stability of the regulator. Use a low ESR output capacitor; ceramic dielectric capacitors are preferred.

For very low ESR capacitors, such as ceramic capacitors, the ripple current due to the capacitance is calculated as follows. Because the capacitor discharges during the on time ( $t_{ON}$ ), the charge removed from the capacitor ( $Q_C$ ) is the load current multiplied by the on time. Therefore, the output voltage ripple ( $\Delta V_{OUT}$ ) is

$$\Delta V_{OUT} = \frac{Q_C}{C_{OUT}} = \frac{I_L \times t_{ON}}{C_{OUT}}$$

where:

$C_{OUT}$  is the output capacitance.

$I_L$  is the average inductor current.

Using the duty cycle and switching frequency ( $f_{sw}$ ), users can determine the on time with the following equation:

$$t_{ON} = \frac{D}{f_{sw}}$$

The input ( $V_{IN}$ ) and output ( $V_{OUT}$ ) voltages determine the switch duty cycle (D) with the following equation:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Choose the output capacitor based on the following equation:

$$C_{OUT} \geq \frac{I_L \times (V_{OUT} - V_{IN})}{f_{sw} \times V_{OUT} \times \Delta V_{OUT}}$$

Capacitor manufacturers include: Murata Manufacturing Co., Ltd., AVX, Sanyo, and Taiyo Yuden Co., Ltd.

### Diode Selection

The output diode conducts the inductor current to the output capacitor and loads while the switch is off. For high efficiency, minimize the forward voltage drop of the diode. Schottky diodes are recommended. However, for high voltage, high temperature applications, where the Schottky diode reverse leakage current becomes significant and degrades efficiency, use an ultrafast junction diode. The output diode for a boost regulator must be chosen depending on the output voltage and the output current. The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. Using Schottky diodes with lower forward voltage drop decreases power dissipation and increases efficiency. The diode must be rated to handle the average output load current. Many diode manufacturers derate the current capability of the diode as a function of the duty cycle. Verify that the output diode is rated to handle the average output load current with the minimum duty cycle.

The minimum duty cycle of the [ADD5207](#) is:

$$D_{MIN} = \frac{V_{OUT} - V_{IN\_MAX}}{V_{OUT}}$$

where  $V_{IN\_MAX}$  is the maximum input voltage.

For example,  $D_{MIN}$  is 0.5 when  $V_{OUT}$  is 30 V and  $V_{IN\_MAX}$  is 15 V.

Schottky diode manufacturers include ON Semiconductor, Diodes Incorporated, Central Semiconductor Corp., and Sanyo.

### Loop Compensation

The external inductor, output capacitor, and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size, and cost. The compensation resistor ( $R_C$ ) and compensation capacitor ( $C_C$ ) at COMP are selected to optimize control loop stability. For typical LED application of the [ADD5207](#), a 6.8 k $\Omega$  compensation resistor in series with a 2.2 nF compensation capacitor at COMP is adequate.

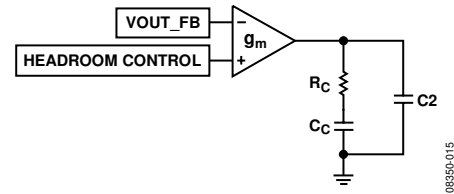


Figure 15. Compensation Components

A step-up converter produces an undesirable right-half plane zero in the regulation feedback loop. Capacitor C2 is chosen to cancel the zero introduced by output capacitance ESR. Solving for C2,

$$C2 = \frac{ESR \times C_{OUT}}{R_C}$$

For low ESR output capacitance, such as with a ceramic capacitor, C2 is optional.

### LAYOUT GUIDELINES

When designing a high frequency, switching, regulated power supply, layout is very important. Using a good layout can solve many problems associated with these types of supplies. The main problems are loss of regulation at high output current and/or large input-to-output voltage differentials, excessive noise on the output and switch waveforms, and instability. Using the following guidelines helps minimize these problems.

Make all power (high current) traces as short, direct, and thick as possible. It is good practice on a standard printed circuit board (PCB) to make the traces an absolute minimum of 15 mil (0.381 mm) per ampere. The inductor, output capacitors, and output diode should be as close to each other as possible. This helps reduce EMI radiated by the power traces that carry high switching currents. Close proximity of the components also reduces lead inductance and resistance, which in turn reduce noise spikes, ringing, and resistive losses that produce voltage errors.

The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable), should be connected close together, and directly to a ground plane. It is also a good idea to have a ground plane on both sides of the PCB. This reduces noise by reducing ground loop errors and by absorbing more of the EMI radiated by the inductor.

For multilayer boards of more than two layers, a ground plane can be used to separate the power plane (power traces and components) and the signal plane (feedback, compensation, and components) for improved performance. On multilayer boards, the use of vias is required to connect traces and different planes. If a trace needs to conduct a significant amount of current from one plane to the other, it is good practice to use one standard via per 200 mA of current. Arrange the components so that the switching current loops curl in the same direction.

Due to how switching regulators operate, there are two power states: one state when the switch is on, and one when the switch is off. During each state, there is a current loop made by the power components currently conducting. Place the power components so that the current loop is conducting in the same direction during each of the two states. This prevents magnetic field reversal caused by the traces between the two half cycles and reduces radiated EMI.

#### **Layout Procedure**

To achieve high efficiency, good regulation, and stability, a good PCB layout is required. It is recommended that the reference board layout be followed as closely as possible because it is already optimized for high efficiency and low noise.

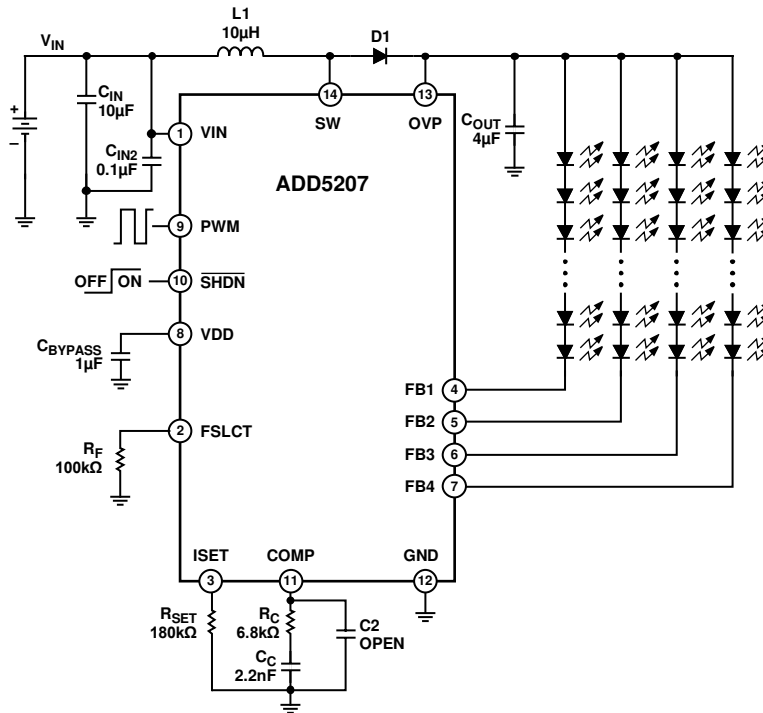
Use the following general guidelines when designing PCBs:

- Keep  $C_{IN}$  close to the  $V_{IN}$  and GND leads of the [ADD5207](#).
- Keep the high current path from  $C_{IN}$  (through L1) to the SW and GND leads as short as possible.
- Keep the high current path from  $C_{IN}$  (through L1), D1, and  $C_{OUT}$  as short as possible.
- Keep high current traces as short and as wide as possible.
- Keep nodes connected to SW away from sensitive traces, such as COMP, to prevent coupling of the traces. If such traces must be run near each other, place a ground trace between the two as a shield.
- Place the compensation components as close as possible to the COMP pin.
- Place the LED current setting resistors as close as possible to each pin to prevent noise pickup.
- Avoid routing noise-sensitive traces near high current traces and components, especially the LED current setting node ( $I_{SET}$ ).
- Use a thermal pad size that is the same dimension as the exposed pad on the bottom of the package.

#### **Heat Sinking**

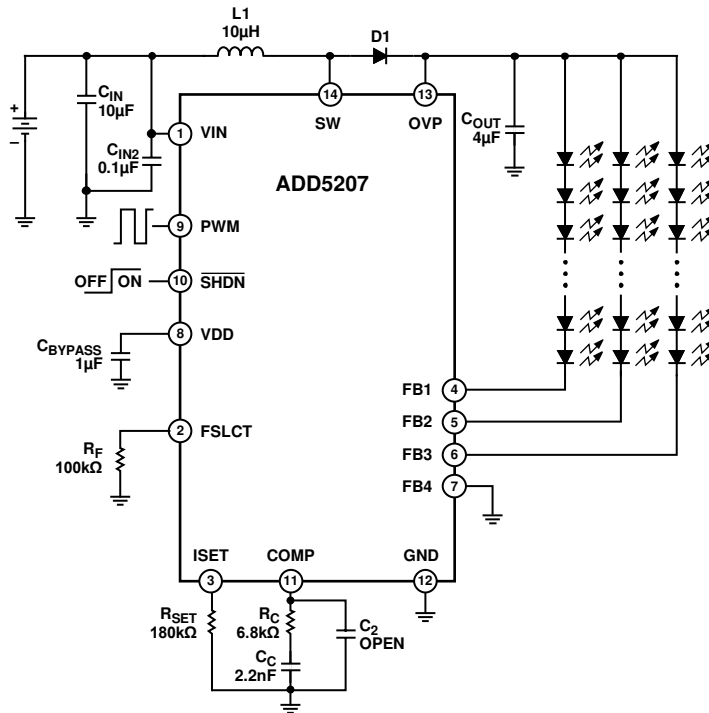
When using a surface-mount power IC or external power switches, the PCB can often be used as the heat sink. This is done by using the copper area of the PCB to transfer heat from the device. Users should maximize this area to optimize thermal performance.

TYPICAL APPLICATION CIRCUITS



08350-016

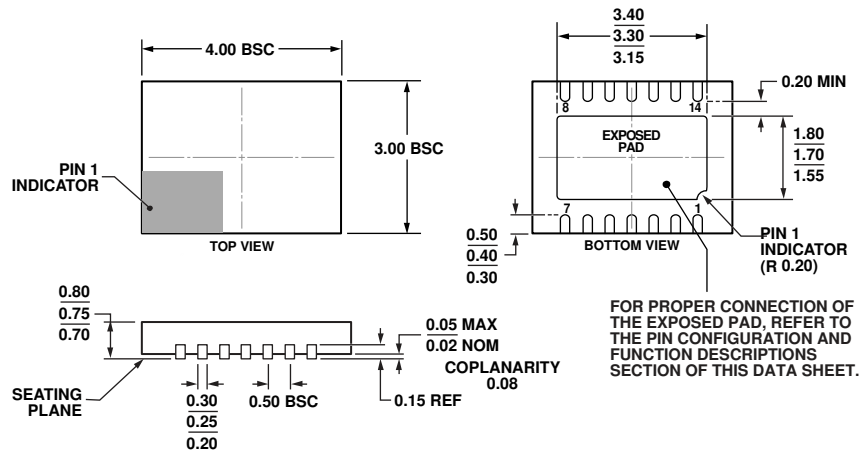
Figure 16. Typical Four-String Application Circuit



08350-017

Figure 17. Typical Three-String Application Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGED

Figure 18. 14-Lead Lead Frame Chip Scale Package [LFCSP\_WD]  
 4 mm × 3 mm Body, Very Very Thin Dual  
 (CP-14-1)  
 Dimensions shown in millimeters

062509-A

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADD5207ACPZ-RL	-25°C to +85°C	14-Lead LFCSP_WD	CP-14-1

<sup>1</sup> Z = RoHS Compliant Part.