High Voltage, Latch-Up Proof, 4-Channel Multiplexer

ADG5204

FEATURES

Latch-up proof
3 pF off source capacitance
26 pF off drain capacitance
−0.6 pC charge injection
Low leakage: 0.4 nA maximum at 85°C
±9 V to ±22 V dual-supply operation
9 V to 40 V single-supply operation
48 V supply maximum ratings
Fully specified at ±15 V, ±20 V, +12 V, and +36 V
V_{SS} to V_{DD} analog signal range

APPLICATIONS

Automatic test equipment
Data acquisition
Instrumentation
Avionics
Audio and video switching
Communication systems

FUNCTIONAL BLOCK DIAGRAM

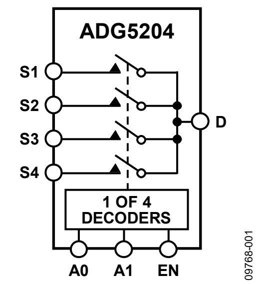

Figure 1.

GENERAL DESCRIPTION

The ADG5204 is a complementary metal oxide semiconductor (CMOS) analog multiplexer, comprising four single channels.

The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed together with high signal bandwidth make the ADG5204 suitable for video signal switching.

The ADG5204 is designed on a trench process, which guards against latch-up. A dielectric trench separates the P and N channel transistors, thereby preventing latch-up even under severe overvoltage conditions.

The ADG5204 switches one of four inputs to a common output, D, as determined by the 3-bit binary address lines, A0, A1, and EN. Logic 0 on the EN pin disables the device. Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action.

PRODUCT HIGHLIGHTS

1. Trench Isolation Guards Against Latch-Up.
   A dielectric trench separates the P and N channel transistors, thereby preventing latch-up even under severe overvoltage conditions.
2. Ultralow Capacitance and <1 pC Charge Injection.
3. Dual-Supply Operation.
   For applications where the analog signal is bipolar, the ADG5204 can be operated from dual supplies up to ±22 V.
4. Single-Supply Operation.
   For applications where the analog signal is unipolar, the ADG5204 can be operated from a single rail power supply up to 40 V.
5. 3 V Logic-Compatible Digital Inputs.
   V_{INH} = 2.0 V, V_{INL} = 0.8 V.
6. No V_L Logic Power Supply Required.

Rev. A

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5/2011—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V max	
On Resistance, R_{ON}	160			Ω typ	V_S = ±10 V, I_S = −1 mA, see Figure 24
	200	250	280	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	4.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	38			Ω typ	V_S = ±10 V, I_S = −1 mA
	50	65	70	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	0.01			nA typ	V_S = V_S = ±10 V, V_D = ∓10 V, see Figure 23
	0.1	0.2	0.4	nA max	
Drain Off Leakage, I_D (Off)	0.01			nA typ	V_S = V_S = ±10 V, V_D = ∓10 V, see Figure 23
	0.1	0.4	2.4	nA max	
Channel On Leakage, I_D, I_S (On)	0.02			nA typ	V_S = V_D = ±10 V, see Figure 26
	0.2	0.5	2.8	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	175			ns typ	R_L = 300 Ω, C_L = 35 pF
	230	285	320	ns max	V_S = 10 V, see Figure 29
t_{ON} (EN)	155			ns typ	R_L = 300 Ω, C_L = 35 pF
	205	255	285	ns max	V_S = 10 V, see Figure 31
t_{OFF} (EN)	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	175	200	215	ns max	V_S = 10 V, see Figure 31
Break-Before-Make Time Delay, t_D	80			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 10 V, see Figure 30
Charge Injection, Q_{INJ}	−0.6			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 32
Off Isolation	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz, see Figure 25
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 28
−3 dB Bandwidth	136			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 27
Insertion Loss	−6.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 27
C_S (Off)	3			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	26			pF typ	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	30			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	45			μA typ	Digital inputs = 0 V or V_{DD}
	55		70	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±9/±22	V min/max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V max	
On Resistance, R_{ON}	140			Ω typ	V_S = ±15 V, I_S = −1 mA, see Figure 24
	160	200	230	Ω max	V_{DD} = +18 V, V_{SS} = −18 V
On-Resistance Match Between Channels, ΔR_{ON}	4.5			Ω typ	V_S = ±15 V, I_S = −1 mA
	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	33			Ω typ	V_S = ±15 V, I_S = −1 mA
	45	55	60	Ω max	
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	0.01			nA typ	V_S = ±15 V, V_D = ∓15 V, see Figure 23
	0.1	0.2	0.4	nA max	
Drain Off Leakage, I_D (Off)	0.01			nA typ	V_S = ±15 V, V_D = ∓15 V, see Figure 23
	0.1	0.4	2.4	nA max	
Channel On Leakage, I_D, I_S (On)	0.02			nA typ	V_S = V_D = ±15 V, see Figure 26
	0.2	0.5	2.8	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	160			ns typ	R_L = 300 Ω, C_L = 35 pF
	215	260	290	ns max	V_S = 10 V, see Figure 29
t_{ON} (EN)	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	185	225	255	ns max	V_S = 10 V, see Figure 31
t_{OFF} (EN)	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	175	195	210	ns max	V_S = 10 V, see Figure 31
Break-Before-Make Time Delay, t_D	75			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 10 V, see Figure 30
Charge Injection, Q_{INJ}	−0.6			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 32
Off Isolation	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz, see Figure 25
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 28
−3 dB Bandwidth	150			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 27
Insertion Loss	−6			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 27
C_S (Off)	3			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	26			pF typ	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	30			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +22 V, V_{SS} = −22 V
I_{DD}	50			µA typ	Digital inputs = 0 V or V_{DD}
	70		110	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1	µA max	
V_{DD}/V_{SS}			±9/±22	V min/max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V max	
On Resistance, R_{ON}	340			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA, see Figure 24
	500	610	700	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	5			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	20	21	22	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	145			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	280	335	370	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	0.01			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 23
	0.1	0.2	0.4	nA max	
Drain Off Leakage, I_D (Off)	0.01			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 23
	0.1	0.4	2.4	nA max	
Channel On Leakage, I_D, I_S (On)	0.02			nA typ	V_S = V_D = 1 V/10 V, see Figure 26
	0.2	0.5	2.8	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	240			ns typ	R_L = 300 Ω, C_L = 35 pF
	350	445	515	ns max	V_S = 8 V, see Figure 29
t_{ON} (EN)	250			ns typ	R_L = 300 Ω, C_L = 35 pF
	335	420	485	ns max	V_S = 8 V, see Figure 31
t_{OFF} (EN)	160			ns typ	R_L = 300 Ω, C_L = 35 pF
	195	220	240	ns max	V_S = 8 V, see Figure 31
Break-Before-Make Time Delay, t_D	140			ns typ	R_L = 300 Ω, C_L = 35 pF
			60	ns min	V_{S1} = V_{S2} = 8 V, see Figure 30
Charge Injection, Q_{INJ}	−1.2			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 32
Off Isolation	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 25
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 28
−3 dB Bandwidth	106			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 27
Insertion Loss	−11			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 27
C_S (Off)	3.5			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	29			pF typ	V_S = 6 V, f = 1 MHz
C_D, C_S (On)	33			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	40			µA typ	Digital inputs = 0 V or V_{DD}
			65	µA max	
V_{DD}			9/40	V min/max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V max	
On Resistance, R_{ON}	150			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA, see Figure 24
	170	215	245	Ω max	V_{DD} = 32.4 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	4.5			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	35			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	50	60	65	Ω max	
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	0.01			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V, see Figure 23
	0.1	0.2	0.4	nA max	
Drain Off Leakage, I_D (Off)	0.01			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V, see Figure 23
	0.1	0.4	2.4	nA max	
Channel On Leakage, I_D, I_S (On)	0.02			nA typ	V_S = V_D = 1 V/30 V, see Figure 26
	0.2	0.5	2.8	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	180			ns typ	R_L = 300 Ω, C_L = 35 pF
	250	275	305	ns max	V_S = 18 V, see Figure 29
t_{ON} (EN)	170			ns typ	R_L = 300 Ω, C_L = 35 pF
	220	251	285	ns max	V_S = 18 V, see Figure 31
t_{OFF} (EN)	170			ns typ	R_L = 300 Ω, C_L = 35 pF
	210	215	220	ns max	V_S = 18 V, see Figure 31
Break-Before-Make Time Delay, t_D	80			ns typ	R_L = 300 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 18 V, see Figure 30
Charge Injection, Q_{INJ}	−0.6			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF, see Figure 32
Off Isolation	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 25
Channel-to-Channel Crosstalk	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 28
−3 dB Bandwidth	136			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 27
Insertion Loss	−6.7			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 27
C_S (Off)	3			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	26			pF typ	V_S = 18 V, f = 1 MHz
C_D, C_S (On)	30			pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 39.6 V
I_{DD}	85			μA typ	Digital inputs = 0 V or V_{DD}
	100		130	μA max	
V_{DD}			9/40	V min/max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR D

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR D PINS				
V_{DD} = +15 V, V_{SS} = −15 V				
TSSOP (θ_{JA} = 112.6°C/W)	24.5	7.5	2.8	mA max
LFCSP (θ_{JA} = 30.4°C/W)	35.7	7.7	2.8	mA max
V_{DD} = +20 V, V_{SS} = −20 V				
TSSOP (θ_{JA} = 112.6°C/W)	26	7.5	2.8	mA max
LFCSP (θ_{JA} = 30.4°C/W)	37	7.7	2.8	mA max
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	18	7	2.8	mA max
LFCSP (θ_{JA} = 30.4°C/W)	28	7.7	2.8	mA max
V_{DD} = 36 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 112.6°C/W)	30	7.7	2.8	mA max
LFCSP (θ_{JA} = 30.4°C/W)	41	7.7	2.8	mA max

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or D Pins	81 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or D[2]	Data + 15%
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP, θ_{JA} Thermal Impedance (4-Layer Board)	112.6°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C

[1] Overvoltages at the Sx and D pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] See Table 5.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

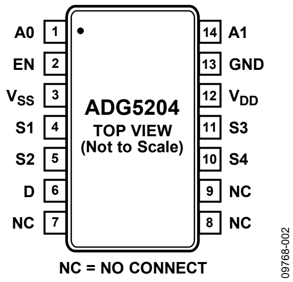

Figure 2. TSSOP Pin Configuration

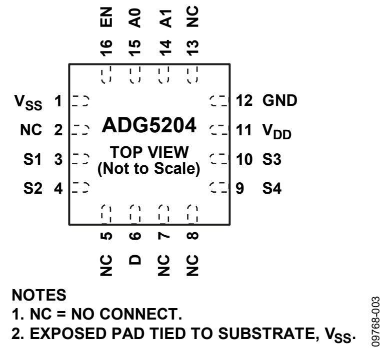

Figure 3. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	A0	Logic Control Input.
2	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switches.
3	1	V_{SS}	Most Negative Power Supply Potential.
4	3	S1	Source Terminal. Can be an input or an output.
5	4	S2	Source Terminal. Can be an input or an output.
6	6	D	Drain Terminal. Can be an input or an output.
7 to 9	2, 5, 7, 8, 13	NC	No Connect. These pins are open.
10	9	S4	Source Terminal. Can be an input or an output.
11	10	S3	Source Terminal. Can be an input or an output.
12	11	V_{DD}	Most Positive Power Supply Potential.
13	12	GND	Ground (0 V) Reference.
14	14	A1	Logic Control Input.
N/A[1]	EP	Exposed Pad	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

[1] N/A means not applicable.

TRUTH TABLE

Table 8.

EN	A1	A0	S1	S2	S3	S4
0	X[1]	X[1]	Off	Off	Off	Off
1	0	0	On	Off	Off	Off
1	0	1	Off	On	Off	Off
1	1	0	Off	Off	On	Off
1	1	1	Off	Off	Off	On

[1] X is don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

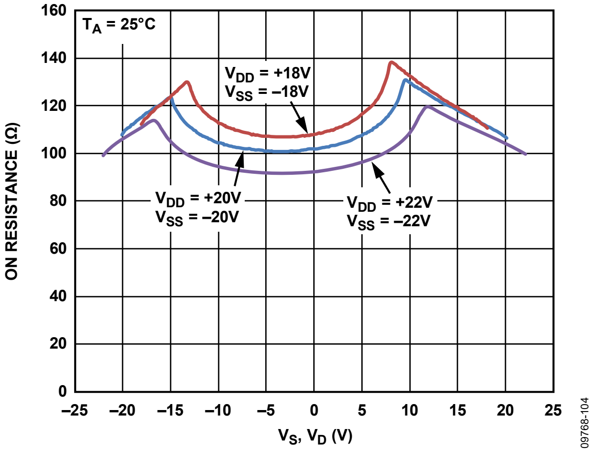

Figure 4. R_{ON} as a Function of V_D or V_S, Dual Supply

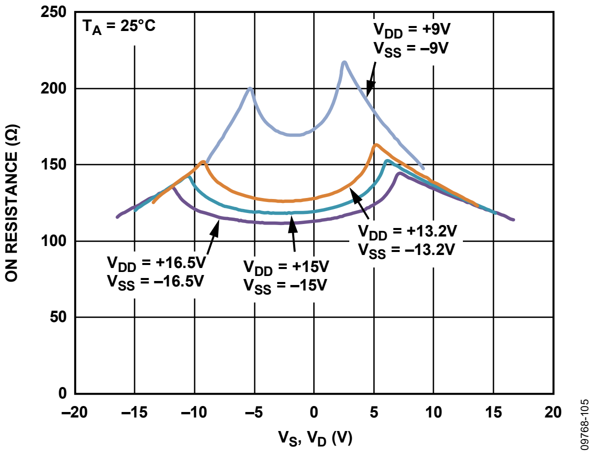

Figure 5. R_{ON} as a Function of V_D or V_S, Dual Supply

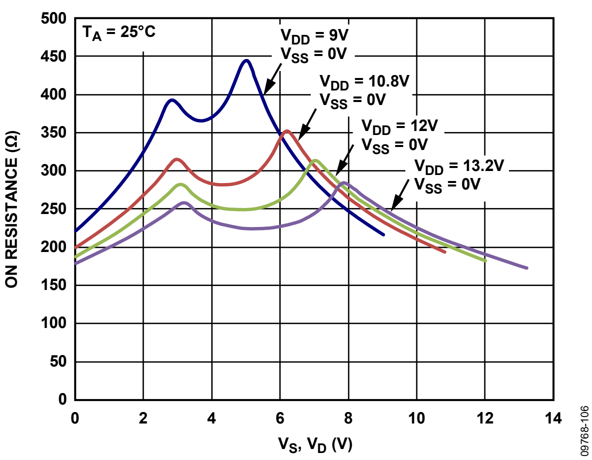

Figure 6. R_{ON} as a Function of V_D or V_S, Single Supply

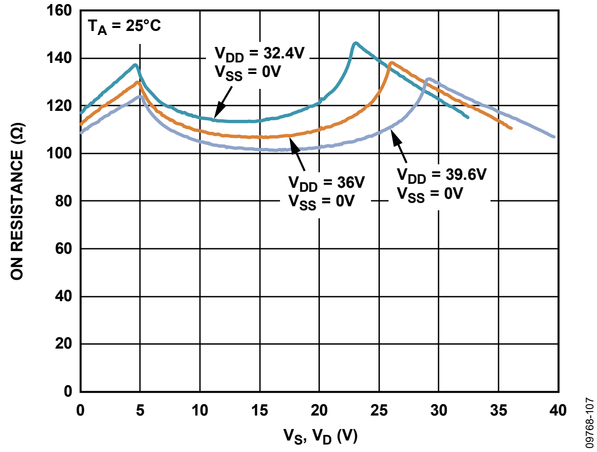

Figure 7. R_{ON} as a Function of V_D or V_S, Single Supply

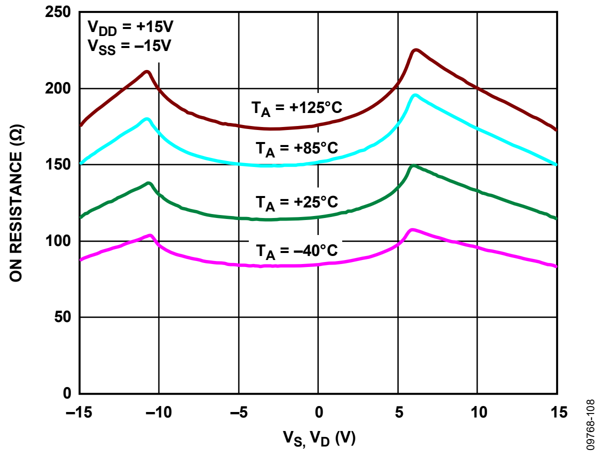

Figure 8. R_{ON} as a Function of V_D or V_S, for Different Temperatures, ±15 V Dual Supply

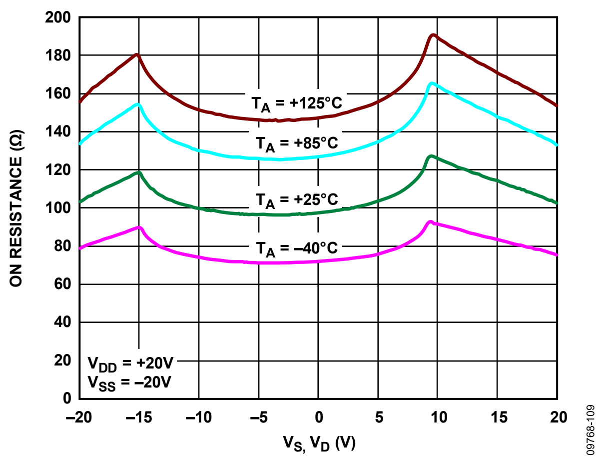

Figure 9. R_{ON} as a Function of V_D or V_S, for Different Temperatures, ±20 V Dual Supply

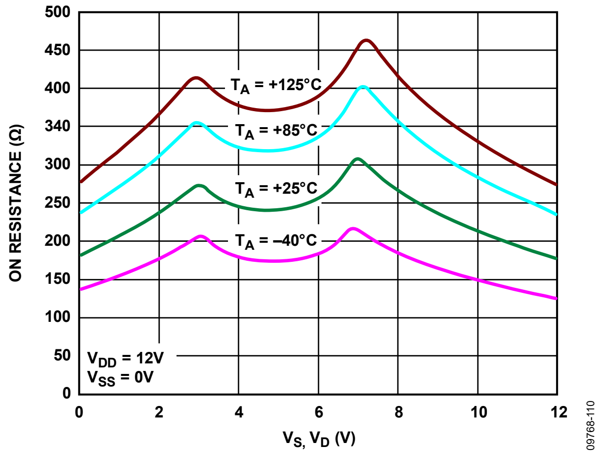

Figure 10. R_{ON} as a Function of V_D or V_S for Different Temperatures, 12 V Single Supply

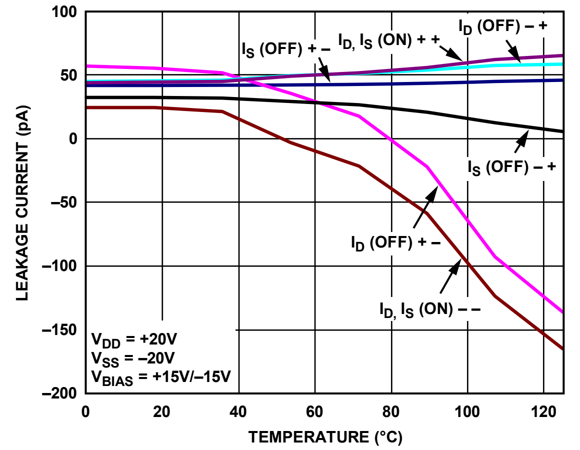

Figure 13. Leakage Current vs. Temperature, ±20 V Dual Supply

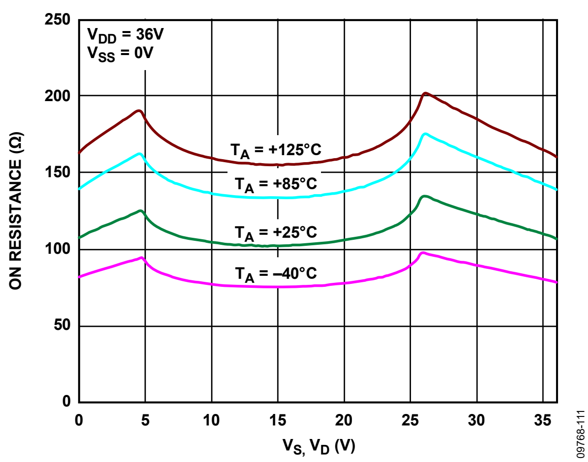

Figure 11. R_{ON} as a Function of V_D or V_S for Different Temperatures, 36 V Single Supply

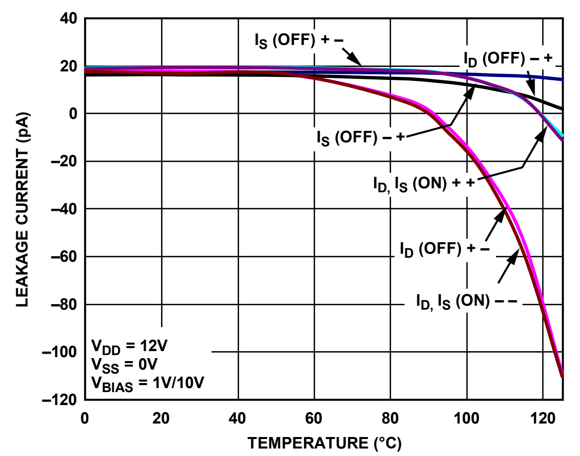

Figure 14. Leakage Current vs. Temperature, 12 V Single Supply

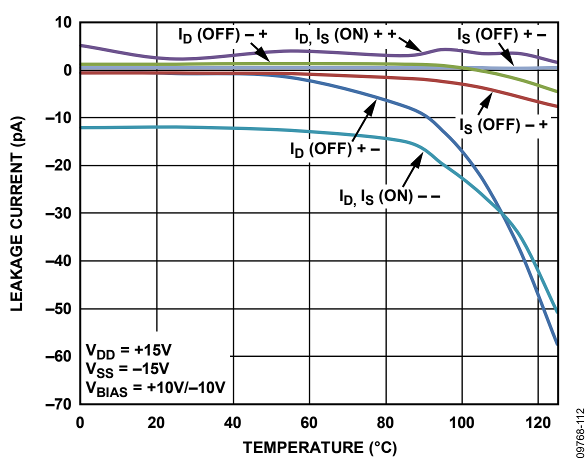

Figure 12. Leakage Current vs. Temperature, ±15 V Dual Supply

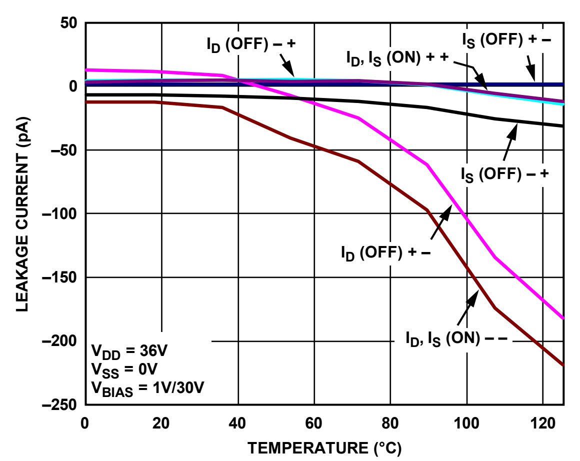

Figure 15. Leakage Current vs. Temperature, 36 V Single Supply

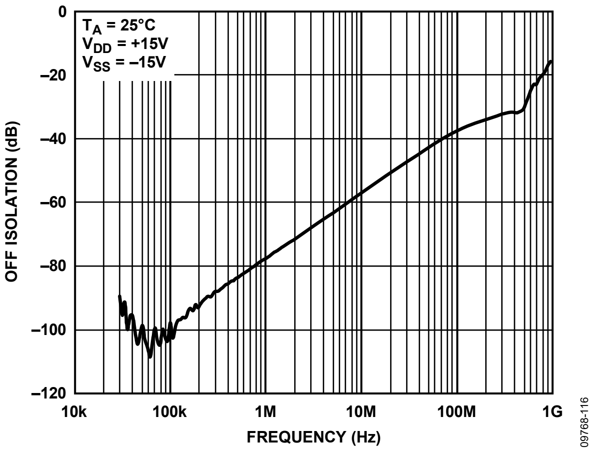

Figure 16. Off Isolation vs. Frequency, ±15 V Dual Supply

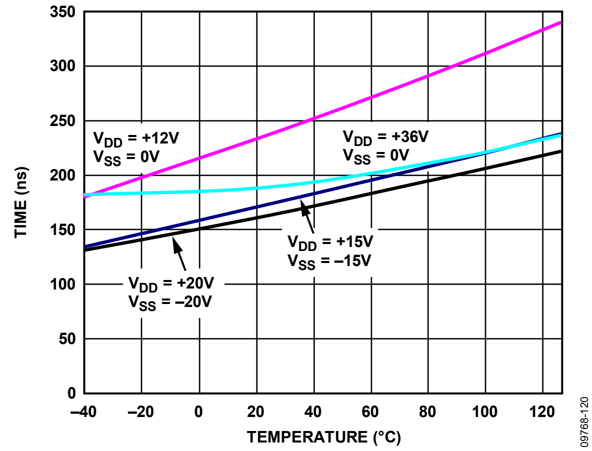

Figure 19. Transition Time vs. Temperature

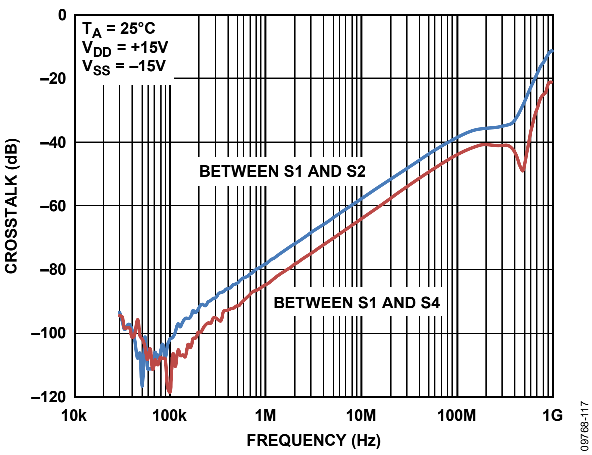

Figure 17. Crosstalk vs. Frequency, ±15 V Dual Supply

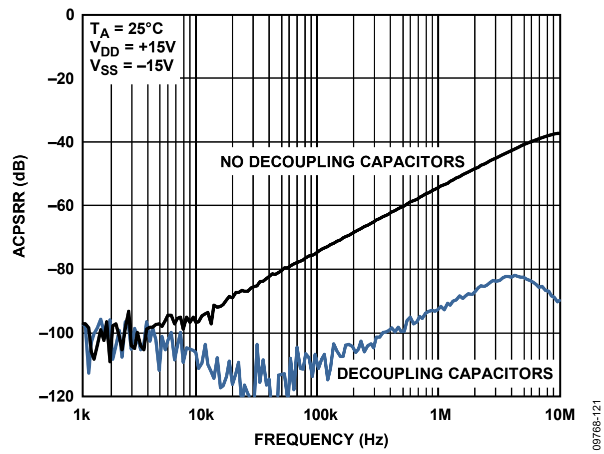

Figure 20. ACPSRR vs. Frequency, ±15 V Dual Supply

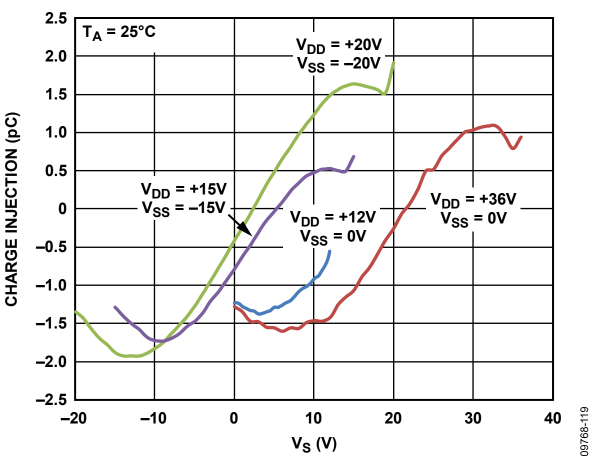

Figure 18. Charge Injection vs. Source Voltage

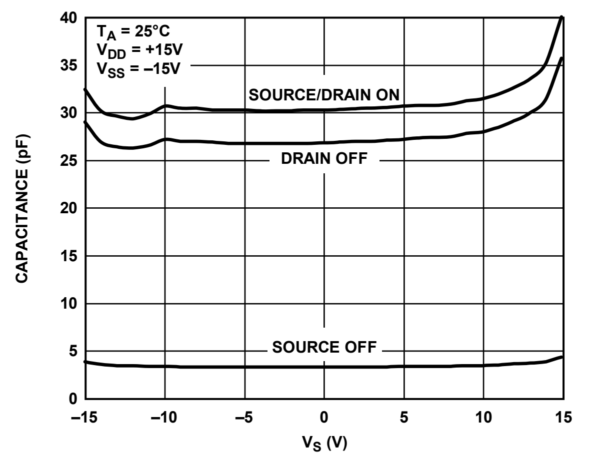

Figure 21. Capacitance vs. Source Voltage, Dual Supply

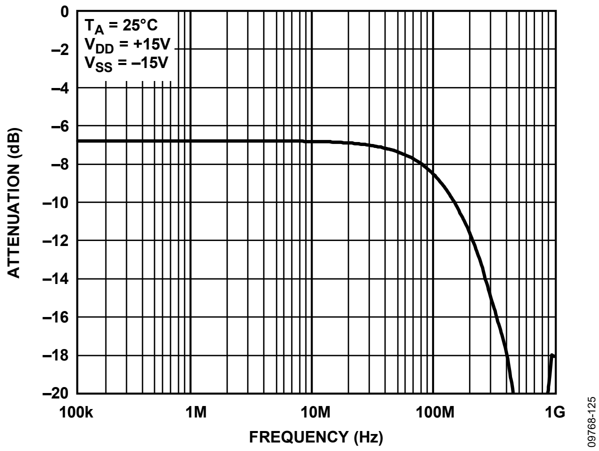

Figure 22. Bandwidth

TEST CIRCUITS

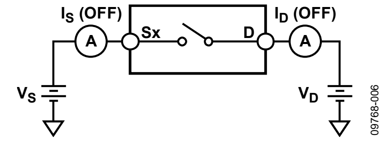

Figure 23. Off Leakage

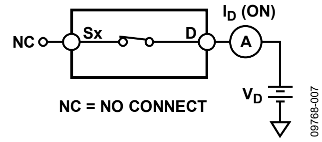

Figure 26. On Leakage

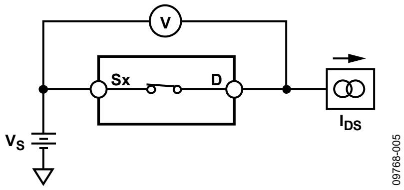

Figure 24. On Resistance

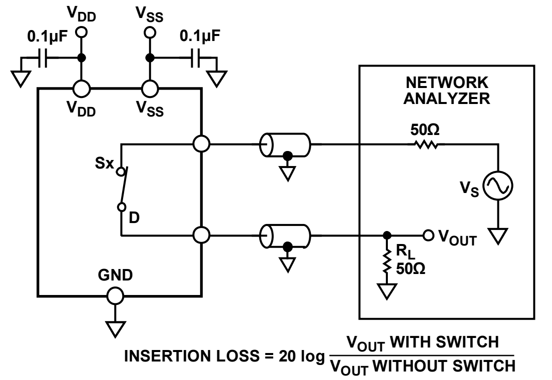

Figure 27. Bandwidth

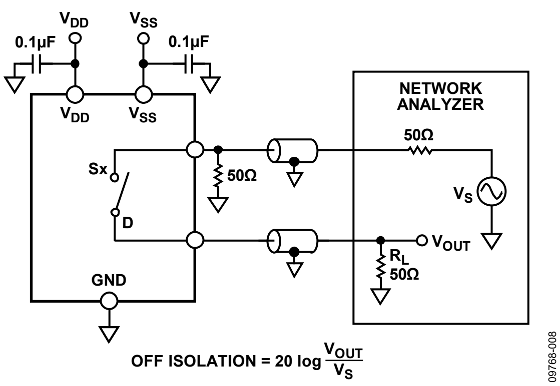

Figure 25. Off Isolation

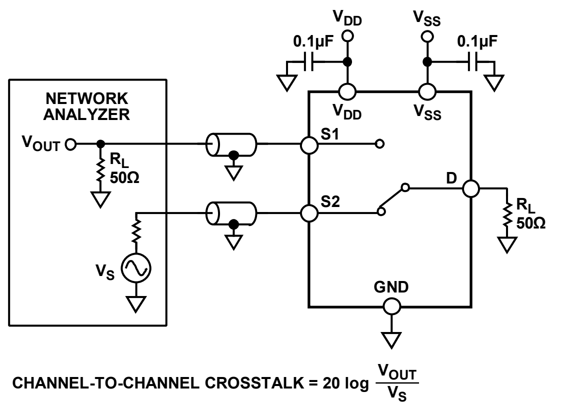

Figure 28. Channel-to-Channel Crosstalk

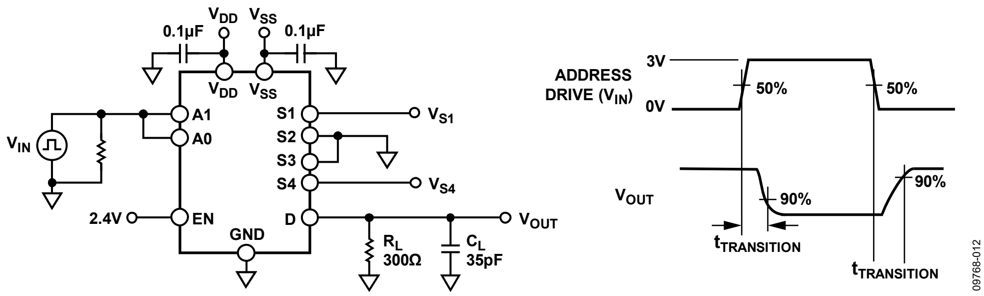

Figure 29. Address to Output Switching Times

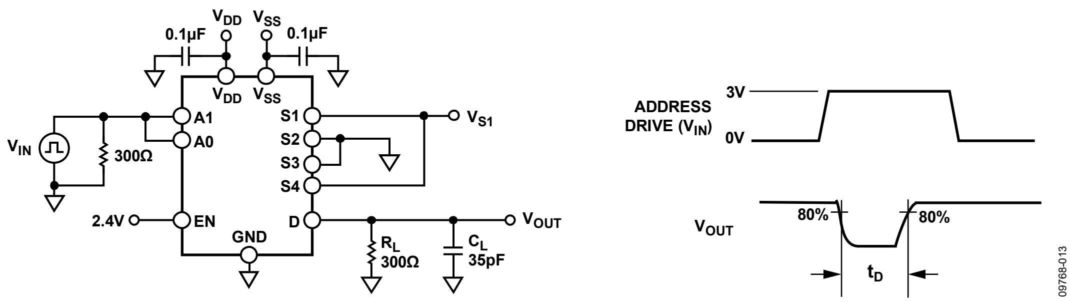

Figure 30. Break-Before-Make Time Delay, t_D

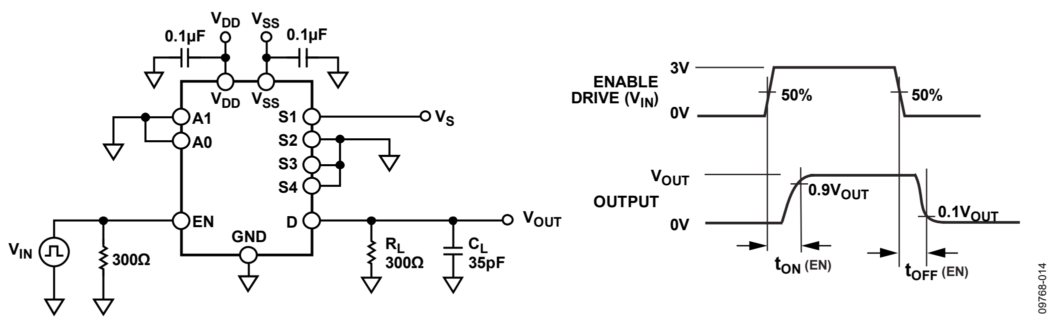

Figure 31. Enable-to-Output Switching Delay

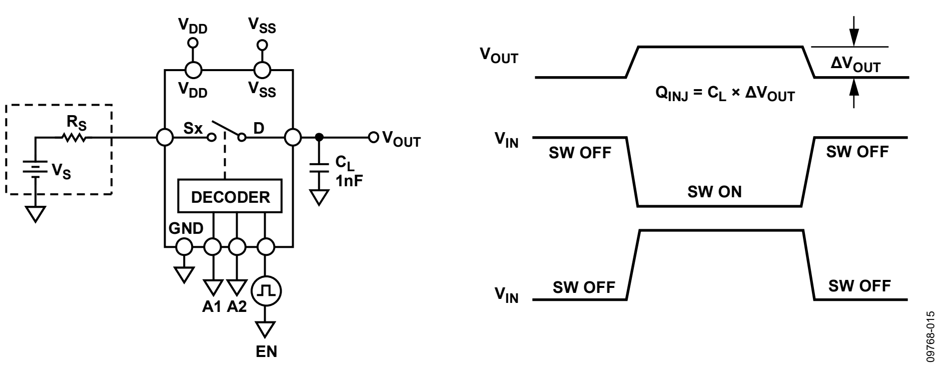

Figure 32. Charge Injection

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D, V_S
The analog voltage on Terminal D and Terminal S.

R_{ON}
The ohmic resistance between Terminal D and Terminal S.

$R_{FLAT(ON)}$
Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL}, I_{INH}
The input current of the digital input.

C_S (Off)
The off switch source capacitance, which is measured with reference to ground.

C_D (Off)
The off switch drain capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
The on switch capacitance, which is measured with reference to ground.

C_{IN}
The digital input capacitance.

$t_{TRANSITION}$
The delay time between the 50% and 90% points of the digital input and switch-on condition when switching from one address state to another.

t_{ON} (EN)
The delay between applying the digital control input and the output switching on. See Figure 31.

t_{OFF} (EN)
The delay between applying the digital control input and the output switching off. See Figure 31.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

ACPSRR (AC Power Supply Rejection Ratio)
The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pins to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

TRENCH ISOLATION

In the ADG5204, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. By using trench isolation, this diode is removed, and the result is a latch-up proof switch.

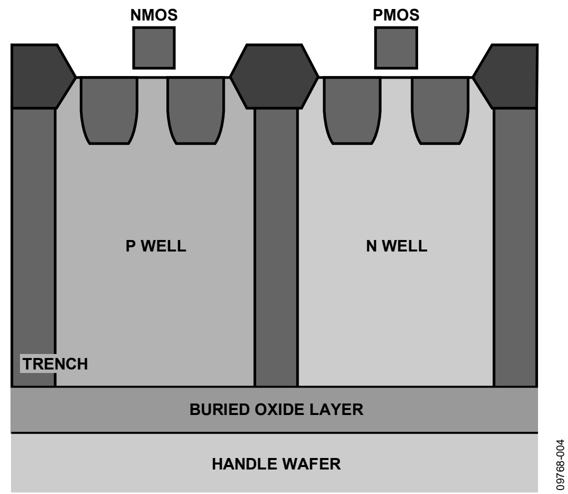

Figure 33. Trench Isolation

APPLICATIONS INFORMATION

The ADG52xx family of switches and multiplexers provide a robust solution for instrumentation, industrial, automotive, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The ADG5204 high voltage multiplexer allows single-supply operation from 9 V to 40 V and dual-supply operation from ±9 V to ±22 V.

OUTLINE DIMENSIONS

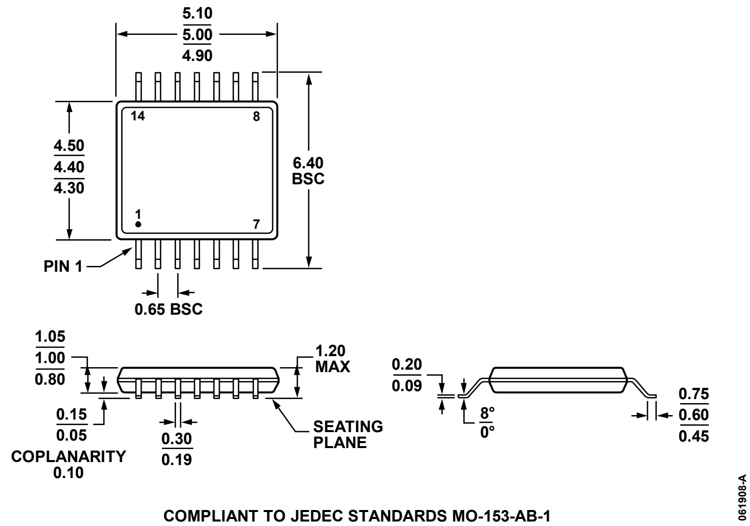

Figure 34. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

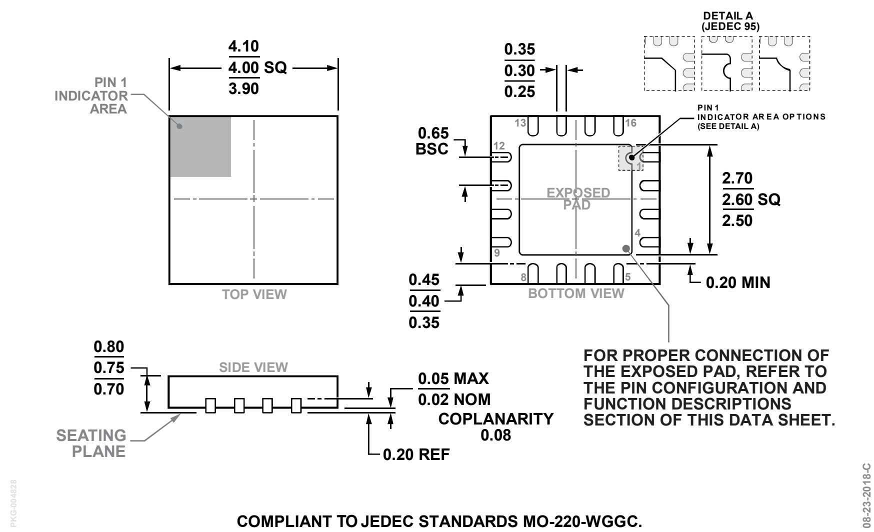

Figure 35. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG5204BRUZ	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG5204BRUZ-RL7	−40°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
ADG5204BCPZ-RL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17

[1] Z = RoHS Compliant Part.

NOTES