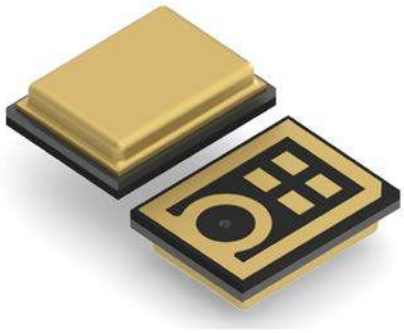
MP34DB02

MEMS audio sensor omnidirectional digital microphone

Datasheet - production data



RHLGA (3 x 4 x 1 mm) 4LD

Features

- Single supply voltage
- Low power consumption
- 120 dBSPL acoustic overload point
- 62.6 dB signal-to-noise ratio
- Omnidirectional sensitivity
- –26 dBFS sensitivity
- PDM single-bit output with option for stereo configuration
- RHLGA package
  - Bottom-port design
  - SMD-compliant
  - EMI-shielded
  - ECOPACK®, RoHS and “Green” compliant

Applications

- Mobile terminals
- Laptop and notebook computers
- Portable media players
- VoIP
- Speech recognition
- A/V eLearning devices
- Gaming and virtual reality input devices
- Digital still and video cameras
- Antitheft systems

Description

The MP34DB02 is an ultra-compact, low-power, omnidirectional, digital MEMS microphone built with a capacitive sensing element and an IC interface with stereo operation capability.

The sensing element, capable of detecting acoustic waves, is manufactured using a specialized silicon micromachining process dedicated to produce audio sensors.

The IC interface is manufactured using a CMOS process that allows designing a dedicated circuit able to provide a digital signal externally in PDM format.

The MP34DB02 has an acoustic overload point of 120 dBSPL with a best-on-the-market 62.6 dB signal-to-noise ratio and -26 dBFS sensitivity.

The MP34DB02 is available in a bottom-port, SMD-compliant, EMI-shielded package and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1: Device summary

Part number	Temp. range [°C]	Package	Packing
MP34DB02TR	-40 to +85	RHLGA 4 LD (3x4x1) mm	Tape and reel

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1 Pin description

Figure 1: Pin connections

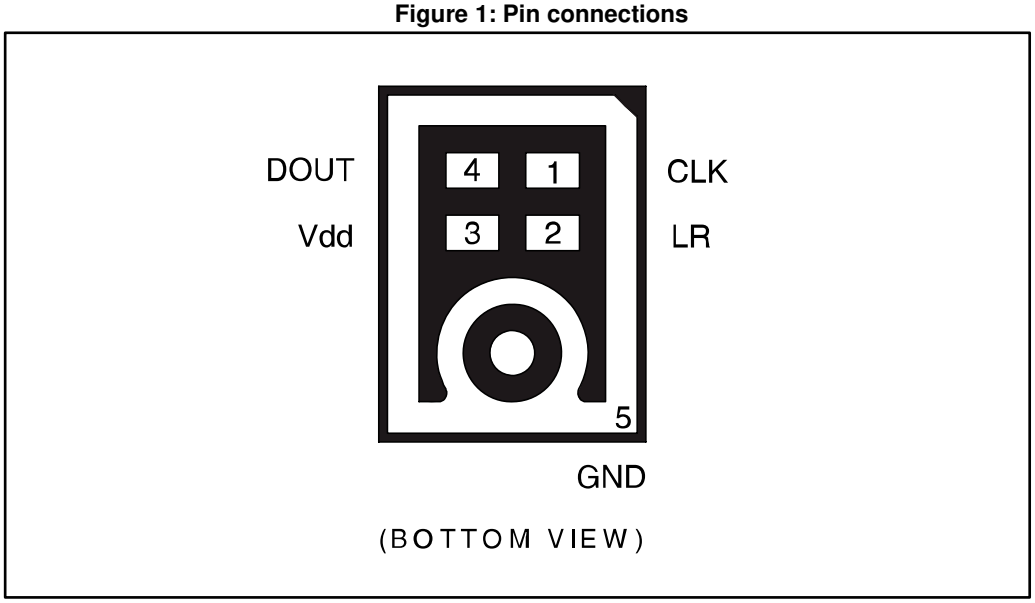


Table 2: Pin description

Pin number	Pin name	Function
1	CLK	Synchronization input clock
2	LR	Left/right channel selection
3	Vdd	Power supply
4	DOUT	Left/right PDM data output
5 (ground ring)	GND	0 V supply

2 Acoustic and electrical specifications

2.1 Acoustic and electrical characteristics

The values listed in the table below are specified for Vdd = 1.8 V, Clock = 2.4 MHz, T = 25 °C, unless otherwise noted.

Table 3: Acoustic and electrical characteristics

Sym.	Parameter	Test condition	Min.	Typ. (1)	Max.	Unit
Vdd	Supply voltage		1.64	1.8	3.6	V
Idd	Current consumption in normal mode	Mean value (2)		0.65		mA
IddPdn	Current consumption in power-down mode (3)			20		µA
Scc	Short-circuit current		1		10	mA
AOP	Acoustic overload point			120		dBSPL
So	Sensitivity	at 1 kHz, 1 Pa	-29	-26	-23	dBFS
SNR	Signal-to-noise ratio	A-weighted at 1 kHz, 1 Pa		62.6		dB
PSR	Power supply rejection	100 mVpp square wave @ 217 Hz, A-weighted		-86		dBFS
Clock	Input clock frequency (4)		1	2.4	3.25	MHz
TWK	Wake-up time (5)	guaranteed by design			10	ms
Top	Operating temperature range		-40		+85	°C

Notes:

(1)Typical specifications are not guaranteed.

(2)No load on DOUT line.

(3)Input clock in static mode.

(4)Duty cycle: min = 40% max = 60%

(5)Time from the first clock edge to valid output data.

Table 4: Distortion specifications

Parameter	Test condition	Value
Distortion	100 dBSPL (50 Hz - 4 kHz)	< 1% THD + N
Distortion	115 dBSPL (1 kHz)	< 5% THD + N

2.2 Timing characteristics

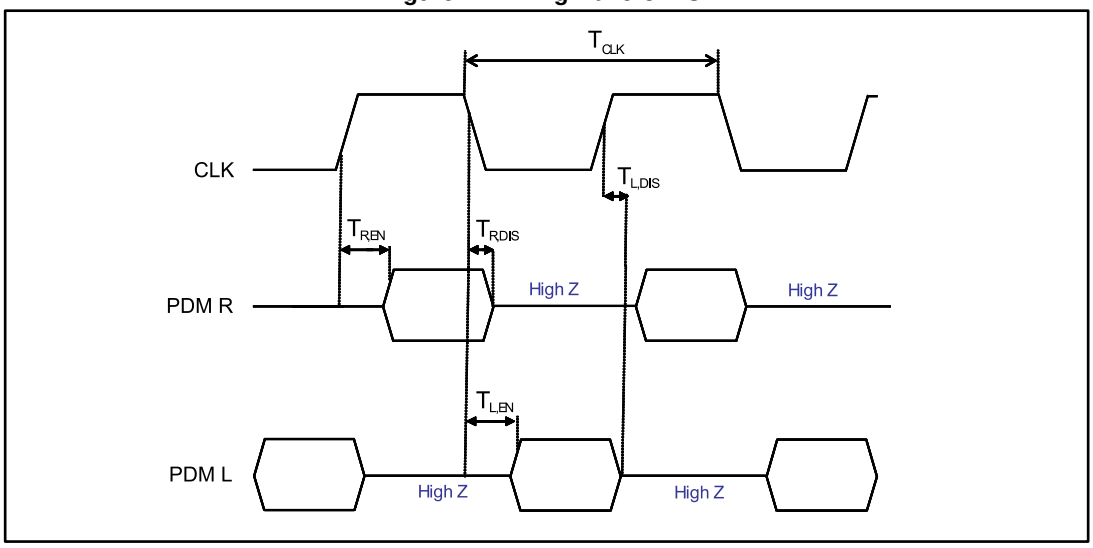
Table 5: Timing characteristics

Parameter	Description	Min	Max	Unit
f_{CLK}	Clock frequency for normal mode	1	3.25	MHz
f_{PD}	Clock frequency for power-down mode		0.23	MHz
T_{CLK}	Clock period for normal mode	308	1000	ns
$T_{R,EN}$	Data enabled on DATA line, L/R pin = 1	18 (1)	30 (1)	ns
$T_{R,DIS}$	Data disabled on DATA line, L/R pin = 1		16 (1)	ns
$T_{L,EN}$	Data enabled on DATA line, L/R pin = 0	18 (1)	30 (1)	ns
$T_{L,DIS}$	Data disabled on DATA line, L/R pin = 0		16 (1)	ns

Notes:

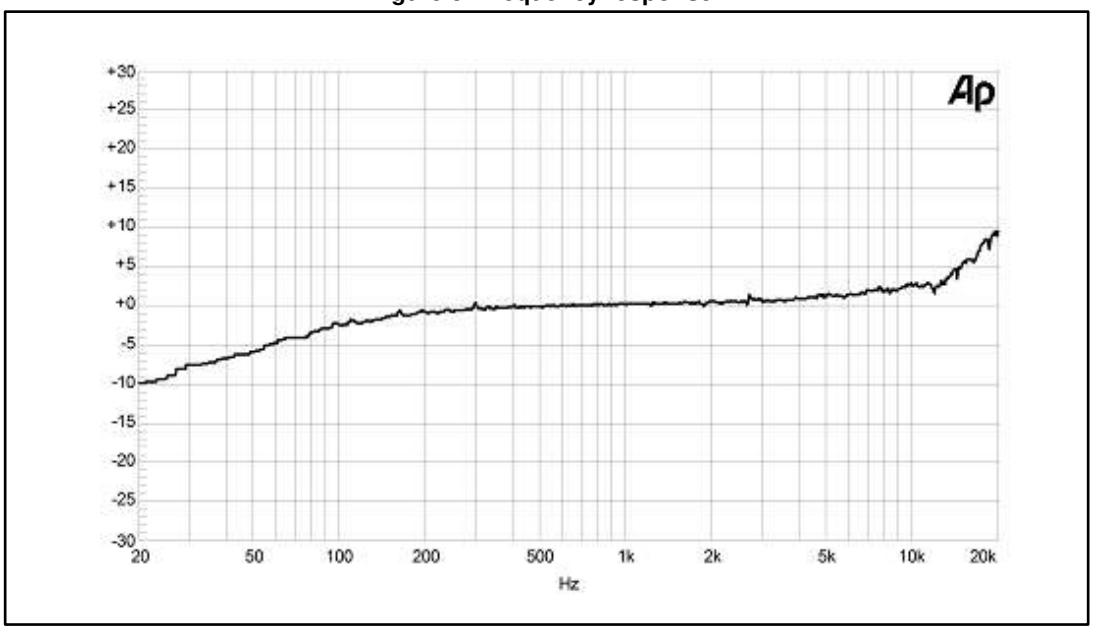
(1) From design simulations

Figure 2: Timing waveforms



2.3 Frequency response

Figure 3: Frequency response



3 Sensing element

The sensing element shall mean the acoustic sensor consisting of a conductive movable plate and a fixed plate placed in a tiny silicon chip. This sensor transduces the sound pressure into the changes of coupled capacity between those two plates.

Omron Corporation supplies this element for STMicroelectronics.

4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6: Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 6	V
Vin	Input voltage on any control pin	-0.3 to Vdd +0.3	V
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

5 Functionality

5.1 L/R channel selection

The L/R digital pad lets the user select the DOUT signal pattern as explained in *Table 7: "L/R channel selection"*. The L/R pin must be connected to Vdd or GND.

Table 7: L/R channel selection

L/R	CLK low	CLK high
GND	Data valid	High impedance
Vdd	High impedance	Data valid

6 Application recommendations

Figure 4: MP34DB02 electrical connections

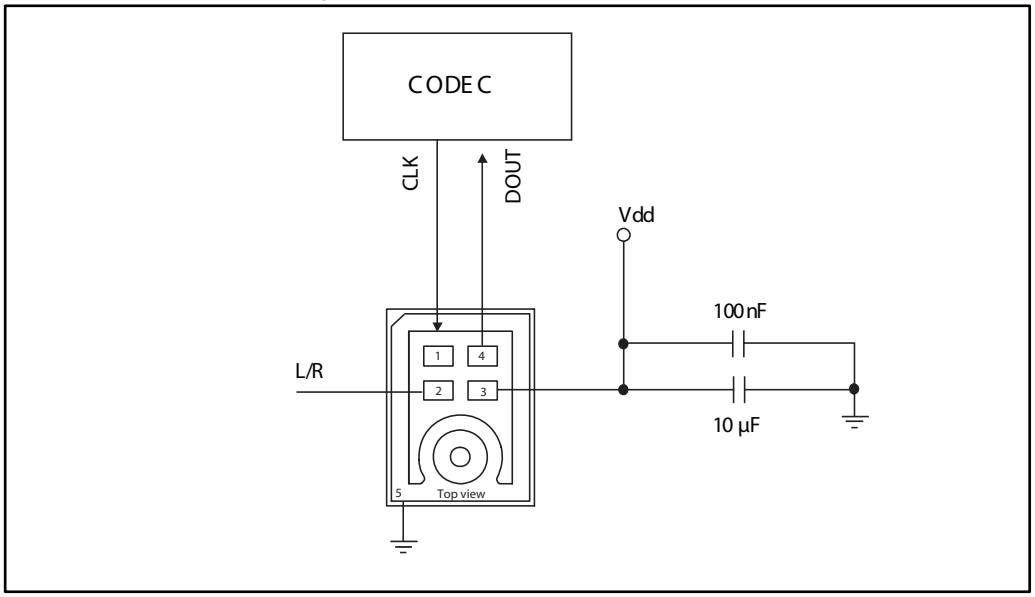
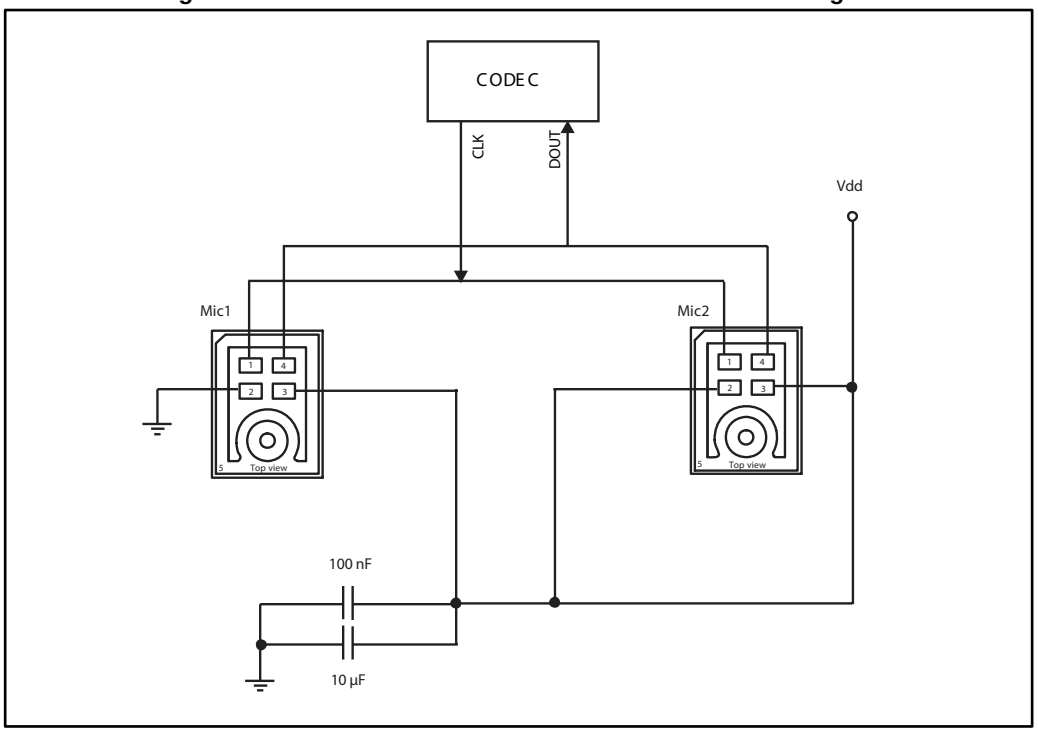


Figure 5: MP34DB02 electrical connections for stereo configuration



Power supply decoupling capacitors (100 nF ceramic, 10 µF ceramic) should be placed as near as possible to pin 3 of the device (common design practice).

The L/R pin must be connected to Vdd or GND (refer to *Table 7: "L/R channel selection"*).

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

7.1 Soldering information

The RHLGA (3 x 4 x 1) mm package is also compliant with the RoHS and “Green” standards and is qualified for soldering heat resistance according to JEDEC J-STD-020.

Landing pattern and soldering recommendations are available at www.st.com.

Figure 6: Recommended soldering profile limits

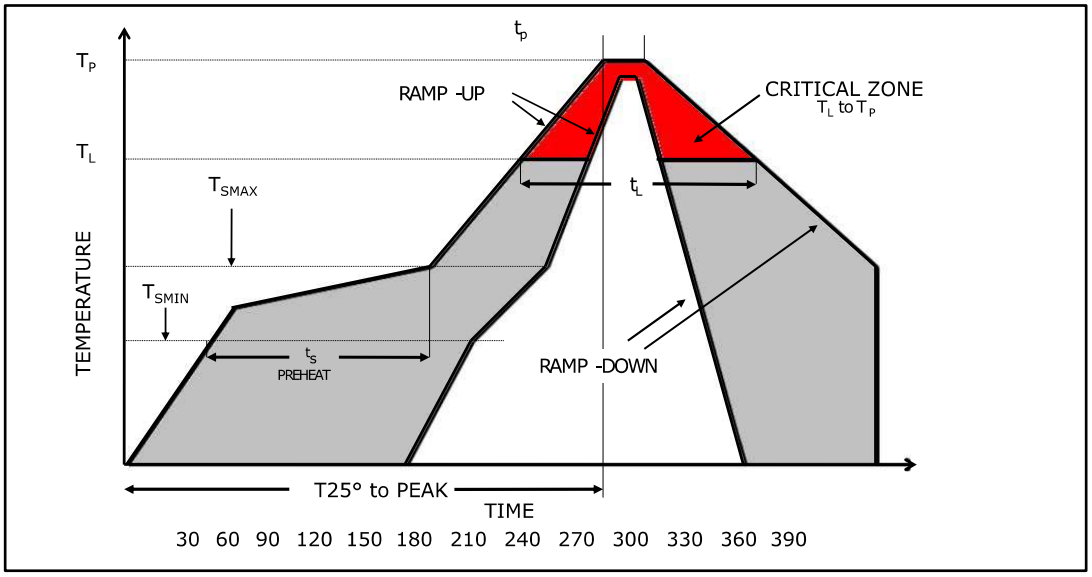


Table 8: Recommended soldering profile limits

Desription	Parameter	Pb free
Average ramp rate	T_L to T_P	3 °C/sec max
Preheat Minimum temperature Maximum temperature Time (T_{SMIN} to T_{SMAX})	 T_{SMIN} T_{SMAX} t_S	 150 °C 200 °C 60 sec to 120 sec
Ramp-up rate	T_{SMAX} to T_L	
Time maintained above liquidus temperature Liquidus temperature	t_L T_L	60 sec to 150 sec 217 °C
Peak temperature	T_P	260 °C max
Time within 5 °C of actual peak temperature		20 sec to 40 sec
Ramp-down rate		6 °C/sec max
Time 25 °C (t25 °C) to peak temperature		8 minutes max

7.2 RHLGA package information

Figure 7: RHLGA 4LD 3x4 mm (metal cap) 0.25 mm port hole package outline

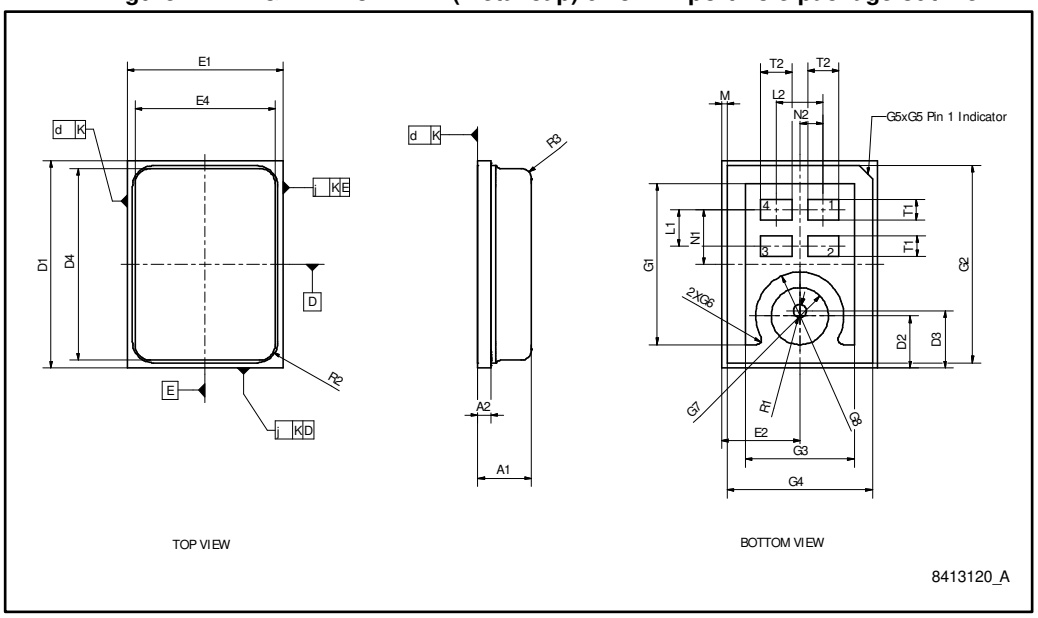


Table 9: RHLGA 4LD 3x4 mm (metal cap) 0.25 mm port hole package mechanical data

Symbol	mm.		
	Min.	Typ.	Max.
A1	0.900	1.000	1.100
A2	0.200	0.250	0.300
D1	3.900	4.000	4.100
D2	0.900	1.000	1.100
D3	1.000	1.100	1.200
D4	3.610	3.700	3.790
R1	0.200	0.250	0.300
R2		0.280	
R3		0.250	
E1	2.900	3.000	3.100
E2	1.300	1.500	1.700
E4	2.610	2.700	2.790
L1	0.650	0.700	0.750
L2	0.850	0.900	0.950
N1	1.000	1.050	1.100
N2	0.400	0.450	0.500
T1	0.350	0.400	0.450
T2	0.550	0.600	0.650
G1	3.050	3.100	3.150
G2	3.750	3.800	3.850
G3	2.050	2.100	2.150

Symbol	mm.		
	Min.	Typ.	Max.
G4	2.750	2.800	2.850
G5	0.250	0.300	0.350
G6	0.050	0.100	0.150
G7	0.500	0.550	0.600
G8	0.800	0.850	0.900
M		0.100	
K		0.050	

8 Revision history

Table 10: Document revision history

Date	Revision	Changes
21-Mar-2014	1	Initial release
28-Apr-2016	2	Updated *Table 1: "Device summary"* Updated PSR in *Table 3: "Acoustic and electrical characteristics"*

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