650 kHz /1.3 MHz Step-Up PWM DC-to-DC Switching Converters

Data Sheet

ADP1612/ADP1613

FEATURES

- Current limit
  - 1.4 A for the ADP1612
  - 2.0 A for the ADP 1613
- Minimum input voltage
  - 1.8 V for the ADP1612
  - 2.5 V for the ADP1613
- Pin-selectable 650 kHz or 1.3 MHz PWM frequency
- Adjustable output voltage up to 20 V
- Adjustable soft start
- Undervoltage lockout
- Thermal shutdown
- 8-lead MSOP
- Supported by ADIsimPower™ design tool
- ADIsimPower downloadable design tools for boost, coupled-SEPIC, and SEPIC Cuk configurations

APPLICATIONS

- TFT LCD bias supplies
- Portable applications
- Industrial/instrumentation equipment

TYPICAL APPLICATION CIRCUIT

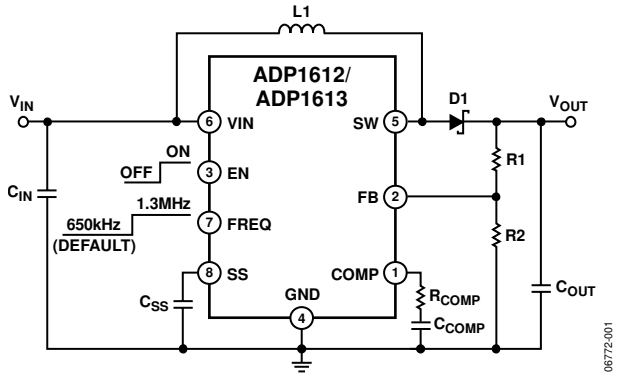

Figure 1. Step-Up Regulator Configuration

GENERAL DESCRIPTION

The ADP1612/ADP1613 are step-up dc-to-dc switching converters with an integrated power switch capable of providing an output voltage as high as 20 V. With a package height of less than 1.1 mm, the ADP1612/ADP1613 are optimal for space-constrained applications such as portable devices or thin film transistor (TFT) liquid crystal displays (LCDs).

The ADP1612/ADP1613 operate in current mode pulse-width modulation (PWM) with up to 94% efficiency. Adjustable soft start prevents inrush currents when the part is enabled. The pin-selectable switching frequency and PWM current-mode architecture allow for excellent transient response, easy noise filtering, and the use of small, cost-saving external inductors and capacitors. Other key features include undervoltage lockout (UVLO), thermal shutdown (TSD), and logic controlled enable.

The ADP1612/ADP1613 are available in the lead-free 8-lead MSOP.

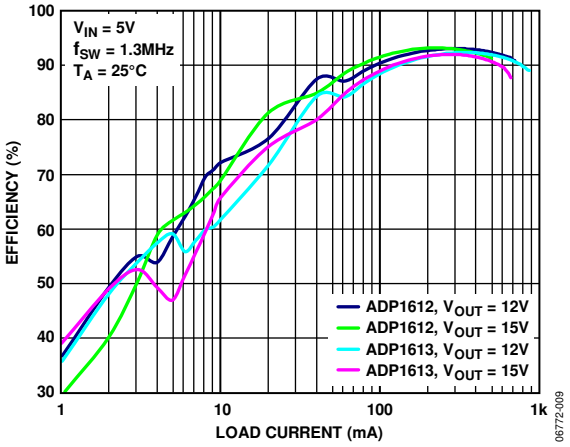

Figure 2. ADP1612/ADP1613 Efficiency for Various Output Voltages

Rev. D

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TABLE OF CONTENTS

REVISION HISTORY

11/12—Rev. C to Rev. D

Changes to Choosing the Input and Output Capacitors Section and Loop Compensation Section ... 14

7/12—Rev. B to Rev. C

Changes to Features Section ... 1
Added ADIsimPower Design Tool Section ... 13
Changes to Ordering Guide ... 25

4/11—Rev. A to Rev. B

Changes to Features Section ... 1
Changes to Reference Feedback Voltage Parameter ... 3
Changes to Ordering Guide ... 25

9/09—Rev. 0 to Rev. A

Changes to Figure 45 ... 17
Changes to Figure 48 and Figure 51 ... 18
Changes to Figure 54 and Figure 57 ... 19
Changes to Figure 60 and Figure 63 ... 20
Changes to Figure 66 and Figure 69 ... 21
Changes to Figure 72 ... 22
Changes to Ordering Guide ... 25

4/09—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3.6 V, unless otherwise noted. Minimum and maximum values are guaranteed for T_J = −40°C to +125°C. Typical values specified are at T_J = 25°C. All limits at temperature extremes are guaranteed by correlation and characterization using standard statistical quality control (SQC), unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY						
Input Voltage	V_{IN}	ADP1612	1.8		5.5	V
		ADP1613	2.5		5.5	V
Quiescent Current						
Nonswitching State	I_Q	V_{FB} = 1.5 V, FREQ = V_{IN}		900	1350	µA
		V_{FB} = 1.5 V, FREQ = GND		700	1300	µA
Shutdown	I_{QSHDN}	V_{EN} = 0 V		0.01	2	µA
Switching State[1]	I_{QSW}	FREQ = V_{IN}, no load		4	5.8	mA
		FREQ = GND, no load		2.2	4	mA
Enable Pin Bias Current	I_{EN}	V_{EN} = 3.6 V		3.3	7	µA
OUTPUT						
Output Voltage	V_{OUT}		V_{IN}		20	V
Load Regulation		I_{LOAD} = 10 mA to 150 mA, V_{IN} = 3.3 V, V_{OUT} = 12 V		0.1		mV/mA
REFERENCE						
Feedback Voltage	V_{FB}		1.215	1.235	1.255	V
Line Regulation		ADP1612, V_{IN} = 1.8 V to 5.5 V; ADP1613, V_{IN} = 2.5 V to 5.5 V		0.07	0.24	%/V
ERROR AMPLIFIER						
Transconductance	G_{MEA}	ΔI = 4 µA		80		µA/V
Voltage Gain	A_V			60		dB
FB Pin Bias Current		V_{FB} = 1.3 V		1	50	nA
SWITCH						
SW On Resistance	R_{DSON}	I_{SW} = 1.0 A		130	300	mΩ
SW Leakage Current		V_{SW} = 20 V		0.01	10	µA
Peak Current Limit[2]	I_{CL}	ADP1612, duty cycle = 70%	0.9	1.4	1.9	A
		ADP1613, duty cycle = 70%	1.3	2.0	2.5	A
OSCILLATOR						
Oscillator Frequency	f_{SW}	FREQ = GND	500	650	720	kHz
		FREQ = V_{IN}	1.1	1.3	1.4	MHz
Maximum Duty Cycle	D_{MAX}	COMP = open, V_{FB} = 1 V, FREQ = V_{IN}	88	90		%
FREQ Pin Current	I_{FREQ}	FREQ = 3.6 V		5	8	µA
EN/FREQ LOGIC THRESHOLD		ADP1612, V_{IN} = 1.8 V to 5.5 V; ADP1613, V_{IN} = 2.5 V to 5.5 V				
Input Voltage Low	V_{IL}				0.3	V
Input Voltage High	V_{IH}		1.6			V
SOFT START						
SS Charging Current	I_{SS}	V_{SS} = 0 V	3.4	5	6.2	µA
SS Voltage	V_{SS}	V_{FB} = 1.3 V		1.2		V
UNDERVOLTAGE LOCKOUT (UVLO)						
Undervoltage Lockout Threshold		ADP1612, V_{IN} rising		1.70		V
		ADP1612, V_{IN} falling		1.62		V
		ADP1613, V_{IN} rising		2.25		V
		ADP1613, V_{IN} falling		2.16		V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Hysteresis				20		°C

[1] This parameter specifies the average current while switching internally and with SW (Pin 5) floating.
[2] Current limit is a function of duty cycle. See the Typical Performance Characteristics section for typical values over operating ranges.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, EN, FB to GND	−0.3 V to +6 V
FREQ to GND	−0.3 V to V_{IN} + 0.3 V
COMP to GND	1.0 V to 1.6 V
SS to GND	−0.3 V to +1.3 V
SW to GND	21 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020
ESD (Electrostatic Discharge)	
Human Body Model	±5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination.

THERMAL RESISTANCE

Junction-to-ambient thermal resistance (θ_{JA}) of the package is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions.

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP			
2-Layer Board[1]	206.9	44.22	°C/W
4-Layer Board[1]	162.2	44.22	°C/W

[1] Thermal numbers per JEDEC standard JESD 51-7.

BOUNDARY CONDITION

Modeled under natural convection cooling at 25°C ambient temperature, JESD 51-7, and 1 W power input with 2- and 4-layer boards.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

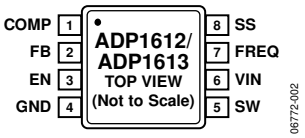


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COMP	Compensation Input. Connect a series resistor-capacitor network from COMP to GND to compensate the regulator.
2	FB	Output Voltage Feedback Input. Connect a resistive voltage divider from the output voltage to FB to set the regulator output voltage.
3	EN	Enable Input. Drive EN low to shut down the regulator; drive EN high to turn on the regulator.
4	GND	Ground.
5	SW	Switching Output. Connect the power inductor from the input voltage to SW and connect the external rectifier from SW to the output voltage to complete the step-up converter.
6	VIN	Main Power Supply Input. VIN powers the ADP1612/ADP1613 internal circuitry. Connect VIN to the input source voltage. Bypass VIN to GND with a 10 µF or greater capacitor as close to the ADP1612/ADP1613 as possible.
7	FREQ	Frequency Setting Input. FREQ controls the switching frequency. Connect FREQ to GND to program the oscillator to 650 kHz, or connect FREQ to VIN to program it to 1.3 MHz. If FREQ is left floating, the part defaults to 650 kHz.
8	SS	Soft Start Timing Capacitor Input. A capacitor connected from SS to GND brings up the output slowly at power-up and reduces inrush current.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{EN} = V_{IN} and T_A = 25°C, unless otherwise noted.

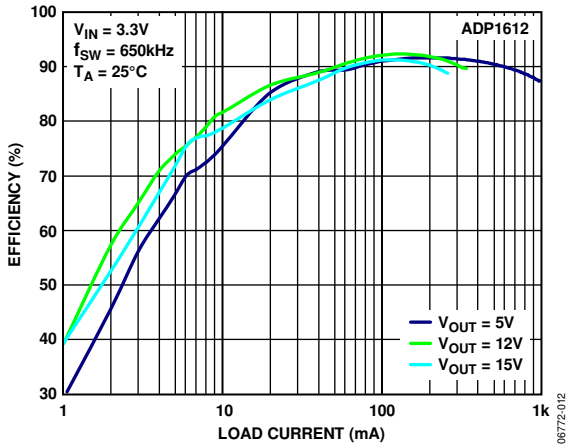


Figure 4. ADP1612 Efficiency vs. Load Current, V_{IN} = 3.3 V, f_{SW} = 650 kHz

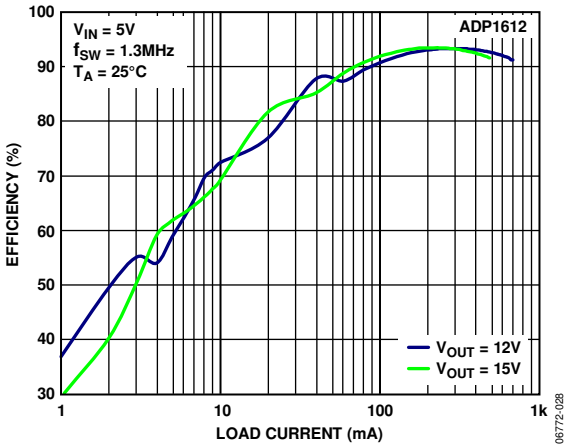


Figure 7. ADP1612 Efficiency vs. Load Current, V_{IN} = 5 V, f_{SW} = 1.3 MHz

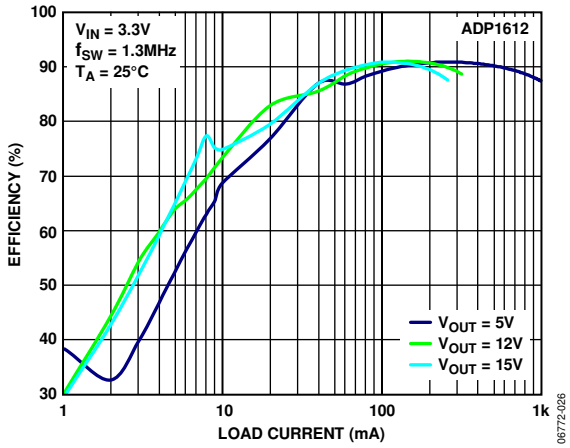


Figure 5. ADP1612 Efficiency vs. Load Current, V_{IN} = 3.3 V, f_{SW} = 1.3 MHz

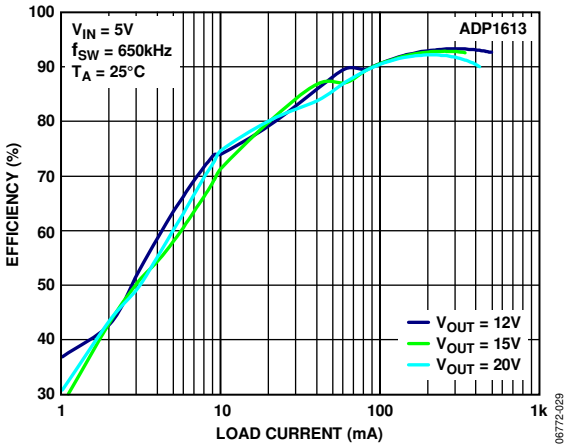


Figure 8. ADP1613 Efficiency vs. Load Current, V_{IN} = 5 V, f_{SW} = 650 kHz

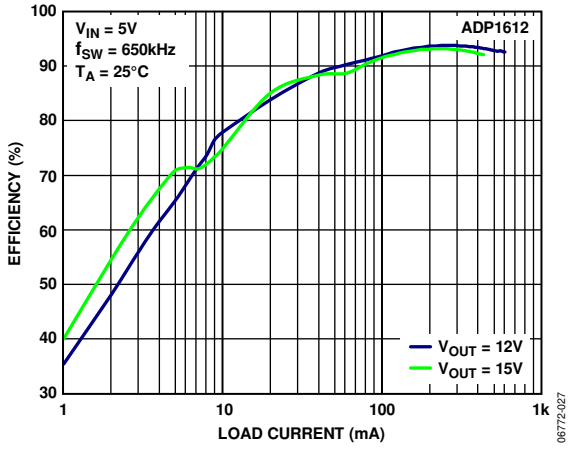


Figure 6. ADP1612 Efficiency vs. Load Current, V_{IN} = 5 V, f_{SW} = 650 kHz

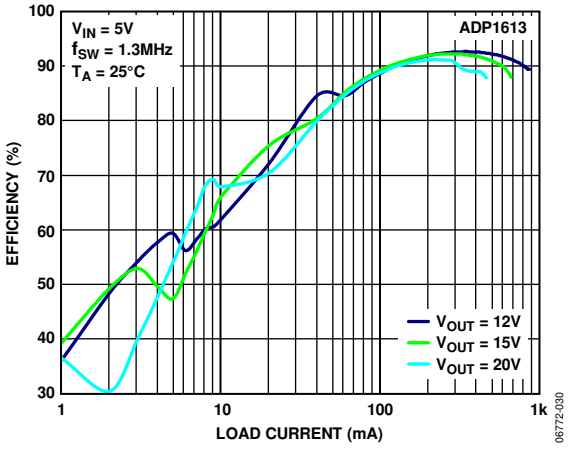


Figure 9. ADP1613 Efficiency vs. Load Current, V_{IN} = 5 V, f_{SW} = 1.3 MHz

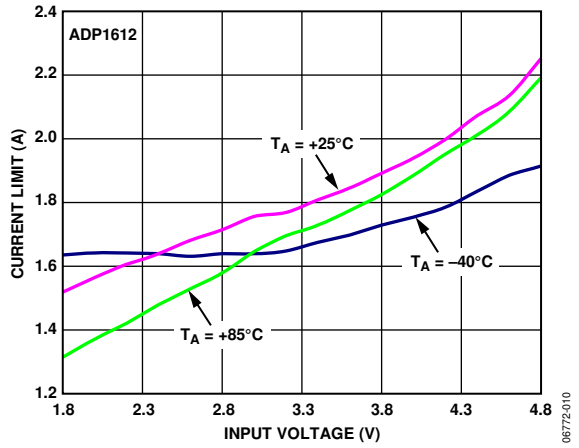


Figure 10. ADP1612 Switch Current Limit vs. Input Voltage, V_{OUT} = 5 V

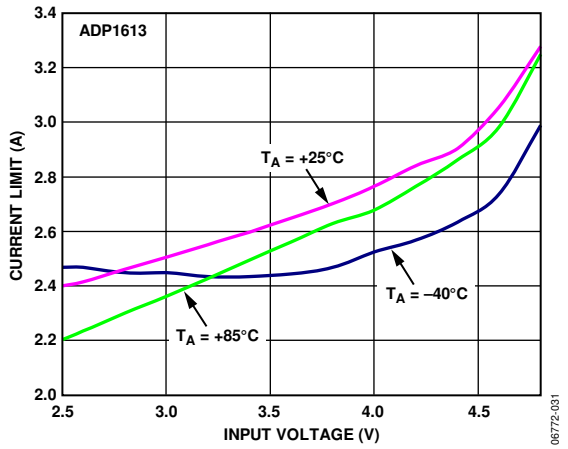


Figure 13. ADP1613 Switch Current Limit vs. Input Voltage, V_{OUT} = 5 V

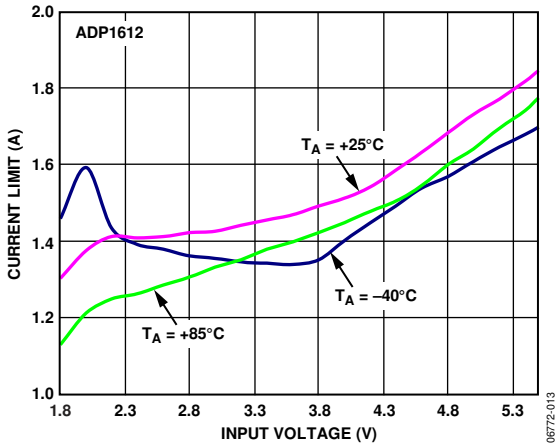


Figure 11. ADP1612 Switch Current Limit vs. Input Voltage, V_{OUT} = 8 V

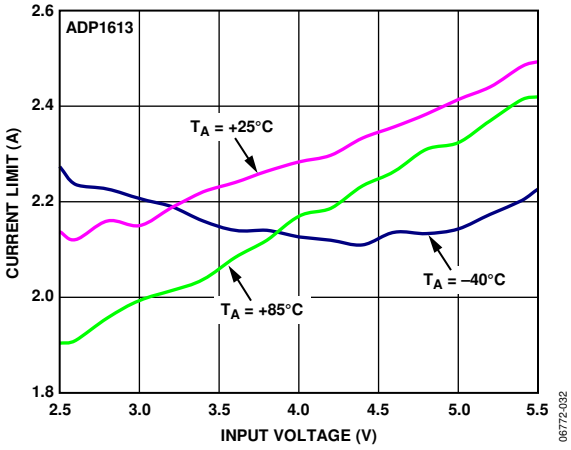


Figure 14. ADP1613 Switch Current Limit vs. Input Voltage, V_{OUT} = 8 V

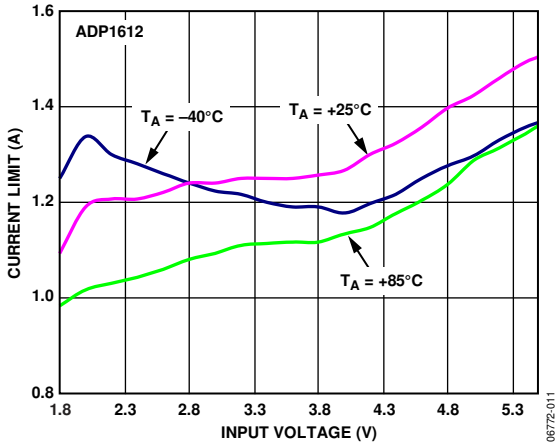


Figure 12. ADP1612 Switch Current Limit vs. Input Voltage, V_{OUT} = 15 V

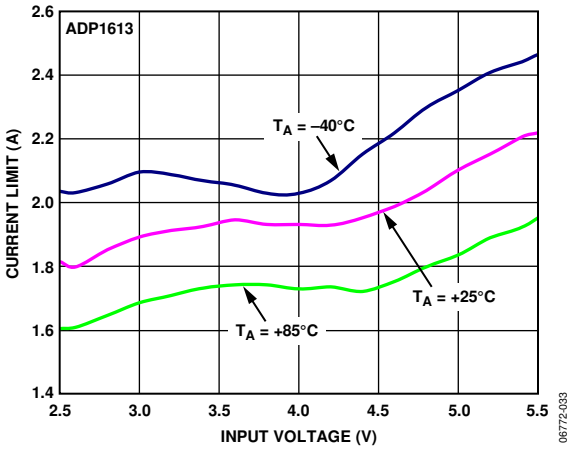


Figure 15. ADP1613 Switch Current Limit vs. Input Voltage, V_{OUT} = 15 V

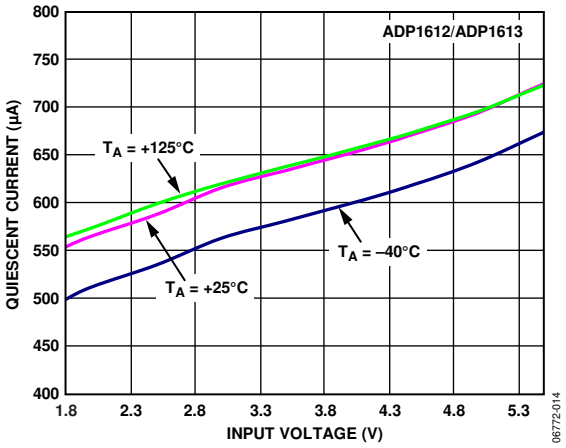


Figure 16. ADP1612/ADP1613 Quiescent Current vs. Input Voltage, Nonswitching, f_{SW} = 650 kHz

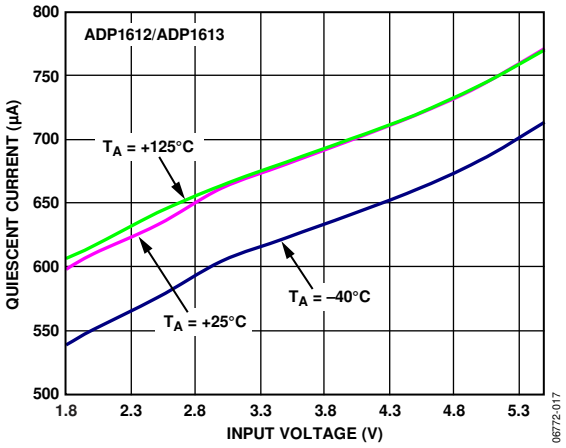


Figure 17. ADP1612/ADP1613 Quiescent Current vs. Input Voltage, Nonswitching, f_{SW} = 1.3 MHz

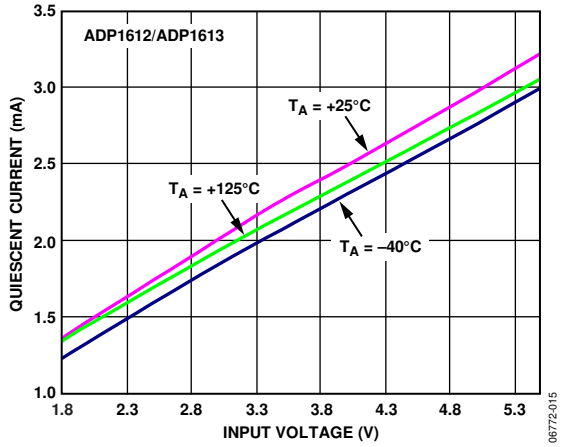


Figure 18. ADP1612/ADP1613 Quiescent Current vs. Input Voltage, Switching, f_{SW} = 650 kHz

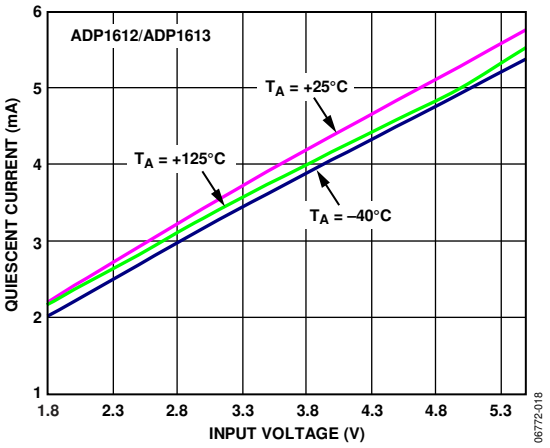


Figure 19. ADP1612/ADP1613 Quiescent Current vs. Input Voltage, Switching, f_{SW} = 1.3 MHz

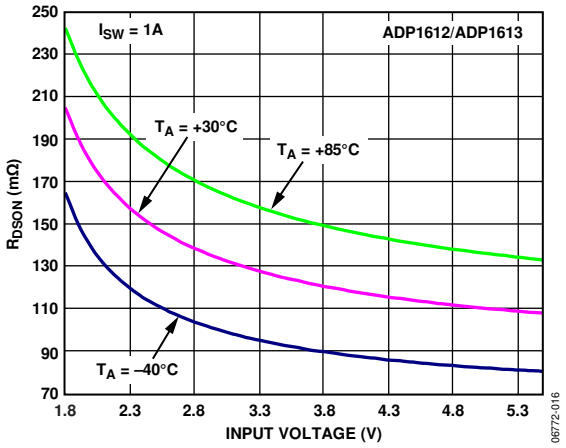


Figure 20. ADP1612/ADP1613 On Resistance vs. Input Voltage

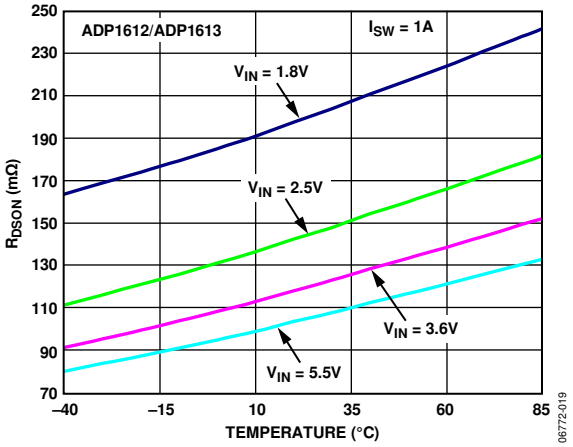


Figure 21. ADP1612/ADP1613 On Resistance vs. Temperature

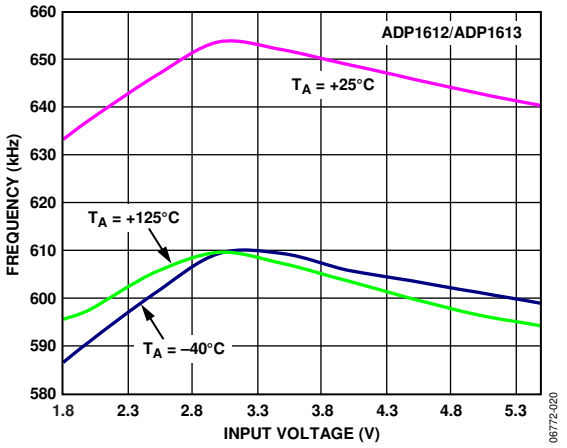


Figure 22. ADP1612/ADP1613 Frequency vs. Input Voltage, f_{SW} = 650 kHz

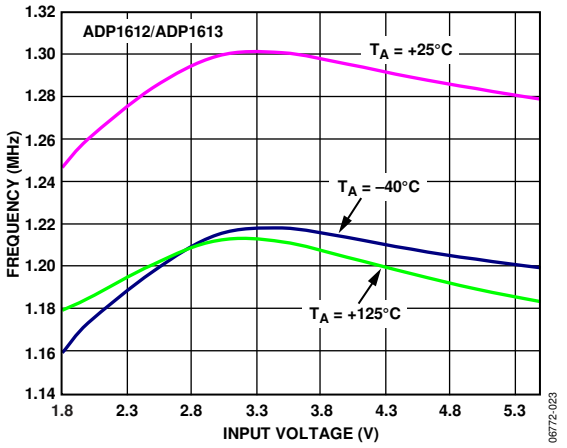


Figure 23. ADP1612/ADP1613 Frequency vs. Input Voltage, f_{SW} = 1.3 MHz

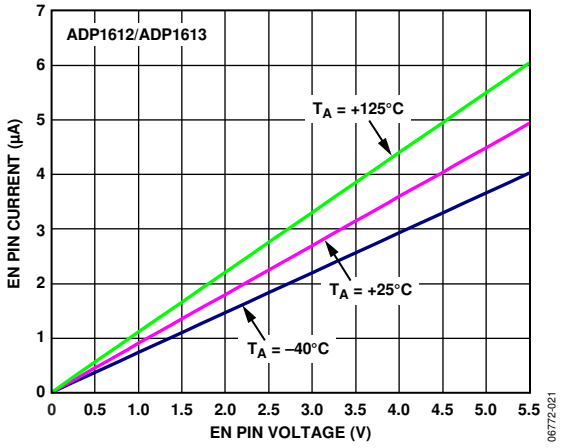


Figure 24. ADP1612/ADP1613 EN Pin Current vs. EN Pin Voltage

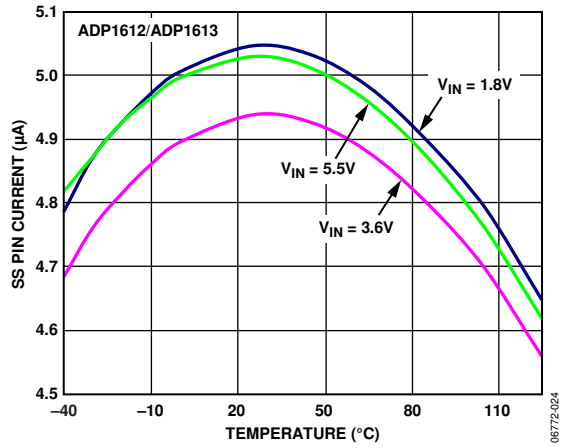


Figure 25. ADP1612/ADP1613 SS Pin Current vs. Temperature

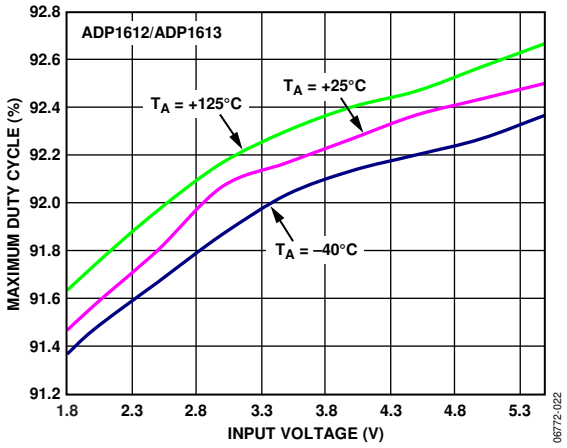


Figure 26. ADP1612/ADP1613 Maximum Duty Cycle vs. Input Voltage, f_{SW} = 650 kHz

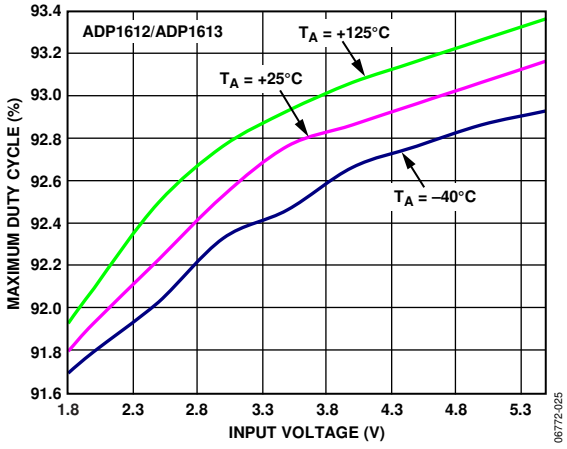


Figure 27. ADP1612/ADP1613 Maximum Duty Cycle vs. Input Voltage, f_{SW} = 1.3 MHz

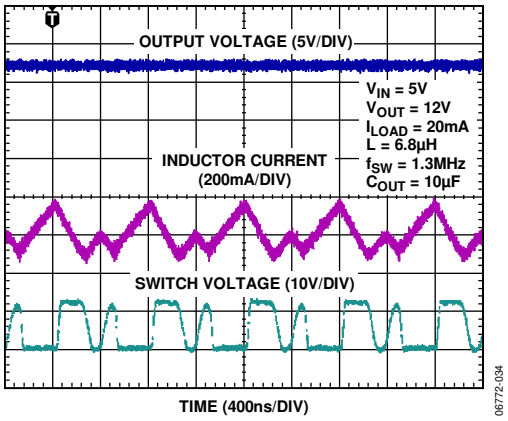


Figure 28. ADP1612/ADP1613 Switching Waveform in Discontinuous Conduction Mode

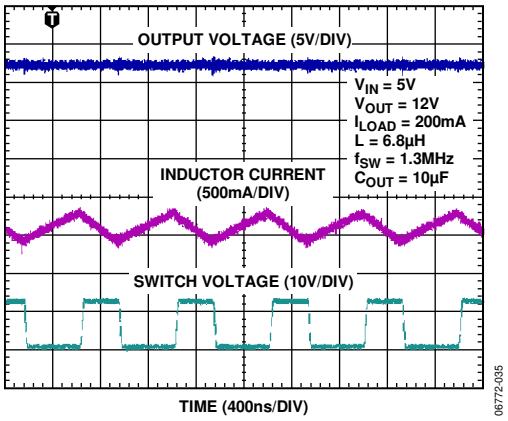


Figure 29. ADP1612/ADP1613 Switching Waveform in Continuous Conduction Mode

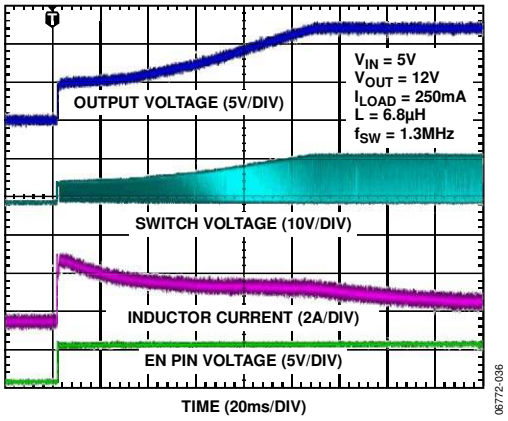


Figure 30. ADP1612/ADP1613 Start-Up from V_{IN}, C_{SS} =33 nF

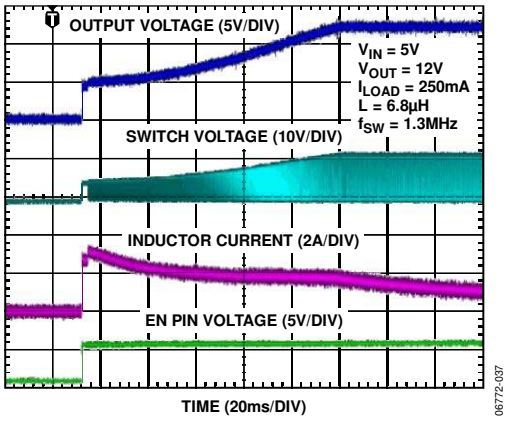


Figure 31. ADP1612/ADP1613 Start-Up from V_{IN}, C_{SS} =100 nF

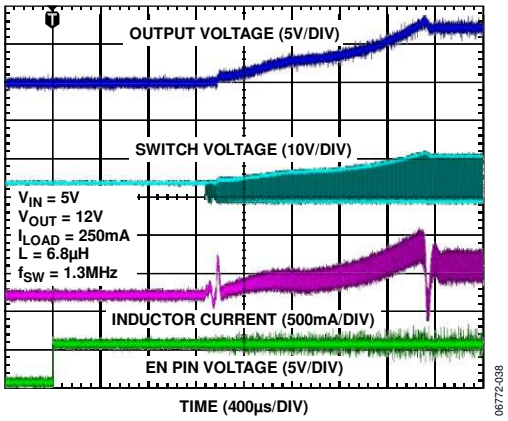


Figure 32. ADP1612/ADP1613 Start-Up from Shutdown, C_{SS} = 33 nF

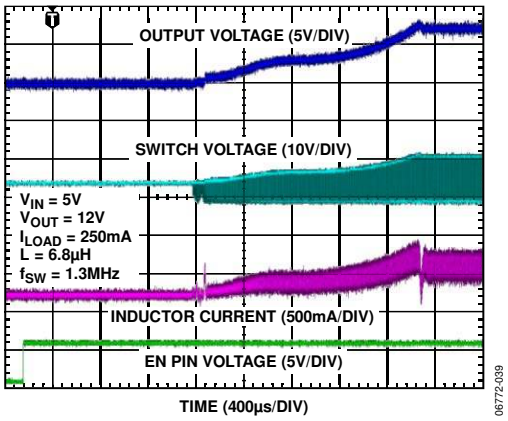


Figure 33. ADP1612/ADP1613 Start-Up from Shutdown, C_{SS} = 100 nF

THEORY OF OPERATION

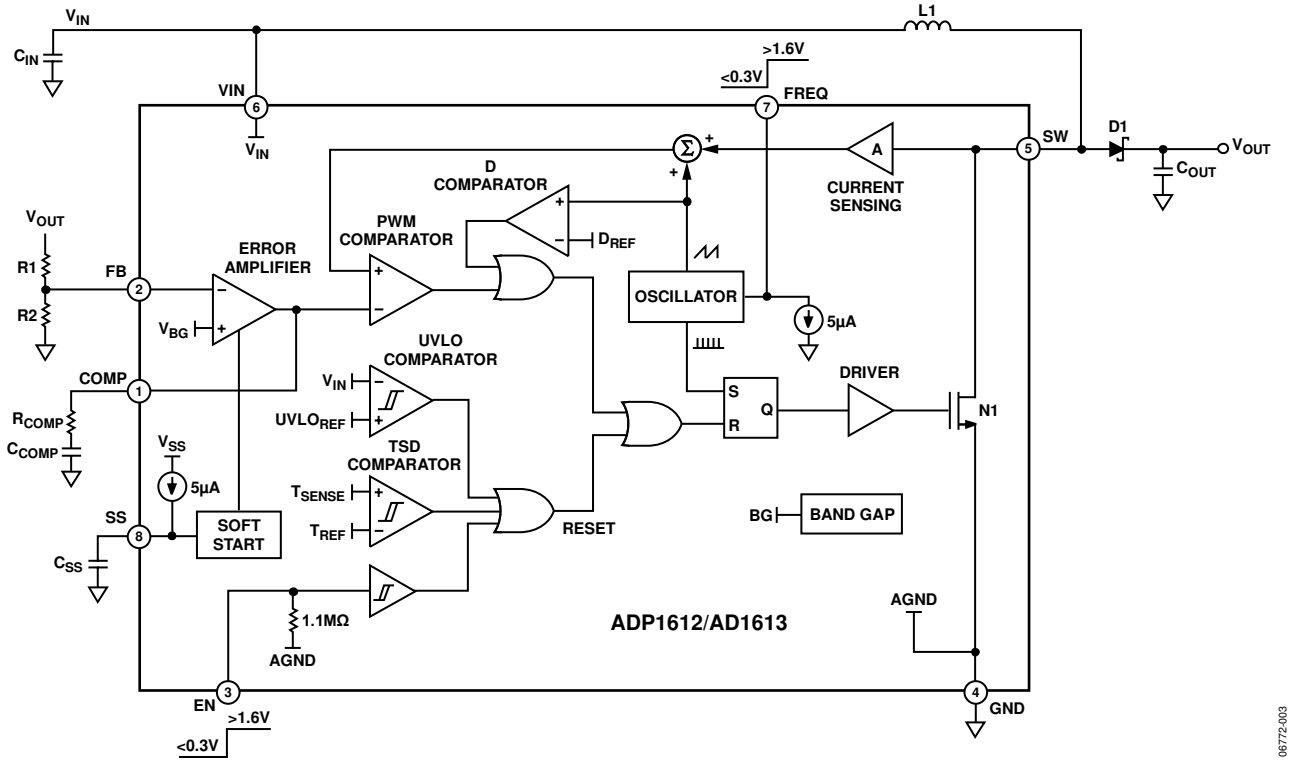


Figure 34. Block Diagram with Step-Up Regulator Application Circuit

The ADP1612/ADP1613 current-mode step-up switching converters boost a 1.8 V to 5.5 V input voltage to an output voltage as high as 20 V. The internal switch allows a high output current, and the high 650 kHz/1.3 MHz switching frequency allows for the use of tiny external components. The switch current is monitored on a pulse-by-pulse basis to limit it to 1.4 A typical (ADP1612) or 2.0 A typical (ADP1613).

CURRENT-MODE PWM OPERATION

The ADP1612/ADP1613 utilize a current-mode PWM control scheme to regulate the output voltage over all load conditions. The output voltage is monitored at FB through a resistive voltage divider. The voltage at FB is compared to the internal 1.235 V reference by the internal transconductance error amplifier to create an error voltage at COMP. The switch current is internally measured and added to the stabilizing ramp. The resulting sum is compared to the error voltage at COMP to control the PWM modulator. This current-mode regulation system allows fast transient response, while maintaining a stable output voltage. By selecting the proper resistor-capacitor network from COMP to GND, the regulator response is optimized for a wide range of input voltages, output voltages, and load conditions.

FREQUENCY SELECTION

The frequency of the ADP1612/ADP1613 is pin-selectable to operate at either 650 kHz to optimize the regulator for high efficiency or at 1.3 MHz for use with small external components. If FREQ is left floating, the part defaults to 650 kHz. Connect FREQ to GND for 650 kHz operation or connect FREQ to VIN for 1.3 MHz operation. When connected to VIN for 1.3 MHz operation, an additional 5 µA, typical, of quiescent current is active. This current is turned off when the part is shutdown.

SOFT START

To prevent input inrush current to the converter when the part is enabled, connect a capacitor from SS to GND to set the soft start period. Once the ADP1612/ADP1613 are turned on, SS sources 5 µA, typical, to the soft start capacitor (C_{SS}) until it reaches 1.2 V at startup. As the soft start capacitor charges, it limits the peak current allowed by the part. By slowly charging the soft start capacitor, the input current ramps slowly to prevent it from overshooting excessively at startup. When the ADP1612/ADP1613 are in shutdown mode (EN ≤ 0.3 V), a thermal shutdown event occurs, or the input voltage is below the falling undervoltage lockout voltage, SS is internally shorted to GND to discharge the soft start capacitor.

THERMAL SHUTDOWN (TSD)

The ADP1612/ADP1613 include TSD protection. If the die temperature exceeds 150°C (typical), TSD turns off the NMOS power device, significantly reducing power dissipation in the device and preventing output voltage regulation. The NMOS power device remains off until the die temperature reduces to 130°C (typical). The soft start capacitor is discharged during TSD to ensure low output voltage overshoot and inrush currents when regulation resumes.

UNDERVOLTAGE LOCKOUT (UVLO)

If the input voltage is below the UVLO threshold, the ADP1612/ADP1613 automatically turn off the power switch and place the part into a low power consumption mode. This prevents potentially erratic operation at low input voltages and prevents the power device from turning on when the control circuitry cannot operate it. The UVLO levels have ~100 mV of hysteresis to ensure glitch free startup.

ENABLE/SHUTDOWN CONTROL

The EN input turns the ADP1612/ADP1613 regulator on or off. Drive EN low to turn off the regulator and reduce the input current to 0.01 μA, typical. Drive EN high to turn on the regulator.

When the step-up dc-to-dc switching converter is in shutdown mode (EN ≤ 0.3 V), there is a dc path from the input to the output through the inductor and output rectifier. This causes the output voltage to remain slightly below the input voltage by the forward voltage of the rectifier, preventing the output voltage from dropping to ground when the regulator is shutdown. Figure 37 provides a circuit modification to disconnect the output voltage from the input voltage at shutdown.

Regardless of the state of the EN pin, when a voltage is applied to VIN of the ADP1612/ADP1613, a large current spike occurs due to the nonisolated path through the inductor and diode between V_{IN} and V_{OUT}. The high current is a result of the output capacitor charging. The peak value is dependent on the inductor, output capacitor, and any load active on the output of the regulator.

APPLICATIONS INFORMATION

ADIsimPower DESIGN TOOL

The ADP1612/ADP1613 are supported by ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can also request an unpopulated board through the tool.

SETTING THE OUTPUT VOLTAGE

The ADP1612/ADP1613 feature an adjustable output voltage range of V_{IN} to 20 V. The output voltage is set by the resistor voltage divider, R1 and R2, (see Figure 34) from the output voltage (V_{OUT}) to the 1.235 V feedback input at FB. Use the following equation to determine the output voltage:

$$V_{OUT} = 1.235 \times (1 + R1/R2) \quad (1)$$

Choose R1 based on the following equation:

$$R1 = R2 \times \left(\frac{V_{OUT} - 1.235}{1.235} \right) \quad (2)$$

INDUCTOR SELECTION

The inductor is an essential part of the step-up switching converter. It stores energy during the on time of the power switch, and transfers that energy to the output through the output rectifier during the off time. To balance the tradeoffs between small inductor current ripple and efficiency, inductance values in the range of 4.7 µH to 22 µH are recommended. In general, lower inductance values have higher saturation current and lower series resistance for a given physical size. However, lower inductance results in a higher peak current that can lead to reduced efficiency and greater input and/or output ripple and noise. A peak-to-peak inductor ripple current close to 30% of the maximum dc input current typically yields an optimal compromise.

For determining the inductor ripple current in continuous operation, the input (V_{IN}) and output (V_{OUT}) voltages determine the switch duty cycle (D) by the following equation:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (3)$$

Using the duty cycle and switching frequency, f_{SW}, determine the on time by the following equation:

$$t_{ON} = \frac{D}{f_{SW}} \quad (4)$$

The inductor ripple current (ΔI_L) in steady state is calculated by

$$\Delta I_L = \frac{V_{IN} \times t_{ON}}{L} \quad (5)$$

Solve for the inductance value (L) by the following equation:

$$L = \frac{V_{IN} \times t_{ON}}{\Delta I_L} \quad (6)$$

Ensure that the peak inductor current (the maximum input current plus half the inductor ripple current) is below the rated saturation current of the inductor. Likewise, make sure that the maximum rated rms current of the inductor is greater than the maximum dc input current to the regulator.

For CCM duty cycles greater than 50% that occur with input voltages less than one-half the output voltage, slope compensation is required to maintain stability of the current-mode regulator. For stable current-mode operation, ensure that the selected inductance is equal to or greater than the minimum calculated inductance, L_{MIN}, for the application parameters in the following equation:

$$L > L_{MIN} = \frac{(V_{OUT} - 2 \times V_{IN})}{2.7 \times f_{SW}} \quad (7)$$

Inductors smaller than the 4.7 µH to 22 µH recommended range can be used as long as Equation 7 is satisfied for the given application. For input/output combinations that approach the 90% maximum duty cycle, doubling the inductor is recommended to ensure stable operation. Table 5 suggests a series of inductors for use with the ADP1612/ADP1613.

Table 5. Suggested Inductors

Manufacturer	Part Series	Dimensions L × W × H (mm)
Sumida	CMD4D11	5.8 × 4.4 × 1.2
	CDRH4D28CNP	5.1 × 5.1 × 3.0
	CDRH5D18NP	6.0 × 6.0 × 2.0
	CDRH6D26HPNP	7.0 × 7.0 × 2.8
Coilcraft	DO3308P	12.95 × 9.4 × 3.0
	DO3316P	12.95 × 9.4 × 5.21
Toko	D52LC	5.2 × 5.2 × 2.0
	D62LCB	6.2 × 6.3 × 2.0
	D63LCB	6.2 × 6.3 × 3.5
Würth Elektronik	WE-TPC	Assorted
	WE-PD, PD2, PD3, PD4	Assorted

CHOOSING THE INPUT AND OUTPUT CAPACITORS

The ADP1612/ADP1613 require input and output bypass capacitors to supply transient currents while maintaining constant input and output voltages. Use a low equivalent series resistance (ESR), 10 µF or greater input capacitor to prevent noise at the ADP1612/ADP1613 input. Place the capacitor between VIN and GND as close to the ADP1612/ADP1613 as possible. Ceramic capacitors are preferred because of their low ESR characteristics. Alternatively, use a high value, medium ESR capacitor in parallel with a 0.1 µF low ESR capacitor as close to the ADP1612/ADP1613 as possible.

The output capacitor maintains the output voltage and supplies current to the load while the ADP1612/ADP1613 switch is on. The value and characteristics of the output capacitor greatly affect the output voltage ripple and stability of the regulator. A low ESR ceramic dielectric capacitor is preferred. The output voltage ripple (ΔV_{OUT}) is calculated as follows:

$$\Delta V_{OUT} = \frac{Q_C}{C_{OUT}} = \frac{I_{OUT} \times t_{ON}}{C_{OUT}} \quad (8)$$

where:
Q_C is the charge removed from the capacitor.
t_{ON} is the on time of the switch.
C_{OUT} is the output capacitance.
I_{OUT} is the output load current.

$$t_{ON} = \frac{D}{f_{SW}} \quad (9)$$

and

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (10)$$

Choose the output capacitor based on the following equation:

$$C_{OUT} \geq \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times \Delta V_{OUT}} \quad (11)$$

Multilayer ceramic capacitors are recommended for this application.

DIODE SELECTION

The output rectifier conducts the inductor current to the output capacitor and load while the switch is off. For high efficiency, minimize the forward voltage drop of the diode. For this reason, Schottky rectifiers are recommended. However, for high voltage, high temperature applications, where the Schottky rectifier reverse leakage current becomes significant and can degrade efficiency, use an ultrafast junction diode.

Ensure that the diode is rated to handle the average output load current. Many diode manufacturers derate the current capability of the diode as a function of the duty cycle. Verify that the output diode is rated to handle the average output load current with the minimum duty cycle. The minimum duty cycle of the ADP1612/ADP1613 is

$$D_{MIN} = \frac{V_{OUT} - V_{IN(MAX)}}{V_{OUT}} \quad (12)$$

where $V_{IN(MAX)}$ is the maximum input voltage.

The following are suggested Schottky diode manufacturers:

- ON Semiconductor
- Diodes, Inc.

LOOP COMPENSATION

The ADP1612/ADP1613 use external components to compensate the regulator loop, allowing optimization of the loop dynamics for a given application.

The step-up converter produces an undesirable right-half plane zero in the regulation feedback loop. This requires compensating the regulator such that the crossover frequency occurs well below the frequency of the right-half plane zero. The right-half plane zero is determined by the following equation:

$$F_Z(RHP) = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{R_{LOAD}}{2\pi \times L} \quad (13)$$

where:
$F_Z(RHP)$ is the right-half plane zero.
R_{LOAD} is the equivalent load resistance or the output voltage divided by the load current.

To stabilize the regulator, ensure that the regulator crossover frequency is less than or equal to one-fifth of the right-half plane zero.

The regulator loop gain is

$$A_{VL} = \frac{V_{FB}}{V_{OUT}} \times \frac{V_{IN}}{V_{OUT}} \times G_{MEA} \times \left|R_{OUT} \parallel Z_{COMP}\right| \times G_{CS} \times \left|Z_{OUT}\right| \quad (14)$$

where:
A_{VL} is the loop gain.
V_{FB} is the feedback regulation voltage, 1.235 V.
V_{OUT} is the regulated output voltage.
V_{IN} is the input voltage.
G_{MEA} is the error amplifier transconductance gain.
R_{OUT} is 125 MΩ.
Z_{COMP} is the impedance of the series RC network from COMP to GND.
G_{CS} is the current sense transconductance gain (the inductor current divided by the voltage at COMP), which is internally set by the ADP1612/ADP1613.
Z_{OUT} is the impedance of the load in parallel with the output capacitor.

To determine the crossover frequency, it is important to note that, at that frequency, the compensation impedance (Z_{COMP}) is dominated by a resistor, and the output impedance (Z_{OUT}) is dominated by the impedance of an output capacitor. Therefore, when solving for the crossover frequency, the equation (by definition of the crossover frequency) is simplified to

$$\left|A_{VL}\right| = \frac{V_{FB}}{V_{OUT}} \times \frac{V_{IN}}{V_{OUT}} \times G_{MEA} \times R_{COMP} \times G_{CS} \times \frac{1}{2\pi \times f_C \times C_{OUT}} = 1 \quad (15)$$

where:
f_C is the crossover frequency.
R_{COMP} is the compensation resistor.

Solve for R_{COMP},

$$R_{COMP} = \frac{2\pi \times f_C \times C_{OUT} \times (V_{OUT})^2}{V_{FB} \times V_{IN} \times G_{MEA} \times G_{CS}} \quad (16)$$

where:
V_{FB} = 1.235 V.
G_{MEA} = 80 µA/V.
G_{CS} = 13.4 A/V.

$$R_{COMP} = \frac{4746 \times f_C \times C_{OUT} \times (V_{OUT})^2}{V_{IN}} \quad (17)$$

Once the compensation resistor is known, set the zero formed by the compensation capacitor and resistor to one-fourth of the crossover frequency, or

$$C_{COMP} = \frac{2}{\pi \times f_C \times R_{COMP}} \quad (18)$$

where C_{COMP} is the compensation capacitor.

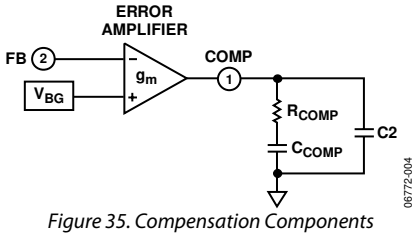


Figure 35. Compensation Components

The capacitor, C2, is chosen to cancel the zero introduced by output capacitance, ESR.

Solve for C2 as follows:

$$C2 = \frac{ESR \times C_{OUT}}{R_{COMP}} \quad (19)$$

For low ESR output capacitance such as with a ceramic capacitor, C2 is optional. For optimal transient performance, R_{COMP} and C_{COMP} might need to be adjusted by observing the load transient response of the ADP1612/ADP1613. For most applications, the compensation resistor should be within the range of 4.7 kΩ to 100 kΩ and the compensation capacitor should be within the range of 100 pF to 3.3 nF.

SOFT START CAPACITOR

Upon startup (EN ≥ 1.6 V), the voltage at SS ramps up slowly by charging the soft start capacitor (C_{SS}) with an internal 5 µA current source (I_{SS}). As the soft start capacitor charges, it limits the peak current allowed by the part to prevent excessive overshoot at startup. The necessary soft start capacitor, C_{SS}, for a specific overshoot and start-up time can be calculated for the maximum load condition when the part is at current limit by:

$$C_{SS} = I_{SS} \frac{\Delta t}{V_{SS}} \quad (20)$$

where:
I_{SS} = 5 µA (typical).
V_{SS} = 1.2 V.
Δt = startup time, at current limit.

If the applied load does not place the part at current limit, the necessary C_{SS} will be smaller. A 33 nF soft start capacitor results in negligible input current overshoot at start up, and therefore is suitable for most applications. However, if an unusually large output capacitor is used, a longer soft start period is required to prevent input inrush current.

Conversely, if fast startup is a requirement, the soft start capacitor can be reduced or removed, allowing the ADP1612/ADP1613 to start quickly, but allowing greater peak switch current.

TYPICAL APPLICATION CIRCUITS

Both the ADP1612 and ADP1613 can be used in the application circuits in this section.

The ADP1612 is geared toward applications requiring input voltages as low as 1.8 V, where the ADP1613 is more suited for applications needing the output power capabilities of a 2.0 A switch. The primary differences are shown in Table 6.

Table 6. ADP1612/ADP1613 Differences

Parameter	ADP1612	ADP1613
Current Limit	1.4 A	2.0 A
Input Voltage Range	1.8 V to 5.5 V	2.5 V to 5.5 V

The Step-Up Regulator Circuit Examples section recommends component values for several common input, output, and load conditions. The equations in the Applications Information section can be used to select components for alternate configurations.

STEP-UP REGULATOR

The circuit in Figure 36 shows the ADP1612/ADP1613 in a basic step-up configuration.

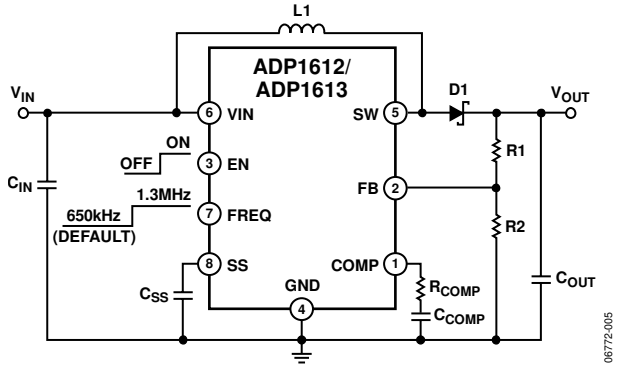


Figure 36. Step-Up Regulator

The modified step-up circuit in Figure 37 incorporates true shutdown capability advantageous for battery-powered applications requiring low standby current. Driving the EN pin below 0.3 V shuts down the ADP1612/ADP1613 and completely disconnects the input from the output.

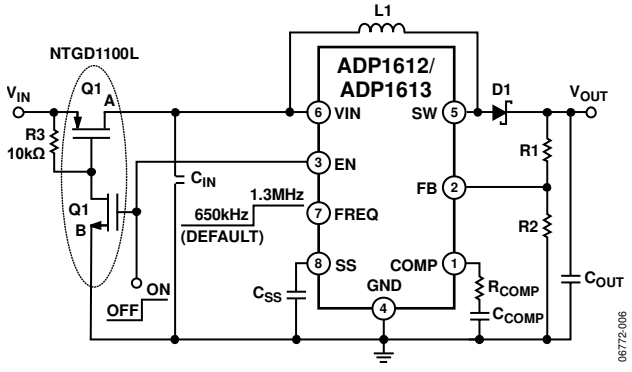


Figure 37. Step-Up Regulator with True Shutdown

STEP-UP REGULATOR CIRCUIT EXAMPLES

ADP1612 Step-Up Regulator

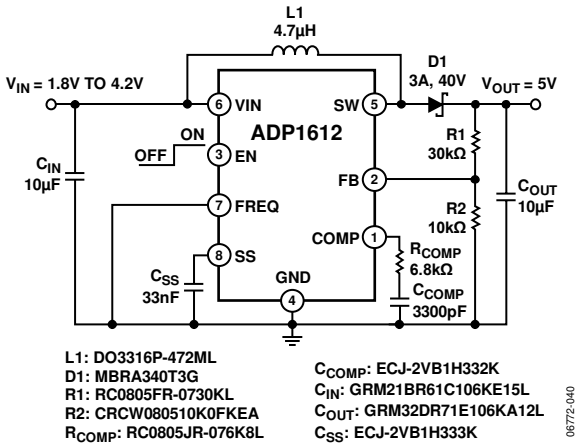


Figure 38. ADP1612 Step-Up Regulator Configuration
V_{OUT} = 5 V, f_{SW} = 650 kHz

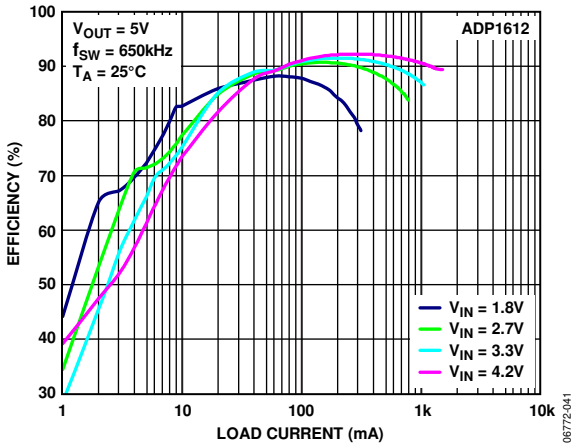


Figure 39. ADP1612 Efficiency vs. Load Current
V_{OUT} = 5 V, f_{SW} = 650 kHz

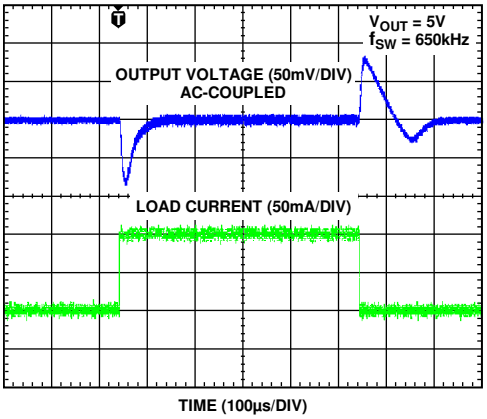


Figure 40. ADP1612 50 mA to 150 mA Load Transient (V_{IN} = 3.3 V)
V_{OUT} = 5 V, f_{SW} = 650 kHz

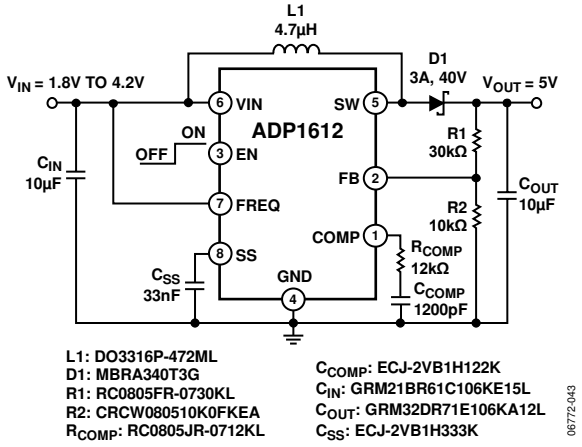


Figure 41. ADP1612 Step-Up Regulator Configuration
V_{OUT} = 5 V, f_{SW} = 1.3 MHz

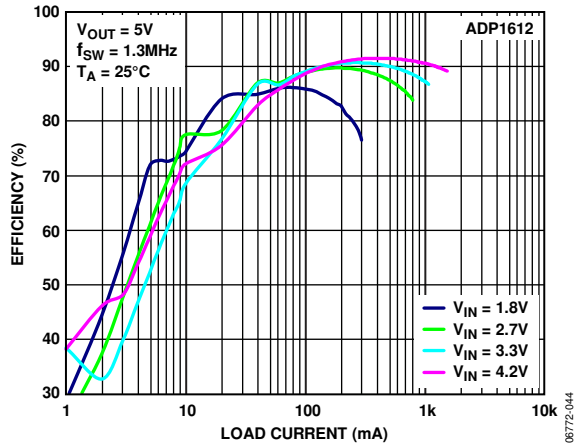


Figure 42. ADP1612 Efficiency vs. Load Current
V_{OUT} = 5 V, f_{SW} = 1.3 MHz

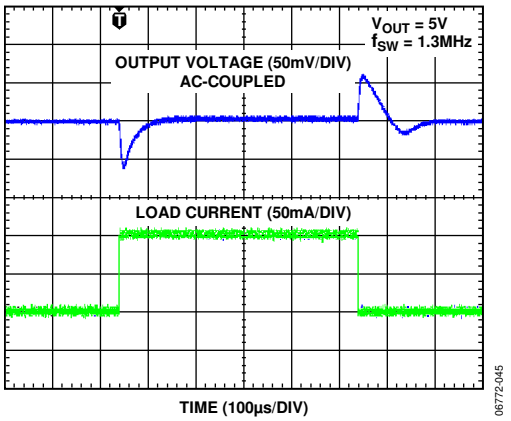


Figure 43. ADP1612 50 mA to 150 mA Load Transient (V_{IN} = 3.3 V)
V_{OUT} = 5 V, f_{SW} = 1.3 MHz

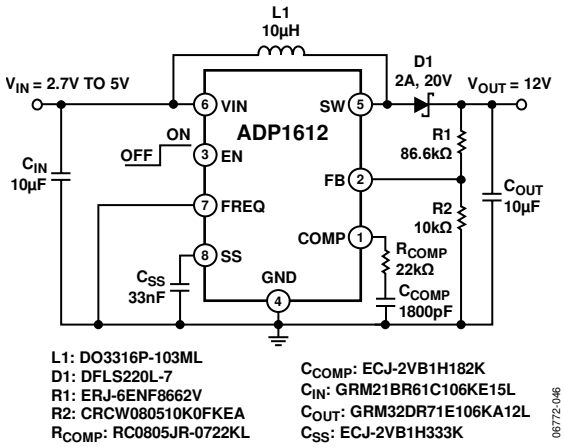


Figure 44. ADP1612 Step-Up Regulator Configuration
V_{OUT} = 12 V, f_{SW} = 650 kHz

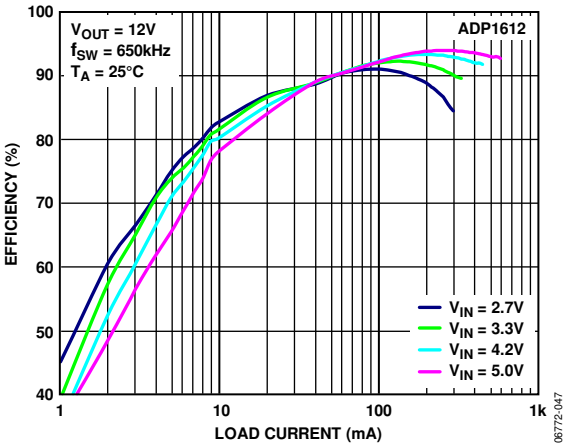


Figure 45. ADP1612 Efficiency vs. Load Current
V_{OUT} = 12 V, f_{SW} = 650 kHz

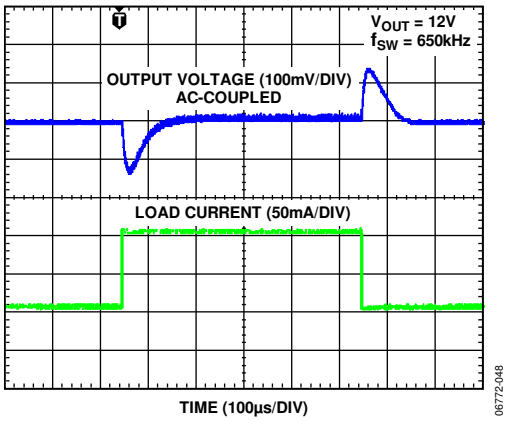


Figure 46. ADP1612 50 mA to 150 mA Load Transient (V_{IN} = 3.3 V)
V_{OUT} = 12 V, f_{SW} = 650 kHz

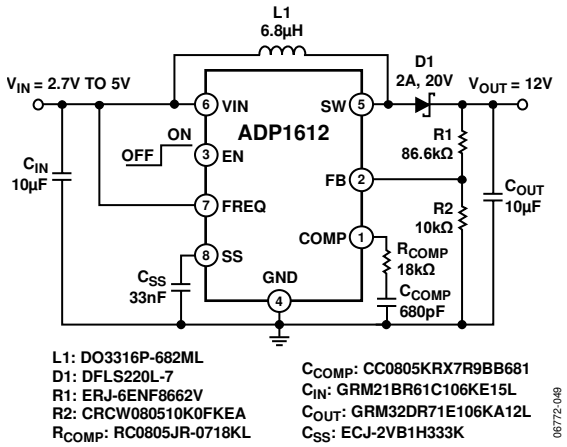


Figure 47. ADP1612 Step-Up Regulator Configuration
V_{OUT} = 12 V, f_{SW} = 1.3 MHz

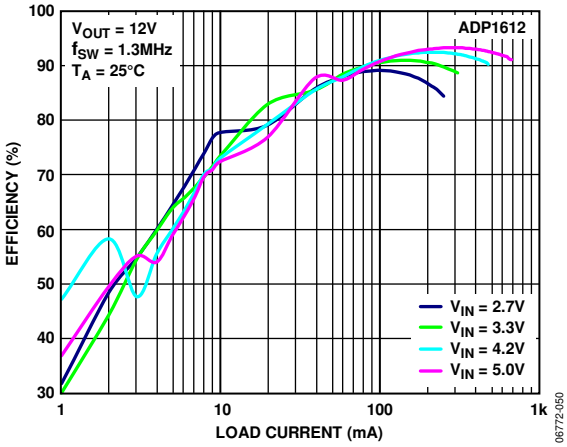


Figure 48. ADP1612 Efficiency vs. Load Current
V_{OUT} = 12 V, f_{SW} = 1.3 MHz

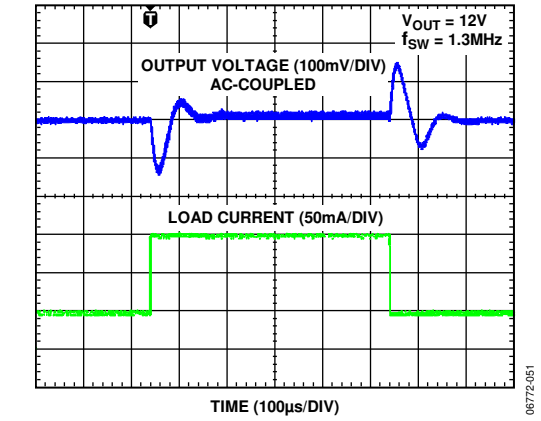


Figure 49. ADP1612 50 mA to 150 mA Load Transient (V_{IN} = 3.3 V)
V_{OUT} = 12 V, f_{SW} = 1.3 MHz

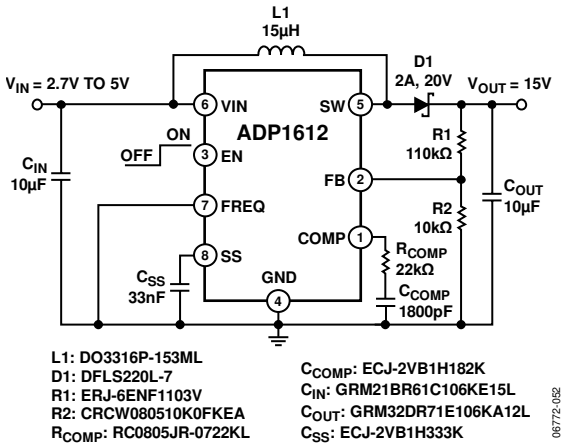


Figure 50. ADP1612 Step-Up Regulator Configuration
V_{OUT} = 15 V, f_{SW} = 650 kHz

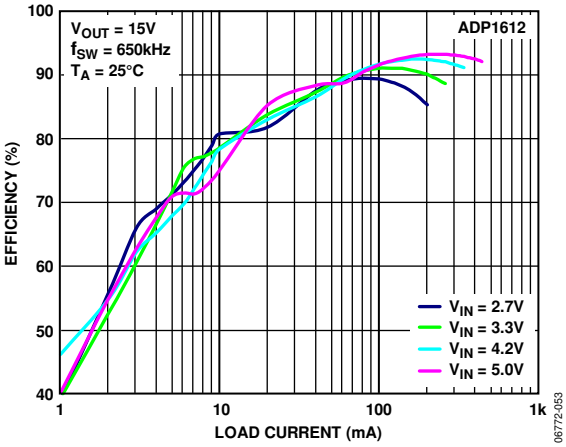


Figure 51. ADP1612 Efficiency vs. Load Current
V_{OUT} = 15 V, f_{SW} = 650 kHz

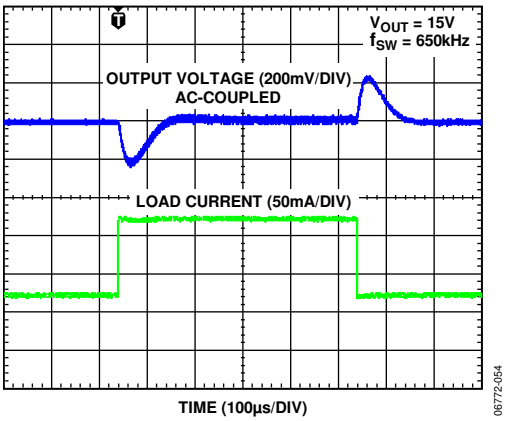


Figure 52. ADP1612 50 mA to 150 mA Load Transient (V_{IN} = 3.3 V)
V_{OUT} = 15 V, f_{SW} = 650 kHz

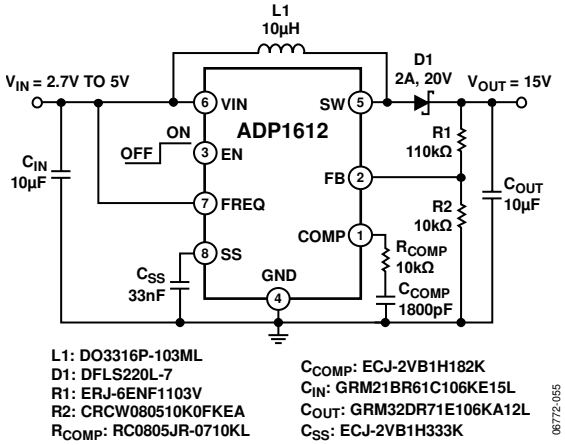


Figure 53. ADP1612 Step-Up Regulator Configuration
V_{OUT} = 15 V, f_{SW} = 1.3 MHz

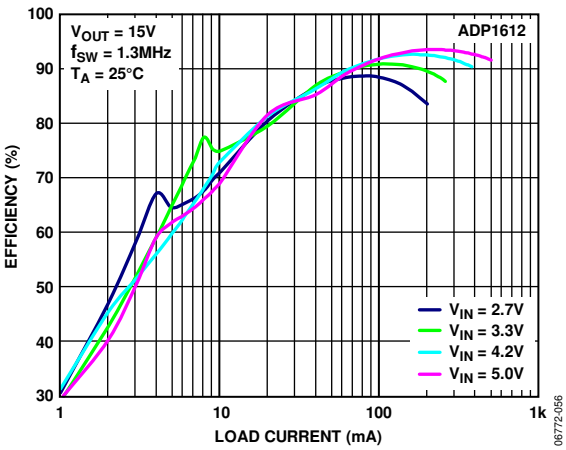


Figure 54. ADP1612 Efficiency vs. Load Current
V_{OUT} = 15 V, f_{SW} = 1.3 MHz

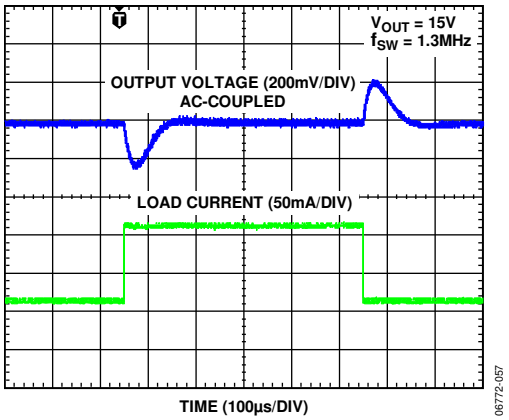


Figure 55. ADP1612 50 mA to 150 mA Load Transient (V_{IN} = 3.3 V)
V_{OUT} = 15 V, f_{SW} = 1.3 MHz

ADP1613 Step-Up Regulator

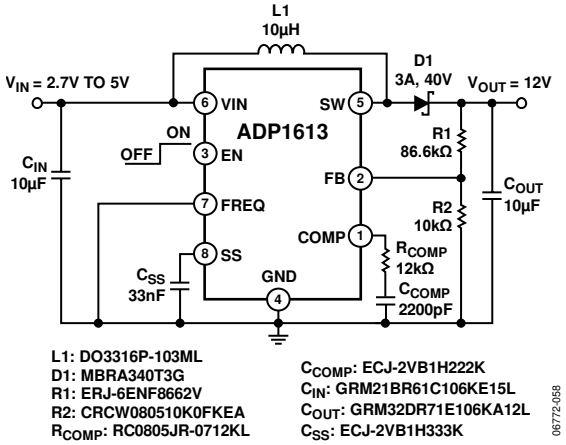


Figure 56. ADP1613 Step-Up Regulator Configuration
V_{OUT} = 12 V, f_{SW} = 650 kHz

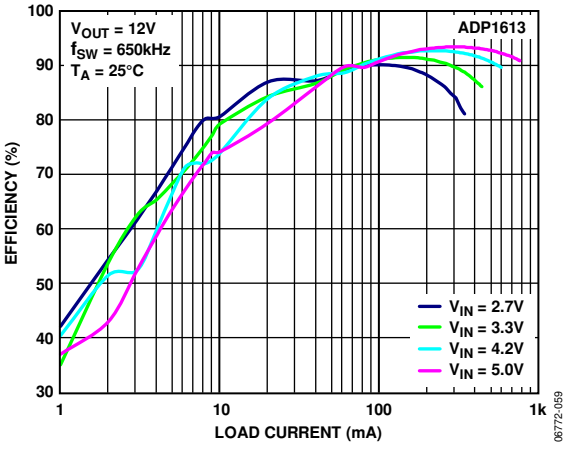


Figure 57. ADP1613 Efficiency vs. Load Current
V_{OUT} = 12 V, f_{SW} = 650 kHz

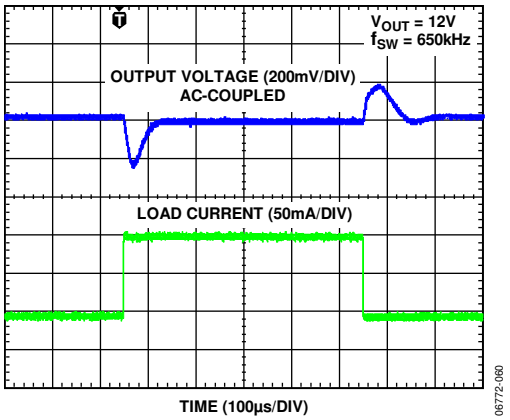


Figure 58. ADP1613 50 mA to 150 mA Load Transient (V_{IN} = 5 V)
V_{OUT} = 12 V, f_{SW} = 650 kHz

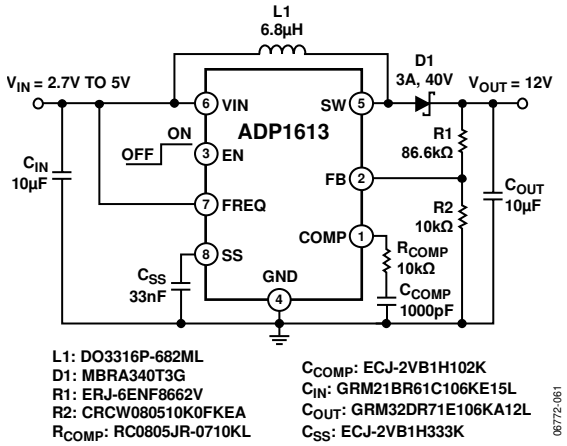


Figure 59. ADP1613 Step-Up Regulator Configuration
V_{OUT} = 12 V, f_{SW} = 1.3 MHz

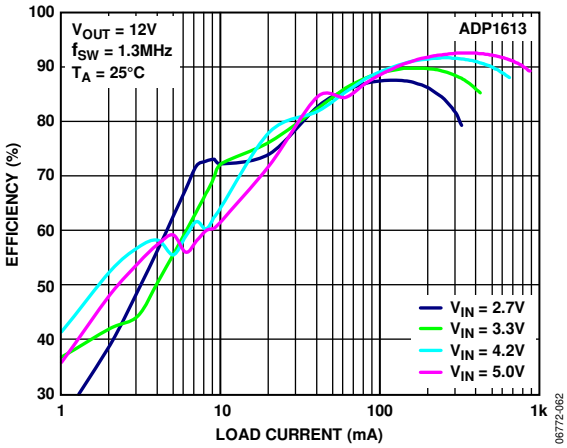


Figure 60. ADP1613 Efficiency vs. Load Current
V_{OUT} = 12 V, f_{SW} = 1.3 MHz

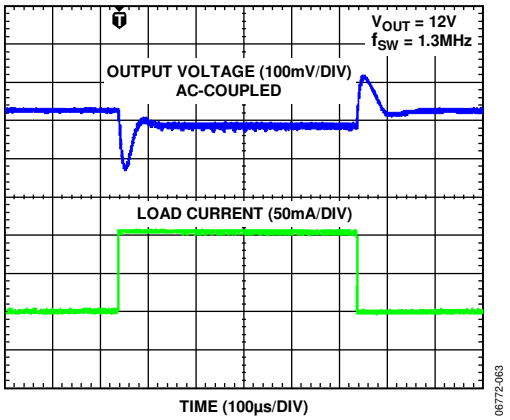


Figure 61. ADP1613 50 mA to 150 mA Load Transient (V_{IN} = 5 V)
V_{OUT} = 12 V, f_{SW} = 1.3 MHz

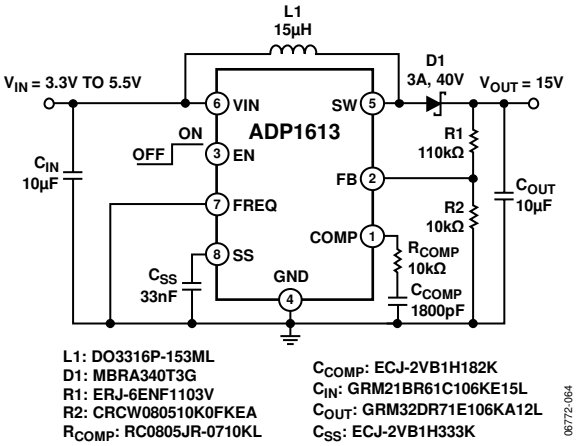


Figure 62. ADP1613 Step-Up Regulator Configuration
V_{OUT} = 15 V, f_{SW} = 650 kHz

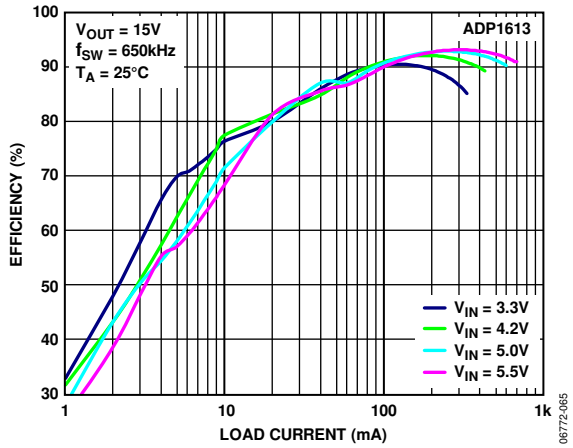


Figure 63. ADP1613 Efficiency vs. Load Current
V_{OUT} = 15 V, f_{SW} = 650 kHz

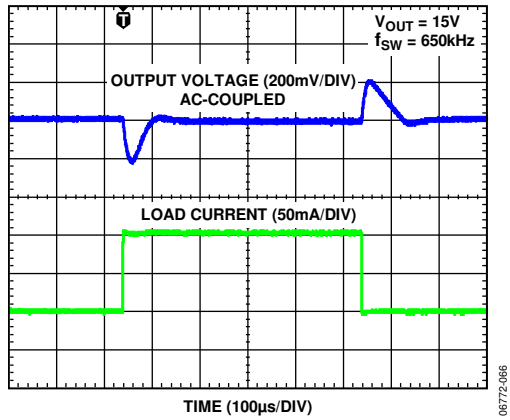


Figure 64. ADP1613 50 mA to 150 mA Load Transient (V_{IN} = 5 V)
V_{OUT} = 15 V, f_{SW} = 650 kHz

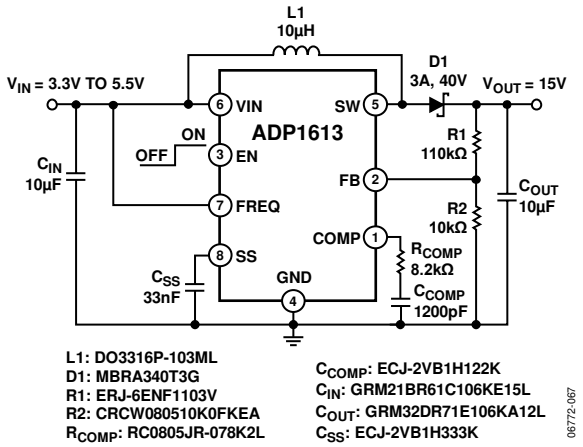


Figure 65. ADP1613 Step-Up Regulator Configuration
V_{OUT} = 15 V, f_{SW} = 1.3 MHz

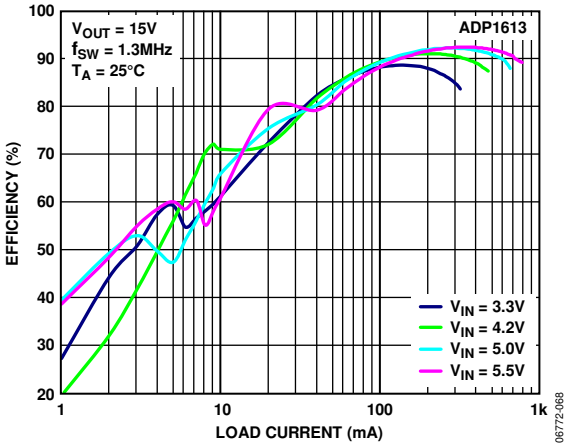


Figure 66. ADP1613 Efficiency vs. Load Current
V_{OUT} = 15 V, f_{SW} = 1.3 MHz

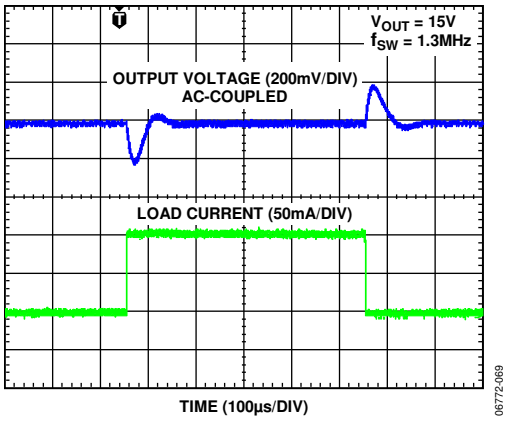


Figure 67. ADP1613 50 mA to 150 mA Load Transient (V_{IN} = 5 V)
V_{OUT} = 15 V, f_{SW} = 1.3 MHz

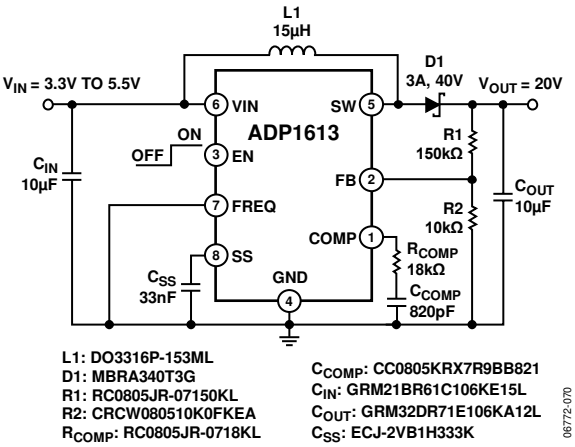


Figure 68. ADP1613 Step-Up Regulator Configuration
V_{OUT} = 20 V, f_{SW} = 650 kHz

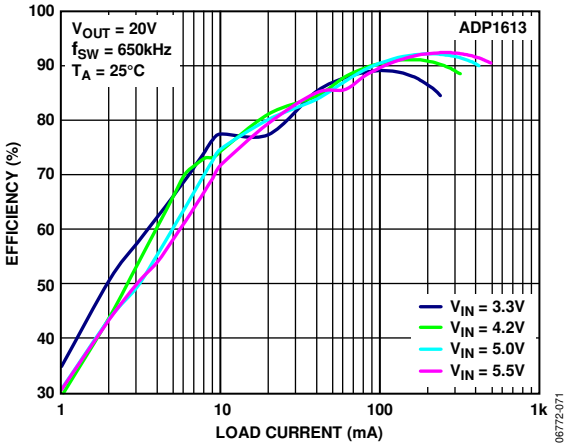


Figure 69. ADP1613 Efficiency vs. Load Current
V_{OUT} = 20 V, f_{SW} = 650 kHz

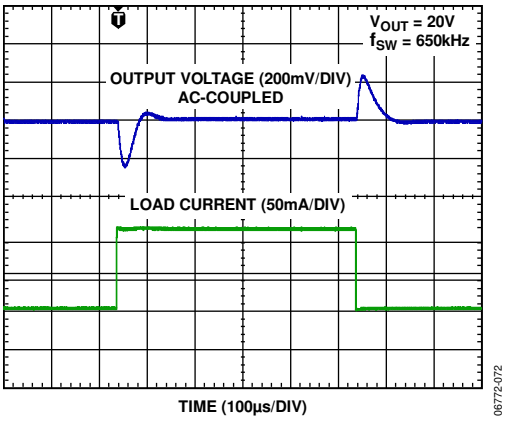


Figure 70. ADP1613 50 mA to 150 mA Load Transient (V_{IN} = 5 V)
V_{OUT} = 20 V, f_{SW} = 650 kHz

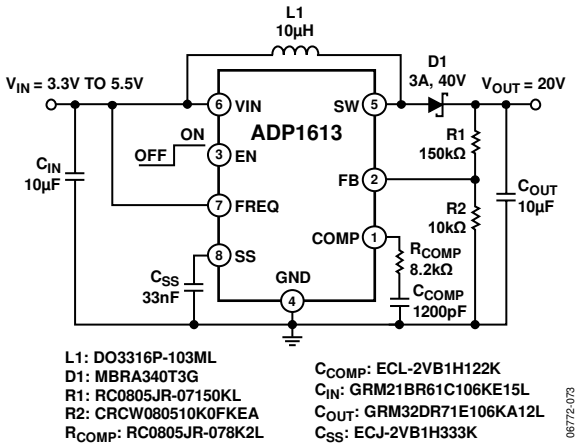


Figure 71. ADP1613 Step-Up Regulator Configuration
V_{OUT} = 20 V, f_{SW} = 1.3 MHz

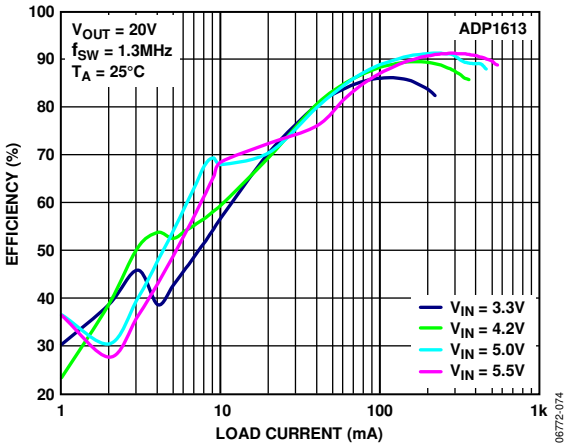


Figure 72. ADP1613 Efficiency vs. Load Current
V_{OUT} = 20 V, f_{SW} = 1.3 MHz

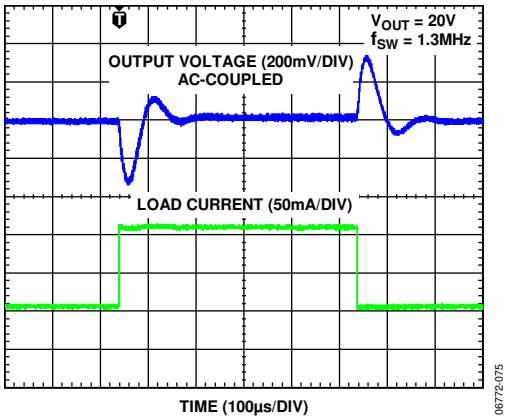


Figure 73. ADP1613 50 mA to 150 mA Load Transient (V_{IN} = 5 V)
V_{OUT} = 20 V, f_{SW} = 1.3 MHz

SEPIC CONVERTER

The circuit in Figure 74 shows the ADP1612/ADP1613 in a single-ended primary inductance converter (SEPIC) topology. This topology is useful for an unregulated input voltage, such as a battery-powered application in which the input voltage can vary between 2.7 V to 5 V and the regulated output voltage falls within the input voltage range.

The input and the output are dc isolated by a coupling capacitor (C1). In steady state, the average voltage of C1 is the input voltage. When the ADP1612/ADP1613 switch turns on and the diode turns off, the input voltage provides energy to L1 and C1 provides energy to L2. When the ADP1612/ADP1613 switch turns off and the diode turns on, the energy in L1 and L2 is released to charge the output capacitor (C_{OUT}) and the coupling capacitor (C1) and to supply current to the load.

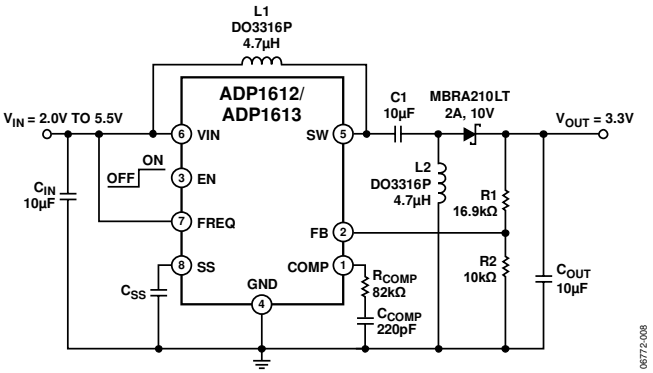


Figure 74. SEPIC Converter

TFT LCD BIAS SUPPLY

Figure 75 shows a power supply circuit for TFT LCD module applications. This circuit has +10 V, −5 V, and +22 V outputs. The +10 V is generated in the step-up configuration. The −5 V and +22 V are generated by the charge-pump circuit. During the step-up operation, the SW node switches between +10 V and ground (neglecting the forward drop of the diode and on resistance of the switch). When the SW node is high, C5 charges up to +10 V. When the SW node is low, C5 holds its charge and forward-biases D8 to charge C6 to −10 V. The Zener diode (D9) clamps and regulates the output to −5 V.

The VGH output is generated in a similar manner by the charge-pump capacitors, C1, C2, and C4. The output voltage is tripled and regulated down to 22 V by the Zener diode, D5.

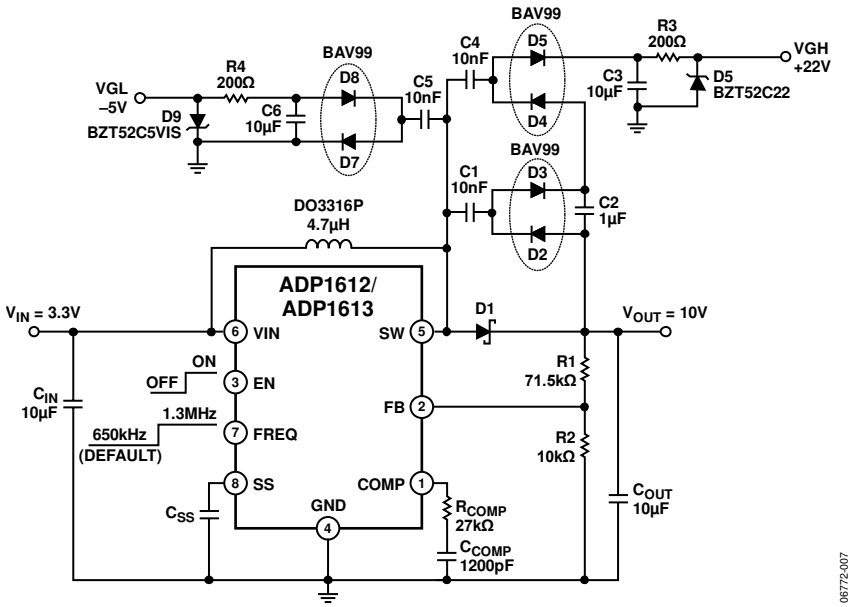


Figure 75. TFT LCD Bias Supply

PCB LAYOUT GUIDELINES

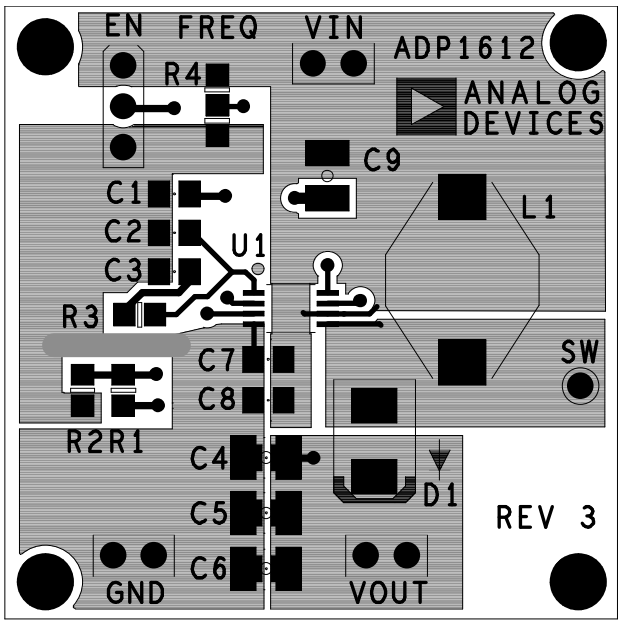


Figure 76. Example Layout for ADP1612/ADP1613 Boost Application (Top Layer)

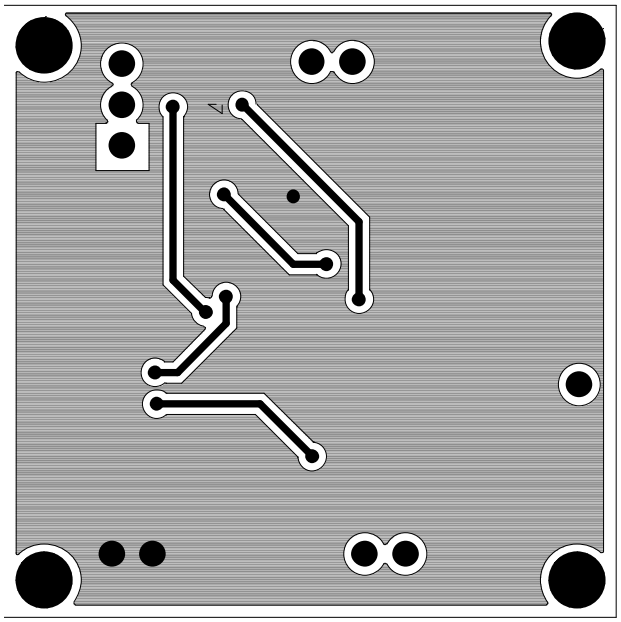


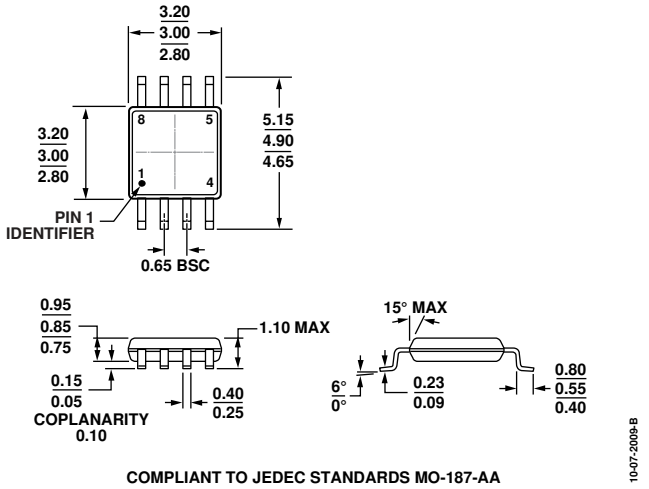
Figure 77. Example Layout for ADP1612/ADP1613 Boost Application (Bottom Layer)

For high efficiency, good regulation, and stability, a well-designed printed circuit board layout is required.

Use the following guidelines when designing printed circuit boards (also see Figure 34 for a block diagram and Figure 3 for a pin configuration).

- Keep the low ESR input capacitor, C_{IN} (labeled as C7 in Figure 76), close to VIN and GND. This minimizes noise injected into the part from board parasitic inductance.
- Keep the high current path from C_{IN} (labeled as C7 in Figure 76) through the L1 inductor to SW and GND as short as possible.
- Keep the high current path from VIN through L1, the rectifier (D1) and the output capacitor, C_{OUT} (labeled as C4 in Figure 76) as short as possible.
- Keep high current traces as short and as wide as possible.
- Place the feedback resistors as close to FB as possible to prevent noise pickup. Connect the ground of the feedback network directly to an AGND plane that makes a Kelvin connection to the GND pin.
- Place the compensation components as close as possible to COMP. Connect the ground of the compensation network directly to an AGND plane that makes a Kelvin connection to the GND pin.
- Connect the softstart capacitor, C_{SS} (labeled as C1 in Figure 76) as close to the device as possible. Connect the ground of the softstart capacitor to an AGND plane that makes a Kelvin connection to the GND pin.
- Avoid routing high impedance traces from the compensation and feedback resistors near any node connected to SW or near the inductor to prevent radiated noise injection.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 78. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description[2]	Package Option	Branding
ADP1612ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	L7Z
ADP1612-5-EVALZ		Evaluation Board, 5 V Output Voltage Configuration		
ADP1613ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	L96
ADP1613-12-EVALZ		Evaluation Board, 12 V Output Voltage Configuration		

[1] Z = RoHS Compliant Part.

NOTES

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D06772-0-11/12(D)