DS90LV047-48AEVM Evaluation Board

1 Overview

The DS90LV047-48AEVM is an evaluation module designed for performance and functional evaluation of the Texas Instruments DS90LV047A 3-V LVDS Quad CMOS Differential Line Driver and DS90LV048A 3-V LVDS CMOS Differential Line Receiver. With this kit, users can quickly evaluate the output waveform characteristics and signal integrity supported by the DS90LV047A and DS90LV048A. Header pins allow access to the DS90LV047A and DS90LV048A inputs and outputs and also facilitate connection to lab equipment or user systems for performance evaluation.

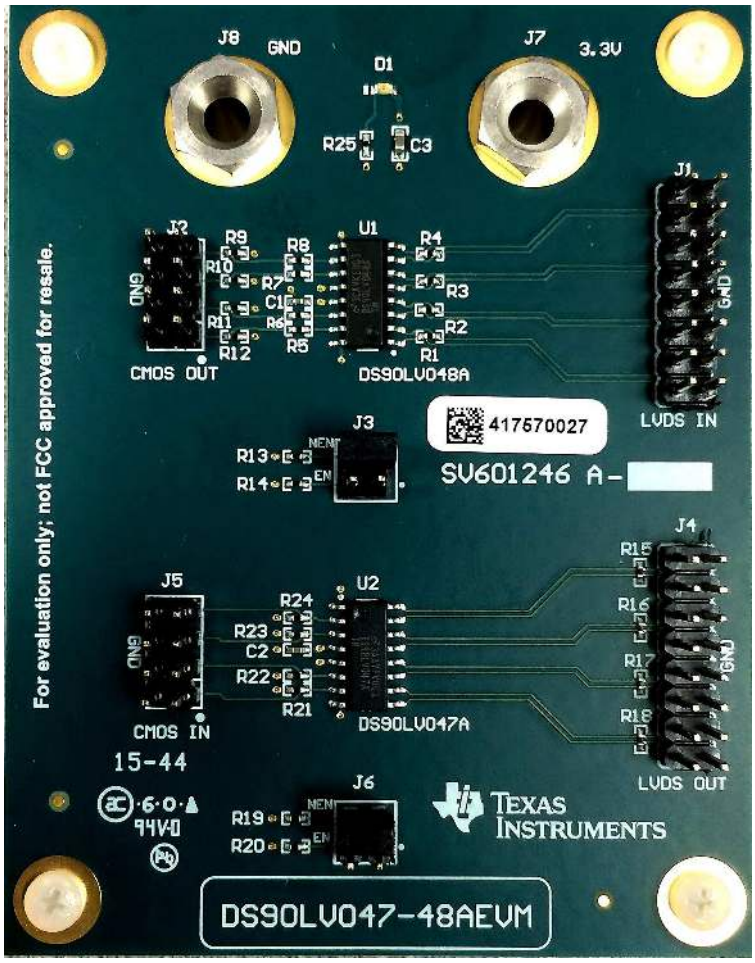


Figure 1. DS90LV047-48AEVM

2 Features

DS90LV047A:

- Converts Single-Ended LVCMOS to Differential LVDS
- >400 Mbps (200 MHz) Switching Rates
- Single Supply Operation: VDD = 3.3 V ± 5%
- ± 350 mV LVDS Signaling
- Low Power (13 mW at 3.3 V Static)

DS90LV048A:

- Converts Differential LVDS to Single-Ended LVCMOS
- >400 Mbps (200 MHz) Switching Rates
- Single Supply Operation: VDD = 3.3 V ± 5%
- Accepts Small ±35 mV Differential Signaling
- Low Power Design (40 mW at 3.3 V Static)

3 Applications

- Wireless/Telecom Infrastructure
- Medical/Health
- Multi-Function Printers
- Factory Automation and Control
- EPOS/ECR/Cash Drawer

4 Ordering Information

EVM ID	Device ID	Device Package
DS90LV047-48AEVM	DS90LV047A, DS90LV048A	SOIC

5 Setup

The DS90LV047A is a LVDS Quad CMOS Differential Line Driver, and the DS90LV048A is a LVDS Quad CMOS Differential Line Receiver. When operating the DS90LV047-48AEVM, jumper setting definitions can be referenced in Table 1, while signal input and output connection descriptions can be found in Figure 2 and Figure 3. When using the DS90LV047A and DS90LV048A together, the typical configuration is to connect the DS90LV047A outputs (J4) such that they drive the inputs of the DS90LV048A (J1).

Table 1. Description of Jumper Settings

Component	Name	Comments
J8	GND	GND power supply
J7	VDD	3.3 V VDD power supply
J3	ENABLE1	Leave Pins 1 and 2 open, and tie Pins 3 and 4 to enable DS90LV048A.
J6	ENABLE2	Leave Pins 1 and 2 open, and tie Pins 3 and 4 to enable DS90LV047A.

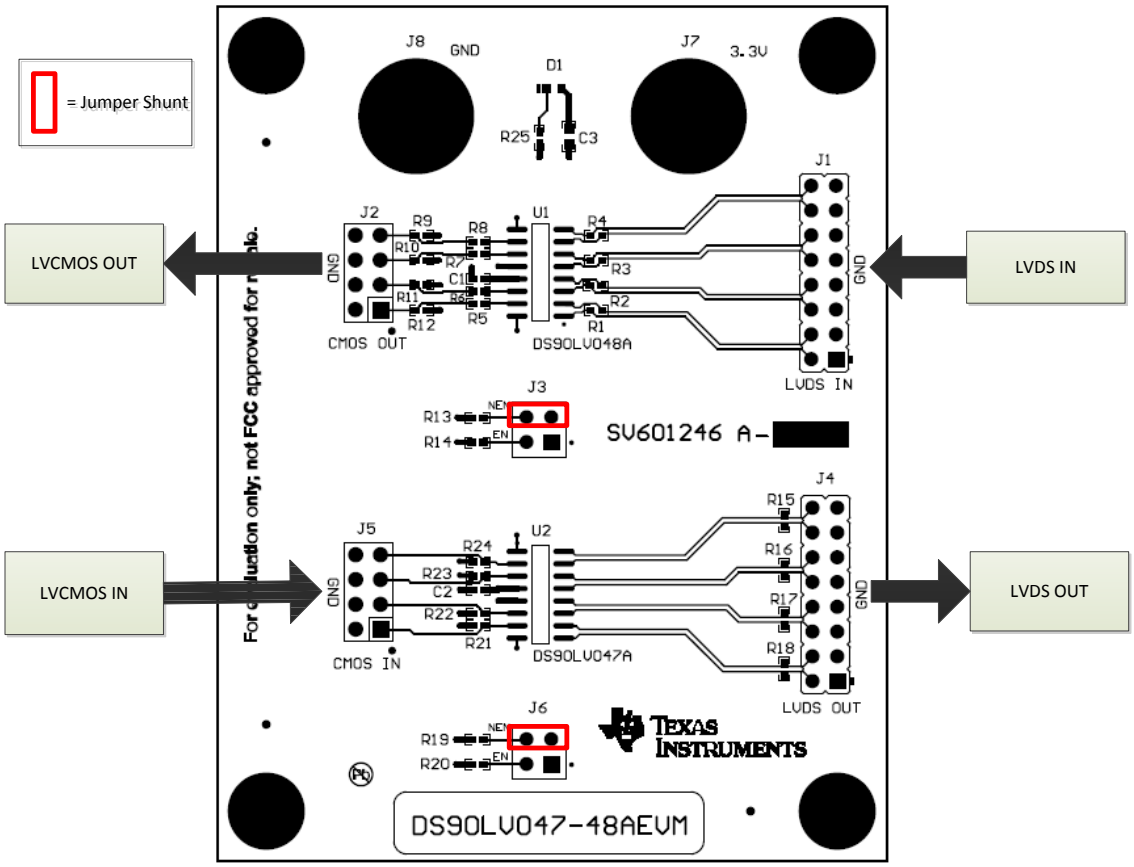


Figure 2. DS90LV047-48AEVM Input and Output Diagram

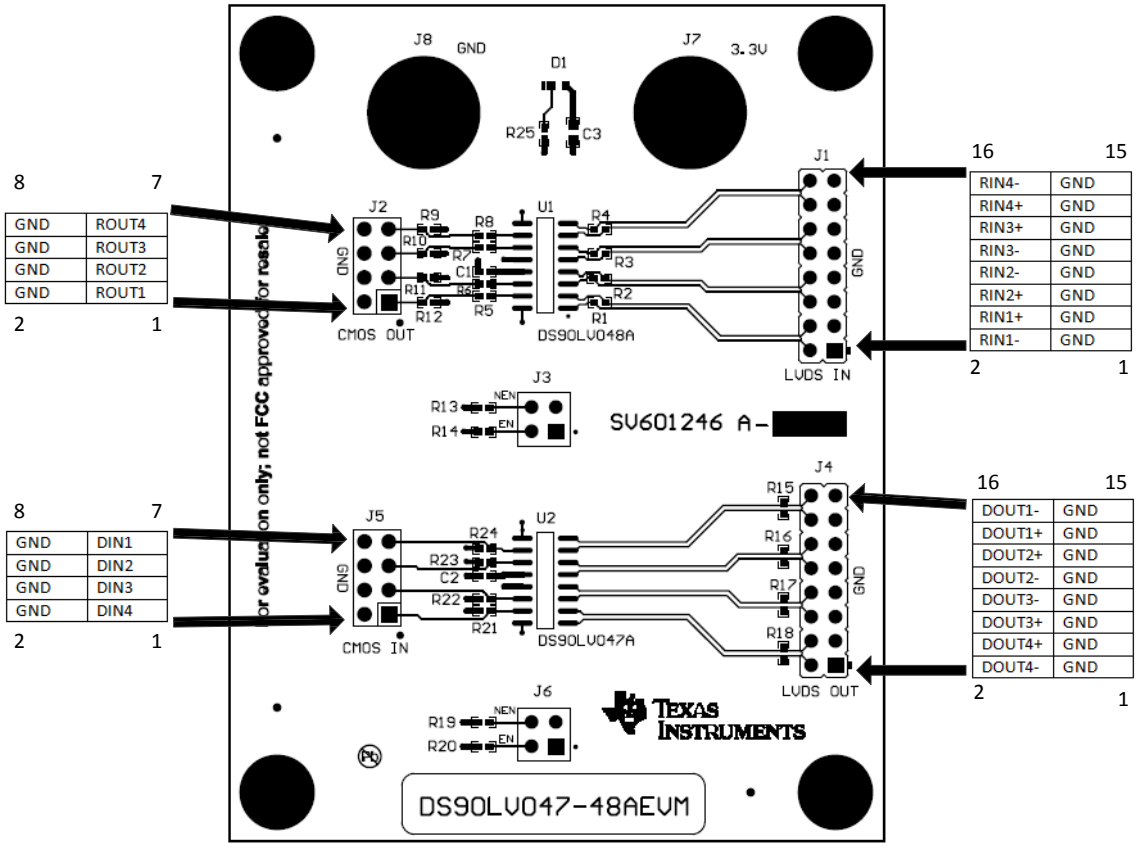


Figure 3. DS90LV047-48AEVM Input and Output Header Connections

5.1 Hardware Description and Setup

For hardware setup and connections, reference the diagrams in Figure 3 and Figure 4.

1. Connect a 3.3 V DC power supply (30 mA max) to the EVM.
   - Connect J7: VIN = 3.3 V and J8: GND.
2. Install the default shunt jumpers for appropriate operation, as shown in Figure 4.
   - Install a shunt jumper on J3 Pins 3-4 to tie DS90LV048A NEN to GND.
   - Install a shunt jumper on J6 Pins 3-4 to tie DS90LV047A NEN to GND.
3. Apply a high-speed 3.3 V LVCMOS signal to the DS90LV047A inputs on header J5.
4. The DS90LV047A LVDS output signals can be measured differentially on an oscilloscope by applying a Tektronix P6247 probe or equivalent differential probe at header J4 to measure the differential signal across the 100 Ω termination resistors R15-R18. The expected output waveform is a ±350 mV LVDS signal.
5. Apply a high-speed ±350 mV (700 mV_{pp} differential) LVDS signal to the DS90LV048A inputs on header J1. If desired, the LVDS inputs can be provided by connecting the LVDS outputs on header J4 to the desired LVDS input pins on header J1. If this is done, remove resistors R15-R18 to avoid double-termination.
6. The DS90LV048A LVCMOS output signals can be measured on an oscilloscope by applying a Tektronix P6247 probe or equivalent differential probe at header J2.

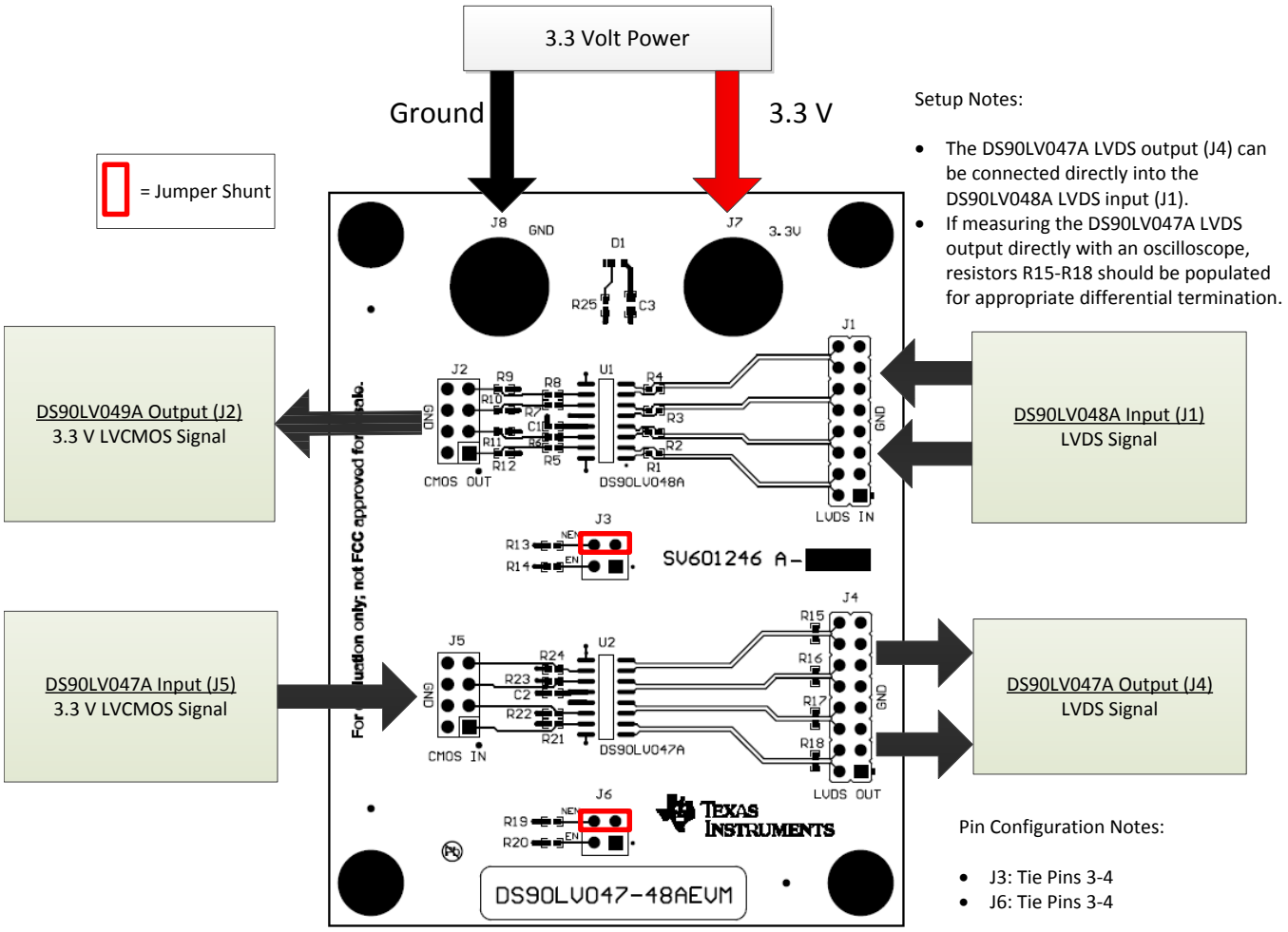


Figure 4. DS90LV047-48AEVM Setup Configuration

In order to measure LVDS signals properly, a 100 Ω termination resistor must be present across each differential pair at the point of measurement. However, if multiple 100 Ω termination resistors are placed across a differential pair between the transmitter and receiver, the signal becomes double terminated. Double termination should be avoided, since this reduces the output amplitude and noise margin.

By factory default, the DS90LV047-48AEVM comes with stuffed termination resistors R1-R4 on the DS90LV048A inputs and stuffed termination resistors R15-R18 on the DS90LV047A outputs.

Remove R15-R18...

- if the DS90LV047A output interfaces with a DS90LV048A input by connecting J4 to J1.
- if the DS90LV047A output interfaces with an external load that has an appropriate 100 Ω differential termination.

Populate R15-R18 with 100 Ω termination resistors (or leave R15-R18 populated)...

- if the DS90LV047A output is measured by a high-impedance differential probe.
- if the DS90LV047A output interfaces with an external load that does **not** have an appropriate 100 Ω differential termination.

5.2 DS90LV047-48AEVM Performance Plots

The following plots show typical waveforms measured on the DS90LV047-48AEVM inputs and outputs using the hardware setup in Figure 4. For these measurements, the following parameters were used:

- Operating Frequency: 200 MHz (400 Mbps)
- DS90LV047A Input: 3.3 V LVCMOS sine wave to DIN1
- DS90LV047A Output: Measured with 100 Ω termination resistor R15 populated across DOUT1±
- DS90LV048A Input: LVDS signal to RIN1± from DS90LV047A output DOUT1±. 100 Ω termination resistor R15 removed
- DS90LV048A Output: Measured at ROUT1

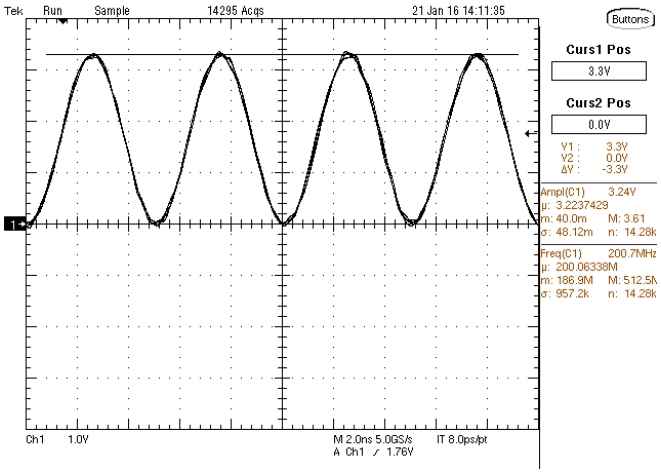


Figure 5. DS90LV047A 3.3 V LVCMOS Input

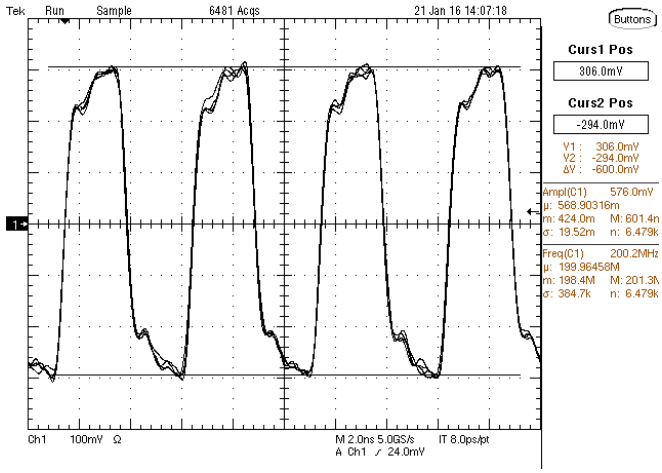


Figure 6. DS90LV047A Differential LVDS Output

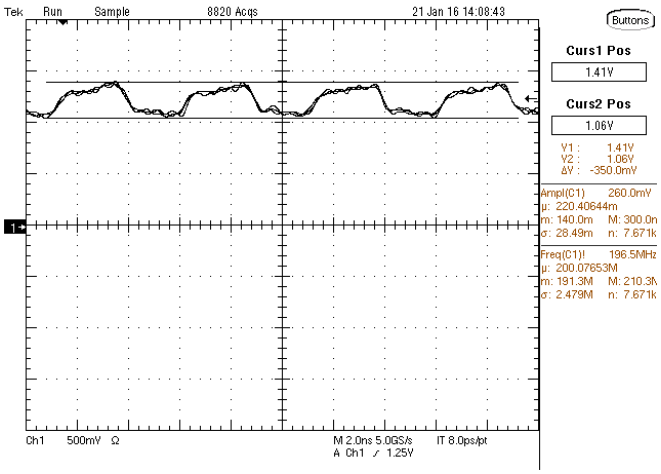


Figure 7. DS90LV047A Single-Ended LVDS Output

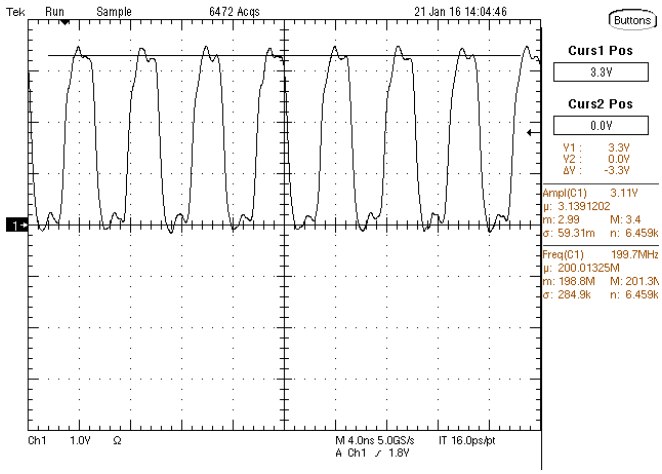
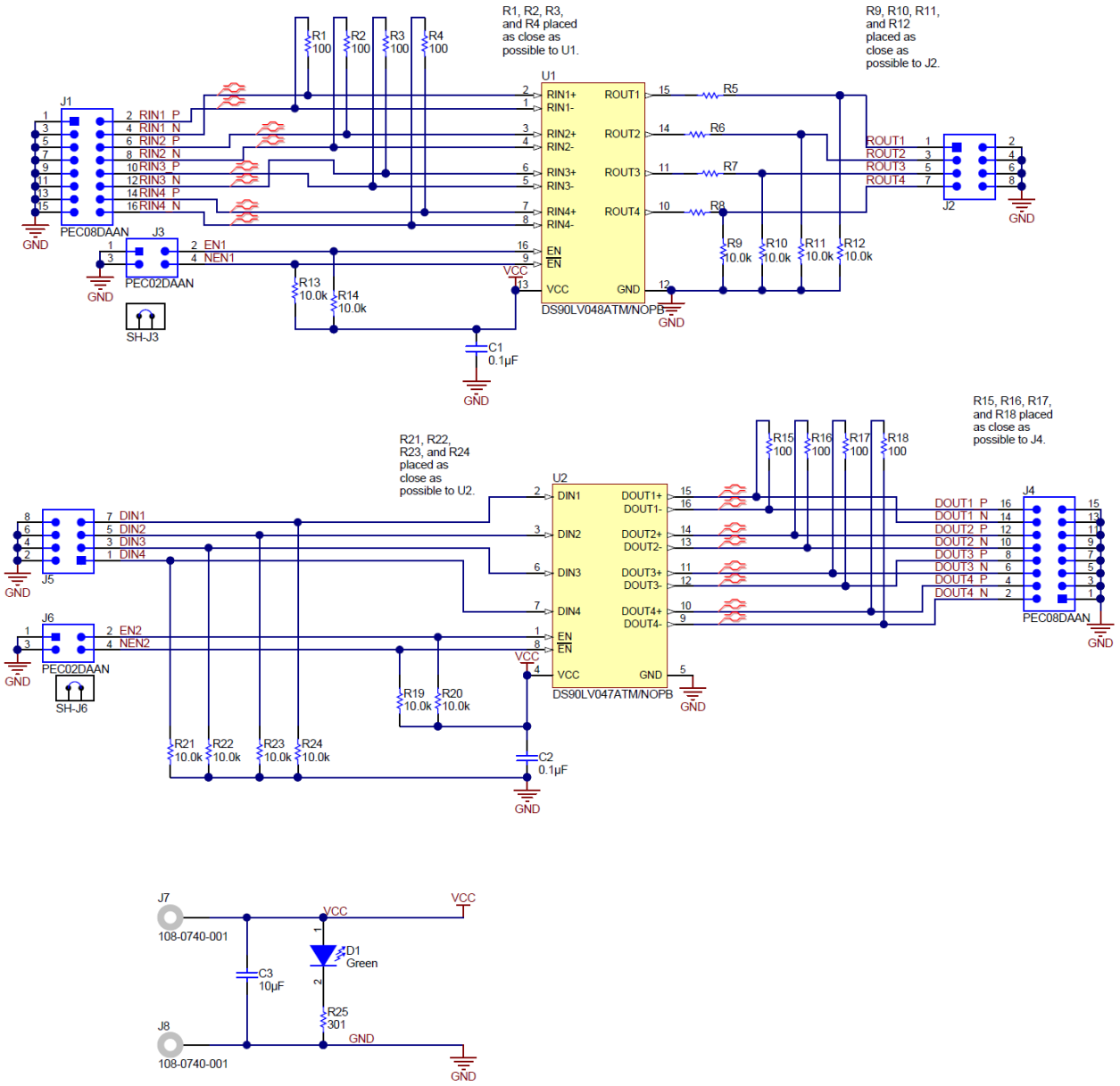


Figure 8. DS90LV048A LVCMOS Output

6 Bill of Materials

Part Number	Description	Designator	Footprint	Quantity
GRM155R61A104KA01D	CAP, CERM, 0.1 µF, 10 V, +/- 10%, X5R, 0402	C1, C2	0402	2
GRM188R61A106ME69	CAP, CERM, 10 µF, 10 V, +/- 20%, X5R, 0603	C3	0603	1
SML-LX0603GW-TR	LED, Green, SMD	D1	LED_SML-LX0603GW	1
Fiducial	Fiducial mark. There is nothing to buy or mount.	FID1, FID2, FID3	Fiducial10-20	3
NY PMS 440 0025 PH	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	H1, H2, H3, H4	NY PMS 440 0025 PH	4
1902C	Standoff, Hex, 0.5"L #4-40 Nylon	H5, H6, H7, H8	Keystone_1902C	4
PEC08DAAN	Header, 2.54 mm, 8x2, Tin, Vertical, TH	J1, J4	Sullins_xxC08DAAN	2
PEC04DAAN	Header, 100mil, 4x2, Tin, TH	J2, J5	CONN_PEC04DAAN	2
PEC02DAAN	Header, 100mil, 2x2, Tin, TH	J3, J6	Sullins_PEC02DAAN	2
108-0740-001	Standard Banana Jack, Uninsulated, 15A	J7, J8	Johnson_108-0740-001	2
Size: 1.25" x 0.25"	Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	LBL1	Label_1250x250	1
CRCW0402100RFKED	RES, 100, 1%, 0.063 W, 0402	R1, R2, R3, R4, R15, R16, R17, R18	0402	8
ERJ-2GE0R00X	RES, 0, 5%, 0.063 W, 0402	R5, R6, R7, R8	0402	4
CRCW040210K0FKED	RES, 10.0 k, 1%, 0.063 W, 0402	R9, R10, R11, R12, R13, R14, R19, R20, R21, R22, R23, R24	0402	12
SNT-100-BK-G	Shunt, 100mil, Gold plated, Black	SH-J3, SH-J6	SNT-100-BK-G	2
DS90LV048ATM/NOPB	3V LVDS Quad CMOS Differential Line Receiver, 16-pin Narrow SOIC, Pb-Free	U1	M16A_N	1
DS90LV047ATM/NOPB	3V LVDS Quad CMOS Differential Line Driver, 16-pin Narrow SOIC, Pb-Free	U2	M16A_N	1

7 Schematic



8 EVM Layout

Figure 9 and Figure 10 show the DS90LV047-48AEVM layout. The DS90LV047A and DS90LV048A inputs and outputs can be accessed via header pins.

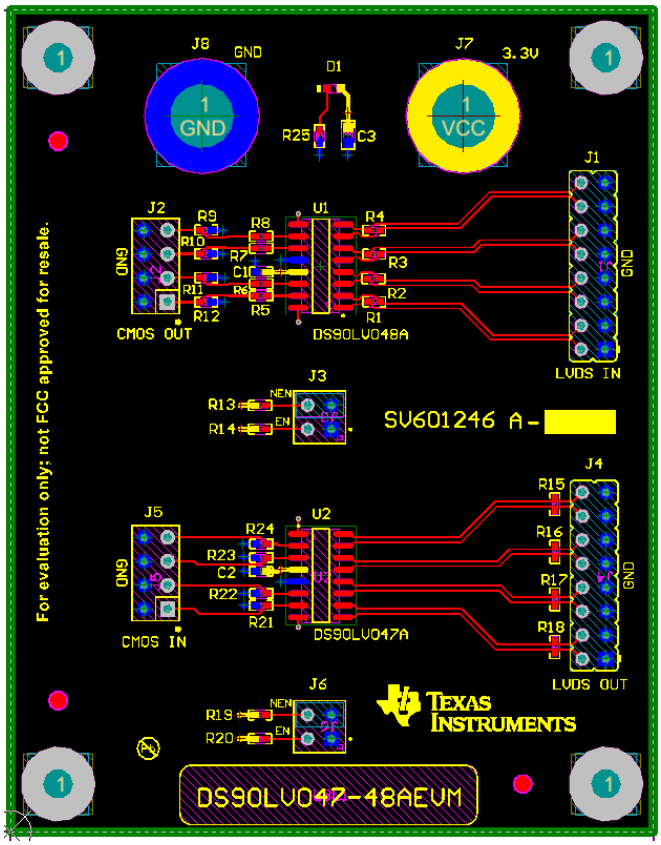


Figure 9. DS90LV047-48AEVM Top Layer

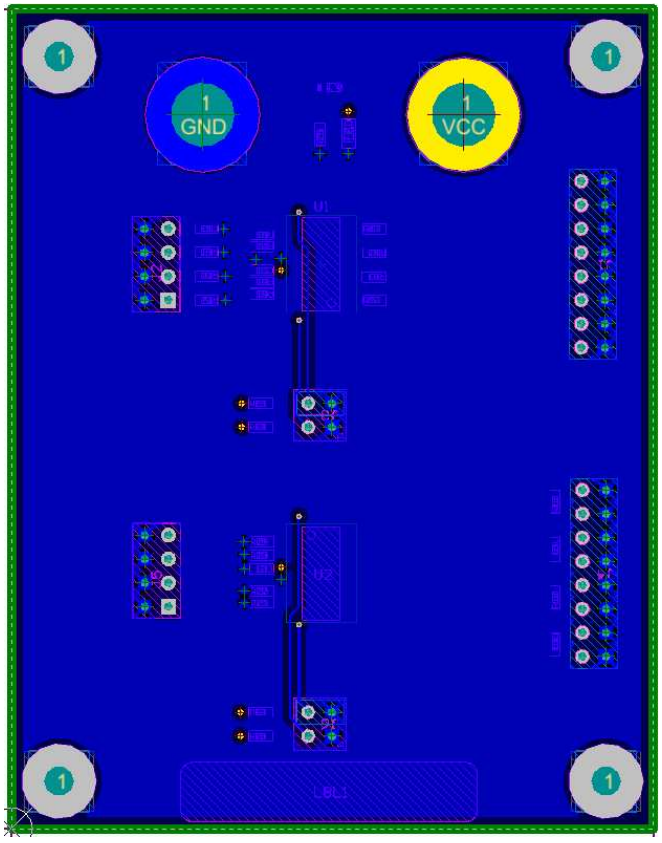


Figure 10. DS90LV047-48AEVM Bottom Layer

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3 *Regulatory Notices:*

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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