Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.101 at V_{GS} = - 4.5 V	- 4.5[a]	4.9 nC
	0.141 at V_{GS} = - 2.5 V	- 4.5[a]	
	0.192 at V_{GS} = - 1.8 V	- 2	

FEATURES

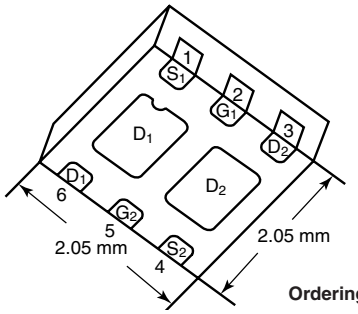
- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
  - Small Footprint Area
  - Low On-Resistance
- Typical ESD Protection 4000 V

Pb-free
RoHS COMPLIANT
HALOGEN FREE

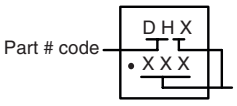
APPLICATIONS

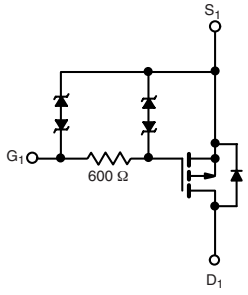
- Load Switch, PA Switch and Battery Switch for Portable Devices

PowerPAK SC-70-6 Dual

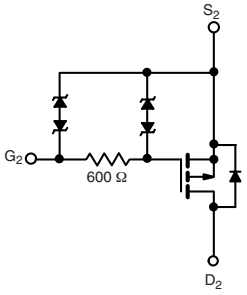


Marking Code





P-Channel MOSFET



P-Channel MOSFET

Ordering Information: SiA911EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 4.5[a]	A
	T_C = 70 °C		- 4.5[a]	
	T_A = 25 °C		- 3.6[b, c]	
	T_A = 70 °C		- 2.9[b, c]	
Pulsed Drain Current		I_{DM}	- 10	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 4.5[a]	
	T_A = 25 °C		- 1.6[b, c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	7.8	W
	T_C = 70 °C		5	
	T_A = 25 °C		1.9[b, c]	
	T_A = 70 °C		1.2[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, f]	t ≤ 5 s	R_{thJA}	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	12.5	16	

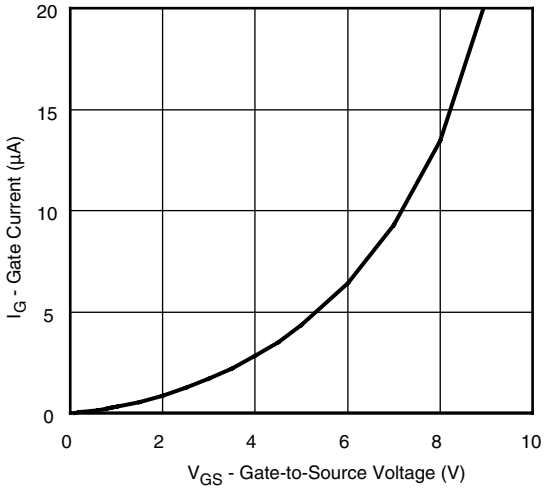
Notes:
a. Package limited.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under Steady State conditions is 110 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 21		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.1		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.4		- 1	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	µA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 10			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 2.7 A		0.083	0.101	Ω
		V_{GS} = - 2.5 V, I_D = - 2.3 A		0.115	0.141	
		V_{GS} = - 1.8 V, I_D = - 1 A		0.153	0.192	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 2.7 A		7		S
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 8 V, I_D = - 3.6 A		7.1	11	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 3.6 A		4.2	6.5	
Gate-Source Charge	Q_{gs}			0.7		
Gate-Drain Charge	Q_{gd}			1.2		
Gate Resistance	R_g	f = 1 MHz		600		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 3.5 Ω $I_D \cong$ - 2.9 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		92	140	ns
Rise Time	t_r			200	300	
Turn-Off Delay Time	$t_{d(off)}$			700	1100	
Fall Time	t_f			400	600	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 3.5 Ω $I_D \cong$ - 2.9 A, V_{GEN} = - 8 V, R_g = 1 Ω		32	50	
Rise Time	t_r			70	105	
Turn-Off Delay Time	$t_{d(off)}$			990	1500	
Fall Time	t_f			410	615	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 4.5	A
Pulse Diode Forward Current	I_{SM}				- 10	
Body Diode Voltage	V_{SD}	I_S = - 2.9 A, V_{GS} = 0 V		- 0.9	- 1.2	V

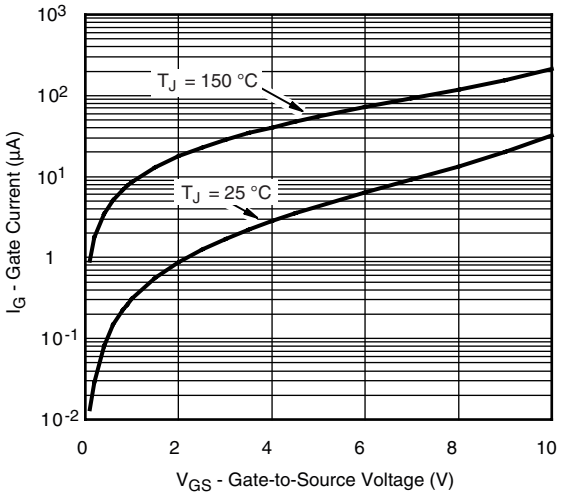
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

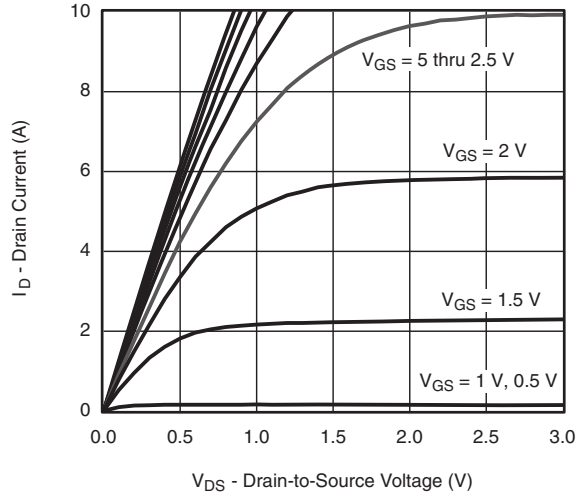
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



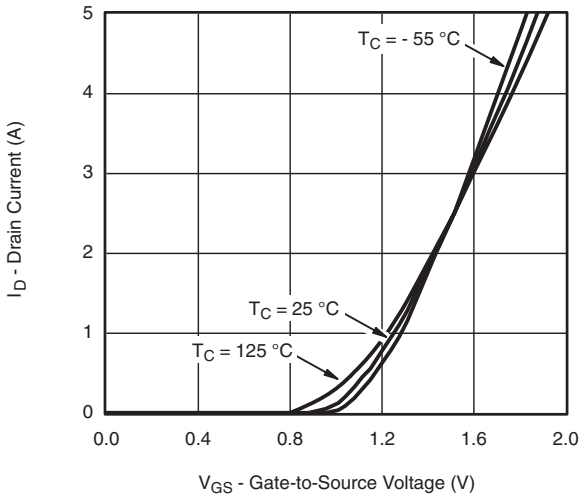
Gate Current vs. Gate-to-Source Voltage



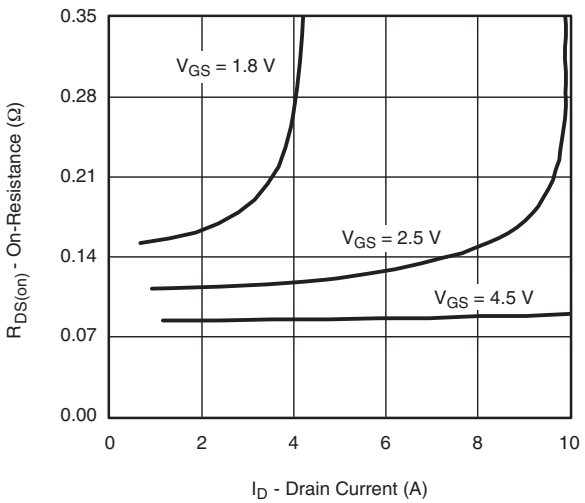
Gate Current vs. Gate-to-Source Voltage



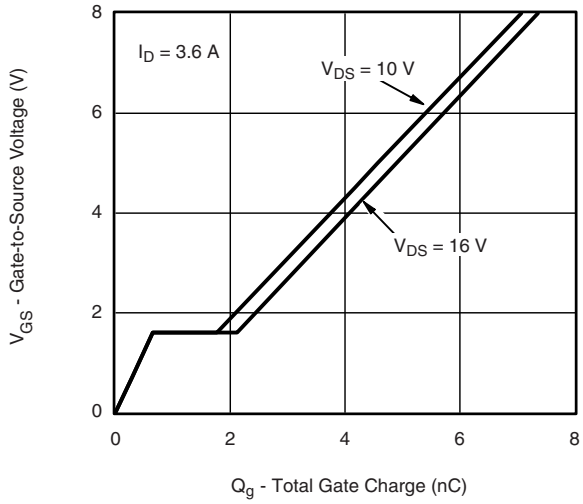
Output Characteristics



Transfer Characteristics

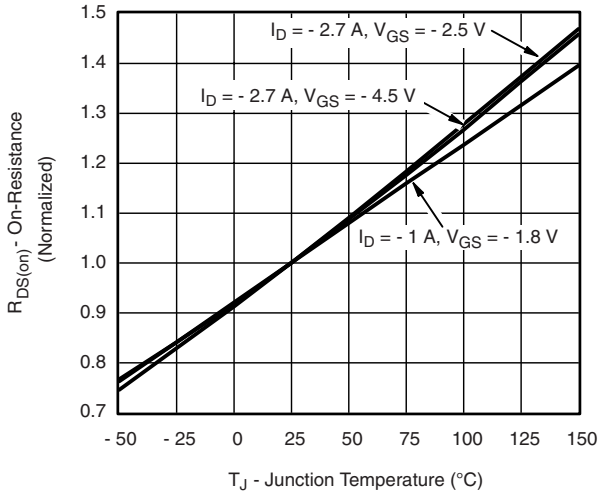


On-Resistance vs. Drain Current and Gate Voltage

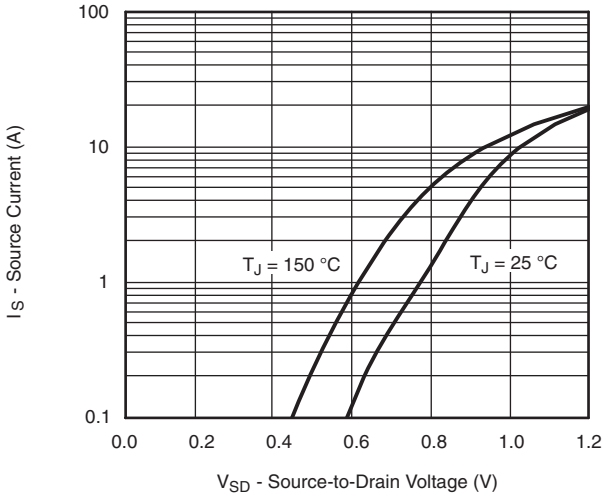


Gate Charge

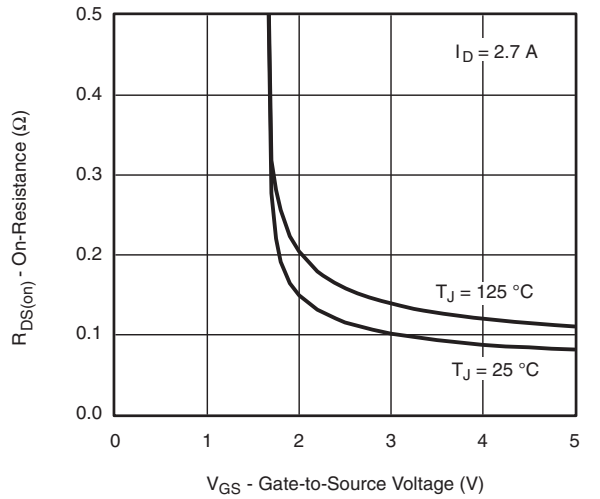
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



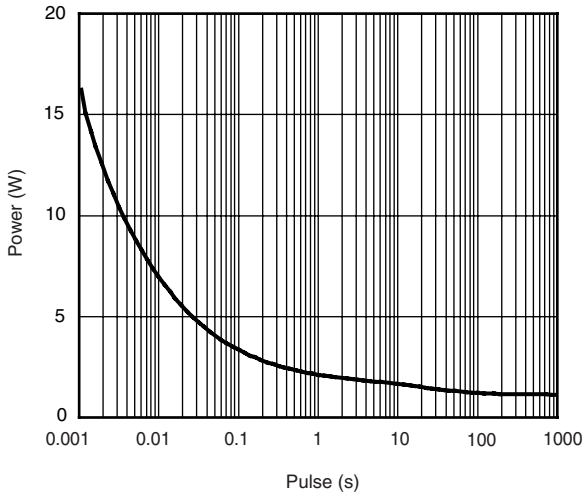
On-Resistance vs. Junction Temperature



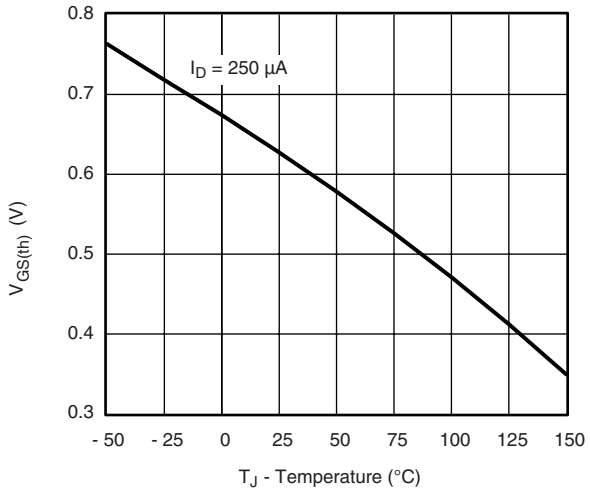
Soure-Drain Diode Forward Voltage



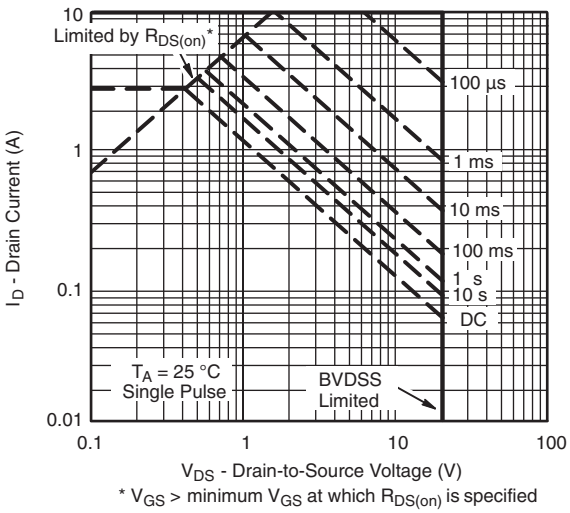
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



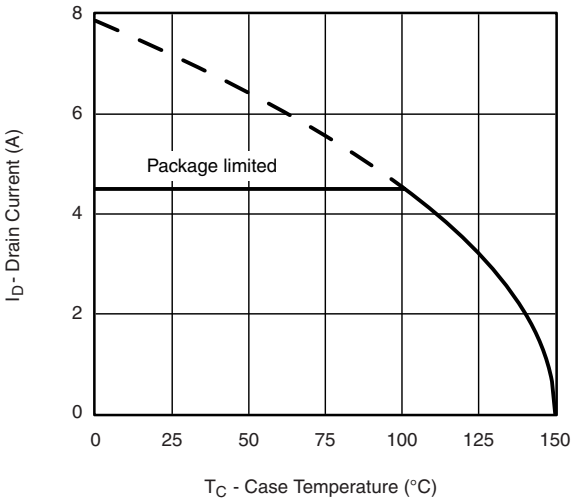
Threshold Voltage



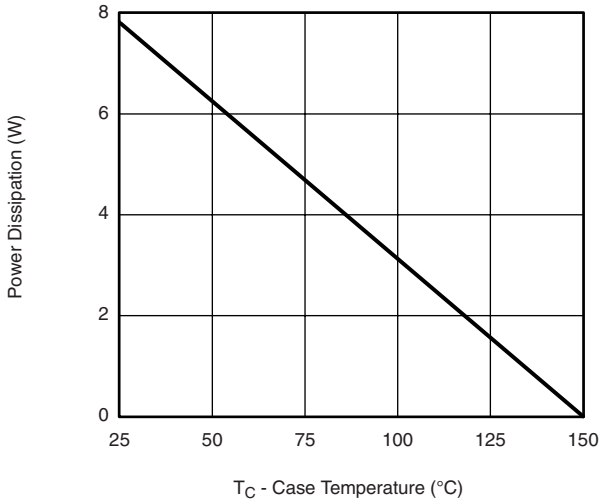
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



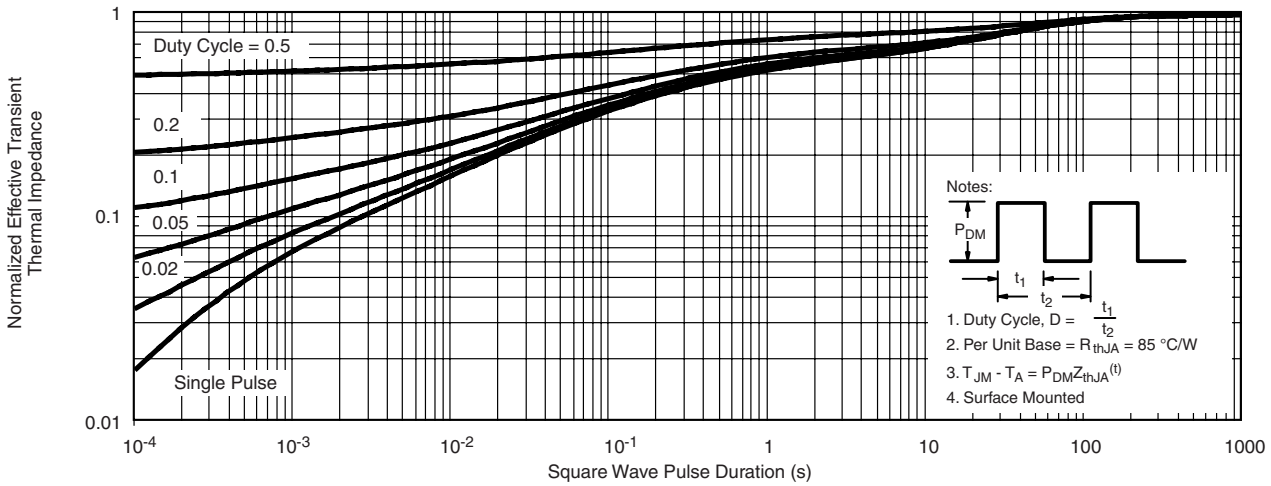
Current Derating*



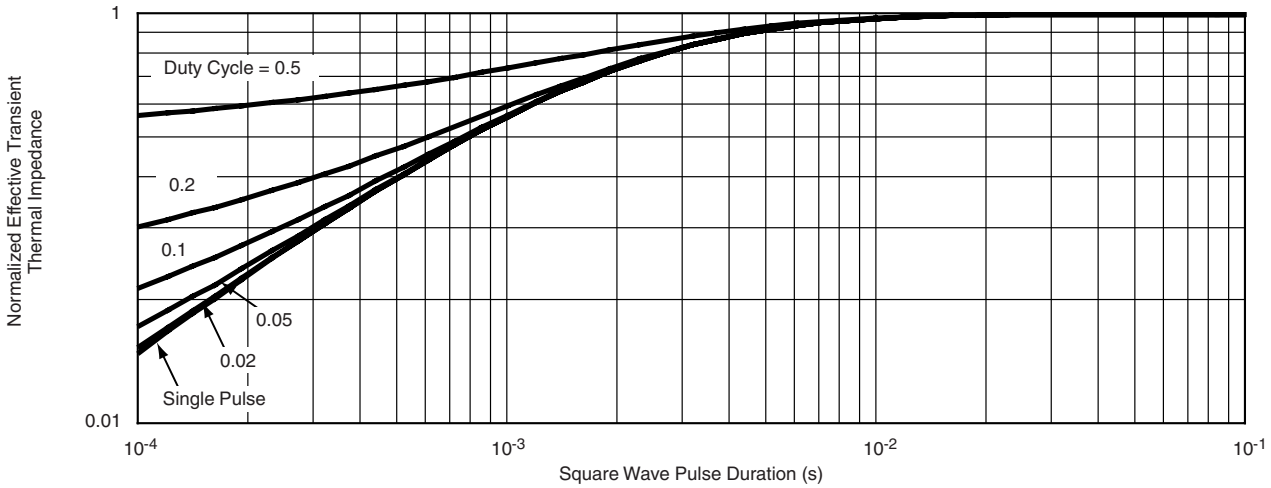
Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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