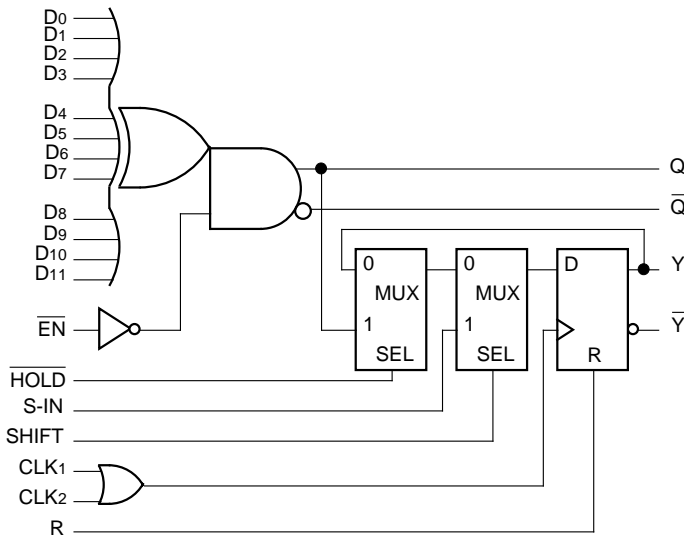


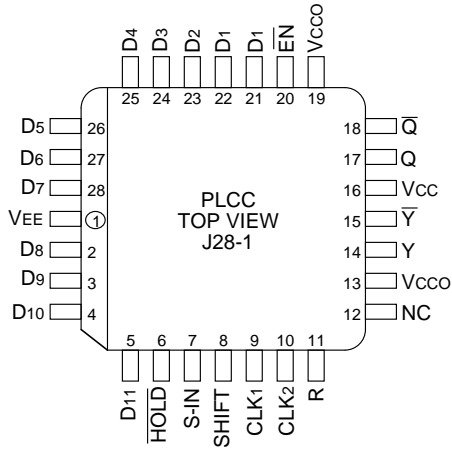
- Provides odd-HIGH parity of 12 inputs
- Extended 100E VEE range of -4.2V to -5.5V
- Output register with Shift/Hold capability
- 900ps max. D to Q, /Q output
- Enable control
- Asynchronous Register Reset
- Differential outputs
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E160
- Available in 28-pin PLCC package

The SY10/100E160 are high-speed, 12-bit parity generator/checkers with differential outputs, for use in new, high-performance ECL systems. The output Q takes on a logic HIGH value only when an odd number of inputs are at a logic HIGH. A logic HIGH on the enable input (EN) forces the output Q to a logic LOW.

An additional feature of the E160 is the output register. Two multiplexers and their associated signals control the register input by providing the option of holding present data, loading the new parity data or shifting external data in. To hold the present data, the Hold signal (HOLD) must be at a logic LOW level. If the HOLD signal is at a logic HIGH, the data present at the Q output is passed through the first multiplexer. Taking the Shift signal (SHIFT) to a logic HIGH will shift the data at the S-IN pin into the output register. If the SHIFT signal is at a logic LOW, the output of the first multiplexer is then passed through to the register.

The register itself is clocked on the rising edge of CLK1 or CLK2 (or both). The presence of a logic HIGH on the reset pin (R) forces the register output Y to a logic LOW.





28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E160JC	J28-1	Commercial	SY10E160JC	Sn-Pb
SY10E160JCTR ⁽²⁾	J28-1	Commercial	SY10E160JC	Sn-Pb
SY100E160JC	J28-1	Commercial	SY100E160JC	Sn-Pb
SY100E160JCTR ⁽²⁾	J28-1	Commercial	SY100E160JC	Sn-Pb
SY10E160JZ ⁽³⁾	J28-1	Commercial	SY10E160JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E160JZTR ^(2, 3)	J28-1	Commercial	SY10E160JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E160JZ ⁽³⁾	J28-1	Commercial	SY100E160JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E160JZTR ^(2, 3)	J28-1	Commercial	SY100E160JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

Pin	Function
D0–D11	Data Inputs
S-IN	Serial Data Input
EN	Enable, active LOW
HOLD	Hold, active LOW
SHIFT	Shift, active HIGH
CLK1, CLK2	Clock Inputs
R	Reset Input
Q, \bar{Q}	Direct Output
Y, \bar{Y}	Register Output
Vcco	Vcc to Output

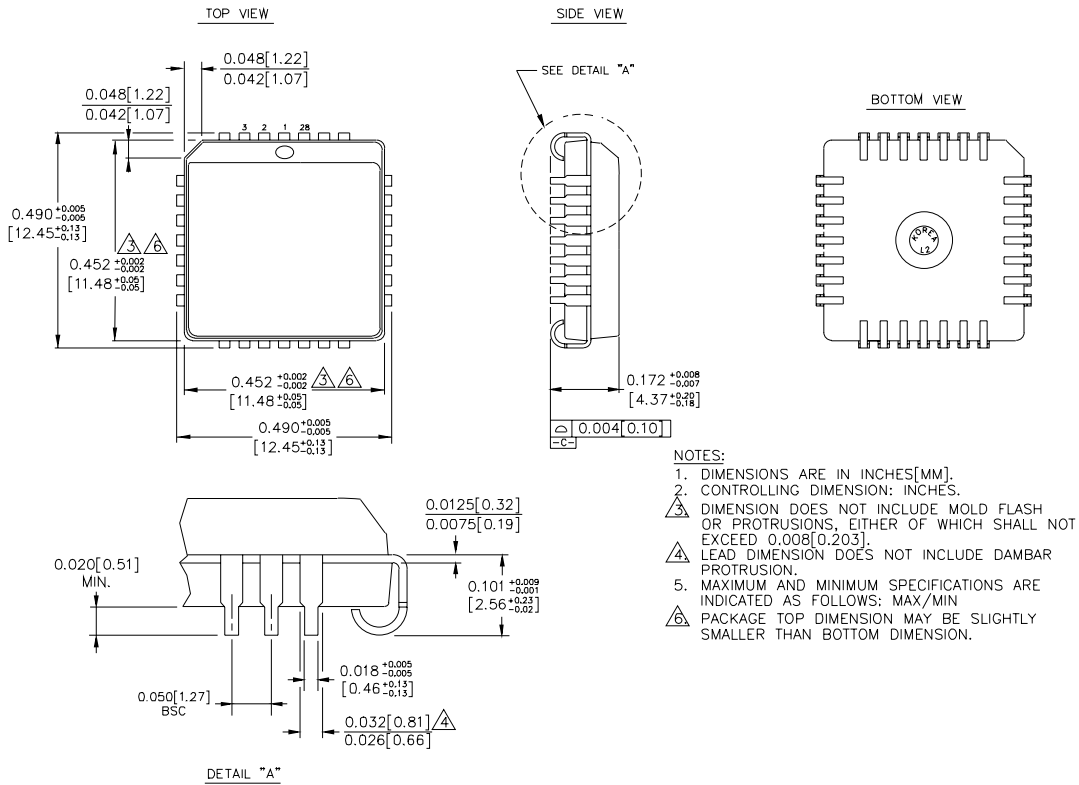
Number of HIGH Inputs	Output Q
Even	LOW
Odd	HIGH

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
IIH	Input HIGH Current	—	—	200	—	—	200	—	—	200	μA	—
	CLK1, CLK2	—	—	300	—	—	300	—	—	300		
	R	—	—	150	—	—	150	—	—	150		
IEE	All Other Inputs	—	—	150	—	—	150	—	—	150	mA	—
	Power Supply Current	—	82	98	—	82	98	—	82	98		
	10E	—	82	98	—	82	98	—	82	98		
	100E	—	82	98	—	82	98	—	94	113		

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
tPD	Propagation Delay to Output										ps	—
	D to Q	400	650	950	400	650	950	400	650	950		
	EN to Q	300	550	750	300	550	750	300	550	750		
	CLK to Y	275	500	700	275	500	700	275	500	700		
	R to Y	275	500	725	275	500	725	275	500	725		
ts	Set-up Time										ps	—
	D	1200	900	—	1200	900	—	1200	900	—		
	HOLD	600	300	—	600	300	—	600	300	—		
	S-IN	350	150	—	350	150	—	350	150	—		
	SHIFT	500	250	—	500	250	—	500	250	—		
tH	Hold Time										ps	—
	D	-400	-900	—	-400	-900	—	-400	-900	—		
	HOLD	100	-300	—	100	-300	—	100	-300	—		
	S-IN	300	-150	—	300	-150	—	300	-150	—		
	SHIFT	200	-250	—	200	-250	—	200	-250	—		
tr	Rise/Fall Time	300	450	650	300	450	650	300	450	650	ps	—
tf	20% to 80%											



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